# Special instructions, e.g.: On-Line Examination This paper will be taken on-line and this is the paper format which will be available as a back-up

# UNIVERSITY OF MANCHESTER SCHOOL OF COMPUTER SCIENCE

**Operating Systems** 

Thursday 22<sup>nd</sup> January 2013?

Time: 14:00 - 16:00?

Please answer any THREE Questions from the FOUR questions provided?

Use a SEPARATE answerbook for each SECTION

For full marks your answers should be concise as well as accurate. Marks will be awarded for reasoning and method as well as being correct

The use of electronic calculators is permitted provided they are not programmable and do not store text.

[PTO]

#### **Section A**

#### 1. **Operating Systems**

e) Explain what is meant by the term multiprogramming.

(2 marks)

1.e.

# Bookwork (2 marks):

The following points should be covered to some degree in the answer:

Answer should cover the 'basic points' and for higher marks put these basic points into context.

#### **Basic points:**

Multiprogramming has been used in the past.

Multiprogramming loads multiple programs into the physical memory.

When using Multiprogramming the operating system switches between the multiple programs and switches them into the physical memory.

When one program has finished [the Multiprogramming operating system] bring in a new program.

#### **Points contextualised:**

In a multiprogrammed system, it is necessary to have more than one program in the memory at one time.

This is because it would be grossly inefficient to save and load processes to/from disk every time a process switch occurs.

As it is, in general, impossible to know which combination of processes will be needed in memory, it would be very restrictive if a program had to be loaded at the same set of addresses every time. Therefore, a scheme is needed where a program can be loaded starting at any convenient memory location, this is relocation.

**2 marks** for an answer that describes and contextualises multiprogramming and gives the salient facts in a sensible way; and provides a well-defined set of brief descriptions of each;

1 mark for some basic understanding (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: Lectures 10 Memory Management (1).

TOTAL marks (2 marks) [2]

#### Marker's feedback 1.g.

#### **Pedagogic assessment [criterion]:**

The question assesses Lectures 10 Memory Management (1) objective 4 directly; 4. Explain multiprogramming.

Well done, most of you were able to state what is meant by the term multiprogramming. The question's answer should clearly evidence knowledge of required salient facts relating to multiprogramming and the key issues such as: loads multiple programs into the physical memory; operating system switches between the multiple programs; switches them into the physical memory; one program has finished bring in a new program.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: loads, multiple, programs, physical, memory, operating system, more than one program, save, load, processes, to/from, disk, process switch, memory location, & relocation.

If you covered all [or most] the points then full marks were awarded. However if the answer did not utilise the correct keywords in context, and did not show you exercised your academic knowledge in this domain issue by not covering most of the issues full marks could not be awarded.

f) Explain the difference between a virtual memory address and a physical memory address. (2 marks)

1.f.

# Critique [Differentiate] (2 marks):

The following points should be covered to some degree in the answer:

A <u>physical</u> memory address is an address which corresponds to a fixed location in <u>physical</u> RAM memory.

A virtual address is an address in a <u>conceptual</u> memory space which a process (program) thinks it is operating.

Virtual addresses are normally translated to physical addresses by Memory Management Unit (MMU) hardware.

**2 marks** for an answer that depicts all the salient facts in a sensible way; and correctly delineated and briefly described;

**1 mark** for some basic understanding (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: Lecture 11: Virtual Memory (1).

TOTAL marks (2 marks) [4]

#### Marker's feedback 1.g.

#### **Pedagogic assessment [criterion]:**

The question assesses Lecture 11: Virtual Memory (1). learning objective 1 directly; 1. Explain what is meant by a paged virtual memory system.

Well done, the majority of you were able to cleanly and explicitly and easily differentiate between the two. If however the answer did not utilise the correct keywords in context, and did not show you exercised your academic knowledge in this domain issue by not differentiating between the two concisely full marks could not be awarded.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: <a href="physical">physical</a>, memory, address, fixed, location, RAM, virtual, <a href="conceptual">conceptual</a>, translated, physical, Memory Management Unit (MMU), & hardware. This theory of the three areas was covered in the lecture series in three different audio visual medias: 1) the actual live lecture; 2) the audio recording of the live lecture; and 3) the real time video of the lecture.

#### g) What is a page replacement algorithm?

(2 marks)

1.g.

# Book (2 marks),

Example answer:- The following points should be covered to some degree in the answer:

In a virtual memory, the <u>memory space</u> is <u>divided</u> into <u>pages</u>. There are normally <u>more pages</u> than can fit into the real (RAM) memory of the system and thus some pages are held on <u>background storage</u> to be moved into main memory only when the CPU wants to access them. When a page needs to be moved into main memory, it is necessary to decide which page to <u>reject</u> to make space for it. The page replacement algorithm is used to make the decision of which page to reject.

**2 marks** for a totally correct explicit delineation of a page table using <u>keywords</u> in context.

1 mark for some basic table (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: 13; Virtual Memory (3); Introduction to: Page Replacement Policies.

TOTAL marks (2 marks) [6]

#### Marker's feedback 1.g.

#### **Pedagogic assessment [criterion]:**

The question assesses 13; Virtual Memory (3); Introduction to: Page Replacement Policies learning objective 1 directly; 1. Discuss the concept of 'Page Replacement'.

Well done, the bulk of you were able to explain what explicitly a page replacement algorithm was – you utilised the correct keywords or technical terminology in context – you also coved enough domain knowledge to show you were [indeed] aware of the key issues with respect to page replacement algorithms – what they are & what they do. However, those that did not gain full marks were either: fuzzy [in respect to their explanation]; or appeared not to cover the issues directly related to portraying they fully comprehended what explicitly page replacement algorithms were – so full marks could not be awarded.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: virtual, memory, memory space, divided, pages, RAM, background storage, CPU, page, reject, replacement, & algorithm.

# h) What is meant by memory mapped I/O?

(2 marks)

1.h.

#### Bookwork (2 marks),

Example answer:- The following points should be covered to some degree in the answer:

There are two basic ways that a CPU can communicate with a peripheral device. Early CPUs used special I/O instructions which included specific peripheral numbers to select data and control information from a device. Modern CPUs use normal memory load and store instructions to <a href="read/write\_from/to">read/write\_from/to</a> areas in the <a href="memory address space">memory address space</a>. This is memory mapped I/O.

**2 marks** for a totally correct explicit delineation of a page table using <u>keywords</u> in context.

**1 mark** for some basic table (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: 14; Controlling Input and Output (1).

TOTAL marks (2 marks) [8]

# Marker's feedback 1.g.

# **Pedagogic assessment [criterion]:**

The question assesses 14; Controlling Input and Output (1) learning objective 1 directly; 1. Explain in simple terms how a processor interacts with an I/O device.

Well done, most could explain the concept of memory mapped input output – some [even added a diagram – which made their explanation even more comprehensive – if they gave a good explanation as well] – but those that did well used the correct terminology & put the correct terminology in context – and showed they were fully aware of the concept of memory mapped I/O. However, some were not to concise in their answer and did not consider a diagram to aid their explanation – others were rather fuzzy in their explanation – and some did not justify their answer by utilising the correct terminology in context – hence full marks could not be awarded.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: CPU, communicate, peripheral, device, I/O (input/output), instructions, peripheral, select, data, control, information, device, load, store, read/write, from/to, areas, memory address space, memory, & mapped I/O.

i) What is a 'page fault'? Describe how a page fault is handled by the Memory Management Unit and the operating system. (2 marks)

#### 1.i.

#### Bookwork (2 marks),

Example answer:- The following points should be covered to some degree in the answer:

In a paged virtual memory system, pages may have copies in real memory or may exist only on <u>backing storage</u> (usually <u>disk</u> or <u>secondary memory</u>). If the MMU attempts an address translation but the page "table indicates that there is <u>no copy</u> in real memory, this is a <u>page fault</u>. The MMU interrupts the CPU and traps to an OS page fault handler. This is responsible for both selecting a page to <u>reject</u> from real memory – and <u>writing</u> it to disk if it has changed since it was last read" – and organising the read of the required page from disk to real memory. It then updates the page tables and transfers control back to the original program to re-execute the instruction which caused the fault.

2 marks for a totally correct using <u>keywords</u> in context, 1 mark for some basic table (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: 11, Virtual Memory (1), Paged Virtual Memory.

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#### Marker's feedback 1.g.

# **Pedagogic assessment [criterion]:**

The question assesses Lecture(s) No(s).: 11, Virtual Memory (1), Paged Virtual Memory learning objective 1 and 2 both directly and indirectly; 1. Explain what is meant by a paged virtual memory system & Establish the outcome of memory references (specified by address) for a paged virtual memory system with a specific page table.

Well done, in the main most were able to explain the issues. The concepts that needed to be explicitly explained are those underlined and put in context in the template answer – these align to utilising all the keywords listed below – putting them in explicitly the right context to fully describe how a page fault is handled by the Memory Management Unit and the operating system.

However, that detail had to be comprehensive with respect to its technical content – see template answer – and in its use of keywords in the correct context – if this was the case full marks were awarded. If not – and the answer was: fuzzy, or not concise with respect to terminology and theory, or did not cover all the required key issues and aligned keywords (in the correct technical context) full marks could not be awarded.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: paged, virtual, memory, system, copies, real memory, <u>backing storage</u>, <u>disk</u>, <u>secondary</u>, <u>MMU</u>, <u>no copy</u>, <u>page fault</u>, <u>MMU</u>, interrupts, CPU, traps, OS page, fault, handler, selecting, <u>reject</u>, <u>writing</u>, changed, last read, updates, page tables, transfers.

# **Section B**

3.

a) On a paged machine with 3 pages frames (PFs) available for it, a particular process makes accesses to the following pages in the order given:

Show the contents of the 3 page frames (PFs) and the cumulative total number of page faults after each memory access assuming that an LRU page replacement algorithm is in use and that the page frames are initially empty. The type of diagram you should draw up is depicted in figure 3.a. (4 marks)

Access: 0 3 7 1 3 2 1 3 7 Most recent: X X X X X X X X Contents of X ) Second most: X X X X X X X X X ) page frames Third most: X X X X X X X X X ) in memory Total PFs: X X X X X X X X X

Question [Figure] 3 a) Typical diagram showing 3 page frames and the cumulative total number of page faults.

3.a.

#### Application (4 marks),

Example answer:- The following points should be covered to some degree in the answer:

| Access:      | 0 | 3 | 7 | 1 | 3 | 2 | 1 | 3 | 7 |   |             |
|--------------|---|---|---|---|---|---|---|---|---|---|-------------|
| Most recent: | 0 | 3 | 7 | 1 | 3 | 2 | 1 | 3 | 7 | ) | Contents of |
| Second most: | - | 0 | 3 | 7 | 1 | 3 | 2 | 1 | 3 | ) | page frames |
| Third most:  | - | - | 0 | 3 | 7 | 1 | 3 | 2 | 1 | ) | in memory   |
| Total PFs:   | 1 | 2 | 3 | 4 | 4 | 5 | 5 | 5 | 6 |   |             |

**4 marks** for a totally correct content, 3 marks for all 3 page frames totally correct and 1 mark for the cumulative total number of page faults totally correct.

2 marks for half issues covered,

1 mark for some basic calculations (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: 13; Virtual Memory (3).

TOTAL marks (4 marks) [4]

#### Marker's feedback 1.g.

#### **Pedagogic assessment [criterion]:**

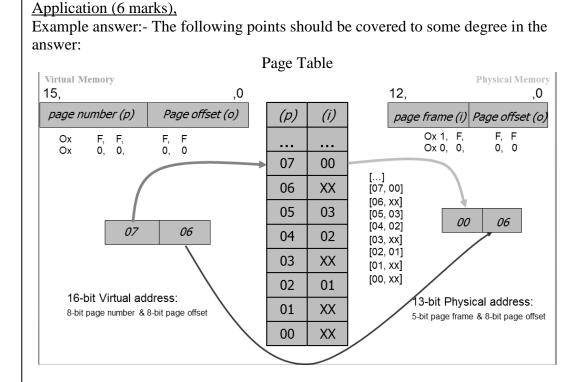
The question assesses lecture 13; Virtual Memory (3) learning objective 1 and 1 directly; 1. Discuss the concept of 'Page Replacement'; 2. Differentiate between First in First Out (FIFO) and Least Recently Used (LRU).

Well done, a large proposition was able to draw up the diagrammatic depiction of a page replacement table in operation. If all pages numbers were placed in exactly the correct 'requested order' Column and in the correct page frame row – plus all the 'totals of page frames' were correct – hopefully, the notation: Most recent, then Second most, then Third most, plus: other labelling – then full marks were awarded.

However, if not all of the above comprehensive diagram [which was fully labelled] was not presented in your answer full marks could not be awarded.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: most recent, second most, third most, contents, page, frames, memory, total.

b) A 16 bit virtual address is divided into an 8-bit page number and an 8-bit page offset; whereas the associated physical address has a 5-bit page frame with the appropriate page offset address sizing. Show, with the aid of a fully labelled diagram, the table structure necessary to convert this virtual address into a real physical address. (6 marks)



**6 marks** for a totally correct content, 2 marks virtual mem. totally correct, 2 marks for example page table totally correct and 2 mark for physical memory totally correct. (totally correct: implies sizing of page no & page off. as well as sizing of page frame & page off.)

**3 marks** for half issues covered.

1 mark for some basic calculations (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: 11; Virtual Memory (1).

TOTAL marks (6 marks) [10]

# Marker's feedback 1.g.

3.b.

#### **Pedagogic assessment [criterion]:**

The question assesses lecture 11; Virtual Memory (1) learning objective 1 and 2 indirectly; 1. Explain what is meant by a paged virtual memory system; 2. Determine the structure of an address in a paged virtual memory system.

Well done, most students were able to draw up a fully labelled diagram, the table structure necessary to convert this virtual address into a real physical address. Those that drew up a concise, readable, well presented & structured, as well as fully labelled diagram were awarded full marks – if they utilised the majority of the keywords depicted in the template answer and in those mentioned below.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context – in the diagram; for example: page number, page offset, page table, page frame, virtual memory, virtual address, physical address, & physical memory. This theory of the three areas was covered in the lecture series in three different audio visual medias: 1) the actual live lecture; 2) the audio recording of the live lecture; and 3) the real time video of the lecture.

With the aid of a diagram, describe the structure of a simple base and limit c) system and explain how it achieves relocation. NOTE: For full marks your answer must contain two components: a fully labelled diagram and a concise explicit description of a base and limits system and how it achieves relocation.

(6 marks)

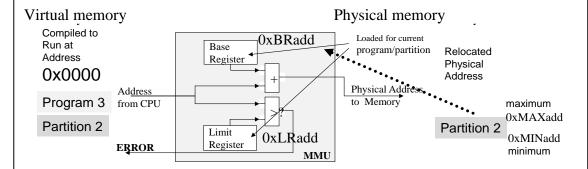
3.c.

#### Bookwork (6 marks),

Example answer:- The following points should be covered to some degree in ing names of the components: [equal 'taken

the answer:

A base+limit system is a piece of hardware which is placed between the CPU and memory. It has a 'base address' register which can be loaded as execution of a program is scheduled and this is added to any address issued by the processor. Note, if the program is represented in binary as if it starts at address 0, this will automatically address the program as if it starts at the base address. (Standard diagram required). The limits register compares the address issued by the processor to the maximum partition address; if greater it throws an error, setting the ERROR line.



Question Answer figure 3.c. Base and limits diagram. Note: MMU implies memory management unit; '+' implies addition; '>' implies compare [if greater than throw ERROR].

6 marks for a totally correct [fully labelled] diagram and, explicit delineation of a base and limits system using keywords in context

**3 mark** for some basic calculations (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: 10; Memory Management (1).

#### Marker's feedback 1.g.

# **Pedagogic assessment [criterion]:**

The question assesses lecture 10; Memory Management (1) learning objective 5 directly; 5. Demonstrate an understanding of Relocation.

Well done, most of you were able to most students did draw up a well-structured and comprehensive diagram [which was fully labelled] – which depicted: the MMU, and inside this the base and limits registers – it also [should] clearly depicted the address from the CPU; coming into the MMU; and an ERROR line emanating from a compare icon [which compares the 'address from the CPU' with the number [or limit] in the limit register – it should also clearly depict an output line [address (bus)] that outputs the 'physical address to memory' which is calculated by adding the 'base address' [in the 'base register'] to the 'address from the CPU;' derived from a "+" icon. If you were able to achieve all this full marks were awarded.

However, if not all of the above comprehensive diagram [which was fully labelled] was not presented in your answer full marks could not be awarded.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: base, limit, hardware, <u>CPU</u>, <u>memory</u>, 'base address,' register, <u>added</u>, processor, starts at address, address 0, <u>compares</u>, <u>maximum</u>, partition, greater, throws, error, & setting the ERROR line.

d) Given a 1G address spaces and associated 128K page sizes; calculate the number of pages that result in the virtual address space. NOTE: To gain full marks you must show full working. (2 marks)

3.d.

# Application (2 marks),

Example answer:- The following points should be covered to some degree in ing names of the components: [equal 'taken

the answer:

Virtual address space 1GB and page size 128KB.

If the virtual address space is 1 GB and the page size is 128 KB there are:

Number of Pages 
$$=$$
  $\frac{\text{Address space}}{\text{Page size}}$   
 $\frac{1 \text{ GB}}{128 \text{ KB}} = \frac{2^{30}}{2^{17}} = \frac{1,073,741,824}{131,072} = 2^{30-17} = 2^{13} \text{ (ar = 8,192)} = 8 \text{ K pages}$ 

2 marks for an answer that calculates the correct answer and is laid out correctly e.g.

2 marks for a correct answer and full working out,

**1 mark** for a 'right lines' approach. Moderate marks will be awarded in the case of correct application for a wrongly calculated.,

½ marks for some basic understanding (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed

#### Marker's feedback 1.g.

# **Pedagogic assessment [criterion]:**

The question assesses lecture 11; Virtual Memory (1) learning objective 1 and 2 directly; 1. Explain what is meant by a paged virtual memory system; 2. Determine the structure of an address in a paged virtual memory system.

Well done, the majority of you were able to first: 1. remember the equation (address space divided by page size); second 2. substitute the correct numbers form address space and page size; third 3. convert these to power of 2; fourthly 4. utilise the mathematical norm for dividing power (i.e. subtract the power of two of the page size [the divisor] from the power of two of the address space [the dividend]); fifth 5. convert the resultant answer (which is a power of 2) in to an integer number – this is the number of pages. If you undertook 1 to 5 and at each stage attained the correct answers – you will have been full marks – if not full marks could not be awarded.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: address space, & page size.

e) Given a physical address size of 2G and associated 64K block size below. Calculate the number of page frames in the physical address space. NOTE: To gain full marks you must show full working. (2 marks)

3.e.

#### Application (2 marks),

Example answer:- The following points should be covered to some degree in ing names of the components: [equal 'taken

the answer:

Given a block [page] size of 128 KB and a physical address space of 2 GB. If the virtual address space is 2 GB and the block size is 128 KB there are:

$$Number of Page frames = \frac{Address \, space}{Block \, size}$$

$$\frac{2G}{64K} = \frac{2^{31}}{2^{16}} = \frac{2,147,483,648}{65,536} = 2^{31-16} = 2^{15} (or = 32,768) = 32K \text{ page frames}$$

2 marks for an answer that calculates the correct answer and is laid out correctly e.g.2 marks for a correct answer and full working out,

**1 mark** for a 'right lines' approach. Moderate marks will be awarded in the case of correct application for a wrongly calculated.,

½ marks for some basic understanding (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: 11; Virtual Memory (1).

#### Marker's feedback 1.g.

# **Pedagogic assessment [criterion]:**

The question assesses lecture 11; Virtual Memory (1) learning objective 1 and 2 directly; 1. Explain what is meant by a paged virtual memory system; 2. Determine the structure of an address in a paged virtual memory system.

Well done, the majority of you were able to first: 1. remember the equation (address space divided by block size); second 2. substitute the correct numbers form address space and page size; third 3. convert these to power of 2; fourthly 4. utilise the mathematical norm for dividing power (i.e. subtract the power of two of the page size [the divisor] from the power of two of the address space [the dividend]); fifth 5. convert the resultant answer (which is a power of 2) in to an integer number – this is the number of pages frames. If you undertook 1 to 5 and at each stage attained the correct answers – you will have been full marks – if not full marks could not be awarded.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: address space, & block size.

4.

a) Explain how a peripheral communicates with the CPU using interrupts.

(3 mark)

4.a.

Bookwork (3 marks):

The following points should be covered to some degree in the answer:

A peripheral wanting to make a transfer raises a hardware signal [interrupt line]. The CPU completes its current instruction and then enters a routine to service the peripheral. This may either be by a single routine address (in which case the routine must use polling to identify the peripheral) or a device specific address via a table. The CPU then reads from or writes to the device before resuming the original program that was interrupted. The address required to do this is saved by the hardware when the interrupt occurs.

Other keywords that may be utilised [in context]: interrupt acknowledgement – IACK, processor saves the current value, interrupt vector, Interrupt Service Routine (ISR).

**3 marks** for an answer that depicts all the salient facts in a sensible way; and the use of keywords in context;

**1 mark** for some basic understanding (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: Lectures 15: Controlling Input and Output 2.

TOTAL marks (3 marks) [3]

#### Marker's feedback 1.g.

#### **Pedagogic assessment [criterion]:**

The question assesses Lectures 15: Controlling Input and Output 2 learning objective 1 and 2 directly; 1. Describe what a processor does in response to an interrupt; 2. Discuss what is meant by interrupt-driven I/O.

Well done, most could explain how a peripheral communicates with the CPU using interrupts in sufficient detail. However, that detail had to be comprehensive with respect to its technical content – see template answer – and in its use of keywords in the correct context – if this was the case full marks were awarded. If not – and the answer was: fuzzy, or not concise with respect to terminology and theory, or did not cover all the required key issues and aligned keywords (in the correct technical context) full marks could not be awarded.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: peripheral, hardware, signal, <u>interrupt line</u>], routine, <u>service</u>, peripheral, polling, identify, device, specific, address, table, CPU, reads, writes, interrupt acknowledgement – IACK, processor saves the current value, interrupt vector, Interrupt Service Routine (ISR).

- b) Segmented memory is an alternative to paged memory; the following questions relate to segmented memory.
  - i) Explain the difference between a *page* and a *segment* in a virtual memory system. (3 marks)

4.b.i.

# Critique [Differentiate] (3 marks):

The following points should be covered to some degree in the answer:

Very basic answer is: Page is <u>fixed</u> size, segment is <u>variable</u> size. In a paged virtual memory system, the pages are <u>all the same size</u>. In a segmented virtual memory system, the segments are of <u>variable size</u>. Segmentation is less about mapping a larger virtual address space onto a smaller physical memory (the purpose of paging), and more about supporting the operating system in general.

2 marks for an answer that depicts all points, and the use of <u>keywords</u> in context; 1 marks for half of the facts;

½ mark for some basic understanding (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: Lectures 12: Virtual Memory (2), Segmented Virtual Memory.

TOTAL marks (3 marks)[6] Final mark RNs is [10]

# Marker's feedback 1.g.

#### **Pedagogic assessment [criterion]:**

The question assesses Lectures 12: Virtual Memory (2), Segmented Virtual Memory learning objective 1 directly; 1. Explain what is meant by segmented virtual memory.

Well done, in the main most were able to concisely differentiate between a page and a segment in virtual memory. If you covered all the required issues – as delineated in the template answer – and utilised the correct keywords in context – full marks were awarded. If not – and the answer was: fuzzy, or not concise with respect to terminology and theory, or did not cover all the required key issues and aligned keywords (in the correct technical context) full marks could not be awarded.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: <u>fixed</u> size, <u>variable</u> size, pages, <u>all the same size</u>, segmented, <u>variable size</u>, mapping, virtual, address, space, smaller, physical, memory, paging, supporting, operating system.

- ii) A computer system uses segmented virtual memory (no pages). The state of the memory at a given time is shown in the figure 4.b.ii. Indicate what happens when a segment requiring 9KB of memory space is loaded using the following algorithms:
  - 1) Best Fit; and
  - 2) First Fit.

State where the 9KB will be placed given 1) and 2); and due to the different alogorithms if any issues arise.

Note that it is assumed that the lowest address is at the bottom of the diagram; and the third column indexes all the segments A, ..., J. (4 marks)

|  | 9 KB Gap      | J |
|--|---------------|---|
|  | 15 KB Segment | 1 |
|  | 8 KB Gap      | Н |
|  | 20 KB Segment | G |
|  | 10 KB Gap     | F |
|  | 10 KB Segment | Е |
|  | 8 KB Gap      | D |
|  | 18 KB Segment | С |
|  | 14 KB Gap     | В |
| Lowest address is at the bottom of the diagram → | 9 KB Segment  | Α |

Question [Figure] 4.b.ii. Typical diagram showing segmented memory.

4.b.ii.

#### Application (4 marks):

The following points should be covered to some degree in the answer:

- 1) The Best Fit algorithm will map it to the 9KB gap [index J] at the top of the memory No real ISSUES: as this will not leave any additional gap [e.g. 0KB gap] between the new segment and the 9KB [index J] segment.
- 2) The first fit algorithm will place it in the 14KB [index B] gap. ISSUE: This will leave an additional 5KB gap between the new segment and the 18KB [index C] segment.
- 4 marks for an answer that depicts all points, and the mentioning of the 5KB gap; 2 marks for half of the facts;
- 1 mark for some basic understanding (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: Lectures 12: Virtual Memory (2), Segmented Virtual Memory.

TOTAL marks (4 marks) [10]

# Marker's feedback 1.g.

#### **Pedagogic assessment [criterion]:**

The question assesses Lectures 12: Virtual Memory (2), Segmented Virtual Memory learning objective 1 directly; 1. Explain what is meant by segmented virtual memory.

Well done, a large proposition was able to deduce the gaps to place the 9K segment – using the two different algorithms. If you drew a diagram and explained the algorithms – using the diagram to aid your explanation – and utilised all the correct technical naming conventions directly aligned to the issues – then full marks were awarded. Full marks would have [also] been awarded if you textual explanation was concise and covered all the issues the template answer covered.

However, if not all of the above comprehensive diagram [which was fully labelled] was not presented in your answer full marks could not be awarded.

However, some were not to concise in their answer and did not consider a diagram to aid their explanation – others were rather fuzzy in their explanation – and some did not justify their answer by utilising the correct terminology in context – hence full marks could not be awarded.

In the answer [some of] the following terminology (keywords and naming conventions) should be utilised in context; for example: Best Fit, algorithm, gap, memory, segment, first fit.

# c) [John Gurds] Given an.

(5 marks)

Application (5 marks),

Example answer:-

The following points should be covered to some degree in the answer:

2 marks for a totally correct calculation,

1 mark for some basic calculations (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: ??.

TOTAL marks (5 marks) [15]

# d) [John Gurd's] Given a.

(5 marks)

Application (5 marks),

Example answer:- The following points should be covered to some degree in the answer:

2 marks for a totally correct calculation,

1 mark for some basic calculations (or attempt).

Reference Learning Resources, Background Reading, and Lecture itself for detailed information; Lecture(s) No(s).: ??.

TOTAL marks (5 marks) [20]

# **END OF EXAMINATION**