COMP25212

Two hours

UNIVERSITY OF MANCHESTER
SCHOOL OF COMPUTER SCIENCE

System Architecture

Date: Tuesday 3rd June 2014

Time: 09:45 - 11:45

Please answer any THREE Questions from the FOUR questions provided

Use a SEPARATE answerbook for each SECTION

This is a CLOSED book examination

The use of electronic calculators is permitted provided they are not programmable and do not store text

[PTO]

Section A

1. **Caches**

a) Explain why CPU caches are important in the design of modern computer architectures, highlighting what would happen in case a computer does not include caches in its design. (3 marks)

b) Explain the terms "Write Back" and "Write Through" in the context of a write operation to cached data. (2 marks)

c) With regards to the types of cache describe:

i) The characteristic of a fully associative cache and the access details of such memory (2 marks)

ii) The characteristic of a direct mapped cache and the access details of such memory (2 marks)

iii) The characteristic of a set associative cache and a comparison to the fully associative and/or direct mapped cache (2 marks)

d) Why does cache memory give rise to functional problems in computer systems that implement Direct Memory Access facilities (DMA) for peripheral devices? Give an example of two problems and two possible solutions. (6 marks)

e) Explain how cache misses can be categorized as Compulsory, Capacity and Conflict misses. (3 marks)

[PTO]

2. **Storage and Virtualization**

a) Explain what "Seek time", "Search time" and "Transfer time" mean when used to describe hard disk operations. (6 marks)

b) A modern desktop drive is specified as having a capacity of 6 terabytes, a transfer rate of 150 megabytes per second, a rotation rate of 7200 revolutions per minute and a mean seek time of 8 milliseconds. Use binary orders of magnitude (as specified by the Joint Electron Device Engineering Council)

i) How long on average would a transfer of 8 kilobytes take from a random position on the disk? (2 marks)

ii) How long would it take to read the entire disk sequentially? (1 mark)

c) What is the difference between process virtualization and system virtualization? (4 marks)

d) What are the major goals of system virtualization? (3 marks)

e) What is “live migration” and how this can be implemented using system virtualization? (4 marks)

[PTO]

Section B

3. **Pipelining**

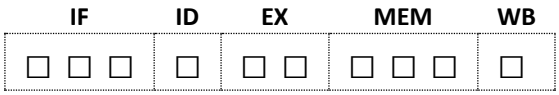
a) Draw the data-dependency graph for the following application. (2 marks)

```
ldr r1, x
ldr r2, y
add r4, r1, r2
ldr r3, z
sub r5, r4, r3
str r5, d
```

b) Draw a space-time diagram simulating the execution of the application above in an in-order 2-way superscalar 5-stage pipeline. Assume all memory accesses hit the cache and that all types of forwarding are implemented. (4 marks)

c) Explain what extra hardware is needed to transform a classic 5-stage pipeline into an out-of-order pipeline. (4 marks)

d) Consider a 10-stage fully pipelined processor as the one below.



(IF and MEM: 3 stages each; EX: 2 stages; ID and WB: 1 stage each)

i) How many cycle penalties will be incurred by the different kinds of Hazards in such processor? (6 marks)
ii) Discuss the techniques to mitigate/solve these penalties. (4 marks)

[PTO]

4. **Multithreading / Multicore**

Consider a modern 6-core processor with 2-way multithreading and 4-way superscalar pipelines.

a) What is this processor's peak IPC? (2 marks)

b) How many concurrent threads are supported by this processor? (2 marks)

c) Assume the processor has a MESI cache coherency protocol with copy back. For the following sequence of accesses to variable 'x', show the bus transactions, the cache states and the actions in main memory. Assume all the corresponding cache lines start in the 'I' state. (10 marks)

core0: LDR r0, x

core1: LDR r1, x

core2: STR r0, x

core3: LDR r3, x

core3: STR r5, x

d) Explain the benefits and limitations of reordering instructions in the compiler or in hardware. (6 marks)

END OF EXAMINATION