# **AVR Instruction Subset**

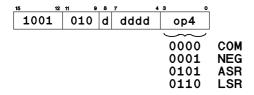
### **ALU Instructions**

15 12	11 10 1	9 8	7	4 3	0
op1	op2	rd	dddd	rr	rr
	<u></u>				
0000	11 00	AD NO	D P		
0001	01 11	CF AD	)C		
0010	00 01 10 11	AN E0 OR M0	R (CL	_R)	

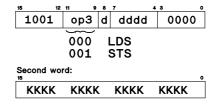
### **Immediate Instructions**

15 12	11 8	7 4	3 0
op1	KKKK	dddd	KKKK
		•	
0011	CPI		
0110	ORI		
0111	AND 1	•	
1110	LDI		
0111	AND I	:	

### **Unary Logical Instructions**



### **Load/Store Instructions**



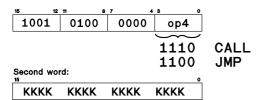
### **Branch Instructions**

15		11 10	9 8		4	3	2	0
	1111	0x	kk	kkkk		k	sss	
		0	BF	RBS			cc	
		1	BF	RBC			• •	

# **Input/Output Instructions**

15	12	11	10	9	8	7		4	3		0
1011		x	Α	A	r	rr	rr		1	AAAA	
		0		0	N U1	-					_

# **Call/Jump Instructions**



### **Return Instructions**

15	12	11	8 7	5	4	3	0
10	01	0101		000	х	1	L000
					0		RET
					1		RETI

### **Stack Instructions**

	15 12	11		7 5 4	3 0
	1001 00		xd	dddd	1111
			0	POP	

### **Relative Jump Instructions**

15	12 1	1 8	7 4	3 0
110x		KKKK	KKKK	KKKK
0		RJMP		
1		RCAL	L	