CS150 - Computer Organization and Architecture

Course Syllabus Spring 2016

Instructor: Michael Wilder `mdwilder@uidaho.edu`

Materials:

Arduino Uno R3: `http://www.adafruit.com/products/50`
Atmel ATmega328P Reference: `http://www.atmel.com/images/doc8161.pdf`
Atmel AVR libc Online Reference: `http://www.nongnu.org/avr-libc`
Atmel AVR Instruction Set Reference: `http://www.atmel.com/images/doc0856.pdf`

Wk	Day			Topic
1	Jan	13	W	Introduction
		15	F	Bits, Data Types, Integers
2		18	M	**** Idaho Human Rights Day (No Classes) ****
		20	W	Base Conversion
		22	F	2's Complement
3		25	M	Binary Arithmetic
		27	W	Binary Arithmetic
		29	F	Logic gates - AND, OR, NOT
4	Feb	1	M	Combinational Logic Circuits
		3	W	Combinational Logic Circuits
		5	F	Storage Elements - Flip Flops
5		8	M	Sequential Logic Circuits
		10	W	Sequential Logic Circuits
		12	F	Finite State Machines
6		15	M	**** Presidents Day (No Classes) ****
		17	W	Finite State Machines
		19	F	*** Exam 1 ***
7		22	M	Arduino basics
		24	W	Arduino basics, C language
		26	F	C language Processing
8		29	M	Computer Organization, the basics
	Mar	2	W	Computer Organization
		4	F	AVR Processor Overview
9		7	M	Instruction Processing
		9	W	Instruction Processing
		11	F	Opcodes, addressing modes
10		14	M	**** Spring Recess (No Classes) ****
		16	W	**** Spring Recess (No Classes) ****
		18	F	**** Spring Recess (No Classes) ****
11		21	M	Instruction Set Architecture
		23	W	AVR Instructions - ALU Operations
		25	F	AVR Instructions - Data Transfer
12		28	M	AVR Instructions - Memory addressing
		30	W	AVR Instructions - Control
	Apr	1	F	The Stack
13		4	M	AVR Instructions - Stack Operations
		6	W	AVR Assembly Language
		8	F	**** Exam 2 ****

Wk	Day		Topic
14	11	M	Assembler Operation
	13	W	Assembler Operation
	15	F	AVR Instructions - I/O
15	18	M	AVR Instructions - I/O
	20	W	Subroutines
	22	F	Subroutines
16	25	M	Subroutines
	27	W	Finite State Machines - processor control
	29	F	Finite State Machines - processor control
17	May 2	M	Performance Enhancements - Pipelining
	4	W	Performance Enhancements - Cache Memory
	6	F	Final Exam Review

Final: Wednesday, May 11, 3:00-5:00PM

Grading:

Two One-Hour Exams (15% ea)	30%
Quizzes	15%
Final Exam	25%
Homework/Programming Projects	30%
Total	100%

The letter grade you receive from the course will be determined as follows:

100%	-	90%	A
89.9%	-	80%	B
79.9%	-	70%	C
69.9%	-	60%	D
59.9%	-	0%	F

The instructor reserves the right to adjust these percentages lower if deemed necessary.

Academic Honesty:

Academic honesty is vital in preserving the integrity of any academic institution. Please do your own work in this course unless the instructor specifically directs otherwise.

Computer Science Support:

For questions involving course content and assignments, please see me or go to the Computer Science Assistance Center (CSAC) located in JEB 211D.

For technical issues involving computing equipment or other resources administered by the Computer Science department, please contact `cshelp@uidaho.edu`.

Disability Support Services Reasonable Accommodations Statement:

Reasonable accommodations are available for students who have documented temporary or permanent disabilities. All accommodations must be approved through *Disability Support Services* located in the Idaho Commons Building, Room 306 in order to notify your instructor(s) as soon as possible regarding accommodation(s) needed for the course.

- phone: 885-6307
- email: `dss@uidaho.edu`
- website: `www.uidaho.edu/dss`