ECE 5780 Lab 01

Postlab Questions

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1. The GPIO registers in this lab are GPIOx_MODER which configures the mode of the I/O pins, GPIOx_OTYPER which configures the output type of the pins, GPIOx_OSPEEDR which configures the output speed, GPIOx_PUPDR which sets the pull-up or pull-down resistance, GPIOx_IDR which can be used to read the input of the corresponding port, GPIOx_ODR which is the output data, GPIOx_BSRR which is write-only and can set the corresponding ODRx bit or clear it, GPIOx_LCKR which locks other configuration registers for a specific pin until a sequence of writes is performed, GPIOx_AFRL/GPIOx_AFRH which configures a pin-depended alternate function, and GPIOx_BRR which is similar to GPIOx_BSRR but has the clearing bits lower.
2. To set the GPIOx_MODER register to analog mode I would set both the low bit and the high bit to 1.
3. To clear the fourth bit in the ODR I would set the BS3 register which is the fourth bit of GPIOx_BSRR.
4. a. 0xAD | 0xC7 = 10101101 | 11000111 = 11101111 = 0xEF
   b. 0xAD & 0xC7 = 10101101 & 11000111 = 10000101 = 0x85
   c. 0xAD & ~(0xC7) = 10101101 & 00111000 = 00101000 = 0x28
   d. 0xAD ^0xC7 = 10101101 ^ 00111000 = 10010101 = 0x95
5. To clear the 5^{th} and 6^{th} bits in a register while leaving the others alone I would use a mask with every bit except the 5^{th} and 6^{th} set and use an AND between the mask and the register. If the mask has a 1, then the register will be set to 1 if it already had a 1 and 0 if it already had a 0. If the mask has a 0, then it will set the register to 0 no matter what it had.
6. When the GPIO pins are set to the lowest speed setting they can handle a max rise and fall time of 125 ns.
7. To enable TIM1 I would manipulate RCC_APB2ENR_TIM1EN. For DMA1 I would manipulate RCC_AHBENR_DMA1EN. For I2C1 I would manipulate RCC_APB1ENR_I2C1EN.