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ECE 5780

Postlab 02

1. Both PA0 and PC0 can't be external outputs at the same time because there are limited EXTI inputs and PA0 to PF0 are on the same multiplexor that assigns a pin to EXTI0.
2. The software priority level with the highest priority is 0. The lowest priority is 3.
3. The NVIC has 8 bits reserved for configuring the priority but only uppermost 2.
4. The latency was about 1.2 ms.
5. The flag has to be cleared because otherwise the interrupt request won't be marked as acknowledged and the handler will get called again.