OLLSCOIL NA hÉIREANN, CORCAIGH
THE NATIONAL UNIVERSITY OF IRELAND, CORK

COLÁISTE NA hOLLSCOILE, CORCAIGH
UNIVERSITY COLLEGE, CORK

Examination Session and Year	**Winter 2023**
Module Code	**CS2507**
Module Title	**Computer Architecture**
Paper Number	**1**
External Examiner	**Prof. Pete Sawyer**
Head of School/ Department	**Prof. Utz Roedig**
Internal Examiners	**Dr. Ahmed Zahran**
Instructions to Candidates	**Answer All questions** **Maximum Mark: 80 marks**
Duration of Paper	**90 min**
Special Requirements	**Do not use RED pen** **Answers must be LEGIBLE to be graded** **calculators are allowed [non-programmable]**

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THEN ENSURE THAT YOU HAVE THE CORRECT EXAM PAPER

Question 1 [30 marks]

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A. [5 marks] Identify three differences between RISC and CISC instruction set architectures.

B. [5 Marks] Considering the following MIPS assembly code

.data

Z: .word 65

X: .double 65

i) **[1 mark]** How many bytes are reserved in the memory?

ii) **[4 marks]** Write down the binary representation of the stored numbers. (show your steps)

C. [5 marks] Your friend claimed that doubling the processor speed is better than using two identical cores. Do you agree or disagree? Explain.

D. [5 marks] Name hazard types in pipelined processor architectures and identify the cause of them.

E. [5 marks] Increasing the pipeline stages has benefits and drawbacks. Discuss this statement based on your understanding of a pipelined processor.

F. [5 Marks] Associative memory has advantages and disadvantages. Explain.

Question 2 [30 marks]

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A. **[30 marks]** Consider the procedure code shown to the right

i- **[2 marks]** Write the code needed to call this function with $a0 =-2 and $a1=6

ii. **[3 marks]** What would be the value in $a0, $a1, $v0 after executing calling the procedure with the values in (i)

iii. **[3 marks]** Can you reduce the number of procedure instructions without impacting the functionality? Why?

iv. **[2 marks]** Identify 2 standard (basic) and 2 pseudo-MIPS instructions in the procedure code.

v- **[2 marks]** What would be the instruction offset stored in "j label3" instructions when the instruction is encoded?

```
1  test_proc:
2      addi $sp, $sp, -4
3      sw $ra, 0($sp)
4      blt $a0, $zero, label1
5      bge $a0, $a1, label2
6      j label3
7  label1:
8      add $a0, $a0, $a1
9      j label3
10 label2:
11     sub $a0, $a0, $a1
12 label3:
13     addi $v0, $a0, 0
14     lw $ra, 0($sp)
15     addi $sp, $sp, 4
16     jr $ra
```

vi- **[2 marks]** which register(s) may change after executing the procedure in comparison to before calling the procedure?

vii- **[2 marks]** Does the "test_proc" procedure follow MIPS convention? If yes, why? If not, how can you fix it?

viii- **[2 marks]** What does "test_proc" do?

ix. **[6 marks]** Identify two pipelining hazards of distinct types in the code.

For each one, identify the instruction(s) and hazard type.

Additionally, indicate if such hazard can be completely avoided or not. If yes, explain how; otherwise, explain why.

x- **[3 marks]** Does the code have double data hazard? If yes, identify the instructions; otherwise explain why.

xi- **[3 marks]** how many clock cycles will be needed to execute this code in case of single clock cycle processor?

Question 3 [20 marks]

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A. [6 marks] What is a multilevel cache? Why do modern processors use it? What is a cache miss? Outline the steps to be taken on an instruction cache miss.

B. [6 marks] Explain the operation of write-back and write-through strategies and compare them with respect to performance and consistency.

C. [8 marks] Consider a direct-mapped cache design with a 24-bit address as shown.

Tag	Index	Offset
23-12	11-6	5-0

i. **[1 mark]** What is the cache block size (in words)?

ii. **[1 mark]** How many blocks does the cache have?

iii. **[1 mark]** What is the cache size?

iv. **[2 marks]** Which block in the cache does the address 0x 6F 0B B8 belong to?

v. **[2 marks]** If the memory is using a two-way set associative caching, which block can this address 0x 0B B8 use?

vi. **[1 mark]** If the memory is using a fully associative cache, which block can this address 0x 0B B8 use?