Digital Logic Design Laboratory Objective and Syllabus

1 Objective

In this lab you will build a MIPS-like single cycle processor using the Xilinx Vivado 2018.3 Design Suite available through the COE VLAB, and target the TUL PYNQ Z2 platform. Your processor will implement a simple instruction set. You will learn the fundamentals of an instruction set, the basics of computer architecture, and you will gain valuable experience programming and testing a design on an FPGA board.

You will also use an assembler to convert your assembly code to machine code. Machine code binary will be used to fill up the instruction memory of your processor.

Digital logic circuits can be divided into three major pieces. The **interface** determines how the user interacts with the circuit. The **datapath** is made up of circuits that operate on data, store it, and the wires that connect them. The **control path** directs the datapath by choosing between several options depending on the current function to be executed.

2 Syllabus

This laboratory course is divided into ten experiments:

Lab 0 Tutorial – introduces the hardware and software you will use throughout the course.

Lab 1 8-bit Adder – You will create an eight bit adder using Verilog HDL and view the result.

Lab 2 Partial Arithmetic Logical Unit (ALU) – You will start building the brain of your processor.

Lab 3 ALU Completion and adding VIO– includes adding the shift and branch instructions. to the partial ALU and introducing the Xilinx Virtual Input Output (VIO) core for monitoring your circuit behavior while stimulating it with test signals.

Lab 4 Register File and Zero Register – in this lab you will create a register file and zero register logic for your processor.

Lab 5 Data Memory – You will create a Data Memory and add it to the processor datapath.

Lab 6 Instruction decoder – You will create an instruction decoder unit for generating the datapath control signals.

Lab 7 Instruction Memory, Straight Line code – You will create the instruction memory logic and run a straight line program on your processor.

Lab 8 Branching Logic and Working Processor – Here you will add the branching mechanism to your processor and combine everything you have designed and test it on the TUL PYNQ Z2 board.

Project You choose a project to expand your processor design, the details of the projects will be discussed in the lectures.

See the schedule for due dates for each lab experiment. Labs 0, 1, 2, &3 will each take one week to complete. Labs 4 & 5 are done together over 3 weeks. Labs 6 & 7 are also done together over three weeks. Lab 8 and the optional project is done the week after Thanksgiving.

Due to COVID, there will be no lab groups. Each student has a hardware kit and is expected to work individually. Scheduled lab sessions will be TA office hours. They are not required but you are welcome to attend part of your assigned lab session. A sign up sheet will be provided.

A lab experiment consists of one or more prelab assignments, design simulations, and hardware implementations. Lab reports are due one week after labs 3, 5, and 8.

Prelab assignments must be completed and turned in on Canvas. Due dates will be communicated on Canvas. Prelabs should be submitted individually by each of student.

TA office hours will be during scheduled lab times. TAs will hold additional on-line office hours and will announce these in their section on Canvas.

The grading policy is as follows. All student work is expected to be individual.

- Prelabs: 25%
- Quizzes: 15%
- Simulation and Hardware: 25%
- Lab Reports: 35%