EECE2323 **Digital Logic Design Lab** **Prelab 2**

Partial Arithmetic and Logic Unit (ALU)

Begin by reading Sections 1, 2, and 3 of your lab manual. Then answer the following questions.

1 Design the Partial ALU

Create a Verilog module called eightbit_palu which has two 8-bit inputs, a and b, and one 2-bit input, sel. The outputs of this module are an 8-bit signal f, and a 1-bit signal ovf. The value of these outputs should change based on the sel signal value which determines the operation.

The partial ALU operations and their descriptions are shown in Table 1.

s[1:0]	**f[7:0]**	**ovf**	**Description**
0 0	$a + b$ (add)	overflow	a plus b
0 1	b (inv)	0	Bitwise inversion of b
1 0	$a \cdot b$ (and)	0	Bitwise AND of a and b
1 1	$a \mid b$ (or)	0	Bitwise OR of a and b

Table 1: Partial ALU operations

2 Create Test Vectors

Similar to what you did in prelab 1, create a set of test vectors that could test all of the bits in inputs, i.e. a, b and s, and outputs, i.e. f and ovf, of the partial ALU. Create a table to show your test vectors.

Run your code with your testbench.

3 What to Submit

Your solution should include your Verilog code for your partial ALU, your Verilog code for your testbench and a screen shot showing your simulation working.