EECE2323	Digital Logic Design Lab	Prelab 4

Adding Register File to ALU

Begin by reading your lab manual. Then answer the following questions.

1 Design a Register File

Create a 4-deep 9-bit wide register file using Verilog. This register file should have seven input ports: rst, clk, wr_en, rd0_addr(1:0), rd1_addr(1:0), wr_addr(1:0), wr_data(8:0) and two output ports: rd0_data(8:0) and rd1_data(8:0). Name the module as `reg_file`.

The interface and dimensions of register file are illustrated in Figure 1.

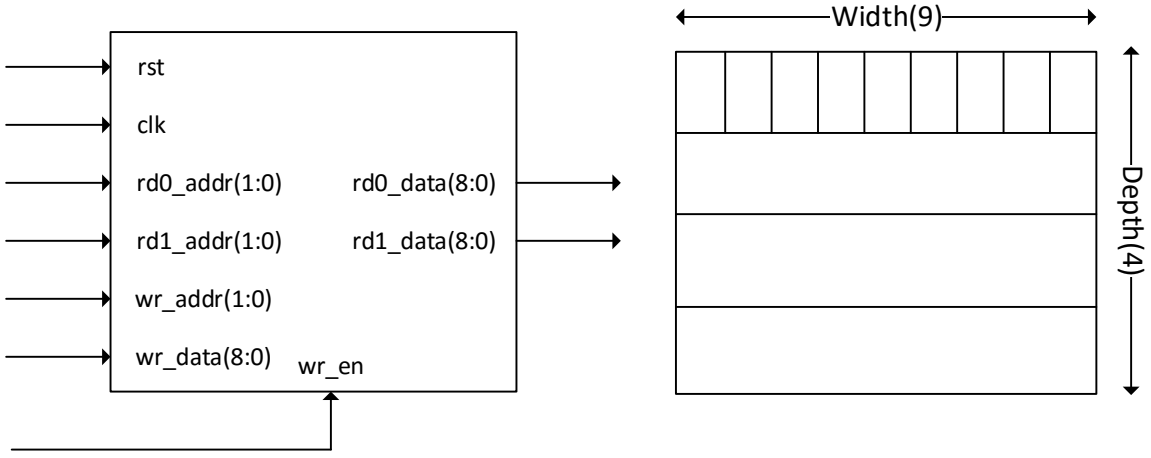

Figure 1: (a) Register file interface (b) Register file dimensions

Please run your code using the Verilog simulator that is part of Vivado and make sure there are no syntax errors in your code.

You should submit your Verilog code and testbench as separate files.

2 Create Test Vectors

Create a set of test vectors for the ALU-Regfile module that could test 1) writing values to the register file, 2) different mux configurations and outputs, and 3) possible ALU outputs. (It is fine if you do not simulate all possible ALU operations.) Explain the function of your test vectors.

Consider Figure 2 of your lab write up when you design your test vectors. Each wire in the diagram should be tested.