EECE2323 **Digital Logic Design Lab** **Prelab 1**

Eight Bit Adder

Begin by reading Sections 1 and 2 of your lab manual. Then answer the following questions. Submit your answers on Blackboard before the deadline.

1. Complete the table below for the expected input and output values for the 8 bit adder circuit you are describing in lab 1. Note that the syntax used for constant values is from Verilog; a,b and f are two's complement number.

a	b	f	ovf
8'd0	8'd0		
8'd12	8'd34		
-8'd12	-8'd34		
8'd100	-8'd50		
-8'd100	8'd50		
8'd100	8'd100		
-8'd100	-8'd100		

   Note: `8'` indicates 8 bits in verilog and d indicates the value is decimal.

2. Write a Boolean or verilog equation for the overflow output `ovf` based on input values `a` and `b`. Your equation can also incorporate output `f`.

3. A good simulation testbench tests that every input and output bit can take the values zero and one. For the values in question 1 answer the following questions:

   (a) The adder has 16 bits of input and 9 bits of output. Do the values in question 1 taken together set every input bit to both one and zero and every output bit to both one and zero? Explain your answer. Identify which bits are not tested in this manner.

   (b) Add additional input (`a` and `b`) values that test every bit in both the inputs and outputs so that every bit takes either a zero or a one value in your test cases.