Lab 1: 8-bit Adder

EECE 2323 – Prof. Miriam Leeser

By: Alex Oswald Due: 09/25/2020

§ 3.2 – Entering Your Design eightbit adder.v

```
1. `timescale 1ns / 10ps
3. // Company:
              EECE 2323: Lab for EECE 2322
4. // Engineer: Alex Oswald
5. //
6. // Create Date: 09/22/2020 11:39:48 AM
7. // Module Name: eightbit adder
9.
10.
11. module eightbit_adder(
12.
      input [7:0] a,
13.
14.
     input [7:0] b,
      output [7:0] f,
15.
16.
     output ovf
17.
      );
18.
19.
      assign f = a + b;
     assign ovf = (a[7] \&\& b[7] \&\& \sim f[7]) \mid | (\sim a[7] \&\& \sim b[7] \&\& f[7]);
20.
21.
22. endmodule
```

§ 3.3 – Entering Your Design adder8_tb.v

```
1. `timescale 1ns / 10ps
3. // Company:
             EECE 2323: Lab for EECE 2322
4. // Engineer: Alex Oswald
5. //
6. // Create Date: 09/22/2020 11:58:54 AM
7. // Module Name: adder8 tb
9.
10.
11. module adder8 tb ();
12. reg signed [7:0] a;
     reg signed [7:0] b;
13.
14.
     wire signed [7:0] f;
15.
     wire ovf;
16.
17.
     eightbit adder uut
18.
        (.a(a),
19.
         .b(b),
20.
         .f(f),
21.
         .ovf(ovf));
22.
      // Test Vectors
23.
24.
      initial
25.
        begin
26.
        #10 a = 8'd0; b = 8'd0;
         #10 a = 8'd12; b = 8'd34;
27.
        #10 a = -8'd12; b = -8'd34;
28.
```

```
29. #10 a = 8'd100; b = -8'd50;

30. #10 a = -8'd100; b = 8'd50;

31. #10 a = 8'd100; b = 8'd100;

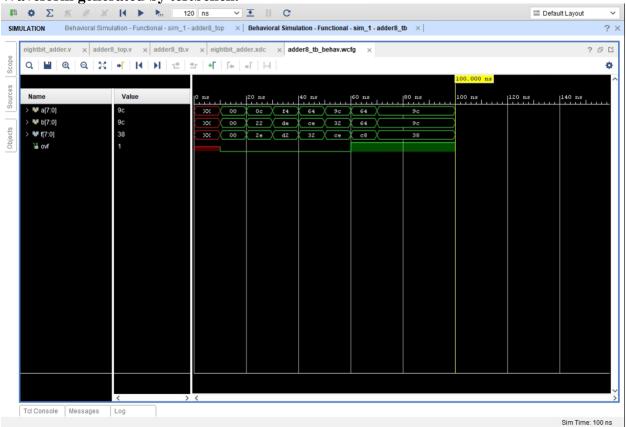
32. #10 a = -8'd100; b = -8'd100;

33. end

34.

35. endmodule
```

Waveform generated by testbench.



§ 4.2.3 – Testing the 8-bit adder in Hardware: Testing your Design in Hardware **See attached video on Canvas.**