**Lab Assignment 8**

Due: 01 Dec 2020

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EECE 2323

**Verilog Code for pdatapath\_top\_lab7.v:**

[insert code bb]

**VIO Output Visualization:**

Evidence is located in attached **lab7-test.mov** file. The following sequence of instructions was followed via a mycode.coe coefficient file.

clr $0 (0xD000)

clr $1 (0xD140)

clr $2 (0xD280)

clr $3 (0xD3C0)

addi $1, $0, 0x10 (0x3110)

sw $0, 0x4($1) (0x1404)

addi $2, $0, 0x0F (0x320F)

sw $0, 0x5($2) (0x1805)

clr $0 (0xD000)

clr $1 (0xD140)

clr $2 (0xD280)

clr $3 (0xD3C0)

lw $1, 0x5($0) (0x0105)

lw $2, 0x4($0) (0x0204)

add $3, $1, $2 (0x26C0)

sw $0, 0x11($3) (0x1C11)

clr $0 (0xD000)

clr $1 (0xD140)

clr $2 (0xD280)

clr $3 (0xD3C0)

lw $1, 0x5($0) (0x0105)

inv $2, $1 (0x4180)

addi $3, $2, 0x01 (0x3B01)

sw $0, 0x12($3) (0x1C12)

clr $0 (0xD000)

clr $1 (0xD140)

clr $2 (0xD280)

clr $3 (0xD3C0)

lw $1, 0x4($0) (0x0104)

lw $2, 0x12($0) (0x0212)

inv $1, $1 (0x4140)

addi $1, $1, 0x1 (0x3501)

add $3, $1, $2 (0x26C0)

sw $0, 0x13($0) (0x1013)