**COL216 Computer Architecture** **Quiz 3** **04.04.2022**

**Q 1.** Consider a virtual memory system with the page table stored in physical memory. The system has one level physically addressed cache and a TLB. What would be the best case and worst-case timings for making a read access? Give answer in terms of access times of cache, TLB, main memory, secondary storage and any other relevant parameter.

**Solution:**

Best case:
- TLB access (result = hit)
- cache access (result = hit)

Worst case:
- TLB access (result = miss)
- cache access for PT (result = miss)
- memory access for missing block of PT and PT look-up (result = page fault)
- page transfer from secondary storage
- cache access for data/instruction (result = miss)
- memory access for missing block containing data/instruction

**Q 2.** In response to an interrupt, while transferring control to an ISR, usually further interrupts are disabled by the hardware. If the ISR wants to permit nested interrupts, it has to explicitly enable these. What could be the reason for this? Why not keep the interrupts enabled and leave these to be disabled by ISR if it does not want to permit nested interrupts?

**Solution:**

An interrupt results in transfer of control to ISR. There is a possibility of another interrupt coming soon after. If this happens before ISR can save LR and other crucial registers, there could be irrecoverable loss of information. To prevent this, further interrupts are automatically disabled by hardware as control gets transferred to ISR in response to some interupt. ISR can explicitly enable interrupts, if required, after securing the crucial information.

**Q 3.** Consider a memory connected to a processor/cache through AMBA-Lite bus. The memory can supply the first word in 4 cycles and up to three subsequent words from consecutive addresses in one cycle each. Find the ratio of throughputs (words transferred per sec) for reading 16 word blocks using burst transfer and without burst transfer.

**Solution:**

Without burst transfer:
1 cycle for address phase of first word + 4x16 cycles of data phase of 16 words
= total 65 cycles (address phase of words 2 - 15 overlaps with data phase)

With burst transfer:
1 cycle for address phase of first word + (4 + 3x1) cycles of data phase of first 4 words
(4 + 3x1) cycles of data phase of words 5 - 8
(4 + 3x1) cycles of data phase of words 9 - 12
(4 + 3x1) cycles of data phase of words 13 - 16
= total 29 cycles (address phase of words 2 - 15 overlaps with data phase)

Ratio = 29/65