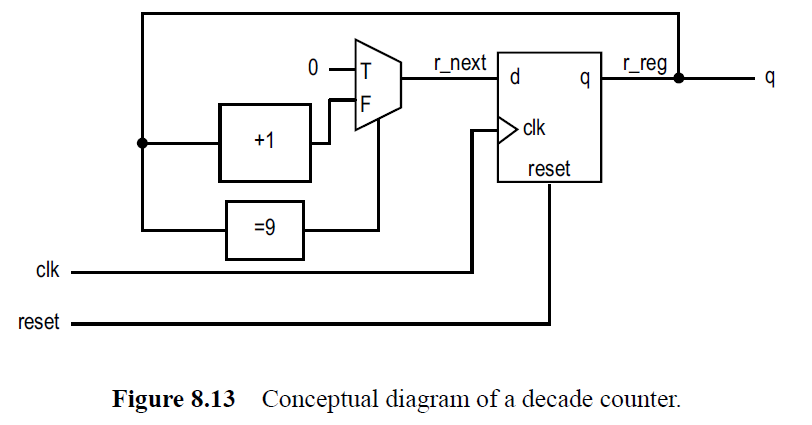
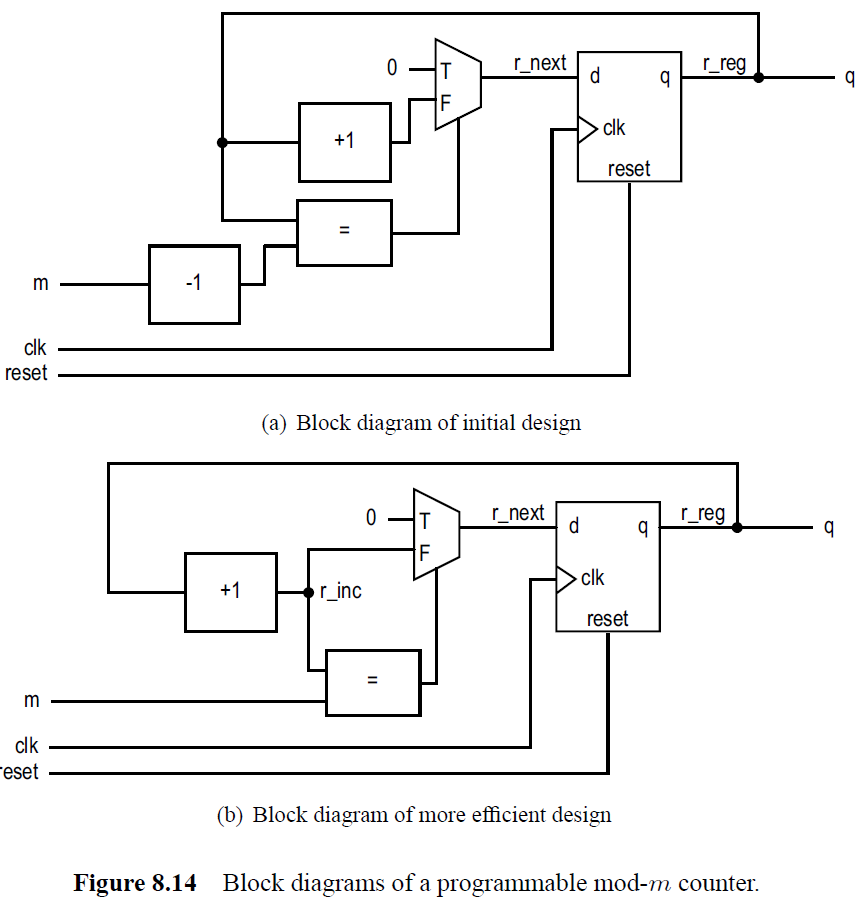
# Homework Assignment

1. [8.11] Consider the block diagram below. Let *Tcq* and *Tsetup* of the D FF be 1 and 0.5 ns, and the propagation delays of the incrementor, comparator, and multiplexer be 5, 3, and 0.75 ns respectively. Assume that no further optimization will be performed during synthesis. Determine the maximal clock rate.



1. [8.12] Consider the two block diagrams (below) of the mod-*m* counter. Let *Tcq* and *Tsetup* of the D FF be 1 and 0.5 ns, and the propagation delays of the incrementor, comparator, and multiplexer be 5, 3, and 0.75 ns respectively. Assume that no further optimization will be performed during synthesis. Determine the maximal clock rates of the two configurations.



# Turn-In Requirements

1. Answers to the above questions
2. Simulation screenshots and source code where appropriate.