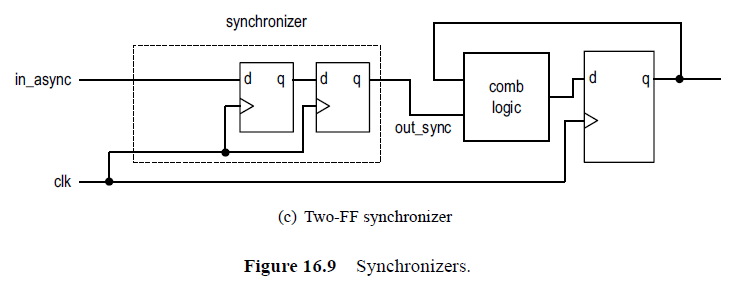
# Homework Assignment

1. [16.1] Assume that a sequential system with an ideal clock signal can operate at a maximal clock rate of 100 MHz. If the physical clock distribution network introduces a 1.5-ns clock skew, what is the new maximal clock rate?
2. [16.2] Consider a D FF with and .
   1. If we improve the D FF by reducing by 10%, discuss the effect on MTBF.
   2. If we improve the D FF by reducing by 10%, discuss the effect on MTBF.
3. [16.4] A two-FF synchronizer is shown in the below diagram. Determine the new MTBF for below scenarios assuming the following parameters:

|  |  |
| --- | --- |
|  |  |

* 1. The placement and routing process adds a 2.5-ns wiring delay.
  2. The system clock rate is decreased by 10%.
  3. The setup time of the D FF is reduced by 10%.
  4. The of the D FF is reduced by 10%.



# Turn-In Requirements

1. Answers to the above questions
2. Simulation screenshots and source code where appropriate.