# Homework Assignment

1. [11.5] Repetitive-subtraction division is an algorithm to implement division operation. Ley a and b be the dividend and divisor respectively. This algorithm obtains the quotient (q) and the remainder (r) by subtracting b from a repeatedly until the remaining of a is smaller than b. Assume that all signals are 8-bits wide and interpreted as unsigned integers.
   1. Derive a pseudo algorithm.
   2. ~~Convert the pseudo algorithm into an ASMD chart.~~
   3. Derive a detailed conceptual diagram.
   4. Derive the VHDL code according to the blocks of the conceptual diagram (i.e., in multi-segment style).
   5. ~~Derive the VHDL code in two-segment style.~~
   6. Is this an efficient algorithm? Explain.

# Turn-In Requirements

1. Answers to the above questions
2. Simulation screenshots and source code where appropriate.