# Homework Assignment

1. Consider a counter that counts from *m* to *n* and then wraps around. Derive VHDL code for the counter. Use generics, M and N, for *m* and *n* of the counter. You may also use a WIDTH parameter for the size of the output. The input signals are clk, reset, and en. The output signal is q. Write a testbench to test the functionality.
2. Derive a function that converts the std\_logic data type into the Boolean data type. The value ‘1’ and ‘H’ will return true, all other values return false. Place this function in a package called helper\_functions. Write a testbench to verify functionality.

# Turn-In Requirements

1. Answers to the above questions
2. Simulation screenshots and source code where appropriate.