Laboratory work 6

CONTROLLER DESIGN IN FREQUENCY DOMAIN BASED ON SECOND ORDER SYSTEM

- part 2 -

1. THE GOALS

- To follow and to understand the design method steps
- To check the resulting performance indicators;

2. THEORETICAL BACKGROUND

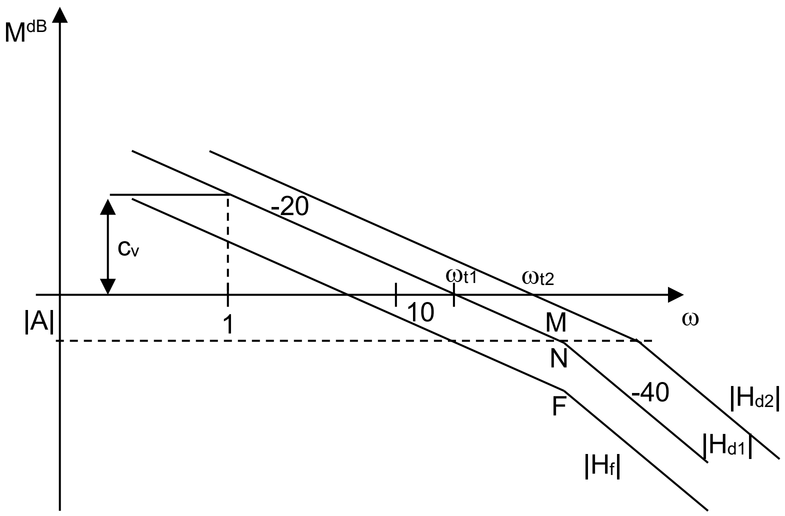
The logarithmic diagrams methods allow a hand over, convenient and direct design of controllers. These advantages are emphasized only if the process has the particular form:

$$H_f(s) = \frac{K_f}{s(T_f s + 1)}.$$

The imposed performance specifications are:

$$\begin{cases} \varepsilon_{stp}^* = 0 \\ \sigma^* \le \sigma \\ t_r^* \le t_r \\ c_v^* \ge c_v \\ \Delta\omega_B^* \le \Delta\omega_B \end{cases}$$

2.1. PD controller design steps



A P controller is first designed and the performance criteria are tested. Assume the settling time is too large and all other performance criteria are fulfilled. In this case a PD controller is useful:

$$H_{PD} = V_R \frac{1 + \tau_D s}{1 + T_N s}$$

In order to determine the controller parameters, ω_{t1} is estimated and $t_r = \frac{2}{\xi^2 \omega_{t1}}$. From $t_r^* = \frac{2}{\xi^2 \omega_{t2}}$ results $\omega_{t2} = \omega_{t1} \frac{t_r}{t_r^*}$. The new cutting frequency $\omega = \omega_{t2}$ is placed on the frequency axis; this is the cutting frequency for the new open loop transfer function:

$H_{d2}(s)=H_f(s)*H_p(s)*H_{PD}(s)$. The shifting to the right of the structure $H_{d1}(s)=H_f(s)*H_p(s)$ requires a PD controller. The parameters are:

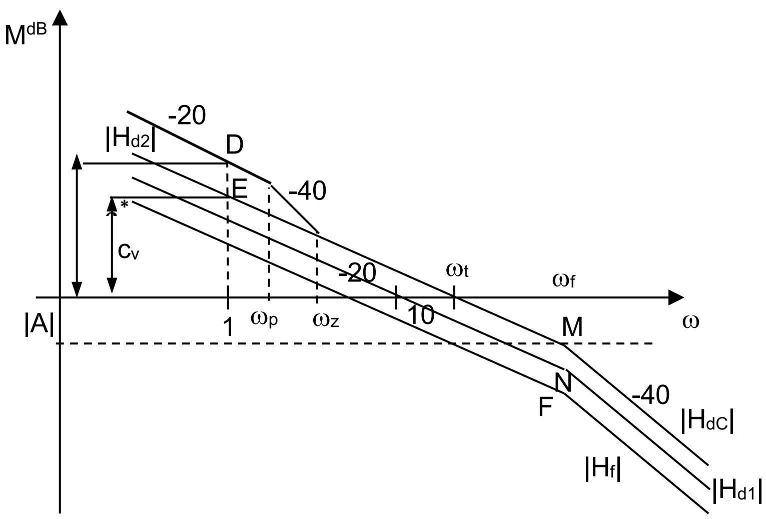
$$V_R|_{dB} = \overline{MN}$$
$$\tau_d = T_f$$
$$T_N = \tau_d \frac{t_r^*}{t_r}$$

The bandwidth, has to be checked, all other performance specifications being fulfilled.

2.2. PID controller design steps

Having a strict performance specifications set, a simple P controller can't fulfill all of them, moreover, neither a PD or PI controller can't solve the problem. In this case a PID controller is recommended, with the structure:

$$H_R(s) = V_R \frac{1+s\tau_d}{1+sT_N} \cdot \frac{1+sT_z}{1+sT_P}.$$



The design starts with the design of a P controller:

- The Bode diagram for $H_f(j\omega)$ is represented first
- (ξ) is determined from the overshoot and then $|A|$, resulting the point N and the structure H_{d1}. The performance criteria are evaluated. The settling time is larger and the velocity coefficient is smaller. A P controller cannot meet all these performance criteria.
- The new cutting frequency for the PD controller that corrects the settling time is computed next (ω_{t2}) and the structure (H_{d1}) is shifted to the right untill (H_{d2})
- The velocity coefficient (c_v) is determined given by H_{d2}. In the event that the velocity coefficient is still too small, a PI controller is deisgned:
- The corner frequency for the zero and pole are computed $\begin{cases} \omega_z \approx 0{,}1\omega_{t2} \\ \omega_p = \dfrac{c_v}{c_v^*}\omega_z \end{cases}$

resulting the complete structure (H_{dC}), in which the modified PI structure is added too, resulting in a final PID controller.
The controller parameters are:

$$\begin{cases} V_R\big|_{dB} = \overline{DE} + \overline{MF} \\ T_z = \dfrac{1}{\omega_z} = \dfrac{1}{0{,}1\omega_t} \\ T_P = \dfrac{1}{\omega_P} = \dfrac{1}{\omega_z} \cdot \dfrac{c_v^*}{c_v} \\ \tau_d = T_f \\ T_N = \tau_d \dfrac{\omega_{t2}}{\omega_{t1}} \end{cases}$$

The V_R gain as computed above contains all three controller gains, $V_R=V_{RP}*V_{RPI}*V_{RPD}$. From the performance indices, only the bandwidth must be checked, all other being fulfilled.

3. PROBLEMS

For the process having the transfer function

$$H_f(s) = \frac{3.5}{s(0.5s+1)}$$

and the performance indices sets

$$\text{a)} \begin{cases} \varepsilon_{stp}^* = 0 \\ \sigma^* \le 10\% \\ t_r^* \le 3[\text{sec}] \\ c_v^* \ge 2 \\ \Delta\omega_B^* \le 15[\text{rad/sec}] \end{cases} \qquad \text{respectively} \qquad \text{b)} \begin{cases} \varepsilon_{stp}^* = 0 \\ \sigma^* \le 10\% \\ t_r^* \le 1[\text{sec}] \\ c_v^* \ge 6 \\ \Delta\omega_B^* \le 15[\text{rad/sec}] \end{cases}$$

Following the steps described above, design a PD and a PID controller. Simulate the output of the closed loop for a step and ramp input to highlight the performance indices.