e-SOM_i.MX6 - System - On - Module

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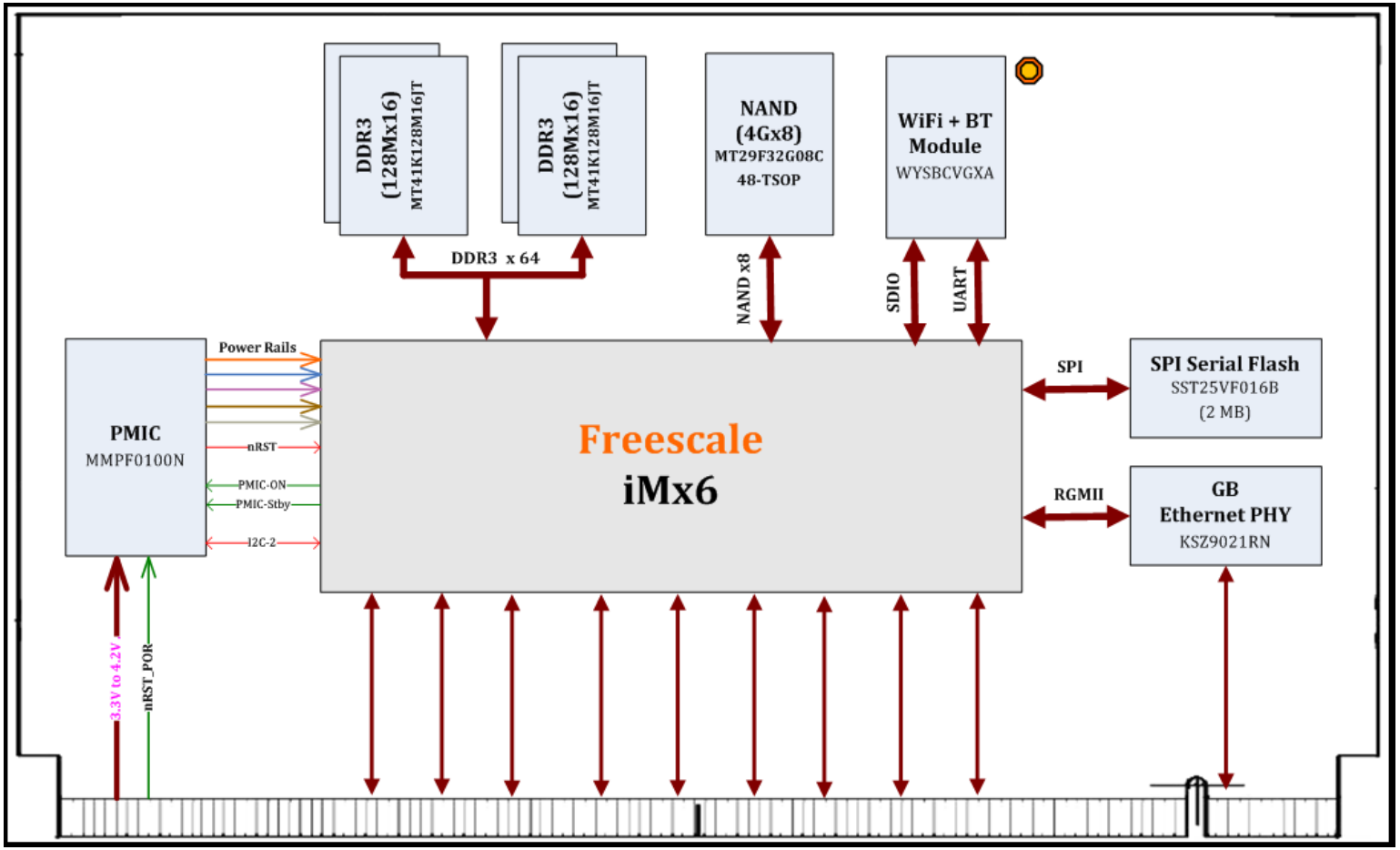

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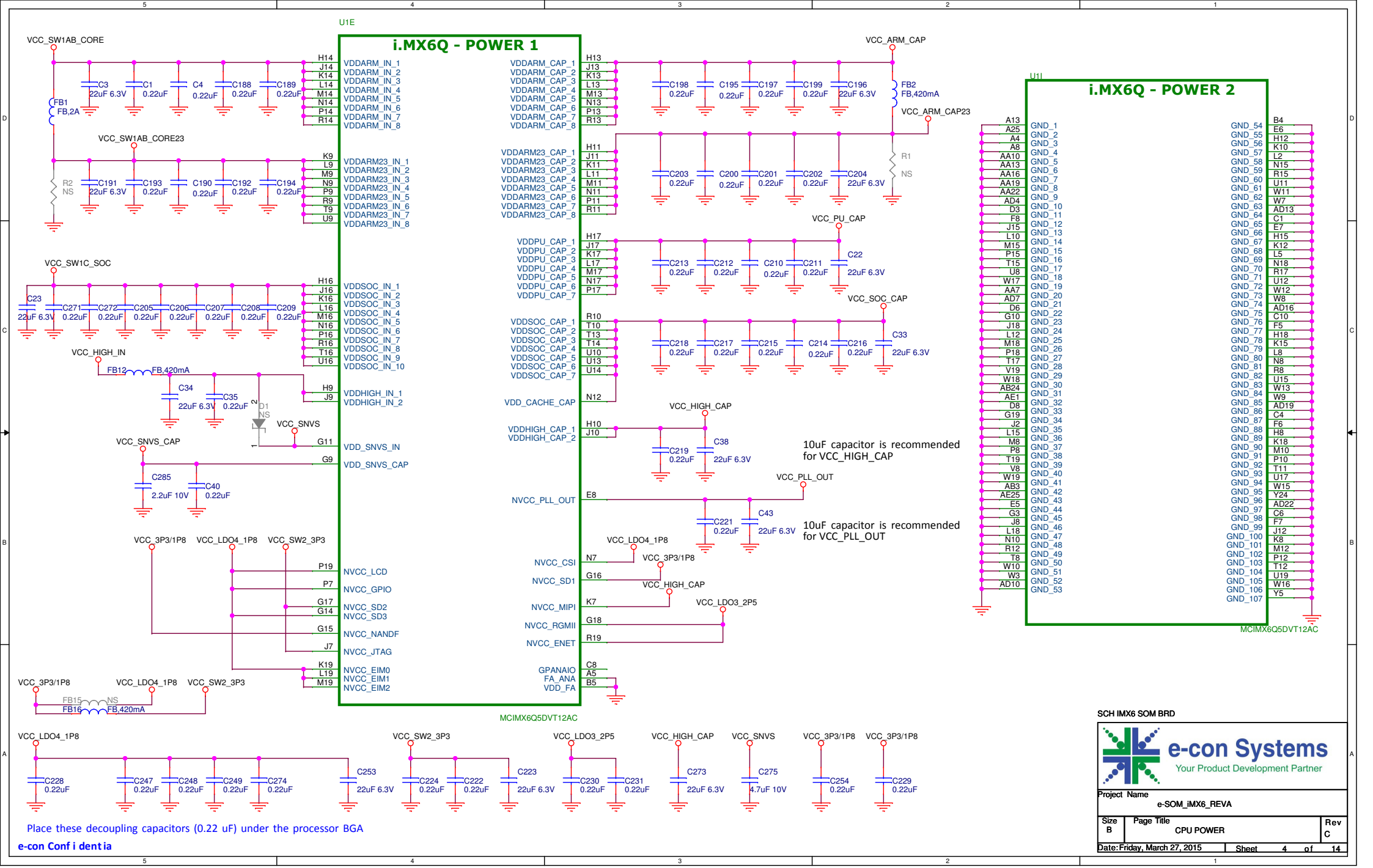
U1E
i.MX6Q - POWER 1
VCC_SW1AB_CORE
VCC_SW1AB_CORE23
VCC_SW1C_SOC
VCC_HIGH_IN
VCC_SNVS_CAP
VCC_ARM_CAP
VCC_ARM_CAP23
VCC_PU_CAP
VCC_SOC_CAP
VCC_HIGH_CAP
VCC_PLL_OUT
VCC_SNVS
VCC_3P3/1P8
VCC_LDO4_1P8
VCC_SW2_3P3
VCC_LDO3_2P5
VDDARM_IN_1
VDDARM_IN_2
VDDARM_IN_3
VDDARM_IN_4
VDDARM_IN_5
VDDARM_IN_6
VDDARM_IN_7
VDDARM_IN_8
VDDARM23_IN_1
VDDARM23_IN_2
VDDARM23_IN_3
VDDARM23_IN_4
VDDARM23_IN_5
VDDARM23_IN_6
VDDARM23_IN_7
VDDARM23_IN_8
VDDSOC_IN_1
VDDSOC_IN_2
VDDSOC_IN_3
VDDSOC_IN_4
VDDSOC_IN_5
VDDSOC_IN_6
VDDSOC_IN_7
VDDSOC_IN_8
VDDSOC_IN_9
VDDSOC_IN_10
VDDHIGH_IN_1
VDDHIGH_IN_2
VDD_SNVS_IN
VDD_SNVS_CAP
NVCC_LCD
NVCC_GPIO
NVCC_SD2
NVCC_SD3
NVCC_NANDF
NVCC_JTAG
NVCC_EIM0
NVCC_EIM1
NVCC_EIM2
VDDARM_CAP_1
VDDARM_CAP_2
VDDARM_CAP_3
VDDARM_CAP_4
VDDARM_CAP_5
VDDARM_CAP_6
VDDARM_CAP_7
VDDARM_CAP_8
VDDARM23_CAP_1
VDDARM23_CAP_2
VDDARM23_CAP_3
VDDARM23_CAP_4
VDDARM23_CAP_5
VDDARM23_CAP_6
VDDARM23_CAP_7
VDDARM23_CAP_8
VDDPU_CAP_1
VDDPU_CAP_2
VDDPU_CAP_3
VDDPU_CAP_4
VDDPU_CAP_5
VDDPU_CAP_6
VDDPU_CAP_7
VDDSOC_CAP_1
VDDSOC_CAP_2
VDDSOC_CAP_3
VDDSOC_CAP_4
VDDSOC_CAP_5
VDDSOC_CAP_6
VDDSOC_CAP_7
VDD_CACHE_CAP
VDDHIGH_CAP_1
VDDHIGH_CAP_2
NVCC_PLL_OUT
NVCC_CSI
NVCC_SD1
NVCC_MIPI
NVCC_RGMII
NVCC_ENET
GPANAIO
FA_ANA
VDD_FA
MCIMX6Q5DVT12AC
U1I
i.MX6Q - POWER 2
MCIMX6Q5DVT12AC
10uF capacitor is recommended for VCC_HIGH_CAP
10uF capacitor is recommended for VCC_PLL_OUT
Place these decoupling capacitors (0.22 uF) under the processor BGA
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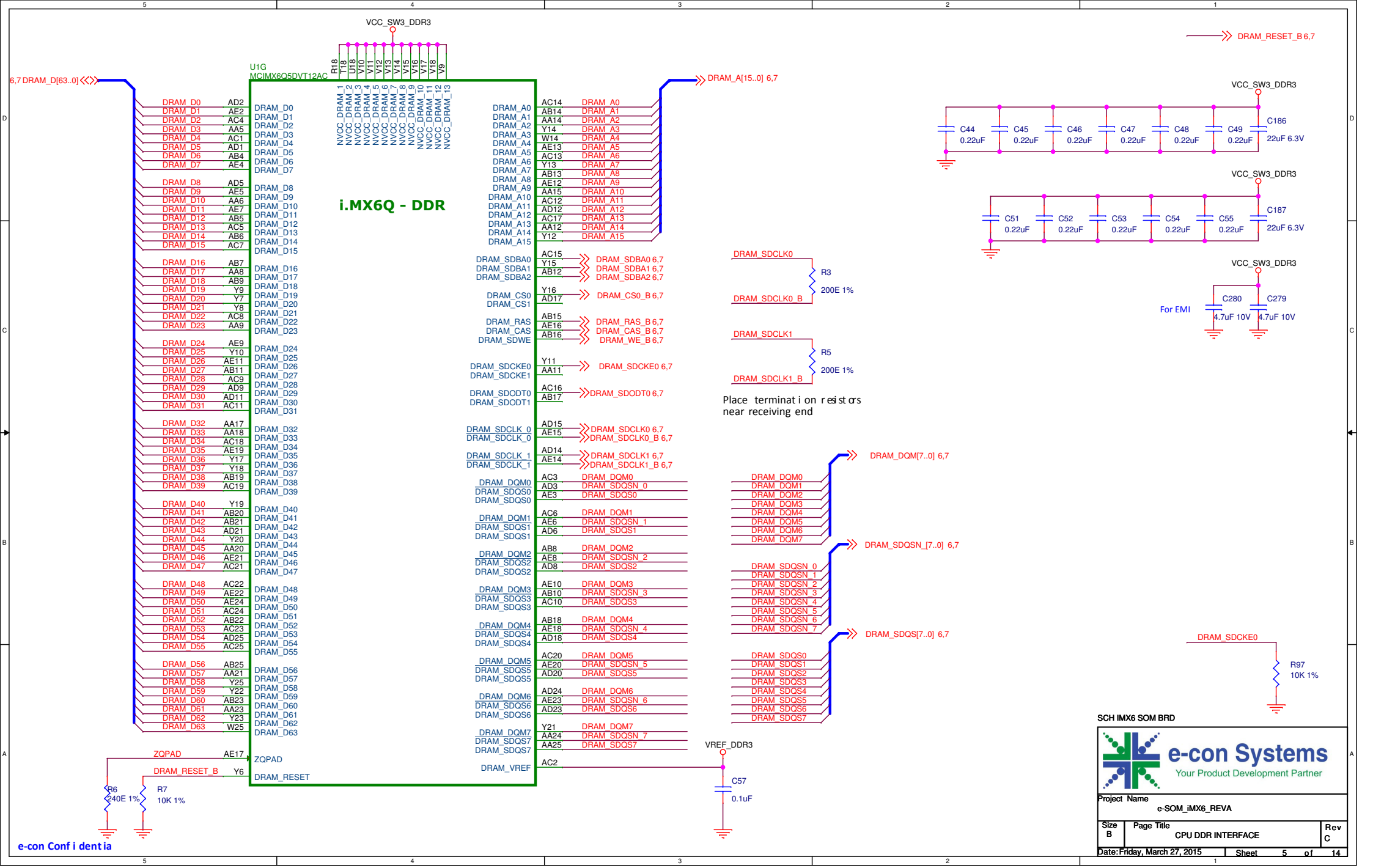
VCC_SW3_DDR3
U1G
MCIMX6Q5DVT12AC
i.MX6Q - DDR
DRAM_RESET_B 6,7
DRAM_A[15..0] 6,7
6,7 DRAM_D[63..0]
DRAM_SDCLK0
DRAM_SDCLK0_B
R3
200E 1%
DRAM_SDCLK1
DRAM_SDCLK1_B
R5
200E 1%
Place terminati on resistors near receiving end
DRAM_DQM[7..0] 6,7
DRAM_SDQSN_[7..0] 6,7
DRAM_SDQS[7..0] 6,7
DRAM_SDCKE0
R97
10K 1%
C44 0.22uF
C45 0.22uF
C46 0.22uF
C47 0.22uF
C48 0.22uF
C49 0.22uF
C186 22uF 6.3V
C51 0.22uF
C52 0.22uF
C53 0.22uF
C54 0.22uF
C55 0.22uF
C187 22uF 6.3V
For EMI
C280 4.7uF 10V
C279 4.7uF 10V
ZQPAD
DRAM_RESET_B
R6 240E 1%
R7 10K 1%
VREF_DDR3
C57 0.1uF
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CPU DDR INTERFACE
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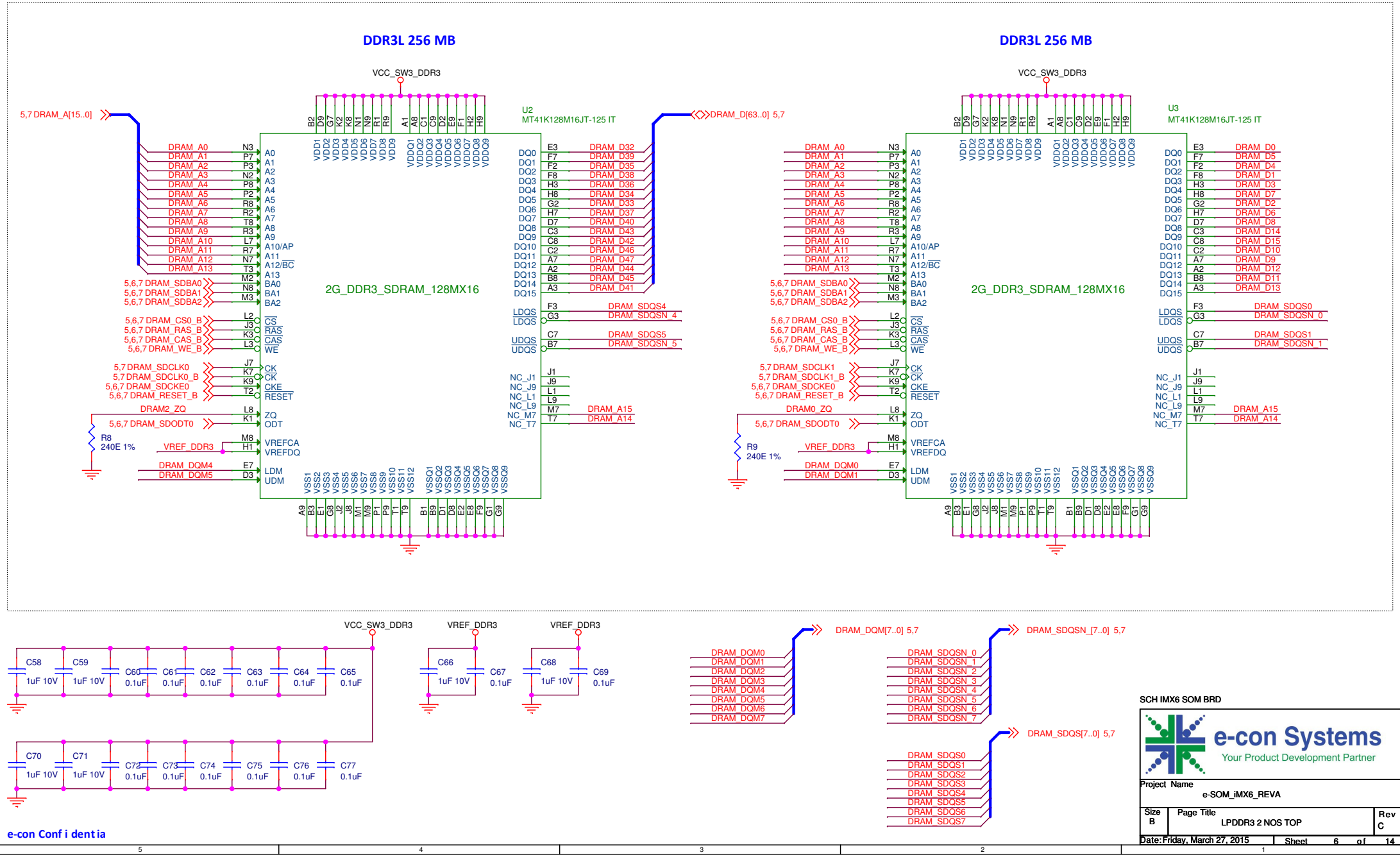
DDR3L 256 MB
VCC_SW3_DDR3
U2
MT41K128M16JT-125 IT
5,7 DRAM_A[15..0]
DRAM_D[63..0] 5,7
2G_DDR3_SDRAM_128MX16
5,7 DRAM_SDBA0
5,7 DRAM_SDBA1
5,7 DRAM_SDBA2
5,7 DRAM_CS0_B
5,7 DRAM_RAS_B
5,7 DRAM_CAS_B
5,7 DRAM_WE_B
5,7 DRAM_SDCLK0
5,7 DRAM_SDCLK0_B
5,7 DRAM_SDCKE0
5,7 DRAM_RESET_B
DRAM2_ZQ
5,7 DRAM_SDODT0
R8
240E 1%
VREF_DDR3
DRAM_DQM4
DRAM_DQM5
DRAM_SDQS4
DRAM_SDQSN_4
DRAM_SDQS5
DRAM_SDQSN_5
DRAM_A15
DRAM_A14
DDR3L 256 MB
VCC_SW3_DDR3
U3
MT41K128M16JT-125 IT
2G_DDR3_SDRAM_128MX16
5,7 DRAM_SDBA0
5,7 DRAM_SDBA1
5,7 DRAM_SDBA2
5,7 DRAM_CS0_B
5,7 DRAM_RAS_B
5,7 DRAM_CAS_B
5,7 DRAM_WE_B
5,7 DRAM_SDCLK1
5,7 DRAM_SDCLK1_B
5,7 DRAM_SDCKE0
5,7 DRAM_RESET_B
DRAM0_ZQ
5,7 DRAM_SDODT0
R9
240E 1%
VREF_DDR3
DRAM_DQM0
DRAM_DQM1
DRAM_SDQS0
DRAM_SDQSN_0
DRAM_SDQS1
DRAM_SDQSN_1
DRAM_A15
DRAM_A14
VCC_SW3_DDR3
VREF_DDR3
VREF_DDR3
C58 1uF 10V
C59 1uF 10V
C60 0.1uF
C61 0.1uF
C62 0.1uF
C63 0.1uF
C64 0.1uF
C65 0.1uF
C66 1uF 10V
C67 0.1uF
C68 1uF 10V
C69 0.1uF
C70 1uF 10V
C71 1uF 10V
C72 0.1uF
C73 0.1uF
C74 0.1uF
C75 0.1uF
C76 0.1uF
C77 0.1uF
DRAM_DQM[7..0] 5,7
DRAM_DQM0
DRAM_DQM1
DRAM_DQM2
DRAM_DQM3
DRAM_DQM4
DRAM_DQM5
DRAM_DQM6
DRAM_DQM7
DRAM_SDQSN[7..0] 5,7
DRAM_SDQSN_0
DRAM_SDQSN_1
DRAM_SDQSN_2
DRAM_SDQSN_3
DRAM_SDQSN_4
DRAM_SDQSN_5
DRAM_SDQSN_6
DRAM_SDQSN_7
DRAM_SDQS[7..0] 5,7
DRAM_SDQS0
DRAM_SDQS1
DRAM_SDQS2
DRAM_SDQS3
DRAM_SDQS4
DRAM_SDQS5
DRAM_SDQS6
DRAM_SDQS7
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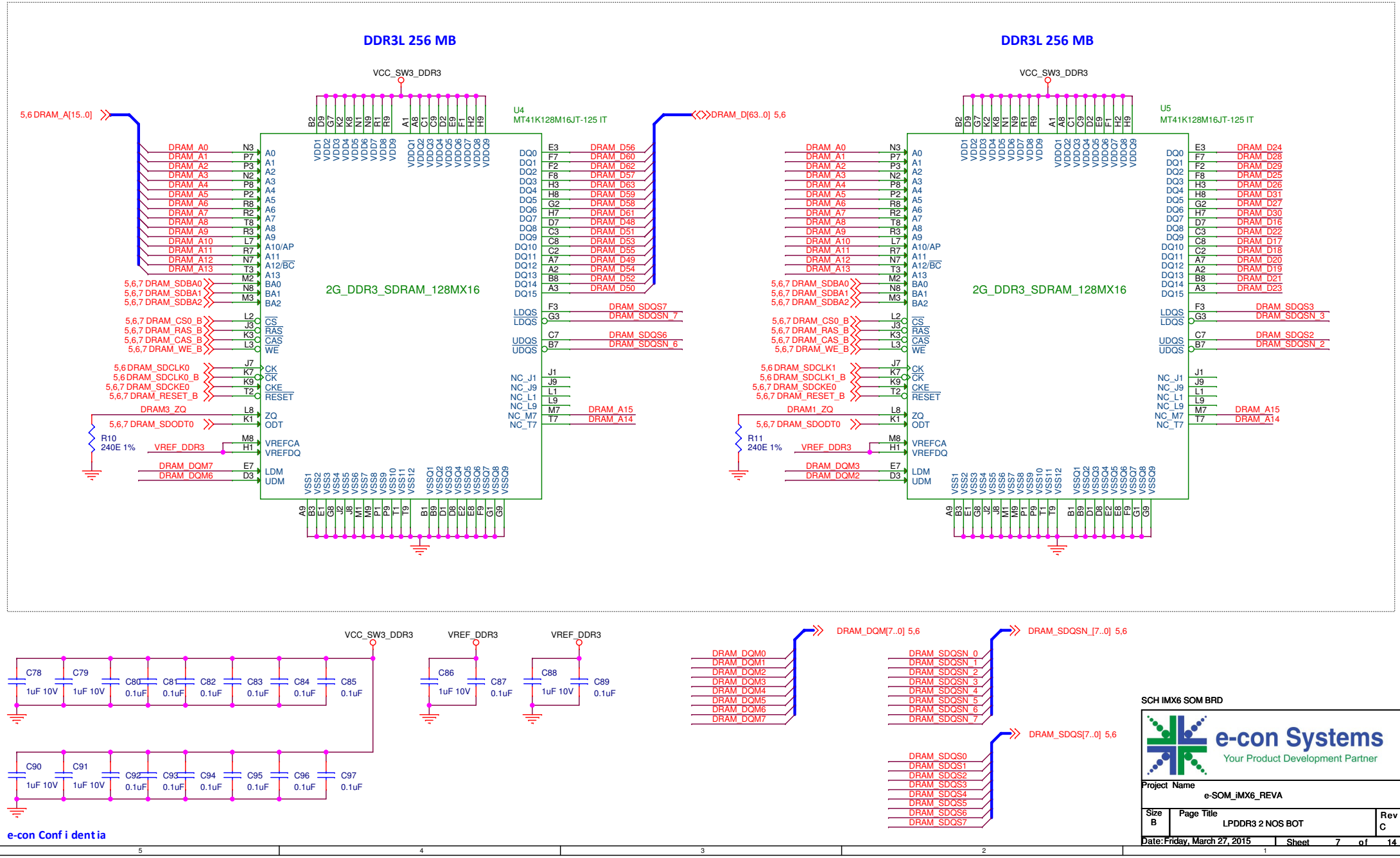
DDR3L 256 MB
VCC_SW3_DDR3
U4
MT41K128M16JT-125 IT
2G_DDR3_SDRAM_128MX16
5,6 DRAM_A[15..0]
DRAM_D[63..0] 5,6
5,6,7 DRAM_SDBA0
5,6,7 DRAM_SDBA1
5,6,7 DRAM_SDBA2
5,6,7 DRAM_CS0_B
5,6,7 DRAM_RAS_B
5,6,7 DRAM_CAS_B
5,6,7 DRAM_WE_B
5,6 DRAM_SDCLK0
5,6 DRAM_SDCLK0_B
5,6,7 DRAM_SDCKE0
5,6,7 DRAM_RESET_B
DRAM3_ZQ
5,6,7 DRAM_SDODT0
R10
240E 1%
VREF_DDR3
DRAM_DQM7
DRAM_DQM6
DRAM_SDQS7
DRAM_SDQSN_7
DRAM_SDQS6
DRAM_SDQSN_6
DRAM_A15
DRAM_A14
DDR3L 256 MB
VCC_SW3_DDR3
U5
MT41K128M16JT-125 IT
2G_DDR3_SDRAM_128MX16
5,6 DRAM_SDCLK1
5,6 DRAM_SDCLK1_B
5,6,7 DRAM_SDCKE0
5,6,7 DRAM_RESET_B
DRAM1_ZQ
5,6,7 DRAM_SDODT0
R11
240E 1%
VREF_DDR3
DRAM_DQM3
DRAM_DQM2
DRAM_SDQS3
DRAM_SDQSN_3
DRAM_SDQS2
DRAM_SDQSN_2
DRAM_A15
DRAM_A14
VCC_SW3_DDR3
VREF_DDR3
VREF_DDR3
C78 1uF 10V
C79 1uF 10V
C80 0.1uF
C81 0.1uF
C82 0.1uF
C83 0.1uF
C84 0.1uF
C85 0.1uF
C86 1uF 10V
C87 0.1uF
C88 1uF 10V
C89 0.1uF
C90 1uF 10V
C91 1uF 10V
C92 0.1uF
C93 0.1uF
C94 0.1uF
C95 0.1uF
C96 0.1uF
C97 0.1uF
DRAM_DQM[7..0] 5,6
DRAM_DQM0
DRAM_DQM1
DRAM_DQM2
DRAM_DQM3
DRAM_DQM4
DRAM_DQM5
DRAM_DQM6
DRAM_DQM7
DRAM_SDQSN[7..0] 5,6
DRAM_SDQSN_0
DRAM_SDQSN_1
DRAM_SDQSN_2
DRAM_SDQSN_3
DRAM_SDQSN_4
DRAM_SDQSN_5
DRAM_SDQSN_6
DRAM_SDQSN_7
DRAM_SDQS[7..0] 5,6
DRAM_SDQS0
DRAM_SDQS1
DRAM_SDQS2
DRAM_SDQS3
DRAM_SDQS4
DRAM_SDQS5
DRAM_SDQS6
DRAM_SDQS7
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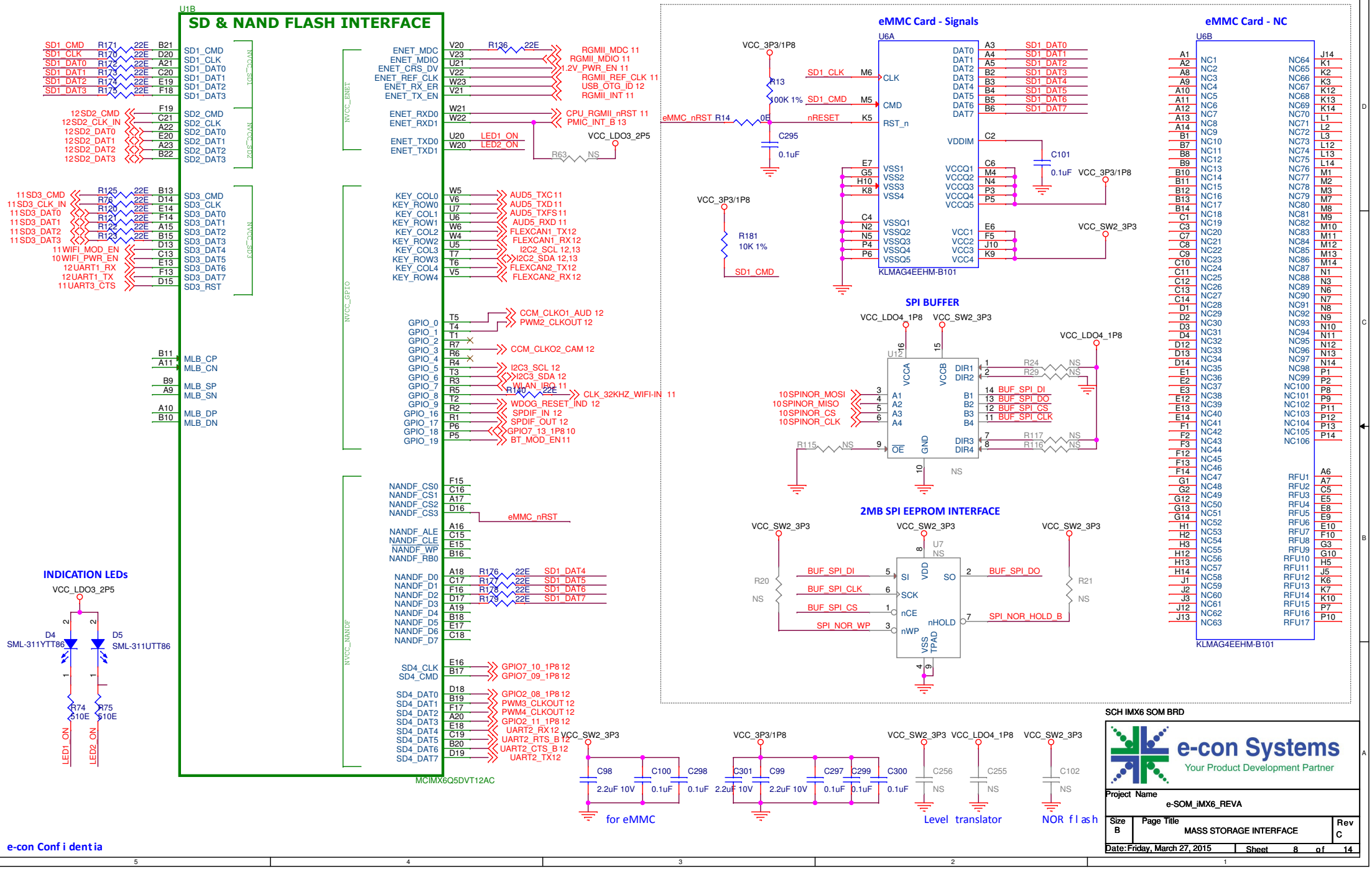
U1B
SD & NAND FLASH INTERFACE
MCIMX6Q5DVT12AC
eMMC Card - Signals
eMMC Card - NC
U6A
U6B
KLMAG4EEHM-B101
SPI BUFFER
2MB SPI EEPROM INTERFACE
INDICATION LEDs
VCC_LDO3_2P5
VCC_3P3/1P8
VCC_SW2_3P3
VCC_LDO4_1P8
for eMMC
Level translator
NOR f l ash
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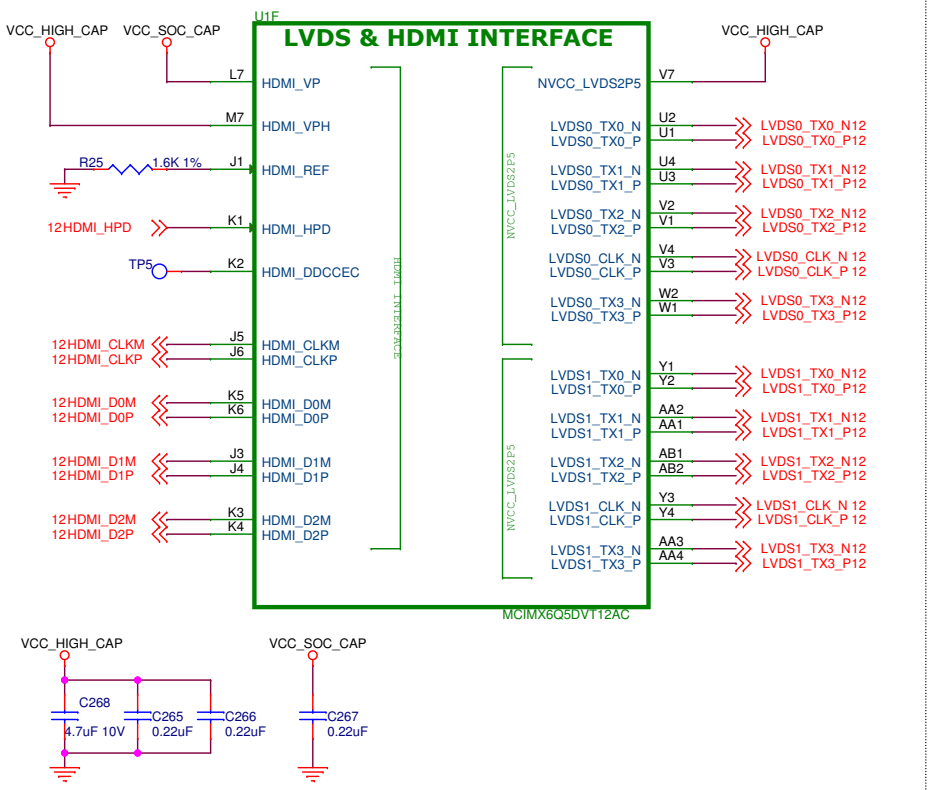
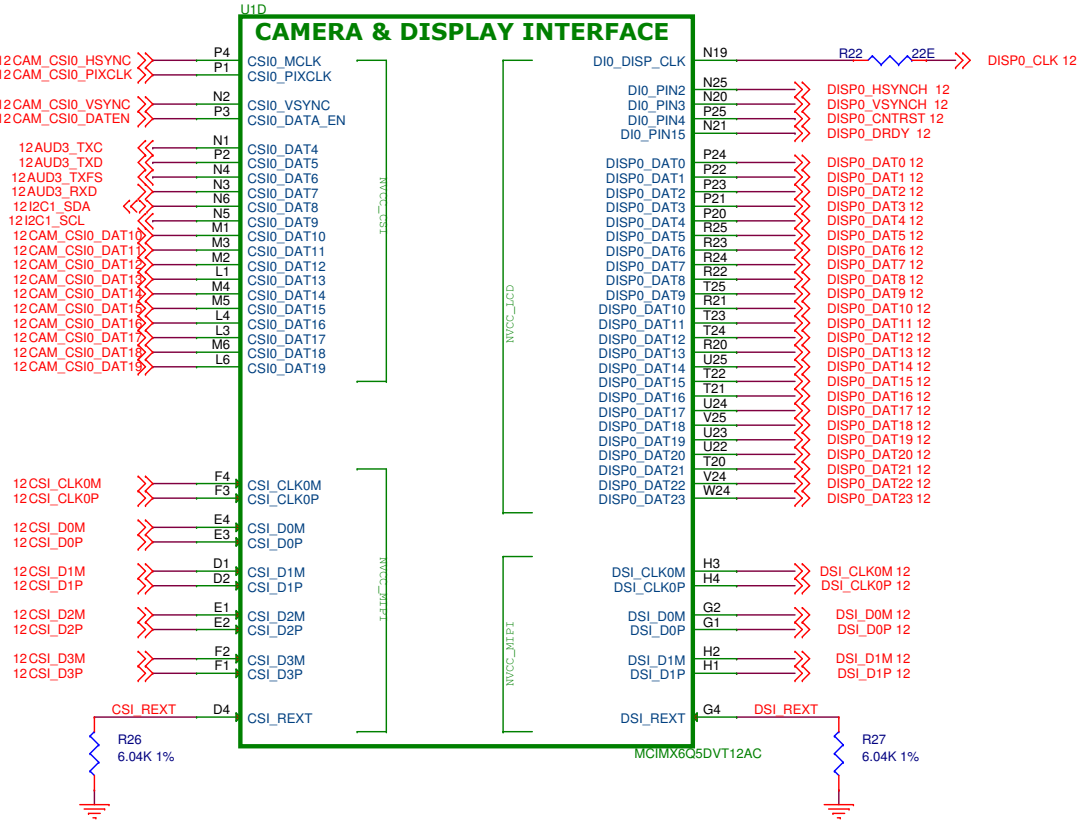
DISPLAY SERIAL INTERFACE



CAMERA & DISPLAY PARALLEL INTERFACE



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U1A

i.MX6Q - EIM

NVCC_EIM1

EIM_LBA	K22	CSPI2_CS1 12
EIM_OE	J24	CSPI2_MISO 12
EIM_RW	K20	CSPI2_CS0 12
EIM_CS0	H24	CSPI2_CLK 12
EIM_CS1	J23	CSPI2_MOSI 12
EIM_A16	H25	CAM_CSI1_PIXCLK 12
EIM_A17	G24	CAM_CSI1_DAT12 12
EIM_A18	J22	CAM_CSI1_DAT13 12
EIM_A19	G25	CAM_CSI1_DAT14 12
EIM_A20	H22	CAM_CSI1_DAT15 12
EIM_A21	H23	CAM_CSI1_DAT16 12
EIM_A22	F24	CAM_CSI1_DAT17 12
EIM_A23	J21	CAM_CSI1_DAT18 12
EIM_A24	F25	CAM_CSI1_DAT19 12
EIM_A25	H19	

NVCC_EIM0

EIM_D16	C25	R138 22E — SPINOR_CLK 8
EIM_D17	F21	SPINOR_MISO 8
EIM_D18	D24	SPINOR_MOSI 8
EIM_D19	G21	SPINOR_CS 8
EIM_D20	G20	INT_TIMER_2 12
EIM_D21	H20	USB_OTG_OC 12
EIM_D22	E23	USB_OTG_PWREN 12
EIM_D23	D25	UART3_RTS 11
EIM_D24	F22	UART3_TX 11
EIM_D25	G22	UART3_RX 11
EIM_D26	E24	EMERGENCY_SHDOWN 13
EIM_D27	E25	
EIM_D28	G23	BT_MOD_ACK 11
EIM_D29	J19	BT_MOD_WU 11
EIM_D30	J20	USB_HOST_OC 12
EIM_D31	H21	USB_HOST_PWREN 12

NVCC_EIM2

EIM_EB2	E22	R133 NS
EIM_EB3	F23	R167 NS
EIM_BCLK	N22	
EIM_WAIT	M25	R134 NS
EIM_EB0	K21	CAM_CSI1_DAT11 12
EIM_EB1	K23	CAM_CSI1_DAT10 12
EIM_DA0	L20	CAM_CSI1_DAT09 12
EIM_DA1	J25	CAM_CSI1_DAT08 12
EIM_DA2	L21	CAM_CSI1_DAT07 12
EIM_DA3	K24	CAM_CSI1_DAT06 12
EIM_DA4	L22	CAM_CSI1_DAT05 12
EIM_DA5	L23	CAM_CSI1_DAT04 12
EIM_DA6	K25	CAM_CSI1_DAT03 12
EIM_DA7	L25	CAM_CSI1_DAT02 12
EIM_DA8	L24	CAM_CSI1_DAT01 12
EIM_DA9	M21	CAM_CSI1_DAT00 12
EIM_DA10	M22	CAM_CSI1_DATEN 12
EIM_DA11	M20	CAM_CSI1_HSYNC 12
EIM_DA12	M24	CAM_CSI1_VSYNC 12
EIM_DA13	M23	GPIO3_13_1P8 12
EIM_DA14	N23	GPIO3_14_1P8 12
EIM_DA15	N24	GPIO3_15_1P8 12

MCIMX6Q5DVT12AC

U1H

HIGH SPEED INTERFACE

VCC_HIGH_CAP VCC_SOC_CAP

PCIE INTERFACE

PCIE_VP	H7	
PCIE_VPTX	G8	
PCIE_VPH	G7	
PCIE_REXT	A2	R28 200E 1%
CLK1_N	C7	12 PCIe_CLK1N
CLK1_P	D7	12 PCIe_CLK1P
PCIE_TXM	A3	C235 0.1uF — 12 PCIe_TXM
PCIE_TXP	B3	C236 0.1uF — 12 PCIe_TXP
PCIE_RXM	B1	12 PCIe_RXM
PCIE_RXP	B2	12 PCIe_RXP

SATA INTERFACE

VCC_HIGH_CAP VCC_SOC_CAP

SATA_VP	G13	R152 0E — SATA_VP
SATA_VPH	G12	R151 0E — SATA_VPH
SATA_RXP	B14	12 SATA_RXP
SATA_RXM	A14	12 SATA_RXM
SATA_TXP	A12	C242 10nF — 12 SATA_TXP
SATA_TXM	B12	C241 10nF — 12 SATA_TXM
SATA_REXT	C14	R31 191E 1%

RGMII INTERFACE

RGMII_TXC	D21	R77 22E — RGMII_TXCLK 11
RGMII_TD0	C22	RGMII_TXD0 11
RGMII_TD1	F20	RGMII_TXD1 11
RGMII_TD2	E21	RGMII_TXD2 11
RGMII_TD3	A24	RGMII_TXD3 11
RGMII_TX_CTL	C23	RGMII_TXEN 11
RGMII_RXC	B25	RGMII_RXCLK 11
RGMII_RD0	C24	RGMII_RXD0 11
RGMII_RD1	B23	RGMII_RXD1 11
RGMII_RD2	B24	RGMII_RXD2 11
RGMII_RD3	D23	RGMII_RXD3 11
RGMII_RX_CTL	D22	RGMII_RXDV 11

USB INTERFACE

VCC_USB_OTG

USB_OTG_VBUS	E9	
USB_OTG_DP	A6	USB_OTG_DP 12
USB_OTG_DN	B6	USB_OTG_DN 12
USB_OTG_CHD	B8	CHARGER_DETECT — TP3
USB_H1_VBUS	D10	VCC_SWBST_5
USB_H1_DP	E10	USB_HOST_DP 12
USB_H1_DN	F10	USB_HOST_DN 12
VDDUSB_CAP	F9	C103 22uF 6.3V — C286 0.22uF

MCIMX6Q5DVT12AC

USB_OTG_CHD_B: To info external PMIC a charger (D+/D- Short) is connected, it is open drain output

10uF capacitor is recommended for VDDUSB_CAP

Configure USB_OTG_PWREN, 1.2V_PWR_EN as open drain output

U1C

i.MX6Q - CONTROL

VDD_SNVS_IN

ONOFF	D12	12 CPU_POWER_ON
POR	C11	13 PMIC_nPWGOOD
BOOT_MODE0	C12	12 CPU_BOOT_MODE0
BOOT_MODE1	F12	12 CPU_BOOT_MODE1
TEST_MODE	E12	TEST_MODE
TAMPER	E11	TP2 TAMPER — R33 0E
PMIC_STBY_REQ	F11	13 PMIC_STBY_REQ
PMIC_ON_REQ	D11	13 PMIC_ON_REQ
XTALI	A7	CPU_XTALI
XTALO	B7	CPU_XTALO
RTC_XTALI	D9	RTC_XTALI
RTC_XTALO	C9	RTC_XTALO

NVCC_JTAG

JTAG_TCK	H5	JTAG_TCK R146 10K 1%
JTAG_TMS	C3	JTAG_TMS R147 10K 1%
JTAG_TDI	G5	JTAG_TDI R148 10K 1%
JTAG_TDO	G6	JTAG_TDO
JTAG_TRST	C2	nJTAG_TRST R149 10K 1%
JTAG_MOD	H6	JTAG_MOD

VCC_SW2_3P3

R102 4.7K

CLK2_N	C5	
CLK2_P	D5	

MCIMX6Q5DVT12AC

JTAG DEBUG CONNECTOR

CN3 — NS

VCC_SW2_3P3	1
JTAG_TCK	2
JTAG_TMS	3
JTAG_TDI	4
JTAG_TDO	5
nJTAG_TRST	6
PMIC_nPWGOOD	7
	8
	9
VCC_SW2_3P3	10

GPIO7_13_1P8 8

VCC_SNVS — R68 NS — PMIC_nPWGOOD

C284 4.7uF 10V

VCC_SOC_CAP: C260 0.22uF, C261 0.22uF, C262 0.22uF — SATA_VP

VCC_HIGH_CAP: C269 4.7uF 10V, C263 0.22uF, C264 0.22uF — SATA_VPH

For i.MX6 warm reset

PMIC_nPWGOOD R103 NS — CPU_RESET 12,13

Pull up to 4.7k for high noise environments

VCC_SNVS — R80 10K 1% — R81 10K 1%

CPU_BOOT_MODE0

CPU_BOOT_MODE1

24 MHz CRYSTAL FOR CPU

CPU_XTALI — R83 NS — CPU_XTALO

X2 (1, 2, 3, 4) 24MHz

R101 2.2M

C105 8pF — C106 8pF

32 KHz CRYSTAL FOR RTC

R98 NS

RTC_XTALI — X1 32.768KHz — RTC_XTALO

C107 18pF — C108 18pF

Q4 FDN306P

VCC_SYS_4P2 — VCC_WIFI_VBAT

R157 10K 1%

C288 1uF 10V — C292 4.7uF 10V

Q3 FDN327N

8 WIFI_PWR_EN

R163 100K 1%

R158 4.7K

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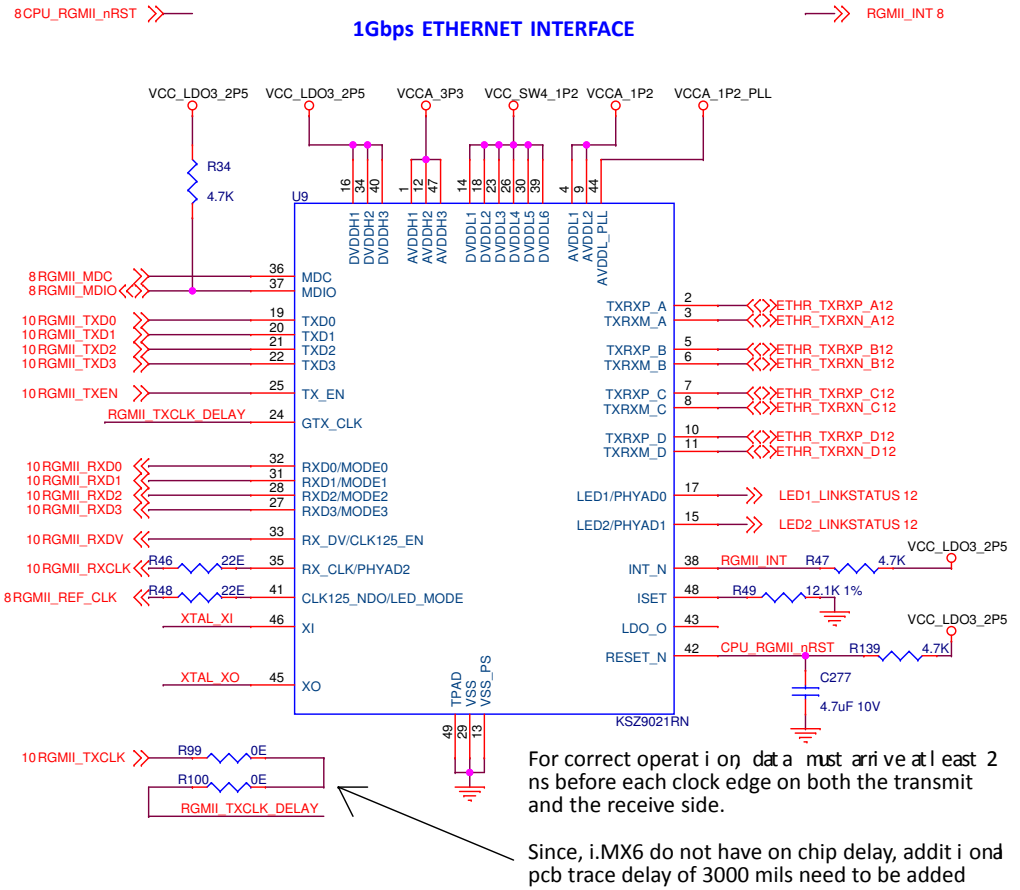
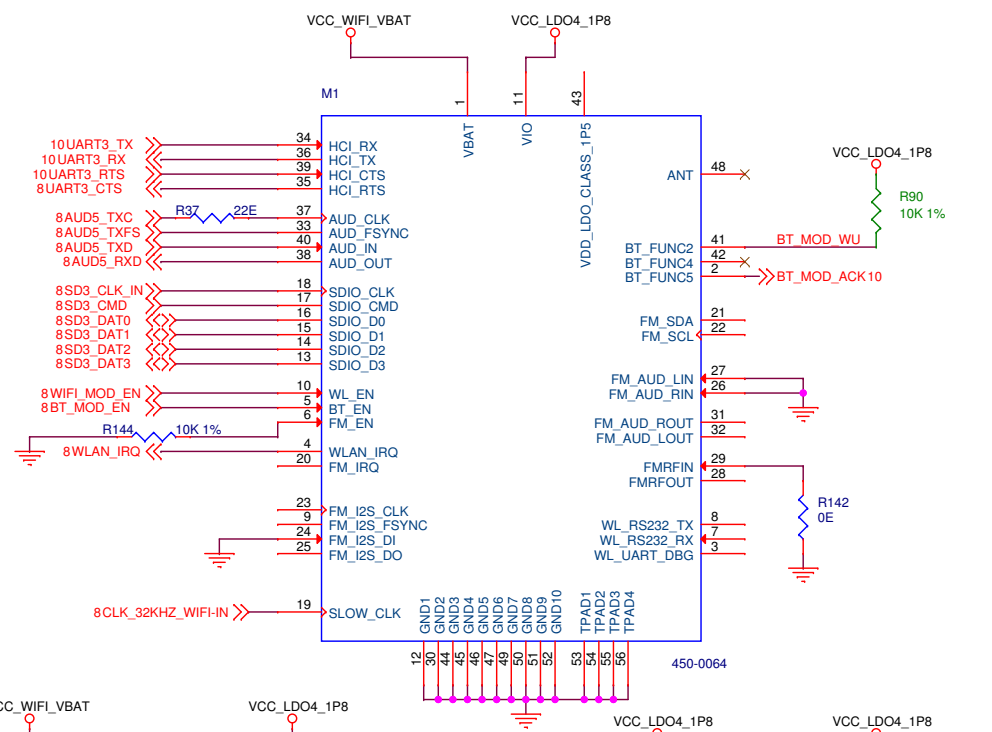
1Gbps ETHERNET INTERFACE



For correct operation data must arrive at least 2 ns before each clock edge on both the transmit and the receive side.

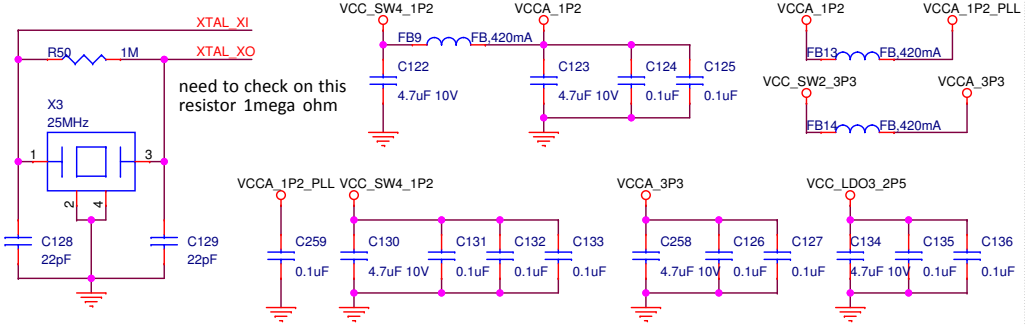
Since, i.MX6 do not have on chip delay, additional pcb trace delay of 3000 mils need to be added

WIFI + BLUETOOTH INTERFACE



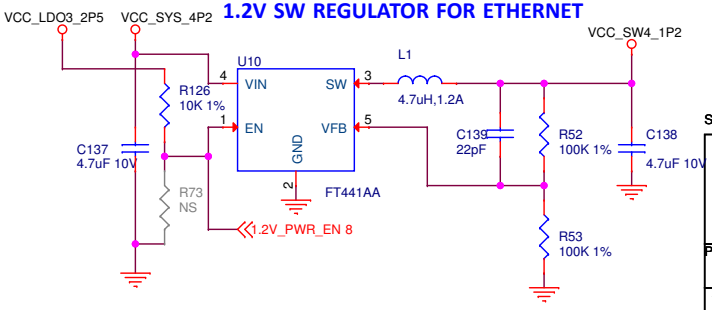
Place this decoupling capacitor near the power pin

Timing Circuit



Place this decoupling capacitor near the power pin

1.2V SW REGULATOR FOR ETHERNET



SCH IMX6 SOM BRD

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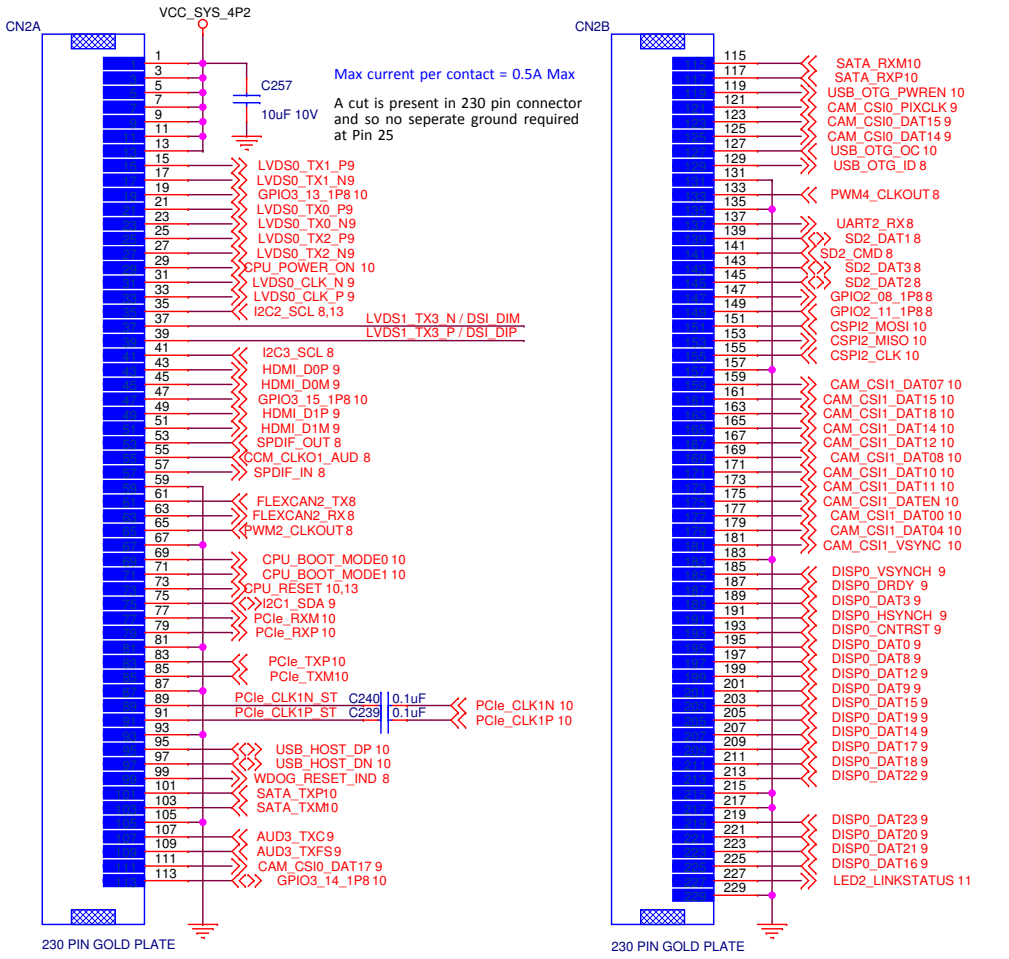
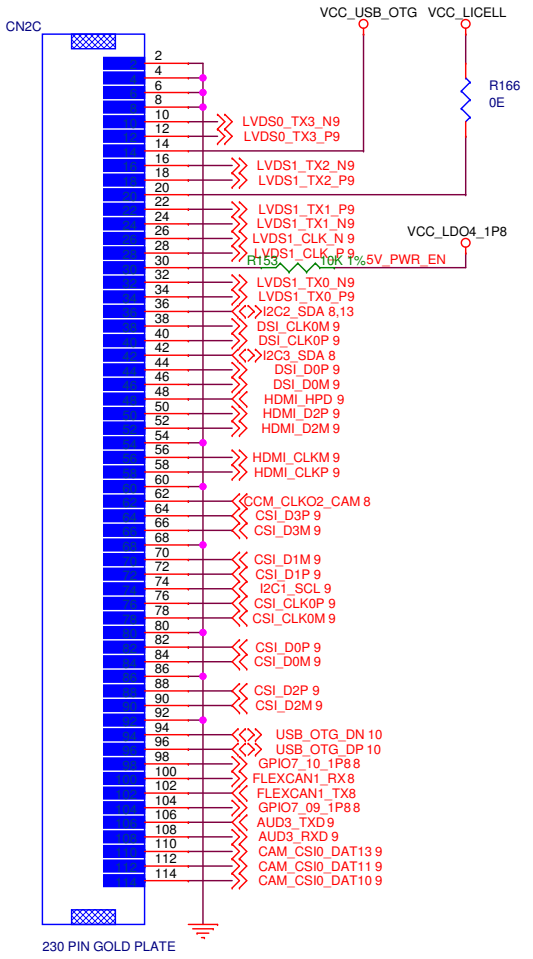
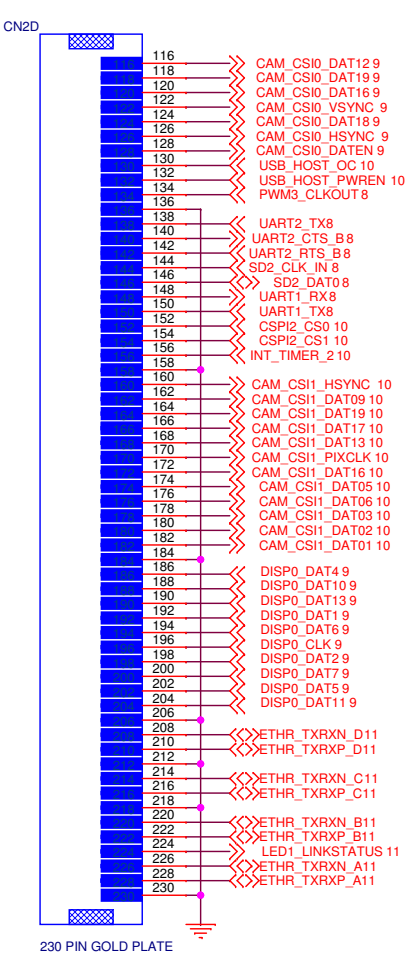
SOM MODULE BOTTOM SIDE

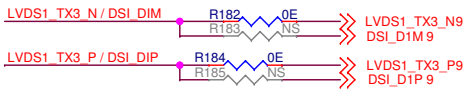


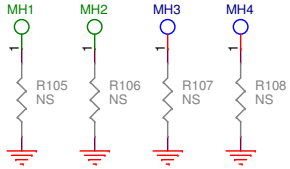
SOM MODULE TOP SIDE

Max current per contact = 0.5A Max









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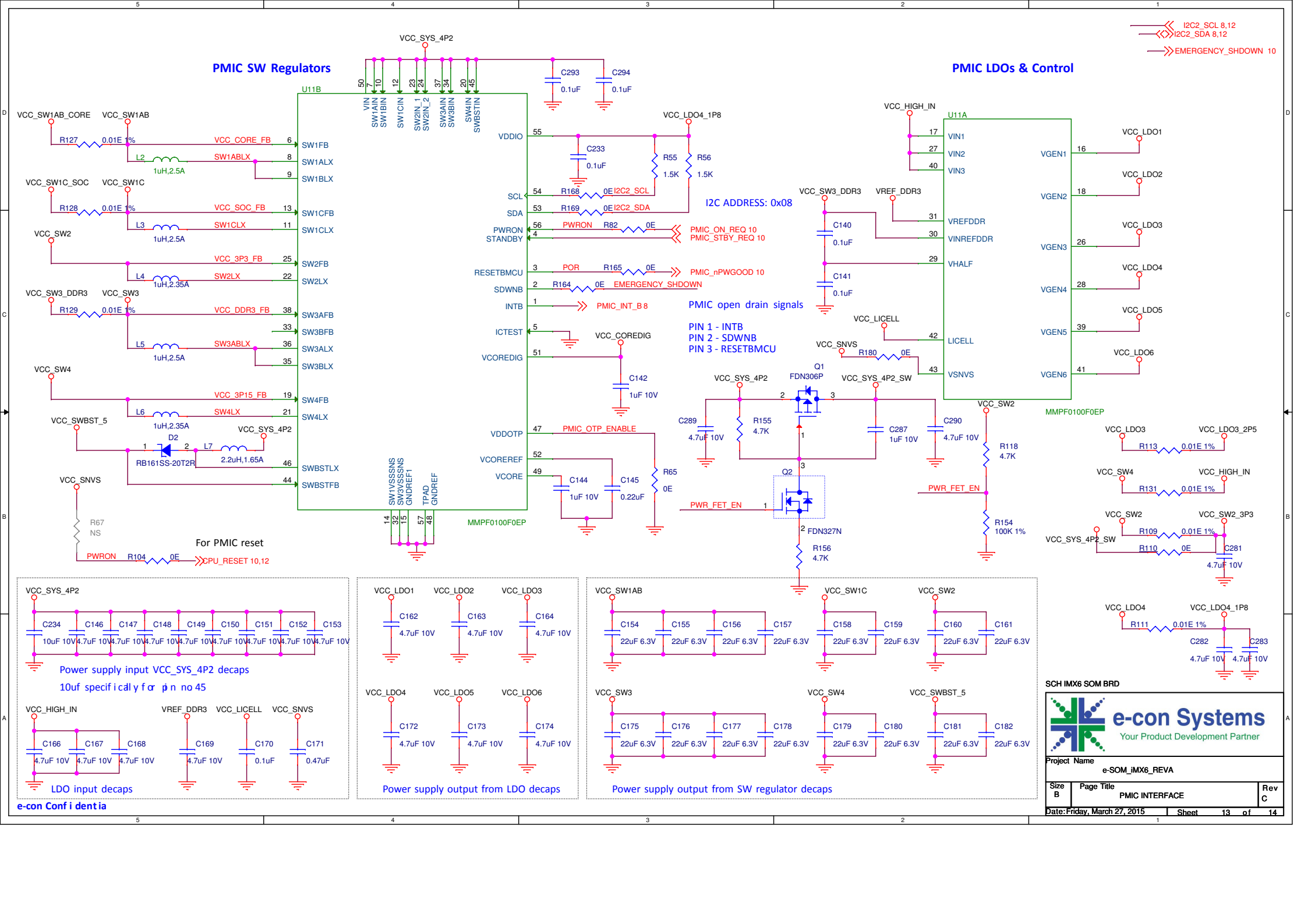
PMIC SW Regulators
PMIC LDOs & Control
I2C2_SCL 8,12
I2C2_SDA 8,12
EMERGENCY_SHDOWN 10
VCC_SYS_4P2
U11B
MMPF0100F0EP
U11A
MMPF0100F0EP
I2C ADDRESS: 0x08
PMIC open drain signals
PIN 1 - INTB
PIN 2 - SDWNB
PIN 3 - RESETBMCU
For PMIC reset
Power supply input VCC_SYS_4P2 decaps
10uf specifically for pin no 45
LDO input decaps
Power supply output from LDO decaps
Power supply output from SW regulator decaps
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PMIC INTERFACE
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REVISION HISTORY

Rev No	Date	Description	Remarks
A	28 OCT 2013	Initial Release	
B	24 SEP 2014	1. Pg.No.4 Removed R135, FB15 and FB16 in pg no.4 2. Pg.No.8 Replaced NAND flash interface with eMMC Connected UART3_CTS to ball D15 Removed FB17 and FB18 Changed R74 and R75 values to 510 ohm 3. Pg.No.10 Connected UART3_RTS to ball D25 Added resistor R167 to ball F23 Set R68 and R103 to NS 4. Pg.No.11 Changed R49 value to 12.1k ohm Set R99 and R100 to mount 5. Pg.No.12 Added resistor R166 to SOM connector pin no.20 6. Pg.No.13 Added resistor R164, R168 and R169 resistors Removed resistors R11O, R112, R114 and R130 Mounted R104 and no mount R67 Removed 3.3V Power Switch section	
C	26 MARCH 2015	1 Pg.No.09 R182 R183 R184 R185 are added to give swapping option for LVDS1_DAT3 and DSI_DAT1 lanes	

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