

DATA SHEET

(DOC No. HX8260-A-DS)

^{>>}HX8260-A

2402CH TFT LCD Source Driver with MIPI/LVDS TCON Version 01 October, 2014

Himax Technologies, Inc. http://www.himax.com.tw

^{>>}HX8260-A

2402 CH TFT LCD Source Driver with MIPI/LVDS TCON



Revision History

Version	Date	Description of changes
01	2014/4/18	New setup
	2014/4/23	Page 10~12
		Modified pin function and pin name
		ERR_CSB →ERR_RES1
		LNSW_RES1 →LNSW_CSB
		PNSW →PNSW_SCL
		MIPITE_SCL →MIPITE_SDA
		TPSYNC_SDA →TPSYNC
		Page 11, .28 and 75
		2. Resolution selection 768RGBx1280→768x1024
		Page 156
		3. Updated section 14.2 chip outline dimension.
		Paeg 104
		4. Updated Gamma PVP/N 8, PVP/N 9, and PVP/N 10 default
		value.
		Page 76
	2014/5/15	5. Updated video timing table. Page 81~102
	2014/5/15	1. Updated section 8.4 User define command for MIPI interface.
	2014/5/29	Page 156
		1. Updated Chip size (w/i scribe line).
	2014/6/10	Page 142
		1. Modified VDDI_RX and VDDI_D operation voltage 1.65~1.95V.
	2014/6/19	Page 131
		Updated OTP read flow chart.
	2014/7/1	Page 142
	0044/40/44	1. Modified VDDI_RX and VDDI_D operation voltage 1.7~1.9V.
	2014/10/14	Page 14
	6	Updadated section 4.2 Value of wiring resistance to each pin. Page 15~19
	~40/2	2. Updated section 5.1~5.4 example circuit.
		Page 29
		3. Updated section 6.2 figure 6.1 GOA connection.
		Page 32
	Y (\)	4. Updated section 6.4 input interface and pin mapping.

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1. General Description

The HX8260-A is a single-chip solution that combines source driver control, gate driver control and power supply circuit to drive TFT LCD.

The HX8260-A supports the resolution of 800RGBx1280, 768RGBx1024, 720RGBx1280, and 600RGBx1024 and with 6bit+2bit dithering in color depth.

The HX8260-A supports several interface modes, including MIPI DSI interface mode LVDS interface mode.





2. Features

- Interface: LVDS (85MHz); MIPI 4 lane (480Mbps/lane)
- Channel Number: 2402 channel output, build in source driver and TCON
- Resolution: 800RGBx1280,768RGBx1024,720RGBx1280,600RGBx1024
- Color: 6bits +2-bit dithering
- SPI interface
- VCOM is programmable adjustment by OTP
- Support GOA gate control signal
- Inversion :1/2/4/8 dot inversion, column inversion
- Support Zigzag panel
- Support CABC function
- Build-in PFM Booster controller to drive DC/DC converter circuit -- VSP & VSN
- Build-in Charge Pump controller to drive DC/DC converter circuit VGH, VGL & VCL



3. Block Diagram

3.1 Function block diagram

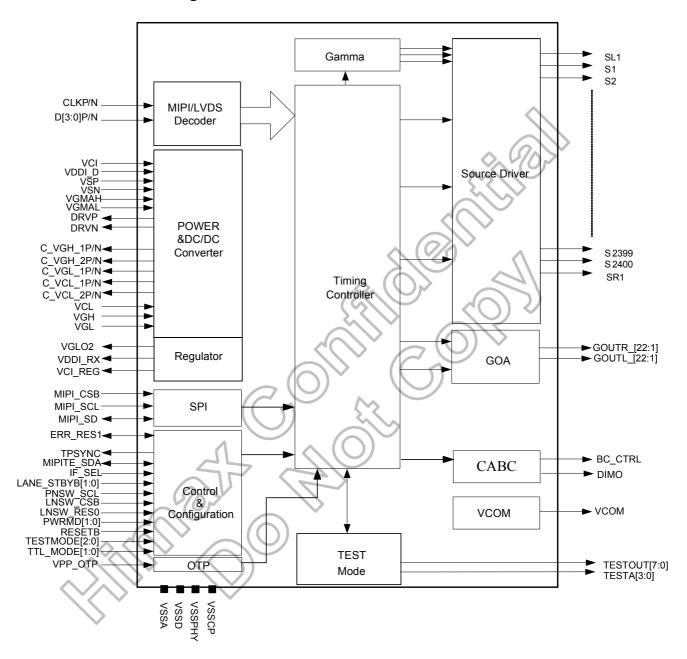


Figure 3.1: Function block diagram



4. Pin Description

Pin Types: I=Input, **O**=Output, **I/O**= Input/Output, **P**=Power, **G**=Ground, **N**=No Connection.

4.1 Pin description

Pin name	I/O	Description
RESETB	ī	Global reset.(VSSD~IOVCC)
		IF SEL=1: MIPI mode (default)
IF_SEL	ı	IF SEL=0: LVDS mode
		MIPI mode (IF_SEL=1): MIPI LANE swap function pin.
LNSW_CSB		LVDS mode (IF SEL=0): SPI CSB signal pin.
	-	Default LNSW_CSB pulled H.
		MIPI mode (IF_SEL=1): MIPI LANE swap function pin (default=11).
		Pad D2P D2N D1P D1N CLKP CLKN D0P D0N D3P D3N
		LNSW_CSB LNSW_RES0 MIPI lanes mapping table
		0 D3P D3N D2P D2N CLKP CLKN D1P D1N D0P D0N
		0 1 D3P D3N D0P D0N CLKP CLKN D1P D1N D2P D2N
		1 0 DOP DON D1P D1N CLKP CLKN D2P D2N D3P D3N
		1 1 D2P D2N D1P D1N CLKP CLKN D0P D0N D3P D3N
LNSW RES0	1	$\Delta (0)$
	•	LVDS mode (IF_SEL=0): Resolution selection pin
		ERR RES1 LNSW RES0 Resolution
		0 0 600RGBx1024
		0 1 720RGBx1280
		1 0 768RGBx1024
		1 800RGBx1280
		(Default LNSW_RES0 pulled H)
		Power mode contorl pin.
		PWRMD[1] PWRMD[0] Driving mode
PWRMD[1]		0 Support HX5186-C power mode.
PWRMD[0]	-	Suppot PFM circuit power mode.
		0 External VSP,VSN, VGH,VGL power mode.
		1 External VSP,VSN power mode (default).
		MIPI mode (IF SEL=1): MIPI LANE number control pin
		LVDS mode (IF_SEL=0): Standby mode signal (L :standby mode)
		LANE1 STBYB LANE0 BISTB MIPI lane
LANE1_STBYB		Others Reserved
		1 1 4-lane
		LANE1_STBYB default pulled H.
		MIPI mode (IF_SEL=1): MIPI LANE number control pin.
LANE0_BISTB	1	LVDS mode (IF_SEL=0): BIST mode signal (L: BIST mode).
L/ (IVLO_DIO I D	•	LANEO_BISTB default pulled H.
		MIPI mode (IF SEL=1): TE output signal.
MIPITE_SDA	I/O	LVDS mode (IF_SEL=0): SPI SDA signal.
WIII 11 L_0D/1	., 0	MIPITE SDA default pulled H.
TPSYNC	0	TPSYNC output signal
		MIPI mode (IF_SEL=1): MIPI and LVDS PN swap function pin.
PNSW SCL	1	LVDS mode (IF SEL=0): SPI clock signal.
	•	Default pulled H.
BC_CTRL	0	ON/OFF LED Backlight driver
DIMO	0	CABC PWM output
		MIPI mode (IF_SEL=1): ERR report
ERR_RES1	I/O	
		ERR RES1 default pulled H.
		Table 44 Clabel via

Table 4.1: Global pin



Pin name	I/O	Description			
CLKP/CLKN	-	MIPI/LVDS clock inp	out pin.		
	D0P/D0N D1P/D1N D2P/D2N D3P/D3N	MIPI/LVDS data inp	ut pin.		
DOD/DOM		Pad name	MIPI mode Pin mapping (default)	LVDS pin mapping	
		D0P/D0N	D0P/D0N	D2P/D2N	
· ·		D1P/D1N	D1P/D1N	D1P/D1N	
· ·		*	D2P/D2N	D2P/D2N	D0P/D0N
DOI /DOIN		D3P/D3N	D3P/D3N	D3P/D3N	
				RES0 and LNSW_CSB pin,but LVDS data	
		lane could not be sv	vapped.		

Table 4.2: MIPI interface

Pin name	I/O	Description
MIPI_CSB	Ι	MIPI mode SPI CHIP enable signal.default pulled H.
MIPI_SD	I/O	MIPI mode SPI DAT signal.default pulled H.
MIPI SCK		MIPI mode SPI clock signal.default pulled H.

Table 4.3: SPI interface

Pin name	I/O	Description	
GOUT_R[22:1]	0	GOA control signal at right side.(VGL~VGH)	
GOUT_L[22:1]	0	GOA control signal at left side. (VGL~VGH)	(0) ?/

Note: (1) IO cell voltage is between VGH and VGL.

Table 4.4: Gate driver (GOA) control pin

Pin name	I/O	Description	
S1 ∫ S2400	0	Source output pin.	
SL1,SR1	0	Source output pin. It is available when zigzag function enable.	

Note: (1) IO cell voltage is between VSP and VSN.

Table 4.5: Source output pin

Pin name	I/O	Description	
VCI	Р	Power input 2.6V ~ 6V.	
VSP	P	Positive power input for source driver and power circuits (4.5V ~ 6V).	
VSN	P	Negative power input for source driver and power circuits (-4.5V ~ -6V).	
VDDI_D	P	Power input 1.8V for TCON and Logic.	
VDDI_RX	P	Power input 1.8V for MIPI & LVDS RX.	
VPP_OTP	Р	Power input for OTP programming (7.6V). Leave this pin open or connect it to VSP when not programming OTP.	
DRVP	0	CLK for VSP PFM and HX5186-C.	
DRVN	0	CLK for VSN PFM and HX5186-C.	
VGLO2	Р	VGLO Regulator output 2.	
VGMAH	Р	Positive gamma high voltage.	
VGMAL	Р	Negative gamma high voltage.	
VCI_REG	Р	Regulator output for internal reference.	
VCL	Р	VCL charge pump output.	
C_VCL_1P C_VCL_1N C_VCL_2P C_VCL_2N	0	VCL flying cap. pin.	
VGH	Р	VGH charge pump output.	
C_VGH_1P C_VGH_1N C_VGH_2P C_VGH_2N	0	GH flying cap. pin.	





Pin name	I/O	Description
VGL	Р	VGL charge pump output.
C_VGL_1P C_VGL_1N	0	GL flying cap. pin.
VCOM	Р	VCOM Regulator output.
VSSD	G	Digital circuit ground (0V).
VSSA	G	Analog circuit ground (0V).
VSSPHY	G	Analog circuit ground (0V).
VSSCP	G	Ground for charge pump circuit (0V).

Table 4.6: Power and ground pin

Pin name	I/O	Description	
TESTOUT[7:0]	0	Test pin. Float these pin for normal operation.	A (QA)
TESTA[3:0]	0	Test pin. Float these pin for normal operation.	V/V/OF
DUMMY	NC	No connection.	13/10

Table 4.7: Others



4.2 Value of wiring resistance to each pin

The input wiring resistance values affect power or signal integrity and the display quality. So be sure to design using values that do not exceed those recommendations as below.

Pin type	Pin name	Resistance value(Ω)	Capacitance value(pF)
	VSSD	< 3	-
	VDD_ID	< 5	-
	VDD_RX	< 5	<u> </u>
Power	VCI	< 5	
- Fower	VSSA	< 3	
Ground	VSP	< 5	\$\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\
Ground	VSN	< 5	W(/O-
	VSSCP	<5	<i>₹</i> (<i>></i>) -
	VPP_OTP	<10	-
	VSSPHY	<5	-

Pin type	Pin name	Resistance value(Ω)	Capacitance value(pF)
	VCOM	< 5	
	VCI_REG	≪5	
	VGLO2	< 5	(C) V
	VGL	< 10	
PFM	VGH	< 10	
& FFIVI	VCOM	<10	-
Charge	VGAMP	< 10	-
Pump	VGAMN	< 10	-
& Regulator	VCL	<5∧	-
	C_VCL_1P,C_VCL_1N C_VCL_2P,C_VCL_2N	55	-
	C_VGH_1P,C_VGH_1N C_VGH_2P,C_VGH_2N	<-5	-
	DRVN,DRVP	< 5	-
	C_VGL_1P,C_VGL_1N	< 3	-

Pin type	Pin name	Resistance value(Ω)	Capacitance value(pF)
GOA	GOUT1_R~GOUT22_R	<100	-
uon (GOUT1_L~GOUT22_L	<100	-

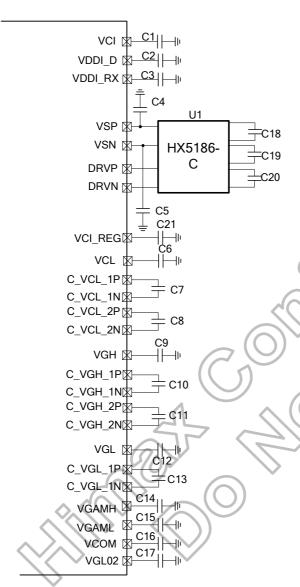
Pin type	Pin name	Resistance value(Ω)	Capacitance value(pF)
	CKP, CLKN		
MIPI/LVDS	D0P, D0N		< 0.9
Interface	D1P, D1N	< 10	
interrace	D2P, D2N		
	D3P, D3N		



5. Power Application

5.1 PWRMD [1:0] =00b

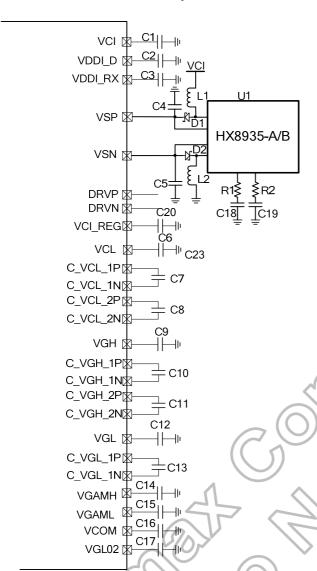
HX5186-C example circuit



Component	Value
C1	2.2uF/10V
C2	2.2uF/6V
C3	2.2uF/6V
C4	2.2uF/10V
C5	2.2uF/10V
C6	1uF/6V
C7	1uF/6V
C8	1uF/6V
C9	1uF/25V
C10	1uF/16V
C11	1uF/16V
C12	1uF/25V
C13	1uF/16V
C14	1uF/10V
C15	1uF/10V
C16	1uF/6V
C17	1uF/25V
C18	Please refer HX5186-C datasheet
C19	Please refer HX5186-C datasheet
C20	Please refer HX5186-C datasheet
C21	1uF/6V
U1	HX5186-C



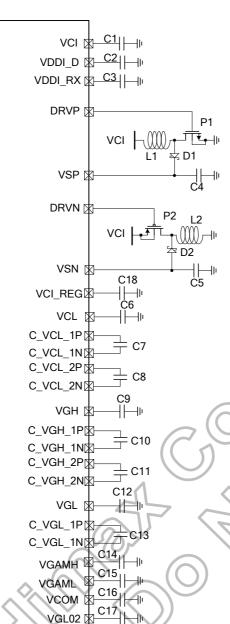
• HX8935-A/B example circuit



Component	Value
C1	2.2uF/10V
C2	2.2uF/6V
C3	2.2uF/6V
C4	2.2uF/10V
C5	2.2uF/10V
C6	1uF/6V
C7	1uF/6V
C8	1uF/6V
C9	1uF/25V
C10	1uF/16V
C11	1uF/16V
C12	1uF/25V
C13	1uF/16V
C14	1uF/10V
C15	1uF/10V
C16	1uF/6V
017	1uF/25V
C18,C19	1nF/6.3V
C20	1uF/6V
R1,R2	100K
D1,D2	VF<0.4V /20mA, VR>30V recommand diode :RB521S-30
L1,L2	4.7uH
U1	HX8935-A/B



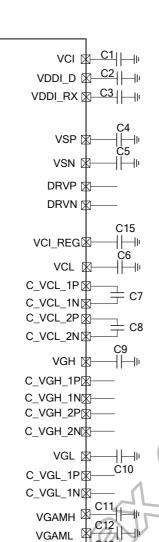
5.2 PWRMD [1:0] =01b



Component	Value
C1	2.2uF/10V
C2	2.2uF/6V
C3	2.2uF/6V
C4	2.2uF/10V
C5	2.2uF/10V
C6	1uF/6V
C7	1uF/6V
C8 (1uF/6V
C9	1uF/25V
C10	1uF/16V
C11	1uF/16V
C12	1uF/25V
C13	1uF/16V
C14	1uF/10V
C15	1uF/10V
C16	1uF/6V
C17	1uF/25V
C18	1uF/6V
D1,D2	VF<0.4V /20mA, VR>30V recommand diode :RB521S-30
P1	NMOS
P2	PMOS
L1	TBD
L2	TBD



5.3 PWRMD [1:0] =10b

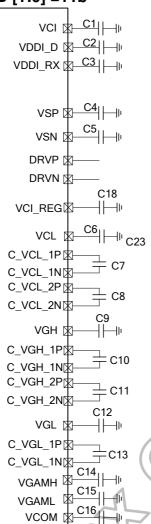


VCOM VGL02

Component	Value
C1	2.2uF/10V
C2	2.2uF/6V
C3	2.2uF/6V
C4	2.2uF/10V
C5	2.2uF/10V
C6	1uF/6V
C7	1uF/6V
C8	1uF/6V
C9	1uF/25V
C10	1uF/25V
C11	1uF/10V
C12	1aF/10V
C13	1uF/6V
C14	1uF/25V
C15	1uF/6V



5.4 PWRMD [1:0] =11b



VGL02

Component	Value
C1	2.2uF/10V
C2	2.2uF/6V
C3	2.2uF/6V
C4	2.2uF/10V
C5	2.2uF/10V
C6	1uF/6V
C7	1uF/6V
C8	1uF/6V
C9	1uF/25V
C10	1uF/16V
C11	1uF/16V
C12	1uF/25V
C13	1uF/16V
C14	1uF/10V
C15	1uF/10V
C16	1uF/6V
C17	1uF/25V
£18	1uF/6V

5.5 Power on/off sequence

5.5.1 Power on sequence PWRMD [1:0] =00b

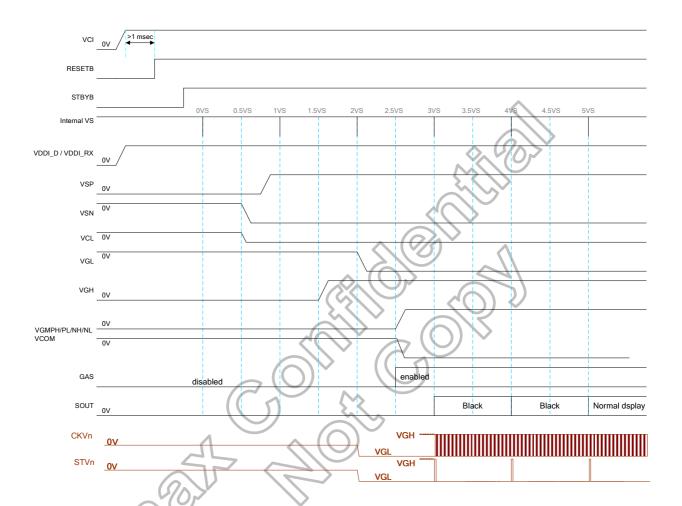


Figure 5.1: Power on sequence with PWRMD[1:0]=00b



5.5.2 Power off sequence PWRMD [1:0] =00b

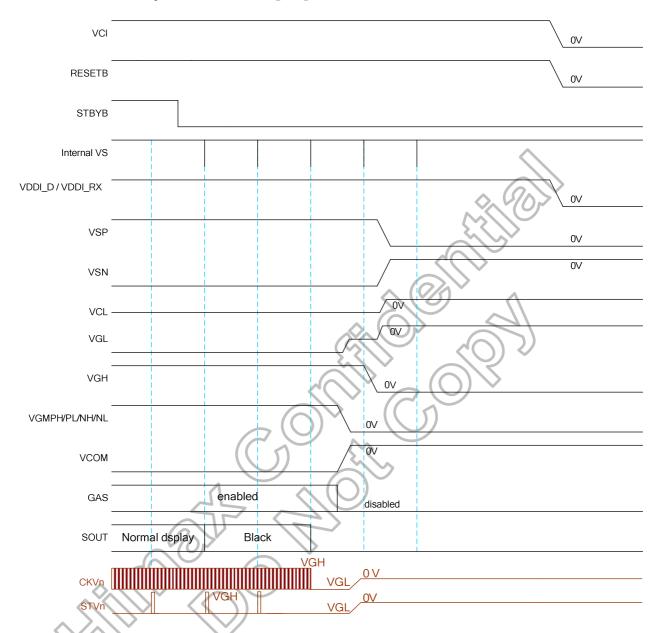


Figure 5.2: Power sequence in power off or standby mode with PWRMD[1:0]=00b



5.5.3 Power on sequence PWRMD [1:0]=01b

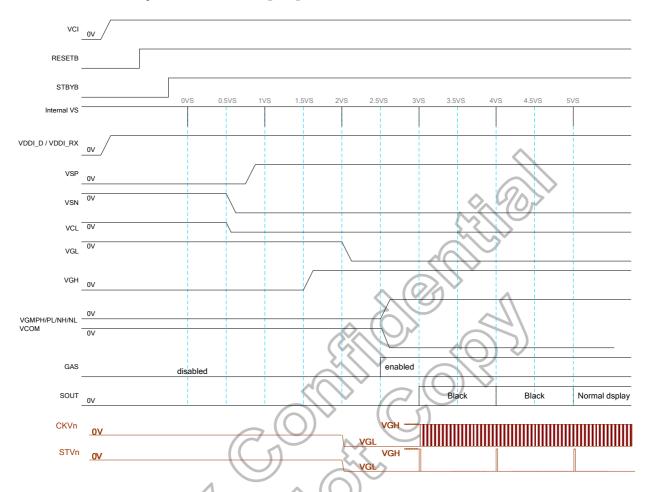


Figure 5.3: Power on sequence with PWRMD[1:0]=01b



5.5.4 Power off sequence PWRMD [1:0]=01b

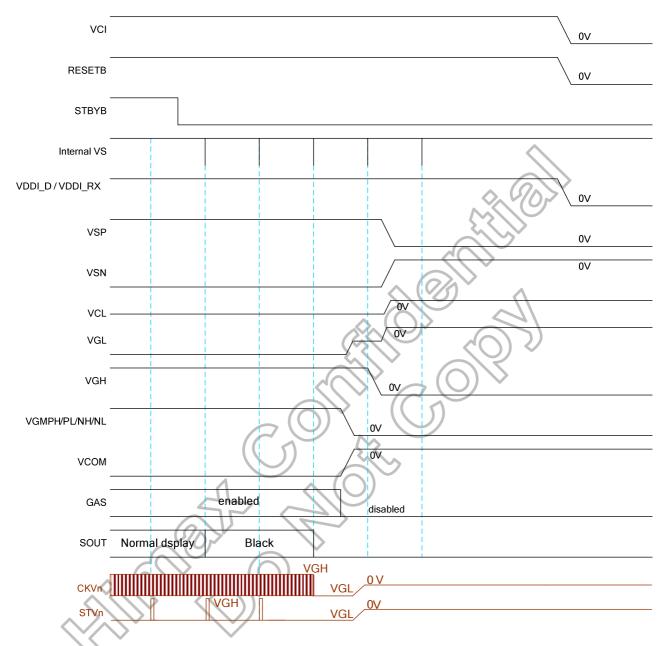


Figure 5.4: Power sequence in power off or standby mode with PWRMD[1:0]=01b



5.5.5 Power on sequence PWRMD [1:0]=10b

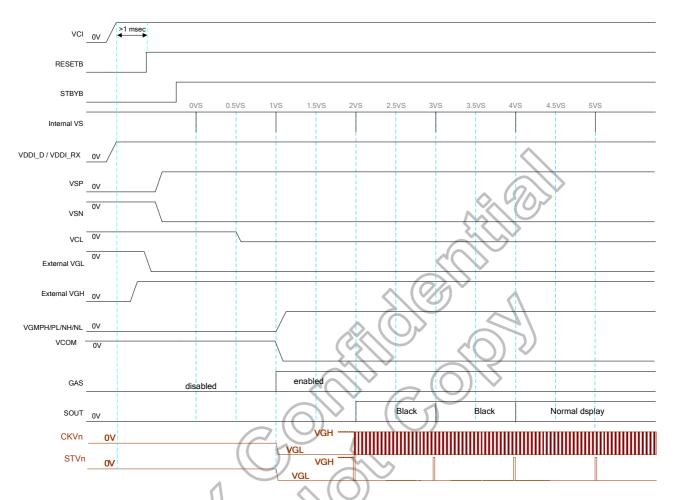


Figure 5.5: Power on sequence with PWRMD[1:0]=10b



5.5.6 Power off sequence PWRMD[1:0]=10b

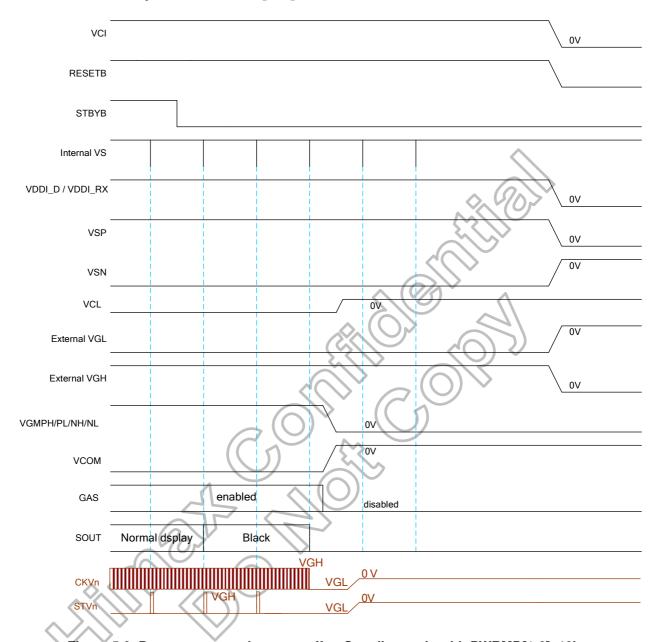


Figure 5.6: Power sequence in power off or Standby mode with PWRMD[1:0]=10b



5.5.7 Power on sequence PWRMD[1:0]=11b

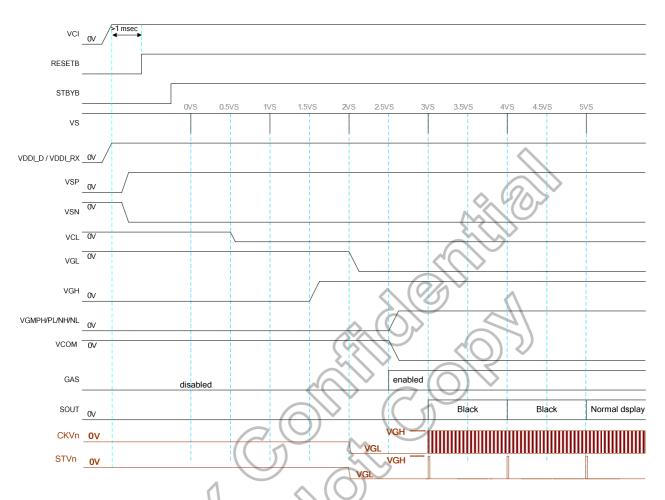


Figure 5.7: Power on sequence with PWRMD[1:0]=11b



5.5.8 Power off sequence PWRMD[1:0]=11b

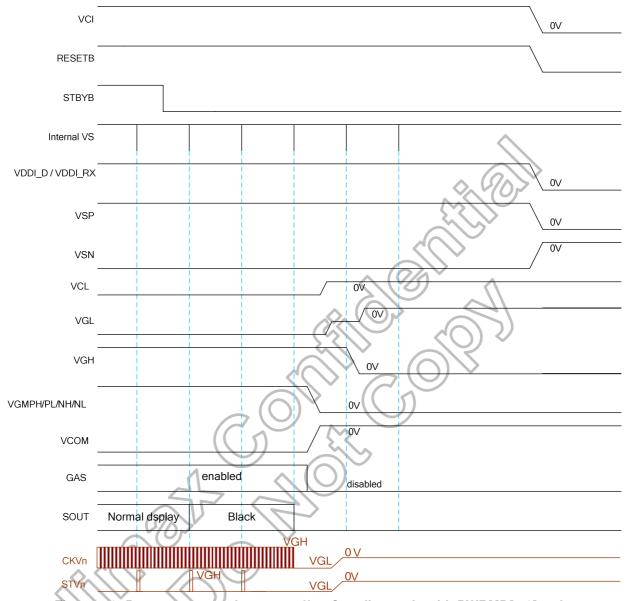


Figure 5.8: Power sequence in power off or Standby mode with PWRMD[1:0]=11b



6. Panel Application

The HX8260-A supports the resolution of 800RGBx1280, 768RGBx1024 720RGBx1280, and 600RGBx1024

The TCON also can generate gate controller timing. These signals can support for general gate driver or GOA (Gate driver on Array).

6.1 Display resolution

6.1.1 Display resolution configuration

Resolution selection can set by hardware or register. Hardware pin name is ERR_RES1 and LNSW_RES0. Register address is locates 0xB3 at page0. The relationship between pin and register is shows below.

ERR_RES1	LNSW_RES0	Resolution	Valid source channel	Disable channel
0	0	600RGBx1024	1(SL1)~900 1501 ~2400(SR1)	901~1500
0	1	720RGBx1280	1(SL1)~1080 1321 ~2400(SR1)	1081~1321
1	0	768RGBx1024	1(SL1)~1152 1249 ~2400(SR1)	1153~1248
1	1	800RGBx1280	1(SL1)~1200 1201 ~2400(SR1)	-

Note: (1) Blue mark is typical application.

Table 6.1: Display resolution setting



⁽²⁾ For zigzag panel type, TCON will enable SR1 and SL1 channel. For strip panel type, TCON will disable SR1 and SL1 channel.

6.2 GOA connection

The HX8260-A can support GOA/GIP (Gate driver on array) function.

GOA output pin define can set by register. A multiplexer is built in GOA function that selects one of several GOA signals. GOA function showed as below. The detail GOA output signal setting please refer application note.

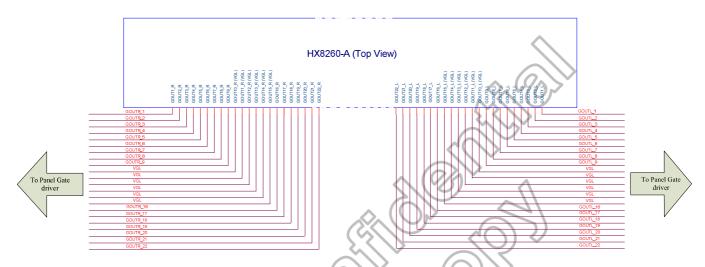


Figure 6.1: GOA wire example

6.3 Panel Structure

6.3.1 Driving method for panel structure

HX8260-A can support 2 types of driving method – stripe and zigzag. User could control Register: ZIGZAG_SEL and ZTYPE_SEL [1:0] select Panel type as following Figure:

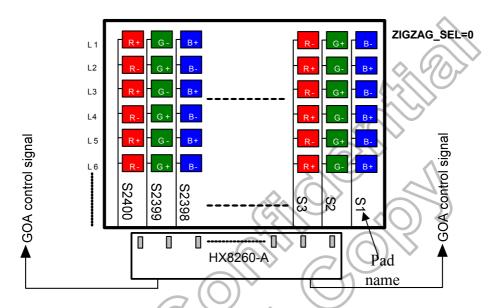


Figure 6.2: Stripe driving method

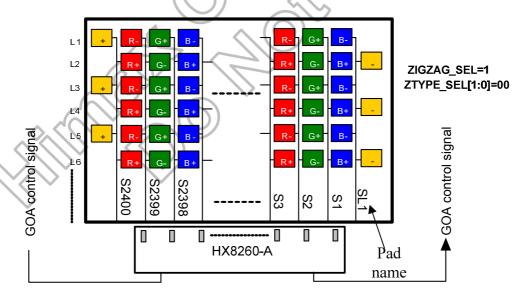


Figure 6.3: Zigzag type0 driving method



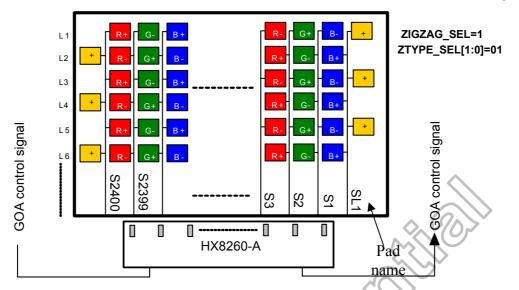


Figure 6.4: Zigzag type1 driving method

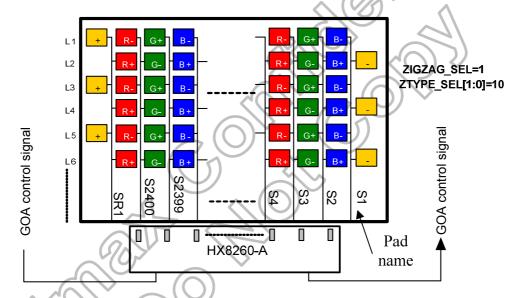


Figure 6.5: Zigzag type2 driving method

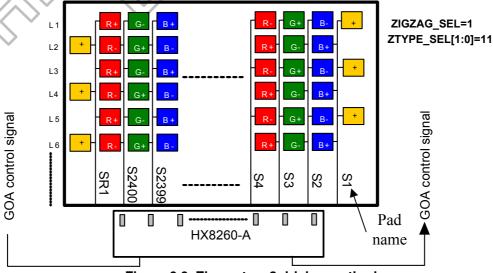


Figure 6.6: Zigzag type3 driving method



6.4 Input interface and pin mapping

HX8260-A support MIPI and LVDS interface, user can select input interface by IF SEL pin

6.4.1 MIPI interface (IF_SEL=1)

When IF_SEL=1 HX8260-A set to MIPI interface, user could configure data lane arrangement by hardware pin PNSW_SCL, LNSW_CSB and LNSW_RES0.

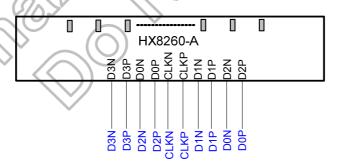
- PNSW SCL is for swap differencial pair polarity.
- LNSW RESO and LNSW CSB are for swap MIPI data pair.

Following table showed the MIPI lane swap pin mapping

Pad name Configuration		D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N	
PNSW_SCL	LNSW_CSB	LNSW_RES0	MIPI lanes mapping table									
0	0	0	D3P	D3	D2	D2	CLK	CLK	D1	D1	D0	D0
				N	P	N	Р	N) P.	N	Р	N
0	0	1	D3P	D3N	D0P	D0N	CLKP	CLKN	D1P	D1N	D2P	D2N
0	1	0	D0P	D0N	D1P	D1N	CLKP	CLKN	D2P	D2N	D3P	D3N
0	1	1	D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N
1	0	0	D3N	D3P	D2N	D2P	CLKN	CLKP	D1N	D1P	D0N	D0P
1	0	1	D3N	D3P	D0N	D0P	CLKN	CLKP	D1N	D1P	D2N	D2P
1	1	0	DON	D0P	DIN	D1P	CLKN	CLKP	D2N	D2P	D3N	D3P
1	1	1	D2N	D2P	DIN	D1P	CLKN	CLKP	D0N	D0P	D3N	D3P

Setting Example:

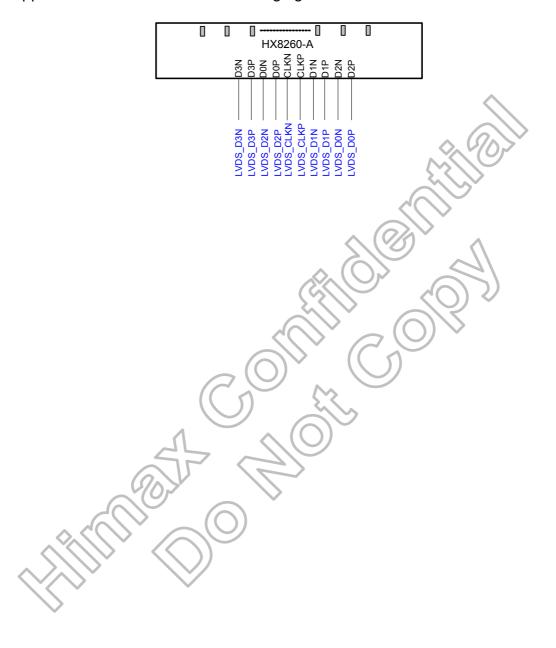
PNSW_SCL=0, LNSW_CSB=1, LNSW_RES0





6.4.2 LVDS interface (IF_SEL=0)

When IF_SEL=0 HX8260-A set to LVDS interface, data lane could not be swapped.Please connection as following figure:



7. Interface

7.1 LVDS interface

The HX8260-A has a built-in single pixel LVDS receiver that converts data from differential serialized format to parallel output.

LVDS mode data input format

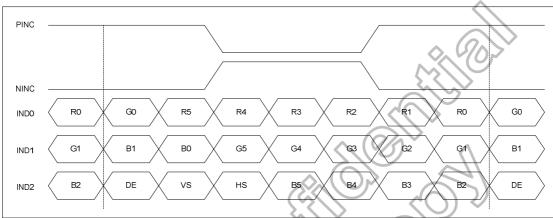


Figure 7.1: 6-bit LVDS input

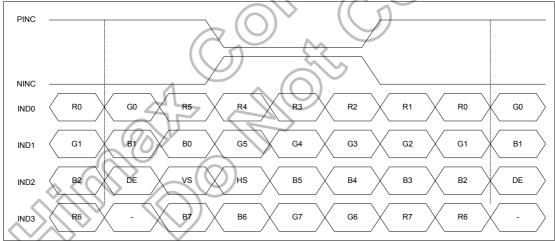


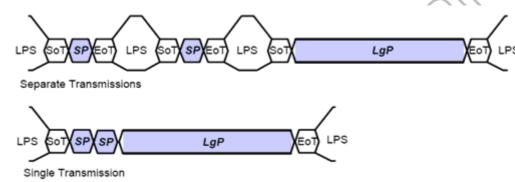
Figure 7.2: 8-bit LVDS Input



7.2 MIPI interface

7.2.1 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Figure 7.3 illustrates multiple HS Transmission packets.



Note: (1) LPS: Low power state

SoT: Start of Transmission

SP: Short Packet LgP: Long Packet

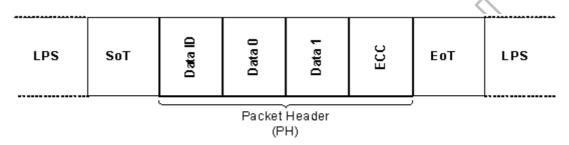
EoT: End of Transmission

Figure 7.3: Multiple packets transmission



The packet includes two types which are Long packet and Short packet. The first byte of the packet, the Data Identifier (**DI**), includes information specifying the type of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

Short packets are four bytes in length including the ECC. Short packet is used for most Command Mode commands and associated parameters. Where Short packets format include an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC. Figure 7.4 shows the structure of the Short packet.



Note: (1) DI (Data ID): Contain Virtual Channel Identifier and Data Type.

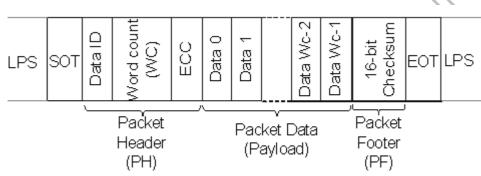
ECC (Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Short Packet.

Figure 7.4: Structure of the short packet





Long packets specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,535 bytes in length. Thus Long packets permit transmission of large blocks of pixel or other data.. Figure 7.5 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. An application-specific Data Payload has Word Count * bytes following the Packet Header. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length. Where 65,541 bytes = 4 bytes PH + (2¹⁶-1) bytes Payload + 2 bytes PF



Note: (1) DI (Data ID): Contain Virtual Channel Identifier and Data Type.

in some cases, the interpretation of the packet contents.

WC (Word Count): The receiver uses WC to determine the packet end.

ECC (Error Correction Code): The Error Correction Code allows single-bit errors to be corrected and

2-bit errors to be detected in the Packet Header. PF (Packet Footer): Mean 16-bit Checksum.

Figure 7.5: Structure of the long packet

According to packet form, basic elements include DI and ECC. Table 7.1 shows format of Data ID.

DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC (Virtua	l channel)		1	DT (D a	ta type)		
Table 7.1.: Format of data ID							

DI[7:6] → These two bits identify the data as directed to one of four virtual channels.
DI[5:0] → These six bits specify the Data Type, which specifies the size, format and,



Due to Data Type (**DT**) mean format of transmission type, following figure Short- / Long-packet transmission command sequence. Long packet writes Command / Parameters / Pixel Data

Using Long Packet to access Command



Short packet writes Command / Parameters

Using Short Packet to access Command

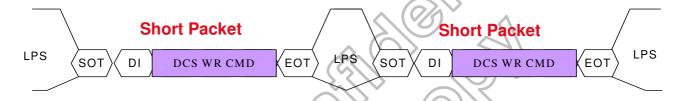


Figure 7.6: Show short- / long-packet transmission command sequence

Using Long Packet and Short Packet to access Command



Don't send more 32 command in one HS



Brust write



7.2.2 Processor to peripheral (forward direction) packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 7.2 Data Types for Processor-sourced Packets.

Data type, hex	Data type, binary	Description packet	Size
01h	00 0001	Sync event, V Sync start.	Short
11h	01 0001	Sync event, V Sync end.	Short
21h	10 0001	Sync event, H Sync start.	Short
31h	11 0001	Sync event, H Sync end.	Short
08h	00 1000	End of transmission packet (EoTp).	Short
02h	00 0010	Color Mode (CM) off command.	Short
12h	01 0010	Color Mode (CM) on command.	Short
22h	10 0010	Shut down peripheral command.	Short
32h	11 0010	Turn on peripheral command.	Short
03h	00 0011	Generic short WRITE, no parameter.	Short
13h	01 0011	Generic short WRITE, 1 parameter.	Short
23h	10 0011	Generic short WRITE, 2 parameter.	Short
04h	00 0100	Generic READ, no parameter.	Short
14h	01 0100	Generic READ, 1 parameter.	Short
24h	10 0100	Generic READ, 2 parameters.	Short
05h	00 0101	DCS short WRITE, no parameter.	Short
15h	01 0101	DCS short WRITE, 1 parameter.	Short
06h	00 0110	DCS READ, no parameters.	Short
37h	11 0111	Set maximum return packet size.	Short
09h	00 1001	Null packet, no data.	Long
19h	01 1001	Blanking packet, no data.	Long
29h	10 1001	Generic long write.	Long
39h	11 1001	DCS long write/write_LUT command packet.	Long
0Eh	00 1110	Packed pixel stream, 16-bit RGB, 5-6-5 format.	Long
1Eh	01 1110	Packed pixel stream, 18-bit RGB, 6-6-6 format.	Long
2Eh	10 1110	Loosely packed pixel stream, 18-bit RGB, 6-6-6 format.	Long
3Eh	01/17/10	Packed pixel stream, 24-bit RGB, 8-8-8 format.	Long
X0h and XFh,	xx 0000	DO NOT USE.	
unspecified	xx 1111	All unspecified codes are reserved.	_

Table 7.2: Data types for processor-sourced packets



Under tables list all detail function of all data types

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)			
Data type, hex	Function description	Number of bytes	
01h	V Sync start, start of VSA pulse.		
11h	V Sync end, end of VSA pulse.	4 bytes	
21h	H Sync start, start of HSA pulse.	(DI + 00h + 00h + ECC)	
31h	H Sync end, end of HSA pulse.		

Note: (1) V Sync start and V Sync end event represents the start and end of the VSA, respectively. Similarly H Sync start and H Sync end event represents the start and end of the HSA, respectively.

End of Transmission packet (EoTp)			
Data type, hex	Data type, hex Function description Number of byte		
08h	End of transmission packet (EoTp).	4 bytes (DI + 00h + 00h + ECC)	

Color mode status (Color Mode On, Color Mode Off)			
Data type, hex	Function description	Number of bytes	
02h	Color mode on that switches a video mode display module to a low-color mode for power saving.	4 bytes	
12h	Color mode off that switches a video mode display module from low-color display to normal display.	(DI + 00h + 00h + ECC)	

Display status (shutdown command, turn-on command)			
Data type, hex	Function description	Number of bytes	
22h	Shutdown peripheral command that turns off the display in a video mode display for power saving.	4 bytes	
32h	Turn on peripheral command that turns on the display in video mode display for normal display.	(DI + 00h + 00h + ECC)	

Note: (1) When use shutdown command; interface shall remain powered in order to receive the turn-on, or wake-up, command.

Generic Short WRITE Packet with 0,1,2 parameter			
Data type, hex	Function description	Number of bytes	
03h	Generic Short WRITE, no parameter.	(DI + 00h + 00h + ECC)	
13h	Generic Short WRITE, 1 parameter.	(DI + P1 + 00h + ECC)	
23h	Generic Short WRITE, 2 parameters. (P1=Addr, P2=Data)	(DI + P1 + P2 + ECC)	
\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \			

Note: (1) P1=parameter1, P2=parameter2.



Generic READ Request with 0,1,2 parameter			
Data type, hex	Function description	Number of bytes	
04h	Generic READ, no parameter.	(DI + 00h + 00h + ECC)	
14h	Generic READ, 1 parameter. (P1=Addr) only read 1 Data.	(DI + P1 + 00h + ECC)	
24h	Generic READ, 2 parameters. (P1=Addr, P2=Burst read length)	(DI + P1 + P2 + ECC)	

Note: (1) P1=parameter1, P2=parameter2.

DCS Show WRITE Command with 0,1 parameter			
Data type, hex	Function description	Number of bytes	
05h	DCS Short WRITE, no parameter.	(DI + DCS + 00h + ECC)	
15h	DCS Short WRITE, 1 parameter. (P1=DCS's data)	(DI + DCS + P1 + ECC)	

Note: (1) P1=parameter1, DCS=DCS command.

DCS command setting			
Data type, hex	Function description	Number of bytes	
06h	DCS Read command, the returned data may be of Short or Long packet format.	4 bytes (DI + DCS CMD.+00h + ECC)	
39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65535 bytes (DI + WC + ECC + DCS CMD. + Payload DATA(WC-1) + PF)	

- Note: (1) For write part, If DCS Short Write command is followed by BTA, the peripheral shall respond with ACK when no error was detected in the transmission (Host -> Slave). Unless an error was detected, the peripheral shall respond with Acknowledge with Error Report.
 - (2) When use DCS Read Command, the Set Max Return Packet Size command will limit the size of returning packets.
 - (3) The peripheral shall respond to DCS Read Command Request in one of the following ways:
 - ♦ If an error was detected and corrected in Packet Header field by the peripheral, it shall send Acknowledge with Error Report. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
 - ♦ If no error was detected by the peripheral, it shall send the requested READ packet (Short or Long) with appropriate ECC and Checksum, if either or both features are enabled. (4) One byte <= Length of payload DATA <= 2^{16} -1

Generic Long Wr	Generic Long Write				
Data type, hex	Function description	Number of bytes			
29h	Generic Long Write Packek is used to transmit arbitrary blocks of data from a host processor to peripheral in a Long packet. Support Burst Write: Parameter_1->MCS Addr(p1>B0) Parameter_2->Address's data Parameter_3->Address+1 's data Parameter_4->Address+2 's data : Parameter_N->Address+N-1 's data	Up to 65535 bytes (DI + WC + ECC + Payload DATA(WC) + PF)			

Note: (1) For write part, If Short Write command is followed by BTA, the peripheral shall respond with ACK when no error was detected in the transmission (Host → Slave). Unless an error was detected, the peripheral shall respond with Acknowledge with Error Report.

- (2) When use Read Command, the Set Max Return Packet Size command will limit the size of returning packets.
- (3) The peripheral shall respond to Read Command Request in one of the following ways:
 - ♦ If an error was detected and corrected in Packet Header field by the peripheral, it shall send Acknowledge with Error Report. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
 - ◆ If no error was detected by the peripheral, it shall send the requested READ packet (Short or Long) with appropriate ECC and Checksum, if either or both features are enabled.
- (4) One byte <= Length of payload DATA <= 2¹⁶-1

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Return packet size setting			
Data type, hex	Function description	Number of bytes	
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.		

Note: (1) The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.

Variable data packet			
Data type, hex	Function description	Number of bytes	
09h	Null Packet is a mechanism for keeping the serial Data Lane(s) in High-Speed mode while sending dummy data.	Up to 65535 bytes (DI + WC + ECC	
19h	Blanking packet is used to convey blanking timing information in a Long packet.	+ DCS CMD. + Payload DATA + PF)	

Note: (1) When Null Packet, the Payload Data belong "null" Data, actual data values sent are irrelevant because the peripheral does not capture or store the data.

(2) When Blanking packet, the packet represents a period between active scan lines of a Video Mode display.





Data stream format – 16bit Format				
Data type, hex		Function description	Number of bytes	
0Eh	image data form display module. P	ream 16-Bit Format is used to transmit atted as 16-bit pixels to a Video Mode rixel format is its) green and (5 bits) blue".	Up to 65535 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)	
		1 byte 1 byte by 1 byte byte byte byte byte byte byte byte		
1 byte 2	bytes 🔒 1 byte	1 byte 1 byte 1 byte 1 byte	2 bytes	
Data Type Virtual Channel	d Count ECC	Pixel 1 Pixel n	Checksum	
PH (Paci	ket Header)	Variable Payload data PF	(Packet Footer)	

Note: (1) Within a color component, the "LSB is sent first, the MSB last ".



Packed Pixel Stream 18-Bit Format is used to transmit Up to 65535 bytes	Data stream format – 18bit Format			
image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is "(6 bits) red, (6 bits) geen and (6 bits) blue". byte	Data type, hex		Number of bytes	
Pixel 1 Pixel 1 Pixel 1 Pixel 1 Pixel 2 Pixel 3 Pixel 4 Pixel 4 Pixel 5 Pixel 1 Pixel 1 Pixel 1 Pixel 1 Pixel 2 Pixel 3 Pixel 4 Pixel 5 Pixel 1 Pixel 5 Pixel 1 Pixel 2 Pixel 1 Pixel 1 Pixel 2 Pixel 2 Pixel 3 Pixel 4 Pixel 3 Pixel 4 Pixel 3 Pixel 3 Pixel 4 Pixel 3 Pixel 4 Pixel 3 Pixel 4 Pixel 3 Pixel 4 Pixel 5 Pixel 5 Pixel 6 Pixel 7 Pix	1Eh	image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is	(DI + WC + ECC + DCS CMD.	
Pixel 1 Pixel 2 Pixel 3 Pixel 4 Pixel 4 Pixel 2 Pixel 3 Pixel 4 Pixel 5 Pixel 5 Pixel 5 Pixel 5 Pixel 5 Pixel 6 Pixel	* * **	Pixel 1 State of byte 1 byte		
1 byte 2 bytes 6b	1 20 1 1 1 2 2 2 2		Pixel 4	
Pixel n-3 Pixel n-2 Pixel n-1 Pixel n	PH (Packet I	Header) Variable Payload Data (First 4 pixels	s packed at 9 bytes)	
Variable Payload Data (First 4 pixels packed at 9 bytes) PF (Packet Footer)		CH		
	Variable Payload Data (First 4 pixels packed at 9 bytes) PF (Packet Footer)			

Note: (1) Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a "clean start" for the next line.



Data stream format – 18bit Format				
Data type, hex	Function description Number of bytes			
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is "(6 bits) red, (6 bits) green and (6 bits) blue". Up to 65535 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)			
	1 byte 1 byte RO RS GO GS GO GS 6b 6b Pixel 1			
Data Type Virtual Channel Approximately 1997	6b 6b 6b 6b			
PH (Packet	Header) Variable Payload Data PF (Packet Footer)			

Note: (1) Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.



Data stream format – 24bit Format				
Data Type, Hex		Function Description	Number of bytes	
3Eh	data formatted a	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is (8 bits) red, (8 bits) green and (8 bits) blue		
	, , ,	1 byte 1		
1 byte 2	bytes 1 byte	1 byte 1 byte 1 byte 1 byte 1 byte	1 byte 2 bytes	
Data Type Virtual Channel	d Count ECC	8b 8b 8b 8b 8b Pixel 1	Checksum	
PH (Paci	ket Header)	Variable payload Data	PF (Packet Footer)	

Note: (1) Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.



7.2.3 Peripheral to processor (reverse direction) packet data type

Table 7.3 present the complete set of peripheral-to-processor Data Types

Data type, hex	Data type, binary	Description packet	Size
0x02	00 0010	Acknowledge and error report.	Short
0x08	00 1000	End of transmission packet (EoTp).	Short
0x11	01 0001	Generic short read response, 1 byte returned.	Short
0x12	01 0010	Generic short read response, 2 byte returned.	Short
0x1A	01 1010	Generic long read response.	Long
0x1C	01 1100	DCS long read response.	Long
0x21	10 0001	DCS short read response, 1 byte returned.	Short
0x22	10 0010	DCS short read response, 2 byte returned.	Short

Table 7.3: Data types for peripheral-sourced packets

Acknowledge types			
Data type, hex	Function description	Number of bytes	
02h	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes (DI + bit0 ~ bit15 + ECC)	
		31/	

Note: (1) When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor.

With error→Acknowledge with error report (Short packet), Without error→ request READ data or Acknowledge (trigger message).

Bit	Description
0	SoT error.
1	SoT Sync error.
2	EoT Sync error.
3	Escape mode entry command error.
4	Low-power transmit Sync error.
5	Peripheral timeout error.
6	False control error.
7	Contention detected.
8	ECC error, single-bit (detected and corrected).
9	ECC error, multi-bit (detected, not corrected).
10	Checksum error (long packet only).
11	DSI data type not recognized.
12	DSI VC ID invalid.
13	Invalid transmission length.
14	Reserved.
15	DSI protocol violation.





Generic Short Read Response (1 byte returned)			
Data type, hex	Function description Number of bytes		
11h	This is the short-packet to Generic Read Request. (1 byte returned).	4 bytes (DI + R1 + 00h + ECC)	

Note: (1) R1=returned byte 1.

Generic Short Read Response (1 byte returned)			
Data type, hex	Function description Number of bytes		
12h	This is the short-packet to Generic Read Request. (1 byte returned).	4 bytes (DI + R1 + R2 + ECC)	

Note: (1) R1=returned byte 1, R2=returned byte 2.

Generic Long Read Response			
Data type, hex	Function description	Number of bytes	
1Ah	This is the long-packet response to Generic Long Read Request.	Up to 65535 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)	

Note: (1) If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h. If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge with Error Report packet shall be sent.

DCS Read Response			
Data type, hex	Function description	Number of bytes	
1Ch	This is the long-packet response to DCS Long Read Request.	Up to 65535 bytes (DI + WC + ECC + DCS CMD. + Payload DATA + PF)	

Note: (1) If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h. If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge with Error Report packet shall be sent.

DCS Short Read Response (1 byte returned)									
Data type, hex	Function description	Number of bytes							
21h	This is the short-packet to DCS Read Request. (1 byte returned).	4 bytes (DI + R1 + 00h + ECC)							

Note: (1) R1=returned byte 1.

DCS Short Read Response (2 byte returned)								
Data type, hex Function description Number of bytes								
22h	This is the short-packet to DCS Read Request. (2 byte returned).	4 bytes (DI + R1 + R2 + ECC)						

Note: (1) R1=returned byte 1, R2=returned byte 2.



7.3 Display command set (DCS)

Command	Hex Code	Description	Number of parameters
Enter invert mode	21h	Displayed image colors are inverted.	0
Enter sleep mode	10h	Power for the display panel is off.	0
Exit invert mode	20h	Displayed image colors are not inverted.	0
Exit sleep mode	11h	Power for the display panel is on.	0
Get address mode	0Bh	Get data order for transfers from the Host to the display module and from the frame memory to the display device.	1
Get display mode	0Dh	Get the current display mode from the peripheral.	1
Get pixel format	0Ch	Get the current pixel format.	1
Get power mode	0Ah	Get the current power mode.	1
Get signal mode	0Eh	Get display module signaling mode.	1
Nop	00h	No operation.	0
Read DDB continue	A8h	Continue reading the DDB from the last read location.	variable
Read DDB start	A1h	Read the DDB from the provided location.	variable
Set address mode	36h	Set the data order for transfers from the host to the display module and from the frame memory to the display device.	1
Set display off	28h	Blanks the display device.	0
Set display on	29h	Show the image on the display device.	0
Set pixel format	3Ah	Defines how many bits per pixel are used in the interface.	1
Set tear off	34h	Synchronization information is not sent from the display module to the host processor.	0
Set tear on	35h	Synchronization information is sent from the display module to the host processor at the start of VFP	1
Set tear scan line	44h	Synchronization information is sent from the display module to the host processor when the display device refresh reaches the provided scan line.	2
Soft reset	01h	Software Reset.	0
Enter_idle_mode	39h	Reduced color depth is used on the display panel.	0
Exit_idle_mode	38h	Full color depth is used on the display panel.	0
Get diagnostic_result	0Fh	Get Peripheral Self-Diagnostic Reslut.	1
RDNUMED	05h	RDNUMED (Read Number of the Errors on DSI).	1

Table 7.4: DCS command list



7.3.1 Enter_invert_mode (21h)

21 H	Enter_invert_mode (Display Inversion On)→INVON												
2111	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
Command	H→D	0	0	1	0	0	0	0	1	21			
Parameter	No parameter.												
	This command makes no chang frame memory to the display.	This command is used to enter into display inversion mode. This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display. This command does not change any other status. (Example)											
Description		Hos		$ \rightarrow $		play		20/2	>				
Restriction	This command has no effect wh	nen mod	dule is	already	in inver	sion on	mode.	<u> </u>					
Register Availability	S	Status leep Ou Sleep Ir	ut	11c	J'	<(" ((lability Yes Yes				
Default	Power S ₂	Status On Sec W Res W Res	et	(() ()	<u> </u>	Di	isplay Ir isplay Ir	ult valu nversion nversion nversion	n Off n Off			
Flow Chart		enter_	invert	_mode)								



7.3.2 Enter_sleep_mode (10h)

10 H	Enter_sleep_mode (Sleep II	n)→SLP	IN								
'	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	H→D	0	0	0	1	0	0	0	0	10	
Parameter	No parameter.	5ll	- 4								
	This command causes the LCI In this mode the DC/DC convestopped. Output[1:320]			Internal						ning is	
	VST etc.(V scanner contr	ol logic)			TOP ISCHAR	GH_	0V				
	DC charge in the capa	acitor				\ \\		0>			
Description	DC/DC Converter					1	0V				
	DC/DC Converter						0V		_		
	DC/DC Converter				(%)	7	0V				
	Reset pulse for circuit insi			\mathcal{O}		RESE					
	Internal Oscillator		ЩЦ	ЩЩ		ЩЦ	ЩЦ	_	TOP		
	MCU interface and memory ar	e still wo	orking a	nd the r	nemory	keeps	its conte	ents.			
	This command has no effect w left by the Sleep Out Comman	nen mod d (11h)	dule is a	ilready	ın sleep	in mod	e. Siee	p in Mod	de can o	only be	
Restriction			re send	ing nex	t comm	and, thi	s is to a	llow tim	е		
Restriction		It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize									
	for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep										
	It will be necessary to wait 120	msec af	fter send	ling Sle	ep Out	comma	nd (wh	en in SI	еер		
		msec af mand ca	iter send an be se	ling Sle	ep Out	comma	nd (wh				
Register	It will be necessary to wait 120 In Mode) before Sleep in com	msec af mand ca Status	fter send an be se	ling Sle	ep Out	comma	nd (who	Availa	ability		
Register Availability	It will be necessary to wait 120 In Mode) before Sleep in com	msec af mand ca Status Sleep Ou	fter send an be se ut	ling Sle	ep Out	comma	nd (who	Availa Ye	ability es		
	It will be necessary to wait 120 In Mode) before Sleep in com	msec af mand ca Status Sleep Ou Sleep Ir	fter send an be se ut	ling Sle	ep Out	comma	nd (who	Availa Ye Ye	ability es		
	It will be necessary to wait 120 In Mode) before Sleep In com	msec af mand ca Status Sleep Ou Sleep In	fter send an be se ut	ling Sle	ep Out	comma	nd (who	Availa Ye Ye	ability es es t value		
	It will be necessary to wait 120 In Mode) before Sleep In com	msec af mand ca Status Sleep Ou Sleep In Status r On Sec	ter send an be se ut n	ling Sle	ep Out	comma	nd (who	Availa Ye Ye Defaul	ability es es t value n Mode		
Availability	It will be necessary to wait 120 In Mode) before Sleep In comi	Status Sleep Ir Status Control Status Sleep Ir Status Control Status Control Status Control Status	tter send an be se ut n quence et	ling Sle	eep Out	comma	nd (who	Availa Ye Ye Defaul Sleep II	ability es es t value n Mode		
Availability	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Ir Status r On Sec S/W Res	ut quence et	ling Sle				Availa Ye Ye Defaul	ability es es t value n Mode		
Availability	It will be necessary to wait 120 In Mode) before Sleep In comi	Status Sleep Ou Sleep Ir Status r On Sec S/W Res H/W Res	ter sendan be se	ling Sle				Availa Ye Ye Defaul Sleep II	ability es es t value n Mode		
Availability	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Ir Status r On Sec S/W Res	ter sendan be se	ling Sle				Availa Ye Ye Defaul Sleep II	ability es es t value n Mode		
Availability	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Ou Sleep Ir Status r On Sec S/W Res H/W Res	ter sendan be se	ling Sle				Availa Ye Ye Defaul Sleep II	ability es es t value n Mode		
Availability	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Ou Sleep Ir Status r On Sec S/W Res H/W Res	dut quence et et mode aft	ling Sle				Availa Ye Ye Defaul Sleep II	ability es es t value n Mode		
Availability	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Or Sleep Ir Status T On Sec S/W Res H/W Res eep In m	dut quence et et mode aft	ling Sle				Availa Ye Ye Defaul Sleep II	ability es es t value n Mode		
Availability	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Ou Sleep Ir Status r On Sec S/W Res H/W Res eep In m Any Mo	dut nut nut nut nut nut nut nut nut nut n	ling Sle				Availa Ye Ye Defaul Sleep II	ability es es t value n Mode		
Availability Default	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Or Sleep Ir Status T On Sec S/W Res H/W Res eep In m	dut nut nut nut nut nut nut nut nut nut n	ling Sle				Availa Ye Ye Defaul Sleep II	ability es es t value n Mode		
Availability	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Ou Sleep Ir Status r On Sec S/W Res H/W Res eep In m Any Mo	dut nut nut nut nut nut nut nut nut nut n	ling Sle				Availa Ye Ye Defaul Sleep II	ability es es t value n Mode		
Availability Default	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Ot Sleep Ir Status Fower off Di	dut nut nut nut nut nut nut nut nut nut n	ling Sle				Availa Ye Ye Defaul Sleep li Sleep li	ability es es t value n Mode		
Availability Default	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Or Sleep Ir Status On Sec S/W Res H/W Res H/W Res H/W Res Slank Display Fower Off Dic Stop Power S	ter sendan be se ut nut nut nut nut nut nut nut nut nut	ling Sle				Availa Ye Ye Defaul Sleep li Sleep li	ability es es t value n Mode		
Availability Default	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Ot Sleep Ir Status Fower Off Di Device	ter sendan be se ut nut nut nut nut nut nut nut nut nut	ling Sle				Availa Ye Ye Defaul Sleep li Sleep li	ability es es t value n Mode		
Availability Default	It will be necessary to wait 120 In Mode) before Sleep In com	Status Sleep Or Sleep Ir Status On Sec S/W Res H/W Res H/W Res H/W Res Slank Display Fower Off Dic Stop Power S	ter sendan be se ut quence et et mode aft perice Device	ling Sle				Availa Ye Ye Defaul Sleep li Sleep li	ability es es t value n Mode		



7.3.3 Exit_invert_mode (20h)

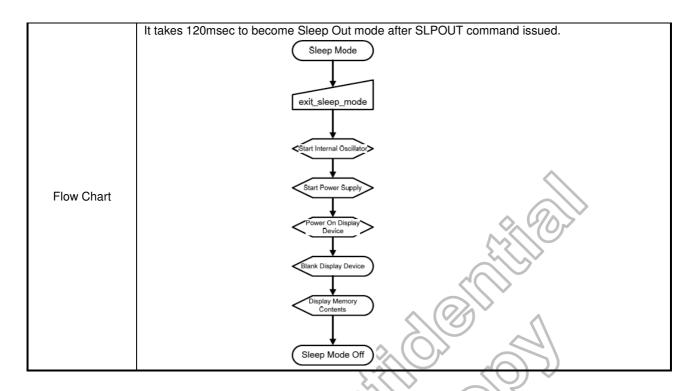
20 H	Exit_invert_mode (Display Inv			INVOF	F								
2011	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
Command	H→D	0	0	1	0	0	0	0	0	20			
Parameter	No parameter.												
	This command makes no chang	his command is used to recover from display inversion mode. his command makes no change of contents of frame memory. his command does not change any other status. (Example)											
Description		Ho	ost		displa	ay		6	>				
Restriction	This command has no effect wh	en mod	dule is a	already	in inver	sion off	mode.						
Register Availability	S	Status leep Ou Sleep In		2	((2))		Y	lability /es /es				
Default	Power S/	Status On Sec W Rese W Rese	et				Di	Defau splay Ir splay Ir splay Ir	nversior	n Off n Off			
Flow Chart		exit_inve	ert_mode) ((] ^{>})	S								



7.3.4 Exit_sleep_mode (11h)

11 H	Exit_sleep_mode (Sleep Out)→SLPOUT									
1711	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	1	0	0	0	1	11
Parameter	No parameter.									
Description	This command turns off sleep r In this mode the DC/DC conve started. Output[1: 320] VST etc.(V scanner control logic) DC charge in the capacitor		nabled,	Interna	CHAF	Blank (If D	Mer	nory Conte	ents	ning is
	DC/DC Converter	0V							-	
	DC/DC Converter	0V 0V) `				
	DC/DC Converter	UV		$\mathcal{L}(C)$			\mathcal{A}		_	
	Reset pulse for circuit inside panel	RES	SET FART		/	_ </td <td>)) <</td> <td>)</td> <td></td> <td></td>)) <)		
	Internal Oscillator	STOP			711					
Restriction	This command has no effect who Mode can only be left by the Skilt will be necessary to wait 5ms for the supply voltages and clood. The display module loads all diduring this 5msec and there can image if factory default and regmodule is already Sleep Out — The display module is doing selt will be necessary to wait 120 to Out mode) before Sleep Out controlled.	eep In (ec befook circui splay su nnot be ister val node. If-diagn	Commaing re send to state to state any about the sendent to sendent recommendation and the sendent recommand the sendent recomment recommand the sendent r	nd (10h ing nex abilize. factory normal same v nctions ding Sle). t command default visual ewhen the	and, this values ffect on is load i	to the r the dis s done ec.	egisters olay and whe	en the c	lisplay
Register		Status						Availa	bility	
Availability		Sleep Out Yes Sleep In Yes								
		Ctotor						Doford		
	Davis	Status						Default		
Default		On Sec /W Res						Sleep Ir Sleep Ir		
		/W Res						Sleep Ir		
							ı	.		







7.3.5 Get_address _mode (0Bh)

0B H	Get_address_mode	(Read Display	y MADO	TL) →F	RDDMAI	DCTL						
ОВ П	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	H→D	0	0	0	0	1	0	1	1	0B		
1 st parameter	D→H	D7	D6	0	0	D3	0	0	0	XX		
Description	Bit Description D7 Not Defined D6 Not Defined D5 Not Defined D6 Not Defined D7 Not Defined D8 Not Defined D9 Not Defined D9 Not Defined D1 Flip Horizontal D1 Flip Vertical								Comment - Set to '0' Set to '0' - Set to '0' Set to '0' Set to '0' Set to '0'			
	'0' = RGB (When '1' = BGR (When Bit D1 - Flip Horizor '0' = Display from '1' = Display from Bit D0 - Flip Vertica	Bit D3 – RGB/BGR Order '0' = RGB (When MADCTL B3 = '0'). '1' = BGR (When MADCTL B3 = '1'). Bit D1 – Flip Horizontal '0' = Display from Left to Right '1' = Display from Right to Left. Bit D0 – Flip Vertical '0' = Display from Top to Bottom										
Restrictions	-		C()	>								
Dominton		Stat	us					Avail	lability			
Register Availability		Sleep	Out			1		Y	'es			
Availability		Slee	o In	^^				Y	'es			
		Stat							It value			
Default		Power On S		ce					00h			
	21	S/W F							hange			
		H/W F	reset					0	0h			
Flow Chart	Host Processor Get_address_mode											



7.3.6 Get_display _mode (0Dh)

OD H	Get_display_mode (Read Display Image Mode→RDDIM												
0011	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX			
Command	H→D	0	0	0	0	1	1	0	1	0D			
1 st parameter	D→H	0	0	D5	0	0	0	0	0	XX			
Description	This command indicates the current status of the display as described in the table below: Bit D5 – Inversion On/Off '0' = Inversion is Off. '1' = Inversion is On. Bit D7,D6,D4,D3,D2,D1,D0- Not Defined Set to '0' -												
Restrictions	-												
Register Availability		Stat Sleep Slee	Out			\$	3//	U 1	lability 'es 'es				
	Dec	Stat							It value				
Default	Po	S/W F H/W F		ce	(9			No c	00h hange 10h				
Flow Chart		dispa	ay_mo	de	_	st Pro							



7.3.7 Get_pixel_format (0Ch)

0C H	Get_pixel_format (Read Display COLMOD)→RDDCOLMOD											
ос п	Direction		D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	H→D		0	0	0	0	1	1	0	0	0C	
1 st parameter	D→H		0	D6	D5	D4	0	0	0	0	XX	
	This command indica	ates the c	urrent	status	of the di	splay as	describ	ed in th	e table k	pelow:	_	
	Bit			Desc	cription				Com	ment		
	D7	Reserve	ed						Set	to '0'		
	D6								-			
	D5	DPI Inte	erface	Pixel fo	rmat				^	-		
	D4									-		
	D3	Reserve	ed						Set	to '0'		
	D2							^ ((Set	to '0'		
	D1	DBI Inte	erface	Pixel fo	rmat ->	Not Def	ined	977	Set	to '0'		
	D0								Set	to '0'		
Description	Bits D6, D5, D4 – DF Bits D2, D1, D0 – DE	BI Pixel Fo		Definition	n-> Not	Defined						
	Interface Color I			De			D5			D4		
	Not Define			0		1	0	\sim		0		
	Not Define			0	$\mathcal{S}(\mathcal{L})$	_\/\	0	\sim		1		
	Not Define			0		7	1/	\rightarrow))	0		
	Not Define			0	$\langle \cdot \rangle$		1	<u> </u>	_	1		
	Not Define			1			0				1	
	16 bit/pixe		-				0)			•		
	18 bit/pixe				/		1			<u>0</u>		
	24 bit/pixe		/	IDDI :	. (V., 3.			1			
	If a particular interfac					a then t	ne corre	sponain	ig bits in	i tne par	ameter	
Restrictions	returned from the dis	ріау тюо	iule ar	e under	nea.							
Restrictions	-		/	-	1							
Register			Stat	us					Avail	lability		
Availability			Sleep	Out)]				Y	'es		
Availability	7	7	Slee	o In					Y	'es		
		_ <		\rightarrow								
			Stat	us					Defau	lt value		
Default				Sequenc	e					it/pixel		
Delault			S/W F	Reset					24-b	it/pixel		
^		$\mathcal{A} \cup \mathcal{A}$	H/W F	Reset					24-b	it/pixel		
Flow Chart		Get_pixel_format Host Processor Parameter 1 Display Module										
			2 dial		_/_	סוס	piay	woul	110			



7.3.8 Get_power_mode (0Ah)

0A H	Get_power_mode (R	ead Display	Power	Mode)→	RDDPI	Л				
UA H	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	1	0	1	0	0A
1 st parameter	D→H	0	0	0	D4	0	D2	0	0	XX
	This command indicat Bit D7	es the curren	Des	of the discription	1	s descrit	oed in th	Con	nment	
	D6			Defined					to '0'	
	D5			Defined					to '0'	
	D4			ep In/Ou					-	
	D3			Defined			. //	Set	to '0'	
	D2			lay On/C			O _A V	(0)	-	
Description	D1			Defined			5	Set	to '0'	
Description	D0			Defined		\$			to '0'	
Restrictions	'1' = Sleep Out Mo Bit D2 - Display On/O '0' = Display is Off '1' = Display is On Bit D7,D6,D5,D3,D1,D Set to '0'	Off :	2			9	9			
Register		Stat							lability	
Availability			Out	(({	1	+		<u>Yes</u> Yes	
		Slee								
		Sta							ılt value)
Default		Power On		ice			+		00h	
				$\overline{}$			+			
Flow Chart	S/W Reset 00h H/W Reset 00h Host Processor get_power_mode Display Module									



7.3.9 Get_signal_mode (0Eh)

0E H	Get_signal_mode (Read D	isplay S	Signal N	/lode)→	RDDSM					
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	1	1	1	0	0E
1 st parameter	D→H	D7	D6	0	0	0	0	0	D0	XX
Description	This command indicates the Bit D7 – Tearing Effect Line '0' = Tearing Effect Line Off. '1' = Tearing Effect On. Bit D6 – Tearing Effect Line see section set_tear_on(35I '0' = Mode 0.(M=0) '1' = Mode 1.(M=1) Bit [D5:D1] –reserved and set [D5:D1] –reserved and set [D5:D1] – Teserved and set	ne On/O	ff ut Mode ode defi	e nitions.		C C		Table 1)	
Restrictions	-			001 10	<u> </u>	1	$\overline{}$			
		Stat	ile					Avail	ability	
Register		Sleep		_	10	// ·			es	
Availability		Sleep			1/1/2)/ 			es ′es	
		0,00	V 111	- (1			7/	\		
		Stat	us		16/			Defau	It value	
D ()	Pov	<u>)))</u>	00h							
Default		S/W F					3		0h	
		H/W F	Reset					0	0h	
Flow Chart		ignal_r] 7		Proce				
			>							



7.3.10 Nop (00h)

00 H	NOP (No Operation)									
0011	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER									
Description	This command is an empty However it can be used to to Write) or RAMRD (Memory	erminate	Frame	Memory						ry
Restriction	-	Í								
Register		Stat Sleep							ability es	
Availability		Slee							es	
	-						<u>0, V/</u>	Ω		
		Stat	us					Defaul	t value	
Default	Pov	ver On S	Sequen	ce		~		N	/A	
Delault		S/W F	Reset	•	•			N	/A	
		H/W F	Reset			4(/		N	/A	
Flow Chart	-				6		_			



7.3.11 Read_DDB_continue (A8h)

A8h	Read_DDB_conti	nue								
Aoii	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	1	0	1	0	1	0	0	0	A8
1 st parameter	D→H	Х	Х	Х	Х	Х	Х	Х	Х	XX
2 nd parameter	D→H	Х	Х	Х	Х	Х	Х	Х	Х	XX
:	D→H	Х	Х	Х	Х	Х	Х	Х	Х	XX
N th parameter	D→H	Χ	Х	Х	Х	Х	Х	Х	Х	XX
Description	A read_DDB_start read_DDB_continu read_DDB_continu	ie comn	nand to	define tl	he read				ta read v	with a
Restrictions	-							(0)		
	Status					Avail	ability			
Register	Sleep Out						es			
Availability	Sleep In					Υ	es	7		
	Status					Defaul	t value			
	Power On Sequence	Δ.	Rea	d PΔ 1 st ~	6 th is the			nd the 7 ^{tl}	^h read is	FFh
Default	S/W Reset	,,,	Rea	d PA 1 st ^	6 th is the	same a	s 00h , a	nd the 7 th	read is	FFh.
	H/W Reset								^h read is	
Flow Chart				D1[15:0	DDB J, D2[15:0] comma					



7.3.12 Read_DDB_start (A1h)

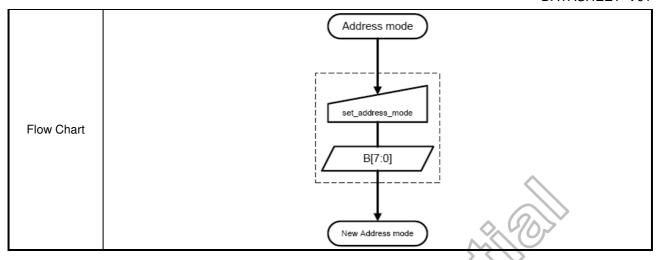
A1h	Read DDB start										
AIII	Direction		D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H->D		1	0	1	0	0	0	0	1	A1
1 st parameter	D->H		Χ	Χ	Χ	Х	Х	Х	Х	Х	XX
2 nd parameter	D->H		Χ	Χ	Χ	Χ	Χ	Χ	Χ	Х	XX
3 rd parameter	D->H		Χ	Χ	Χ	Χ	Χ	Χ	Χ	Х	XX
4 th parameter	D->H		Χ	Χ	Χ	Χ	Χ	Χ	Χ	Х	XX
:	D->H		Χ	Χ	Χ	Х	Х	Х	Х	Χ	XX
7 th parameter	D->H		1	1	1	1	1	1	1	1	FF
Description	The format of returned data Parameter 1: LS (least sign each peripheral supplier by Parameter 2: MS (most sign Parameter 3: LS (least sign determined by the supplier. Parameter 4: MS (most sign Parameter 7: single-byte Estermined by the supplier. FFh - Exit code – there is - 00h - Escape code – the to any MIPI standard)	nificant) I the MIPI gnificant) nificant) I It could in gnificant) scape or less no more	byte o organ byte o nclude byte o Exit C data	nization of Supple mode of Supple of Supple of Supple of Supple of the	n. plier II plier Ele el num plier E E EC) . T	D. ective ber or lective The co	Data. revision Data de is i	This is on info	a byte ormatic eted as	e of info on, for o	ormation that is example.
Restrictions	-					1/			_ / / /		
1100110110110	Chatria			_		A	ا ما مانات	lia.			
Register	Status			7.6		AV	ailabi	iity	\ \	,	
Availability	Sleep Out			73	///		Yes) <		
	Sleep In			\sim	/~		Yes	7/1			
	Status					Def	ault va	alue	_		
	Power On Sequence			<u></u>	ΡΔ 1		=00h, F		–FFh		
Default	S/W Reset	10	7)	V	ΡΔ 1	st~6 th	=00h, F	Δ 7 th	<u></u> -FFh		
	H/W Reset	7 (\mathcal{I}		PA 1	st~6 th	=00h, F	<u>Λ</u> 7 th	<u></u>		
	n/w neset	7		_^	FAI			- A /	=		
Flow Chart				[15:0] Dr	DDB DDB D2[15 n[15:0]	5:0],,]				



7.3.13 Set_address_mode (36h)

	Set address mode	(Memory Δc	cess Cont	rol\→M	ADCTI					
36 H	Direction	D'		D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0		1	1	0	1	1	0	36
1st parameter	H→D	0		0	0	BGR	0	Flip V	Flip H	-
13t parameter	This command defining this command make Bit Assignment	es read/write	scanning d	irection o	of frame			ription	<u> </u>	
	B7		Hame		-		DC30	ліраоп		
	B6	-			 -			\wedge		
	B5	Not Defined			- -			- 		
	B4	Not Defined						$\rightarrow + +$,	
	B3	RGB-BGR C		GR)	0=	olor select RGB co BGR co	lor filter	panel.	ol.	
	B2	Not Defined			-					
	B1	Flip Horizon			0= 1=	p Horizo Display Display	from Le from Ri			
	ВО	Flip Vertical			0=	p Vertica Display Display	from To	p to Bot	tom. Top.	
	Hos		Display P	anel		Host	B0=1	V	splay Panel	
Description	Top Left	Top Lef		To	p Left	8	Top) Left		
	Top Left	Top Le	Display I	T	op Left	Host	Тор	Dis Left.	splay Panel	
			Host R G B	—Sent	RGB -	Display R G				
Deskibilen		[Host R G B		= 1 : BGR+>	Display				
Restriction	-						-			
Register			atus					Availa		
Availability			p Out					Ye		
Availability		Sle	ep In					Ye	S	
			atus					Default		
Default			Sequence)				001		
Delault		S/W	Reset					No cha	ange	
			Reset					001		
						<u> </u>				







7.3.14 Set_display_off (28h)

Direction	D7								
	וט	D6	D5	D4	D3	D2	D1	D0	HEX
H→D	0	0	1	0	1	0	0	0	28
No parameter.									
Memory is disabled and blank This command makes no chan This command does not chang	page ins ge of co le any of	serted. Intents of ther state ton the	of frame tus. display	memor		e, the o	utput fro	om Fran	ie
							%	>	
This command has no effect w	hen mod	dule is a	already i	n displa	y off mo	ode.			
				کری			Y	'es	
	Ctatus					\sim	Dofou	lt valua	
Power									
)		$\overline{\mathcal{C}}$				
				(?	\sim				
						II.		,	
Se	et_displa	y_off							
	This command is used to enter Memory is disabled and blank This command makes no chan This command does not chang There will be no abnormal visits This command has no effect w Power S L Dis	This command is used to enter into DIS Memory is disabled and blank page ins This command makes no change of co This command does not change any o There will be no abnormal visible effect This command has no effect when more Status Sleep Or Sleep Ir Status Power On Sec S/W Res H/W Res Display par	This command is used to enter into DISPLAY Memory is disabled and blank page inserted. This command makes no change of contents of the command does not change any other state of the command the command visible effect on the command th	This command is used to enter into DISPLAY OFF mode Memory is disabled and blank page inserted. This command makes no change of contents of frame This command does not change any other status. There will be no abnormal visible effect on the display (Example Host Host Sleep Out Sleep In Status Power On Sequence S/W Reset H/W Reset Display panel on Set_display_off	This command is used to enter into DISPLAY OFF mode. In the Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) Host display. This command has no effect when module is already in display. Status Sleep Out Sleep In Status Power On Sequence S/W Reset H/W Reset Display panel on Display panel on	This command is used to enter into DISPLAY OFF mode. In this mod Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) Host display This command has no effect when module is already in display off module is already in display off module is already. Status Sleep Out Sleep In Status Power On Sequence S/W Reset H/W Reset Display panel on	This command is used to enter into DISPLAY OFF mode. In this mode, the o Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) Host display This command has no effect when module is already in display off mode. Status Sleep Out Sleep In Status Power On Sequence S/W Reset H/W Reset Display panel on	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) Host display This command has no effect when module is already in display off mode. Status Avail Sleep Out Y Sleep In Y Status Defau Power On Sequence Disples S/W Reset Disples H/W Reset Disples Disple	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Fram Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) Host display This command has no effect when module is already in display off mode. Status Availability Sleep Out Yes Sleep In Yes Status Default value Power On Sequence Display Off By Reset Display Off Display Off Display panel on Display Off



7.3.15 Set_display_on (29h)

29 H	Set_display_on (Display Or	ı) → DIS	PON							
2911	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	0	1	0	0	1	29
Parameter	No parameter.									
	This command is used to reco Memory is enabled. This command makes no char This command does not chang	nge of co	ontents other sta	of frame	e memor		from the	Frame		
Description		mer	mory		dis	play	~ (>	
								\ \ \		
Restriction	This command has no effect w	hen mo	dule is	already	in displa	y on mo	ode.	1		
Register		Status			7				ability	
Availability		Sleep O Sleep I				<	\bigcirc		es es	
		Status	;					Defaul	t value	
Defects	Powe	r On Se	quence	>			_		ay Off	
Default		S/W Res			(<	1			ay Off	
	ŀ	I/W Res	set					Displa	ay Off	
Flow Chart		set_d	y panel o)					



7.3.16 Set_pixel _format (3Ah)

3A H	Set_pixel_format (Inte	rface Pixel Fo	rmat) >	COLMC	D					
3A 11	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	1	0	1	0	3A
1 st parameter	H→D	0	D6	D5	D4	0	0	0	0	-
	This command is used to system and RGB interfation. Bit D6,D5,D4 - DPI Pixed DPI interface:	ice. The format	s are sh		the table	e:	h is to b	e transt		ne
	Interface Format	D6			D				D4	
	Not Defined	0			0				0	
	Not Defined	0			0	1	~ (/ 1	
Description	Not Defined	0			1		Q_{\wedge}^{\vee}	<u> </u>	0	
	Not Defined	0			1	_			1	
	Not Defined	1			0			>	0	
	16 Bit/Pixel	1			0	-			1	
	18 Bit/Pixel	1			1	$C(\cdot)$	\Diamond		0	
	24 Bit/Pixel	1							1	
Restriction	Bit D7,D3,D2,D1,D0 – I Set to '0' There is no visible effec		e Memo	ory is wr	itten to.	<i>!</i>				
Desistes		Status						Avail	ability	
Register Availability		Sleep Ou	ıt				77	Υ	'es	
Availability		Sleep In	W()					Y	'es	
		Status						Defau	lt value	
Default		Power On Sec							it/pixel	
Delault		S/W Res		\					hange	
		H/W Res	et					24-b	it/pixel	
Flow Chart		n bpp Mo	ormat ter							



7.3.17 Set_tear _off (34h)

34 H	Set_tear_off (Tearing Effect	Line OF	F) → TE	OFF						
34 11	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	0	1	0	0	34
Parameter	No parameter.									
Description	This command is used to turn							E signa	l line.	
Restriction	This command has no effect w	hen Tea	aring Eff	ect outp	ut is alre	eady OF	F.			
Register Availability		Status Sleep O						Availa Ye		
7 (Valiability		Sleep I	า					Υe	es	
		04-4						Defaul		
		Status					/	Default		,,
Default		r On Se						earing E		
		S/W Res				_		earing E		
	L	I/W Res	eı					earing E	ilect O	
Flow Chart			et_tea							



7.3.18 Set_tear _on (35h)

05.11	Set_tear_off (Tearing Effect	Line ON	V)→TEC	N						
35 H	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	0	1	0	1	35
1 st parameter	H→D				-		- <u> </u>	<u> </u>	М	-
Description	This command is used to turn line. The Tearing Effect Line On har Tearing Effect Output Line. (Xs.) When M=0 (mode0): The Tearing Effect Output line Vertical Time Scale When M=1 (mode1): The Tearing Effect Output Line information: Vertical Time Scale Note: (1) During Sleep In Model In the control of t	consist	aramete Care). s of V-B	lanking twell	describe	ion only	node of t	he	- n will be	active
Restriction	Low. This command has no effect w	hen Te	aring Ef	fect outp	out is alre	eady Ol	٧.			
		Status						Availa	bility	
Register		Sleep O		2.5				Ye		
Availability		Sleep I		11/2)			Υe		
				71						
		Status					-	Default		"
Default		On Se S/W Res	quence					earing E earing E		
		I/W Res						earing E		
Flow Chart			set_tea)] 7					



7.3.19 Set_tear _scanline (44h)

44 H	Set_tear_scanline (Tear Effect S	can Lir	nes) → T	ESL						
44 11	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	1	0	0	0	1	0	0	44
1 st parameter	H→D	N15	N14	N13	N12	N11	N10	N9	N8	00FF
2 nd parameter	H→D	N7	N6	N5	N4	N3	N2	N1	N0	00FF
Description	This command is turns on the disp Line when the display module read The Tearing Effect Line On has on Output Line. The Tearing Effect Output line con Vertical Time Scale Note: (1) That N=0 is equivalent to The Tearing Effect Output mode.	efes line e parar sists of	e N. meter w V-Blan tw	hich de	ormatio	n only:	ode of th	ne Tear	ing Eff	ect
Restriction	The command has no effect when	Tearing	Effect	output	is alrea	dy ON.				
		atus		-	101			Availa	ability	
Register		p Out					~ //		es	
Availability		ep In		\mathcal{C}			$\overline{\mathcal{A}}$		es	
			733	#						
		atus	- X					Defaul		
Default	Power On		nce		$-\alpha$	\rightarrow		V[15:0]		
		Reset Reset			> (/	\mathcal{I}		V[15:0] V[15:0]		
	11///	nesei		-			<u> </u>	ν [13.0]	=00001	
Flow Chart			set_teal	r_scanli N (LSB)	7 7					



7.3.20 Soft_reset (01h)

01 H	Soft reset (Software Reset)	SWRE	SET							
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	0	0	0	1	01
Parameter	No parameter.									
Description	When the Software Reset com and parameters to their S/W F description.) The display is blank immediate Note: The frame memory cont	Reset de ely. ents are	fault va e unaffe	lues. (Se	ee defau	ult table mand.	s in eac	ch comm	nand	ands
Restriction	It will be necessary to wait 5m The display module loads all of sec. If SW Reset is applied during Sleep Out command. SW Reset command cannot b	display s Sleep C	supplier Out mod	's factory	y defaul be nece	t values	to the r	egisters	during t	
		Status	S					Availa	bility	
Register		Sleep C	Out			C(I)	>	Υe		
Availability		Sleep I			6			Ye		
					\overline{C}	4) ×	_			
Default		Status r On Se S/W Res H/W Res	quence		کری			Default N/ N/ N/	'A 'A	
Flow Chart		Blank	t to SW	set Device Defaults						



7.3.21 Exit Idle mode (38h)

38 H	Exit idle mode (Idle Mode	Off)								
30 11	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	1	0	0	0	38
Parameter	No parameter.									
Description	This command causes the di In the idle off mode, LCD ca	n displa	y maxin	num 262	,144 col	ors.				
Restriction	This command has no effect	t when r	nodule	is alread	y in idle	off mod	e.			
Register Availability		Stat Sleep	Out					\wedge	ilability Yes	
7 (Vallability		Slee	p In						Yes	
i							_		3	
		Stat	us						ult value	
Default	Pov		Sequen	ce					Mode Off	
20.00.0		S/W F							Mode Off	
		H/W F	Reset					Idle I	Mode Off	
Flow Chart		ex	dle mo	_mode				5)		



7.3.22 Enter Idle mode (39h)

	Enter idle me	do (Idlo Modo ()NI)									
39 H	Direc	de (Idle Mode C	אכ) D7	D6	D5	D4	D3	D2	D1	D0	HEX	
Command	H		0	0	1	1	1	0	0	1	39	
Parameter	No parameter.				-		<u> </u>			<u> </u>		
	This command causes the display module to enter Idle Mode. In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed. (Example) Host Didplay											
Command Parameter No Th In of					\Box				20/	>		
	Memory contents vs. Display Color											
		R5 R4 R3 R			G5 G4	G3 G2	G1 G0	Е	5 B4 B3	B2 B1	B0	
	Black	0XXX	ХХ		0	XXXXX		\sim	0XX	(XXX		
	Blue	0XXX	XX			XXXXX			1XX	(XXX		
	Red	1XXXX				XXXXX				(XXX		
	Magenta	1XXX		2		XXXX				XXX		
	Green	0XXX				XXXX				(XXX		
	Cyan	0XXX		<u>~(1)</u>		XXXXX				XXX		
	Yellow	1XXX				XXXXX				XXX		
	White	1XXX		// Y		XXXXX			1 X X	XXX		
Restriction	This command	d has no effect w	hen mo	odule is	already	in idle o	ff mode	-				
			Statu	s	///				Availa	ability		
			Sleep C			7				es		
Availability		1	Sleep							es		
		71										
			Statu	S					Default	t value		
Dofault				equence	Э				Idle Mo	de Off		
Delault			S/W Re						Idle Mo			
			I/W Re	set					Idle Mo	de Off		
Flow Chart			ente	er_idle	mode]						



7.3.23 Get diagnostic result (0Fh)

0F H	Get diagnostic result (Read Display Self-Diagnostic Result)→RDDSDR											
OF II	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX		
Command	H→D	0	0	0	0	1	1	1	1	0F		
1 st parameter	H→D	D7	D6	0	0	0	0	0	0	-		
Description	The display module returns the Bit D7 – Register Loading Dete Bit D6 – Functionality Detection Bits D[5:0] – Reserved, Set to '6	ction 1	gnostic	results	following	g a Slee	ep Out o	ommar	ıd.			
Restriction	-							_				
Register		Status leep Ou	ı÷						ability es			
Availability		Sleep Ir					0, (\sim	es			
		Status							lt value			
Default		On Sec					0		<u>0h</u>			
		/W Res							<u>0h</u>			
	<u> </u>	/W Res	et					0	0h			
Flow Chart	get	diagnos	stic_resul		Host - Displa							



7.3.24 RDNUMED (05h)

05 H	RDNUMED (Read Number of t	he erro	ors on [OSI)						
03 11	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	1	0	0	1	05
1 st parameter	H→D	D7	D6	D5	D4	D3	D2	D1	D0	-
Description	The parameter is telling a numb D[6:0] bits are telling number of D[7] is set to '1' if there is overfl D[7:0] bits are set to '00h' (as w time). Please also refer to get_signal	the erro ow with rell as g	ors. D[6:0] jet_sig i	bits.)'s D0 i	s settin	ig to '0'	at the s	same
Restriction	-									
Dogistor		Status						Avail	ability	
Register Availability	S	leep Οι	ıt				3///	Υ	es	
Availability		Sleep In)			~		Y	es	
							$\overline{}$			
		Status						Defaul	t value	
Default	Power	On Sec	quence		(0	$\searrow \lor$		0	0h	
Delault	S/	W Rese	et		SIII	<i>5)</i>		0	0h	
	H/	W Res	et					0	0h	
Flow Chart				\rightarrow	- 7(C					



7.3.25 LVDS/MIPI video input timing

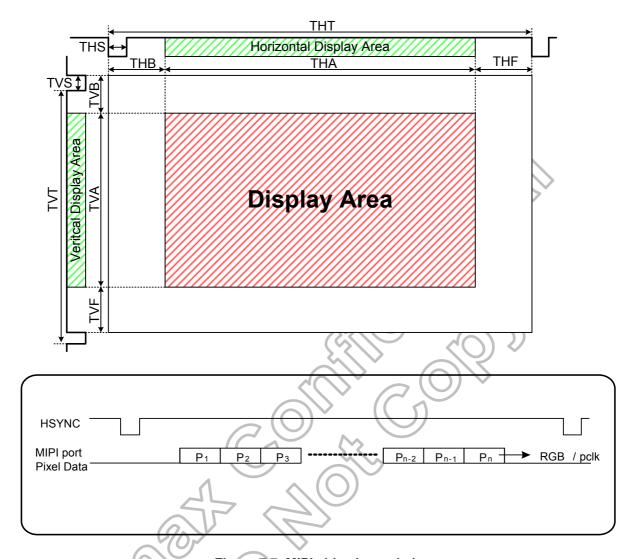


Figure 7.7: MIPI video input timing



Video input timing

Resolution		80	0RGBx12	:80	76	8RGBx10	24	Unit
Input Timing	Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Oilit
PCLK frequency	-	-	71.9	80	-	55.8	80	MHz
Horizontal total	THT	880	920	1600	848	888	1536	DCLK
Horizontal synchronization	THS	10	24	-	10	24	-	DCLK
Horizontal back porch	THB	10	24	-	10	24	-	DCLK
Horizontal address	THA	-	800	-	-	768	-	DCLK
Horizontal front porch	THF	20	72	-	20	72	-	DCLK
Vertical frequency	-	-	60	-	-	60	-	Hz
Vertical total	TVT	1300	1304	2047	1044	1048	2047	THT
Vertical synchronization	TVS	1	2	-	1	2	V -	THT
Vertical back porch	TVB	8	10	-	8	100	/ -	THT
Vertical address	TVA	-	1280	-	- (>	1024	-	THT
Vertical front porch	TVF	8	12	-	8	12	-	THT

Resolution		72	0RGBx12	80	60	0RGBx10	24	Unit
Input Timing	Symbol	Min.	Тур.	Max.	Min.	Тур.	Max.	Oilit
PCLK frequency	-	•	65.7	80	0)-	45.2	80	MHz
Horizontal total	THT	800	840	1440	680	720	1200	DCLK
Horizontal synchronization	THS	10	24	くして	10	24	1	DCLK
Horizontal back porch	THB	10	24	<u> </u>	10	24	-	DCLK
Horizontal address	THA	-	720	\\\-		600	-	DCLK
Horizontal front porch	THF	20	72	/ - (20	72	-	DCLK
Vertical frequency	-	-	60		(60	-	Hz
Vertical total	TVT	1300	1304	2047	1044	1048	2047	THT
Vertical synchronization	TVS)) 2		/ 1	2	-	THT
Vertical back porch	TVB	8	10)	8	10	-	THT
Vertical address	TVA		1280	\\ \-	-	1024	-	THT
Vertical front porch	TVF	8	12	<u> </u>	8	12	-	THT

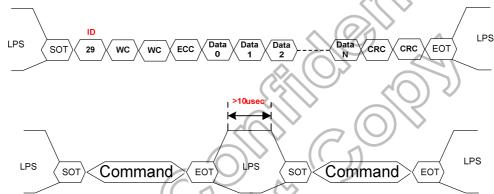
Table 7.5: MIPI input video timing

8. Register table

The HX8260-A supports set internal register by MIPI interface and SPI interface. MIPI and SPI interface use different register address. The MSB bit [7] of address is only for MIPI interface. The SPI must be ignored its. "MIPI address" and "SPI address" showed in register table.

8.1 MIPI command mode control register

The HX8260-A supports the generic long write command to set internal register. User could use HS or LP mode to write internal register. Figure 8.1 showed the reference long package structure. There is a LP timing request between HS command to next HS command. This time needs more than 10usec as figure 8.1. Detial MIPI commands describation showed in Section 8.4.



Note: (1) Data ID: Contain virtual channel identifier and data type.

(2) ECC (Error Correction Code): The error correction code allows single-bit errors to be corrected and 2-bit errors to be detected in the short packet..

Figure 8.1: Support the DSI data short write



8.2 SPI format

The HX8260-A supports the 3-pin serial peripheral interface (SPI) to set internal register. The data is written to the register of assigned address when "End of transfer" is detected after the 16th SCL rising cycles.

Data is not accepted if there are less or more than 16 cycles for one transaction. Only when SCL is input 16 times and CSB is in the "Low" period simultaneously, SDA is accepted.

The first 7 bits (A6 ~ A0) specify the address of the register. The 8th bit means Read/Write command. "0" is WRITE. "1" is READ. The last 8 bits are for Data setting (D7 ~D0). The address and data are transferred from the MSB to LSB sequentially. And next cycle is turn-round cycle.

For the MIPI mode 3-wire SPI pin are "MIPI_CSB, MIPI_SCK and MIPI_SD" For the LVDS mode 3-wire SPI pin are ""LNSW CSB, PNSW SCL, MIPITE SDA"

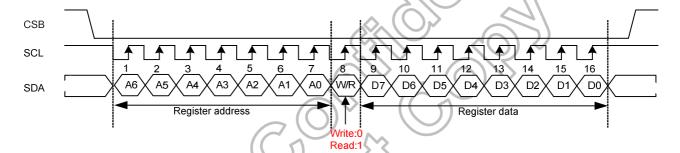
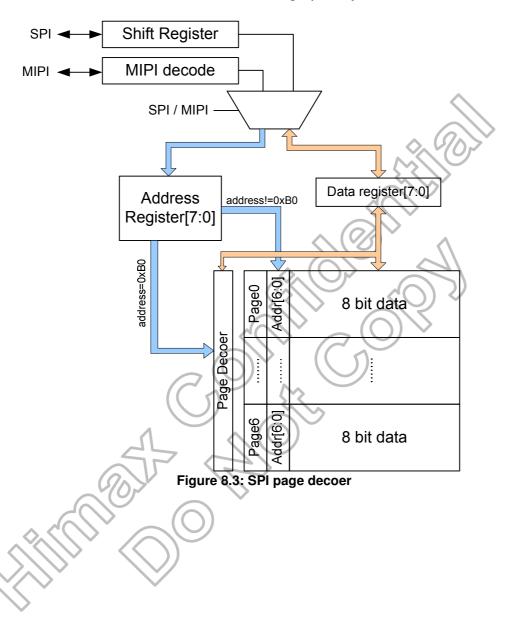


Figure 8.2: SPI format



8.3 Page change

The HX8260-A supports multi-page for register write. TCON have two path control register—SPI and MIPI. MIPI command has high priority than SPI.





8.4 User define command list and description (For MIPI command mode)

8.4.1 User define command list table

Second S	Page	Hex	operation	parameter index	D7 1	D6 0	D5 1	D4 1	D3 0	D2 0	D1 0	D0	Default Hex		
No. State State							•	VC	OMS						
Number Section Secti					-	STB	UPDNB	LR	ZIGZAG_SEL	DISP_ON	NBW_SEL	BIST			
Name					ZTYPE	_SEL	PWRN			-	RE	S			
Description Control															
O CB Control 7 PCLK SEL RX DINT RX VB LUDS VB LVOS PM 53						N	DATOM			OTD!	M	T			
Barrier Barr	0	B1											03		
Second S			COLLLO			KX_DINT		/B				LVDS_FMT			
10 BLREV BIFFCONDEF SD SSEL INV SEL A9					_	_		RW	_						
11					BLR	EV			ISSEL						
12 GAS_GOA_EN VERS_BLACK GORE_Bleewing - - - ED												-			
Note										4.12		-			
Note				parameter	1	0	1	1	1 (0	1			
Second					'			'	٠ ٧(112112	U	'			
Note							SPS		1/0/						
A															
Second S					-	-		roc		5					
Second S						VSF	PON	163	Serve	VSPOF	+	Name			
SU			_						U Y			Name			
Note	0	BD	Power					(0//	PFMFREN						
1				8				W	PHS			•	04		
1					CGPP	_INV	SOFT_EN				CMD	_SEL			
12							~())					
13							VCL_CF	PCTL			VGH_C	CPCTL			
14					POCSI	D_CIL	(0)	<u> </u>	EQU						
Parameter 1					-										
O CB Gamma						-76		∼ >				1	10		
1					1	1\))0	0	1	0	1	1			
A								P	VP1	l			3F		
A						4									
Second S															
CB Gamma						7	(2)								
CB Gamma					(0)	<u>V</u>									
CB Gamma					~(0)			P P	VP7						
O CB Gamma							7								
CB Gamma						\sim ())								
12															
1 1 1 1 1 1 1 1 1 1	0	СВ	Gamma		> <<								16		
Note															
B1 ST ST ST ST ST ST ST S						<u> </u>									
B1 B1 B1 B1 B1 B1 B1 B1															
B			Ì												
B1 B1 B1 B1 B1 B1 B1 B1															
19															
PVN9 21 PVN10 1F 16 22 PVN11 16 16 23 PVN11 16 16 23 PVN11 16 PVN11 16 PVN1 PVNN															
B1 OTP								P'	VN9						
B1 OTP				21											
B1 OTP DATE Parameter index 1 1 0 0 1 0 1 1 1 0 0				22				P۱	/N11				16		
B1				23					VE	BP .	VE	BN	B5		
B1				parameter	-1	-1	0	^	4	0	4	_			
B1				index		I	U	_		U	Į.				
1 B1 OTP 3 OTP_PTM OTP_prog_sel OTP_re_Load OTP_RD OTP_WR 00 4 OTP_ADDR 00 5 OTP_PDOB 00 6 OTP_PDIN 00 7 OTP_MANUAL 5A 8 POR PPROG VPS PWE 00															
BI							OTD DTM			IOTD !	OTD DD	OTD WO			
5 OTP_PDOB 00 6 OTP_PDIN 00 7 OTP_MANUAL 5A 8 POR PPROG VPS PWE 00	1	B1	OTP				OTP_PTM			UIP_re_Load	OIP_RD	OIP_WR			
6 OTP_PDIN 00 7 OTP_MANUAL 5A 8 POR PPROG VPS PWE 00 2 B1 MUXI															
7 OTP_MANUAL 5A 8 POR PPROG VPS PWE 00 2 B1 MUX															
2 B1 MUX															
2 B1 MUX								<u> </u>		PPROG	VPS	PWE			
	2	B1	MUXL		4	0	4	4	0						

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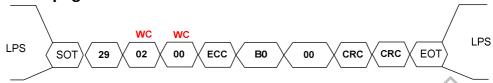
Page	Hex	operation	parameter	D7	D6	D5	D4	D3	D2	D1	D0	Default
			index index	1	0	1	1	0	0	0	1	Hex
			1	GOUTL1 S	TBYB MOD			GOUTL	l 1 SFI			08
			2		TBYB_MOD			GOUTL_	2_SEL			08
			3		TBYB_MOD			GOUTL_				06
			4		TBYB_MOD			GOUTL_				06
			5 6		TBYB_MOD TBYB MOD			GOUTL_ GOUTL_				0C 0C
			7		TBYB_MOD			GOUTL_				0A
			8	GOUTL8_S				GOUTL_				0A
			9	GOUTL9_S	TBYB_MOD			GOUTL_	9_SEL			02
			10		STBYB_MOD			GOUTL_1				00
			11		TBYB_MOD			GOUTL_1				00
			12 13	GOUTL12_S	TBYB_MOD			GOUTL_1 GOUTL_1				00
			14	GOUTL14 S				GOUTL_1		7 .>		00
			15		STBYB_MOD			GOUTL_1		0)"		00
			16		STBYB_MOD			GOUTL_1				04
			17		TBYB_MOD			GOUTL_1				00
			18 19	GOUTL18_S	TBYB_MOD			GOUTL 1				00
			20		STBYB MOD			GOUTL_2				00
			21		STBYB MOD			GOUTL				00
			22	GOUTL22_S	STBYB_MOD			GOUTL_2				00
			parameter	1	1	0	0	0	4	1	1	
			index						1 651			07
			2	GOUTR1_S GOUTR2 S			(6//	GOUTR_ GOUTR) 		07 07
			3		TBYB MOD		11/2	GOUTR				05
			4	GOUTR4_S		.6		GOUTR				05
			5	GOUTR5_S		(1)		GOUTR_				0B
			6	GOUTR6_S				GOUTR_				0B
			7 8	GOUTR7_S	TBYB_MOD	(())		GOUTR_ GOUTR				09 09
			9	GOUTR9_S		7	Λ.	GOUTR				09
			10	GOUTR10_S		n	2.3	GOUTR_				00
2	C7	MUXR	11		STBYB_MOD			GOUTR_				00
			12		STBYB_MOD			GOUTR_				00
			13 14	GOUTR13_S	STBYB_MOD			GOUTR_1 GOUTR_1	_			00
			15	GOUTR15_S				GOUTR_				00
			16		STBYB_MOD	11		GOUTR_				03
			17	GOUTR17_S	TBYB_MOD			GOUTR_	I7_SEL			00
			18		STBYB_MOD			GOUTR_	_			00
			19 20		STBYB_MOD STBYB MOD))		GOUTR_2	_			00
			21		STBYB MOD			GOUTR_2				00
			22		STBYB_MOD			GOUTR_2				00
			23	VGL_GAS	GOA_VGOFF_EN	GOA_PWROFF	GOA_HZ_EN	_				40
			parameter	1	1	0	0	0	1	1	1	
			index 1			DIM EN	BL EN	CABC AGAIN		CABC AGAIN		3B
			2			DIM_EN	DL_EIN		STEP	DIM F		09
	D4	0400	3			1	DUT	Y UD	012.		1 (1V) E	FF
4	B1	CABC	4					C_MB				10
			5			,	PWN	<u>/_PRD</u>				00
			6			l	D-		<u> </u>	PWM_DIV		02
			7 8					serve DUTY				00 FF
			parameter			<u> </u>			<u> </u>			11
			index	1	0	1	1	0	0	0	1	
			1	EoTp_EN	CRCEN	CRCErr_FilterOut	VC4FRAME	VC	_S	VC	_m	E0
			2					serve				80
6	B1	MIPI	3					serve				80
			<u>4</u> 5			RT3	res	serve		RT2		00 55
	i i		6		<u> </u>	RT1				RT0		53
		l.							10			



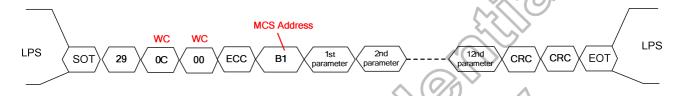
8.4.2 Function Control register (page0 B1h)

User could use HS or LP command send data.

Step 1 set to page0



Step 2 set function control register



Page	B1H			Fu	nction con	trol register				
	Command	D7	D6	D5	D4	D3	D2	D1	D0	Hex
	Command	1	0	1	1	0	0	0	1	B1
	1st parameter			40	VCOMS					-
	2nd parameter	-	STB	UPDNB	LR	ZIGZAG_SEL	DISP_ON	NBW_SEL	BIST	-
	3rd parameter	ZTYPE	_SEL	PWRM	ID OIL	VRES_FIX	-	RI	ES	-
	4th parameter			$\sim (())$	VRES					-
0	5th parameter				ZDATA					-
U	6th parameter	LNS	SW	PNSW	HFRC_INV	CABC_	CTRL	DITHER_EN	HFRC_EN	-
	7th parameter	PCLK_SEL	RX_DINT	RX_V	В	-	LVD	S_VB	LVDS_FMT	-
	8th parameter	-	1	LVDS_TD		-		LVDS_TC		-
	9th parameter	1	-	LVDS_E	3W	-		LVDS_CPB		-
	10th parameter	BLF	REV	BLREVONOFF	SD_	_ISSEL		INV_SEL		-
	11th parameter	BC_CTRL	GOA_EN	RB_SWAP	DPFM_	OSC_SEL	LN	SEL	-	-
	12th parameter	GAS GOA EN	VRES BLACK	GCHL Blanking	-	-	-	-	-	-

This command is used for function control.

VCOMS[7:0]: Adjust the VCOM output voltage (default VCOM voltage -1.48V).

VCOMS[7:0]	VCOM voltage
0000000	-0.2V
0000001	-0.21V
0000010	-0.22V
<u>:</u>	:
:	:
1000000	-1.48V (default)
:	:
:	:
11111111	-2.75V

Description

BIST: BIST mode selection.

- 1: Normal display mode.
- 0: BIST mode.

NBW_SEL: Normal Black and Normal white panel selection.

- 1: Normally black.
- 0: Normally White.

DISP_ON: MIPI DCS: 0x28 display on, 0x29 display off.

- 1: Reverse MIPI DCS command (to MIPI DCS command do "XOR" operation).
- 0: Follow MIPI DCS command.

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DATASHEET V01

ZIGZAG SEL: Panel driving method selection.

1: Zigzag type panel.

0: Strip panel.

LR: Horizontal direction select.

MIPI DCS 0x36 set address mode[6] command and SPI register do XOR operation.

UPDNB: Vertical direction select.

MIPI DCS 0x36 set_address_mode[7] command and SPI register do XOR operation.

STB: TCON sleep mode selection.

MIPI DCS 0x10 (Enter sleep mode), and 0x11 (exit sleep mode). MIPI DCS command do XOR with SPI register.

RES[1:0]: Resolution selection (to pin HW RES do XOR operation).

Resolution setting please refer section 6.1

VRES_FIX: Display vertical Line decide by

1: RES[2:0].

0: VRES (4th parameter).

PWRMD[1:0]: POWR ON mode (to pin PWRMD do XOR operation).

PWRMD[1]	PWRMD[0]	Driving mode
0	0	Support HX5186-C power mode
0	1	Suppot PFM circuit power mode
1	0	External VSP, VSN, VGH, VGL power mode
1	1	External VSP,VSN power mode

ZTYPE_SEL[1:0]: Zigzag type slection (panel type please refer section 6.3).

VRES [7:0]: Vertical Resolution select, HX8260-A support user define vertical resolution. User could enable the set VRES_FIX=1 and set VRES [7:0]. Range=80~ 253, step= 8H

ZDATA [5:0]: Setting ZigZag dummy data select.range 0~63

HFRC EN: Hi-FRC function enable.

1: HFRC enable.

0: HFRC disable.

DITHER_EN: Dithering function enable.

1: Dithering enable.

0: Dithering disable.

CABC CTRL[1:0]: CABC-Mode selection:

OVDOZOTITE[1:0]:	CAIDO MIDAG SCICOL	1011:
CABC_CTRL[1]	CABC_CTRL[0]	CABC Mode
0	0	Bypass Mode <default></default>
0	1	Still-Mode
1	0	Ul-Mode
1	1	Movingl-Mode

HFRC INV: HI-FRC function inversion.

1: HFRC code 4, 9, 14 (Default=1).

0: HFRC code=241, 246, 251

PNSW: MIPI/LVDS pin change polarity (to pin PNSW do XOR operation).

1: P/N swap.

0: P/N follow pin name.

LNSW[1:0]: MIPI lane swap (to pin LNSW do XOR operation).

				D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N
LNSW[1]	LNSW[0]		MIPI lanes mapping table								
0	0	D3P	D3N	D2P	D2N	CLKP	CLKN	D1P	D1N	D0P	D0N
0	1	D3P	D3N	D0P	D0N	CLKP	CLKN	D1P	D1N	D2P	D2N
1	0	D0P	D0N	D1P	D1N	CLKP	CLKN	D2P	D2N	D3P	D3N
1	1	D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	DON	D3P	D3N

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LVDS_FMT: LVDS data format selection.

1: Thine or VESA format.

0: NS or JEIDA format.

LVDS_VB[1:0]: LVDS DLL bias current selection.

LVDS_VB[1]	LVDS_VB[0]	LVDS DLL bias current
0	0	82%
0	1	100% (default)
1	0	137%
1	1	160%

LVDS RX[1:0]: LVDS bias current selection.

LVDS_RX[1]	LVDS_RX[0]	LVDS bias current
0	0	75%
0	1	100% (default)
1	0	125%
1	1	150%

RX DINT: LVDS 8/6 bit mode.

1: 8bit mode.

0: 6 bit mode.

PCLK_SEL:TCON PCLK source selection.

1: From EXT_CLK.

0: Fome internal OSC25M.

LVDS_TC[2:0]: LVDS_TC skew tuning for LVDS Clock lanes 1setp delay 0.18 nsec. LVDS_TD[2:0]: LVDS_TC skew tuning for LVDS Data lanes 1setp delay 0.18 nsec.

LVDS_CPB[2:0]: LVDS DLL pump current selection. I=20u*CPB[2]+10u*CPB[1]+5u*CPB[0]

LVDS_BW[1:0]: LVDS DLL bandwidth selection.

LVDS_BW[1]	LVDS_BW[0]	LVDS bias current
0	(0) 0	100%
0	1	91% (default)
	0	83%
	1	77%

INV_SEL[2:0]: Normal mode POL inversion type selection (for strip panel only).

	_ /	31	\ 11 37	
	INV_SEL[2]	INV_SEL[1]	INV_SEL[0]	Inversion tpye
	0	0	0	line inversion
	0	0	1	2-line inversion
ĺ	0	1	0	4-line inversion
	0	1	1	column inversion
Ì	1	0	0	8-line inversion

SD_ISSEL[1:0]: Source output bias current selection.

BLREV[1:0]: Source output status at V-blanking.

00:SD keep output the last line.

01: Hi-Z.

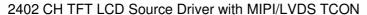
1X: GND.

LNSEL[1:0]: MIPI lane number control. The register do XOR with LANE1_STBYB & LANE0_BISTB pin.

DPFM_OSC_SEL[1:0]: DPFM clock selection (for BIST mode use).

DPFM_OSC_SEL[1]	DPFM_OSC_SEL[0]	DPFM frequency
0	0	6.25MHz
0	1	12.5MHz
1	0	25MHz
1	1	25MHz

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RB_SWAP: Red and Blue color swap.

1: R/B swap.

0: Non-swap.

GOA_EN: GOA signals enable.

1: Enable.

0: Disable.

BC CTRL: H/W pin BC CTRL control.

 $\label{lem:clr} \textbf{GCHL_Blanking:} \textbf{CLR power on status selection}.$

1: CLR1 =GND, CLR2=High level ,when power on status.

0: CLR1/2 =GND, when power on status.

VRES_BLACK: when user change VRES register, TCON will send two black pattern

1: Enable.

0: Disable.

GAS GOA EN: when enable gas function, GOA CKV/STV pulled to high level.

1: Enable.

0: Disable.



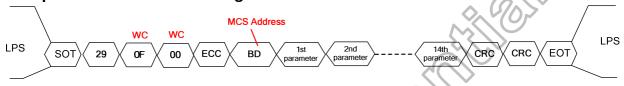
8.4.3 Power Control register(page0 BDh)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set Gamma control register



BDH				Functio	n control register			
Command	D7	D6	D5	D4	D3 D2	D1	D0	Hex
	1	0	1	1 🔊	1	0	1	BD
1st parameter		VS	PS		>	SNS		-
2nd parameter	ı	1		> <	VGHS			-
3rd parameter	ı	1			VGLS			-
4th parameter				Reser				-
5th parameter		VSF	PON		VS	POFF		-
6th parameter		VS1	NON					-
7th parameter		VGLXSP	VGHXSP)、	PFMFRE T_OFFS N ET	6		-
8th parameter			(7)		S			-
9th parameter	CGPP	_INV	SOFT_EN		CLK_SEL	CMD	_SEL	-
10th parameter		1		VNH	S			-
11th parameter	1	Ì	VCL_C	PCTL	VGL_CPCTL	VGH_	CPCTL	-
12th parameter	POCSE	CTL	16	7	EQ0W			-
13th parameter	- 6//) <u>-</u>	-		EQ1W			-
14th parameter		-		>	EQ2W			-
	Command 1st parameter 2nd parameter 3rd parameter 4th parameter 5th parameter 6th parameter 7th parameter 8th parameter 9th parameter 10th parameter 11th parameter 12th parameter 13th parameter	Command D7 1st parameter 2nd parameter 3rd parameter 4th parameter 5th parameter 6th parameter 7th parameter 8th parameter 9th parameter 11th parameter 12th parameter 13th parameter	Command D7 D6 1 0 1st parameter VS 2nd parameter 3rd parameter 4th parameter 5th parameter VSF 6th parameter VSN 7th parameter VGLXSP 8th parameter 9th parameter CGPP_INV 10th parameter 12th parameter POCSD_CTL 13th parameter	Command D7 D6 D5 1 0 1 1st parameter VSPS 2nd parameter - - 3rd parameter - - 4th parameter VSPON 6th parameter VSNON 7th parameter VGLXSP VGHXSP 8th parameter - CGPP_INV SOFT_EN 10th parameter - VCL_C 12th parameter - - VCL_C 13th parameter - - -	Command D7 D6 D5 D4 1 0 1 1 1st parameter VSPS VSPS 2nd parameter - - 3rd parameter - - 4th parameter VSPON 6th parameter VSNON 7th parameter VGLXSP VGHXSP 8th parameter VPH 9th parameter CGPP_INV SOFT_EN 10th parameter - VCL_CPCTL 12th parameter POCSD_CTL - 13th parameter - -	Command D7 D6 D5 D4 D3 D2 1 0 1 1 1 1 1st parameter VSPS V V 2nd parameter - VGHS VGHS 3rd parameter - VGLS VGLS 4th parameter VSPON VS 6th parameter VSNON VS 7th parameter VGLXSP VGHXSP PFMFRE T_OFFS N ET 8th parameter CGPP_INV SOFT_EN CLK_SEL 10th parameter - VCL_CPCTL VGL_CPCTL 12th parameter - - VCL_CPCTL EQ0W 13th parameter - - - EQ1W	Command D7 D6 D5 D4 D3 D2 D1 1 0 1 1 1 1 0 1st parameter VSPS VSNS VSNS VSNS 2nd parameter - VGHS VSNS VSNS 3rd parameter - VGLS VGLS VGLS 4th parameter VSPON VSPOFF VSNOFF 6th parameter VSNON VSNOFF VSNOFF 7th parameter VGLXSP VGHXSP PFMFRE T OFFS N ET VPHS 9th parameter CGPP INV SOFT EN CLK SEL CMD CVNHS 10th parameter - VCL CPCTL VGL CPCTL CPCTL VGL CPCTL CPCT	Command D7 D6 D5 D4 D3 D2 D1 D0 1 0 1 1 1 1 0 1 1st parameter VSPS VSNS VSNS VSNS VSNS 2nd parameter - - VGHS VSNS VSNS 3rd parameter - - VGLS VGLS VGLS VSPOFF 4th parameter VSPON VSPOFF VSNOFF VSNOFF VSNOFF VSNOFF PFMFRE T OFFS N ET N ET VPHS Sth parameter VPHS VPHS VSNOFF VSNOFF

VSNS[3:0]: VDDN voltage selection (step=0.1V).

VSNS [3:0]	Voltage
0000	-4.5V
0001	-4.6V
0010	-4.7V
:	:
:	:
1010	-5.5V (default)
:	:
:	:
1111	-6V

Description

VSPS[3:0]: VDDP voltage selection (step=0.1V). VSPS [3:0]	Voltage
0000	4.5V
0001	4.6V
0010	4.7V
:	:
:	:
1010	5.5V (default)
:	:
:	:
1111	6V

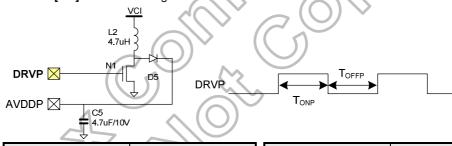


VGHS [5:0]: VGH voltage selection.	
VGHS [5:0]	Voltage
000000	8V
000001	8.2V
000010	8.4V
:	:
:	:
100011	15V (default)
:	:
:	:
111111	20.6V

VGLS [5:0]: VGL voltage selection.

Valo [3:0]. Val Voltage selection.	
VGLS [5:0]	Voltage
000000	-6V
000001	-6,2V
000010	-6.4V
:	
010100	-10V (default)
:	
111111	-18.6V

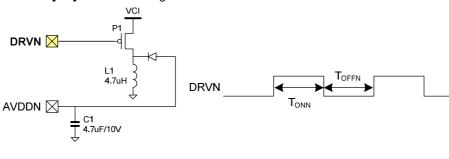
VSPON [3:0]: Set VSP voltage PFM TON time. VSPOFF [3:0]: Set VSP voltage PFM TOFF time.



VSPON_T[3:0]	T _{ONP} (μs)
//0	1.0
	1.2
2	1.4
3	1.6
13	3.6
14	3.8
15	4.0

VSPOFF_T[3:0]	T _{OFFP} (μs)
0	1.0
1	1.2
2	1.4
3	1.6
	ſ
13	3.6
14	3.8
15	4.0

VSNON [3:0]: Set VSN voltage PFM TON time. VSNOFF [3:0]: Set VSN voltage PFM TOFF time.



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DATASHEET V01

VSNON_T[3:0]	T _{ONN} (μs)	VSNOFF_T[3:0]	T _{OFFN} (μs)
0	1.0	0	1.0
1	1.2	1	1.2
2	1.4	2	1.4
3	1.6	3	1.6
			J
13	3.6	13	3.6
14	3.8	14	3.8
15	4.0	15	4.0

T OFFSET: PFM ton / toff time offset.

- 1: Enable.
- 0: Disable.

PFMFREN: enablefrequency randomizer of both VDDP and VDDN PFM

- 1: Enable.
- 0: Disable.

VGHXSP[1:0]: VGL boost function selection.

00: 2VSP.

01: 2VSP+(-VSN).

1x: 2VSP+2(-VSN).

VGLXSP: VGL boost function selection.

- 1: 2VSN-VSP.
- 0: VSN-VSP.

VPHS [4:0]: Positive gamma H selection.

VPHS [4:0]	Voltage
00000	4
00001	4.05V
00010	4.1V
00100	4.2V (default)
25	:
11111	5.5V

CMD_SEL[1:0]: Power mode 00: charge Pump command selection.

CMD_SEL[1]	CMD_SEL[0]	Pump command
0	0	x1.5
0	1	x2 (default)
\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\\	0	x3
1	1	x3

CLK_SEL[2:0]: Power mode 00: charge Pump frequency selection.

zak_oza[zio]: i onei mede ee: enarge i amp medaeney eereenem									
CLK_SEL[2:0]	Frequency								
000	403kHz								
001	595kHz								
010	781 kHz								
011	963kHz (default)								
100	1136 kHz								
101	1389kHz								
110	1786kHz								
111	2083kHz								

SOFT_EN: Power mode 00: Charge Pump soft start enable.

- 1: Enable.
- 0: Disable.



CGPP_INV[1:0]: Power mode 00 charge pump output signal invert. CGPP_INV [1] set the DRVN signal, CGPP_INV [0] set the DRVP signal.

1: Invert.

0: Non-invert.

VNHS[4:0]: Negative gamma high selection.

VNHS [4:0]	Voltage
00000	-4
00001	-4.05V
00010	-4.1V
:	
00100	-4.2V (default)
: :	
11111	-5.5V

VGH_CPCTL[1:0]: VGH charge pump clock frequency selection. VGL_CPCTL[1:0]: VGH charge pump clock frequency selection. VCL_CPCTL[1:0]: VGH charge pump clock frequency selection.

CPCTL[1]	CPCTL[0]	Pump frequency (unit:line frequency)
0	0	x1
0	1	x2 (default)
1	0	(x4)
1	1	X8

EQ0W[5:0]: Source EQ0 time setting.

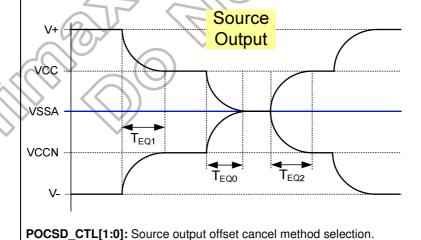
TEQ0=EQ0W[4:0]x4 DCLK (Min is 12DCLK).

EQ1W[4:0]: Source EQ1 time setting.

TEQ1=EQ1W[4:0]x4 DCLK.

EQ2W[4:0]: Source EQ1 time setting.

TEQ2=EQ2W[4:0]x4 DCLK (TEQ2≤TOEV-22DCLK satisfies gate driver settle time).



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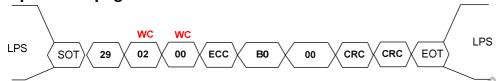
	POCSD_CTL=00b	POCSD_CTL=01b
	L1 L2 L3 L4 L5 L6 L7 L8	L1 L2 L3 L4 L5 L6 L7 L8
Frame	1 0 1 1 0 0 1 1 0	Frame1 1 1 0 0 1 1 0 0
Frame	2 0 0 1 1 0 0 1 1	Frame2 1 1 0 0 1 1 0 0
Frame	3 1 0 0 1 1 0 0 1	Frame3 0 0 1 1 0 0 1 1
Frame ⁴	1 1 0 0 1 1 0 0	Frame4 0 0 1 1 0 0 1 1
Frames	0 1 1 0 0 1 1 0	Frame5 1 1 0 0 1 1 0 0
Frame	6 0 0 1 1 0 0 1 1	Frame6 1 1 0 0 1 1 0 0
	POCSD_CTL=10b	POCSD_CTL=11b
	L1 L2 L3 L4 L5 L6 L7 L8	L1 L2 L3 L4 L5 L6 L7 L8
Frame	1 1 0 1 0 1 0 1 0	Frame1 0 0 0 0 0 0 0 0
Frame	2 1 0 1 0 1 0 1 0	Frame2 0 0 0 0 0 0 0 0
Frame	3 0 1 0 1 0 1 0 1	Frame3 0 0 0 0 0 0 0 0
Frame	1 0 1 0 1 0 1 0 1	Frame4 0 0 0 0 0 0 0 0
Frames	1 0 1 0 1 0 1 0	Frame5 0 0 0 0 0 0 0 0
Frame	6 1 0 1 0 1 0 1 0	Frame6 0 0 0 0 0 0 0 0



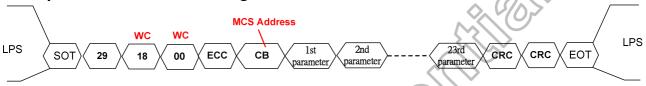
8.4.4 Gamma Control register(page0 CBh)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set Gamma control register



Page	CBH				Gan	nma control register						
	Command	D7	D6	D5	D4	D3 D2	D1 D0	Hex				
	Command	1	1	0	0	1 0	1	СВ				
	1st parameter		PVP1									
	2nd parameter				P\	VP2		-				
	3rd parameter		PVP3 -									
	4th parameter					VP4) / `	-				
	5th parameter					VP5		-				
	6th parameter					/P6		-				
	7th parameter				P	VP7		-				
	8th parameter		PVP8 PVP9									
	9th parameter		-									
	10th parameter		-									
0	11th parameter		PVP1)									
	12th parameter		PVN1									
	13th parameter			C <		/N2		-				
	14th parameter		(0,)		P۱	/N3		-				
	15th parameter		<u> </u>			/N4		-				
	16th parameter					/N5		-				
	17th parameter			\sim (\odot)		/N6		-				
	18th parameter					/N7		-				
	19th parameter					/N8		-				
	20th parameter			//		/N9		-				
	21st parameter					′N10		-				
	22nd parameter				PV	<u>'N11</u>	_	-				
	23rd parameter	-	-	-	-	VBP	VBN	-				

	Name	Description
	PVP1	Control 1st Positive gamma op's input voltage. default:3.462V~4.250V step=12.5mV
	PVP2	Control 2nd Positive gamma op's input voltage. default:3.312V~4.100V step=12.5mV
		Control 3dr Positive gamma op's input voltage. default:3.212V~4.000V step=12.5mV
		Control 4th Positive gamma op's input voltage. default:2.750V~3.537V step=12.5mV
		Control 5th Positive gamma op's input voltage. default:2.350V~3.137V step=12.5mV
	PVP6	Control 6th Positive gamma op's input voltage. default:1.862V~2.650V step=12.5mV
Description	PVP7	Control 7th Positive gamma op's input voltage. default:1.337V~2.125V step=12.5mV
		Control 8th Positive gamma op's input voltage.default:1.175V~1.962V step=12.5mV
		Control 9th Positive gamma op's input voltage.default:0.500V~1.287V step=12.5mV
		Control 10th Positive gamma op's input voltage. default:0.237V~1.025V step=12.5mV
		Control 11th Positive gamma op's input voltage. default:0.012V~0.800V step=12.5mV
		Control 1st Negative gamma op's input voltage.default:-3.462V~-4.250V step=-12.5mV
		Control 2nd Negative gamma op's input voltage. default:-3.312V~-4.100V step=-12.5mV
		Control 3dr Negative gamma op's input voltage. default:-3.212V~-4.000V step=-12.5mV
	PVN4	Control 4th Negative gamma op's input voltage.default:-2.750V~-3.537V step=-12.5mV

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PVN5	Control 5th Negative gamma op's input voltage.default:-2.350V~-3.137V step=-12.5mV
PVN6	Control 6th Negative gamma op's input voltage.default:-1.862V~-2.650V step=-12.5mV
PVN7	Control 7th Negative gamma op's input voltage. default:-1.337V~-2.125V step=-12.5mV
PVN8	Control 8th Negative gamma op's input voltage.default:-1.175V~-1.962V step=-12.5mV
PVN9	Control 9th Negative gamma op's input voltage.default:-0.500V~-1.287V step=-12.5mV
PVN10	Control 10th Negative gamma op's input voltage.default:-0.237V~-1.025V step=-12.5mV
PVN11	Control 11th Negative gamma op's input voltage.default:0.012V~0.800V step=-12.5mV

Register	P11 gam								==		
setting	PVP1	PVP2	PVP3	PVP4	PVP5	PVP6	PVP7	PVP8	PVP9	PVP10	PVP11
3F	4.25	4.1	4	3.5375	3.1375	2.65	2.125	1.9625	1.2875	1.025	0.8
3E	4.2375	4.0875	3.9875	3.525	3.125	2.6375	2.1125	1.95	1.275	1.0125	0.7875
3D	4.225	4.075	3.975	3.5125	3.1125	2.625	2.1	1.9375	1.2625	1	0.775
3C	4.2125	4.0625	3.9625	3.5	3.1	2.6125	2.0875	1.925	1.25	0.9875	0.7625
3B	4.2	4.05	3.95	3.4875	3.0875	2.6	2.075	1,9125	1.2375	0.975	0.75
3A	4.1875	4.0375	3.9375	3.475	3.075	2.5875	2.0625	1.9	1.225	0.9625	0.7375
39	4.175	4.025	3.925	3.4625	3.0625	2.575	2.05	1.8875	1.2125	0.95	0.725
38	4.1625 4.15	4.0125	3.9125 3.9	3.45	3.05 3.0375	2.5625	2.0375	1.875	1.2 1.1875	0.9375 0.925	0.7125 0.7
37 36	4.1375	3.9875	3.8875	3.4375 3.425	3.0375	2.55 2.5375	2.025	1.8625 1.85	1.175	0.925	0.6875
35	4.1373	3.975	3.875	3.4125	3.0125	2.525	2.0123	1.8375	1.175	0.9123	0.675
34	4.1125	3.9625	3.8625	3.4	3.0123	2.5125	1.9875	1.825	1.1023	0.8875	0.6625
33	4.1	3.95	3.85	3.3875	2.9875	2.5	1.975	1.8125	1.1375	0.875	0.65
32	4.0875	3.9375	3.8375	3.375	2.975	2.4875	1.9625	1.8	1.125	0.8625	0.6375
31	4.075	3.925	3.825	3.3625	2.9625	2.475	1.95	1.7875	1.1125	0.85	0.625
30	4.0625	3.9125	3.8125	3.35	2.95	2.4625	1.9375	1.775	1.1	0.8375	0.6125
2F	4.05	3.9	3.8	3.3375	2.9375	2.45	1.925	1.7625	1.0875	0.825	0.6
2E	4.0375	3.8875	3.7875	3.325	2.925	2.4375	1.9125	1.75	1.075	0.8125	0.5875
2D	4.025	3.875	3.775	3.3125	2.9125	2.425	1.9	1.7375	1.0625	8.0	0.575
2C	4.0125	3.8625	3.7625	3.3	2.9	2.4125	1.8875	1.725	1.05	0.7875	0.5625
2B	4	3.85	3.75	3.2875	2.8875	2.4	1.875	1.7125	1.0375	0.775	0.55
2A	3.9875	3.8375	3.7375	3.275	2.875	2.3875	1.8625	1.7	1.025	0.7625	0.5375
29	3.975	3.825	3.725	3.2625	2.8625	2.375	1.85	1.6875	1.0125	0.75	0.525
28	3.9625	3.8125	3.7125	3.25	2.85	2.3625	1.8375	1.675	1	0.7375	0.5125
27	3.95	3.8	3.7	3.2375	2.8375	2.35	1.825	1.6625	0.9875	0.725	0.5
26	3.9375	3.7875	3.6875	3.225	2.825	2.3375	1.8125	1.65	0.975	0.7125	0.4875
25	3.925	3.775	3.675	3.2125	2.8125	2.325	1.8	1.6375	0.9625	0.7	0.475
24	3.9125	3.7625	3.6625	3.2	2.8	2.3125	1.7875	1.625	0.95	0.6875	0.4625
23	3.9	3.75	3.65	3.1875	2.7875	2.3	1.775	1.6125	0.9375	0.675	0.45
22	3.8875	3.7375	3.6375	3.175	2.775	2.2875	1.7625	1.6	0.925	0.6625	0.4375
21 20	3.875	3.725	3.625	3.1625	2.7625 2.75	2.275	1.75	1.5875	0.9125	0.65	0.425
1F	3.8625 3.85	3.7125 3.7	3.6125	3.15		2.2625	1.7375	1.575		0.6375	0.4125 0.4
1E	3.8375	3.6875	3.5875	3.1375 3.125	2.7375 2.725	2.25 2.2375	1.725 1.7125	1.5625 1.55	0.8875 0.875	0.625 0.6125	0.3875
.1D	3.825	3.675	3.575	3.1125	2.7125	2.2373	1.7 123	1.5375	0.8625	0.6123	0.375
10	3.8125	3.6625	3.5625	3.1	2.7	2.2125	1.6875	1.525	0.85	0.5875	0.3625
1B	3.8	3.65	3.55	3.0875	2.6875	2.2	1.675	1.5125	0.8375	0.575	0.35
1A	3.7875	3.6375	3.5375	3.075	2.675	2.1875	1.6625	1.5	0.825	0.5625	0.3375
19	3.775	3.625	3.525	3.0625	2.6625	2.175	1.65	1.4875	0.8125	0.55	0.325
18	3.7625	3.6125	3.5125	3.05	2.65	2.1625	1.6375	1.475	0.8	0.5375	0.3125
17	3.75	3.6	3.5	3.0375	2.6375	2.15	1.625	1.4625	0.7875	0.525	0.3
16	3.7375	3.5875	3.4875	3.025	2.625	2.1375	1.6125	1.45	0.775	0.5125	0.2875
15	3.725	3.575	3.475	3.0125	2.6125	2.125	1.6	1.4375	0.7625	0.5	0.275
14	3.7125			3	2.6	2.1125	1.5875	1.425	0.75	0.4875	0.2625
13	3.7	3.55	3.45	2.9875	2.5875	2.1	1.575	1.4125	0.7375	0.475	0.25
12	3.6875	3.5375	3.4375	2.975	2.575	2.0875	1.5625	1.4	0.725	0.4625	0.2375
11	3.675	3.525	3.425	2.9625	2.5625	2.075	1.55	1.3875	0.7125	0.45	0.225
10	3.6625	3.5125	3.4125	2.95	2.55	2.0625	1.5375	1.375	0.7	0.4375	0.2125
F	3.65	3.5	3.4	2.9375	2.5375	2.05	1.525	1.3625	0.6875	0.425	0.2
E	3.6375	3.4875	3.3875	2.925	2.525	2.0375	1.5125	1.35	0.675	0.4125	0.1875
D	3.625	3.475	3.375	2.9125	2.5125	2.025	1.5	1.3375	0.6625	0.4	0.175
С	3.6125	3.4625	3.3625	2.9	2.5	2.0125	1.4875	1.325	0.65	0.3875	0.1625
	3.6	3.45	3.35	2.8875	2.4875	2	1.475	1.3125	0.6375	0.375	0.15
В	0 5075		3.3375	2.875	2.475 2.4625	1.9875	1.4625	1.3	0.625	0.3625	0.1375
B A	3.5875	3.4375	2 200		- ノ 4カンカ	1.975	1.45	1.2875	0.6125	0.35	0.125
B A 9	3.575	3.425	3.325	2.8625			1 /1075	1 075	0.6		
B A 9	3.575 3.5625	3.425 3.4125	3.3125	2.85	2.45	1.9625	1.4375	1.275	0.6	0.3375	0.1125
B A 9 8 7	3.575 3.5625 3.55	3.425 3.4125 3.4	3.3125 3.3	2.85 2.8375	2.45 2.4375	1.9625 1.95	1.425	1.2625	0.5875	0.3375 0.325	0.1125 0.1
B A 9 8 7 6	3.575 3.5625 3.55 3.5375	3.425 3.4125 3.4 3.3875	3.3125 3.3 3.2875	2.85 2.8375 2.825	2.45 2.4375 2.425	1.9625 1.95 1.9375	1.425 1.4125	1.2625 1.25	0.5875 0.575	0.3375 0.325 0.3125	0.1125 0.1 0.0875
B A 9 8 7	3.575 3.5625 3.55	3.425 3.4125 3.4	3.3125 3.3	2.85 2.8375	2.45 2.4375	1.9625 1.95	1.425	1.2625	0.5875	0.3375 0.325	0.1125 0.1

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2	3.4875	3.3375	3.2375	2.775	2.375	1.8875	1.3625	1.2	0.525	0.2625	0.0375
1	3.475	3.325	3.225	2.7625	2.3625	1.875	1.35	1.1875	0.5125	0.25	0.025
0	3.4625	3.3125	3.2125	2.75	2.35	1.8625	1.3375	1.175	0.5	0.2375	0.0125

Register setting	PVN1	PVN2	ge map	PVN4	PVN5	PVN6	PVN7	PVN8	PVN9	PVN10	PVN11
3F	-4.25	-4.1	-4	-3.5375	-3.1375	-2.65	-2.125	-1.9625	-1.2875	-1.025	-0.8
3E	-4.2375	-4.0875	-3.9875	-3.525	-3.125	-2.6375	-2.1125	-1.95	-1.275	-1.0125	-0.787
3D	-4.225	-4.375	-3.975	-3.5125	-3.1125	-2.625	-2.1	-1.9375	-1.2625	-1	-0.775
3C	-4.2125	-4.0625	-3.9625	-3.5	-3.1	-2.6125	-2.0875	-1.925	-1.25	-0.9875	-0.762
3B	-4.2	-4.35	-3.95	-3.4875	-3.0875	-2.6	-2.075	-1.9125	-1.2375	-0.975	-0.75
3A	-4.1875	-4.0375	-3.9375	-3.475	-3.075	-2.5875	-2.0625	-1.9	-1.225	-0.9625	-0.737
39	-4.175	-4.325	-3.925	-3.4625	-3.0625	-2.575	-2.05	-1.8875	-1.2125	-0.95	-0.725
38 37	-4.1625	-4.0125 -4.3	-3.9125 -3.9	-3.45 -3.4375	-3.05 -3.0375	-2.5625 -2.55	-2.0375 -2.025	-1.875 -1.8625	-1.2 -1.1875	-0.9375 -0.925	-0.712 -0.7
36	-4.15 -4.1375	-3.9875	-3.8875	-3.425	-3.0375	-2.5375	-2.025		-1.175	-0.925	-0.7
35	-4.1373	-4.275	-3.875	-3.425	-3.0125	-2.525	-2.0123	-1.8375	-1.1625	-0.9	-0.675
34	-4.1125	-3.9625	-3.8625	-3.4	-3.0123	-2.5125	-1.9875	-1.825	-1.15	-0.8875	-0.662
33	-4.1	-4.25	-3.85	-3.3875	-2.9875	-2.5	-1.975	-1.8125	-1.1375	-0.875	-0.65
32	-4.0875	-3.9375	-3.8375	-3.375	-2.975	-2.4875	-1.9625	-1.8	-1.125	-0.8625	-0.637
31	-4.075	-4.225	-3.825	-3.3625	-2.9625	-2.475	-1.95	-1.7875	-1.1125	-0.85	-0.625
30	-4.0625	-3.9125	-3.8125	-3.35	-2.95	-2.4625	-1.9375	-1.775	-1.1	-0.8375	-0.612
2F	-4.05	-4.2	-3.8	-3.3375	-2.9375	-2.45	-1.925	-1.7625	-1.0875	-0.825	-0.6
2E	-4.0375	-3.8875	-3.7875	-3.325	-2.925	-2.4375		-1.75	-1.075	-0.8125	-0.587
2D	-4.025	-4.175	-3.775	-3.3125	-2.9125	-2.425	-1.9	-1.7375	-1.0625	-0.8	-0.57
2C	-4.0125	-3.8625	-3.7625	-3.3	-2.9	-2.4125	-1.8875	-1.725	-1.05	-0.7875	-0.562
2B	-4	-4.15	-3.75	-3.2875	-2.8875	-2.4	-1.875	-1.7125	-1.0375	-0.775	-0.55
2A	-3.9875	-3.8375	-3.7375	-3.275	-2.875	-2.3875	-1.8625	-1.7	-1.025	-0.7625	-0.537
29	-3.975	-4.125	-3.725	-3.2625	-2.8625	-2.375	-1.85	-1.6875	-1.0125	-0.75	-0.525
28	-3.9625	-3.8125	-3.7125	-3.25	-2.85	-2.3625	-1.8375	-1.675	-1	-0.7375	-0.512
27	-3.95	-4.1	-3.7	-3.2375	-2.8375	-2.35	-1.825	-1.6625	-0.9875	-0.725	-0.5
26	-3.9375	-3.7875	-3.6875	-3.225	-2.825	-2.3375	-1.8125	-1.65	-0.975	-0.7125	-0.487
25	-3.925	-4.075	-3.675		-2.8125	-2.325	-1.8	-1.6375	-0.9625	-0.7	-0.47
24	-3.9125	-3.7625	-3.6625	-3.2	-2.8	-2.3125	-1.7875	-1.625	-0.95	-0.6875	-0.462
23 22	-3.9 -3.8875	-4.05 -3.7375	-3.65 -3.6375	-3.1875 -3.175	-2.7875 -2.775	-2.3 -2.2875	-1.775 -1.7625	-1.6125 -1.6	-0.9375 -0.925	-0.675 -0.6625	-0.45 -0.437
21	-3.875	-4.025	-3.625	-3.1625	-2.7625	-2.275	-1.75	-1.5875	-0.925	-0.65	-0.437
20	-3.8625	-3.7125	-3.6125	-3.1023	-2.75	-2.2625	-1.7375	-1.575	-0.9123	-0.6375	-0.42
1F	-3.85	-4	-3.6	-3.1375	-2.7375	-2.25	-1.725	-1.5625	-0.8875	-0.625	-0.4
1E		-3.6875	-3.5875	-3.125	-2.725	-2.2375	-1.7125	-1.55	-0.875	-0.6125	-0.387
1D	-3.825	-3.975	-3.575	-3.1125	-2.7125	-2.225	-1.7	-1.5375	-0.8625	-0.6	-0.375
1C	-3.8125	-3.6625	-3.5625	-3.1	-2.7	-2.2125	-1.6875	-1.525	-0.85	-0.5875	-0.362
1B	-3.8	-3.95	-3.55	-3.0875	-2.6875	-2.2	-1.675	-1.5125	-0.8375	-0.575	-0.35
1A	-3.7875	-3.6375	-3.5375	-3.075	-2.675	-2.1875	-1.6625	-1.5	-0.825	-0.5625	-0.337
19	-3.775	-3.925	-3.525	-3.0625	-2.6625	-2.175	-1.65	-1.4875	-0.8125	-0.55	-0.325
18	-3.7625	-3.6125	-3.5125	-3.05	-2.65	-2.1625	-1.6375	-1.475	-0.8	-0.5375	-0.312
17	-3.75	-3.9	-3.5	-3.0375	-2.6375	-2.15	-1.625	-1.4625	-0.7875	-0.525	-0.3
16	-3.7375	-3.5875	-3.4875	-3.025	-2.625	-2.1375	-1.6125	-1.45	-0.775	-0.5125	-0.287
15	-3.725	-3.875	-3.475	-3.0125	-2.6125	-2.125	-1.6	-1.4375	-0.7625	-0.5	-0.27
14				-3	-2.6	-2.1125		-1.425	-0.75	-0.4875	-0.262
13	-3.7	-3.85	-3.45		-2.5875	-2.1	-1.575	-1.4125	-0.7375	-0.475	-0.25
12	-3.6875	-3.5375	-3.4375	-2.975	-2.575	-2.0875	-1.5625	-1.4	-0.725	-0.4625	
11 10	-3.675 -3.6625	-3.825 -3.5125	-3.425 -3.4125	-2.9625 -2.95	-2.5625	-2.075 -2.0625	-1.55 1.5275	-1.3875 -1.375	-0.7125	-0.45	-0.225 -0.212
F	-3.65	-3.8	-3.4123	-2.9375	-2.55 -2.5375	-2.0625	-1.5375 -1.525	-1.3625	-0.7 -0.6875	-0.4375 -0.425	-0.212
E	-3.6375	-3.4875	-3.3875	-2.925	-2.525	-2.0375	-1.5125	-1.35	-0.675	-0.425	-0.187
	-3.625	-3.775	-3.375	-2.9125	-2.5125	-2.025	-1.5	-1.3375	-0.6625	-0.4123	-0.17
C	-3.6125	-3.4625	-3.3625	-2.9	-2.5	-2.0125	-1.4875	-1.325	-0.65	-0.3875	-0.162
B	-3.6	-3.75	-3.35	-2.8875	-2.4875	-2	-1.475	-1.3125	-0.6375	-0.375	-0.15
A	-3.5875	-3.4375	-3.3375	-2.875	-2.475	-1.9875		-1.3	-0.625	-0.3625	-0.137
9	-3.575	-3.725	-3.325	-2.8625	-2.4625	-1.975	-1.45	-1.2875	-0.6125	-0.35	-0.12
8	-3.5625	-3.4125	-3.3125	-2.85	-2.45	-1.9625		-1.275	-0.6	-0.3375	-0.112
7	-3.55	-3.7	-3.3	-2.8375	-2.4375	-1.95	-1.425	-1.2625	-0.5875	-0.325	-0.1
6	-3.5375	-3.3875	-3.2875	-2.825	-2.425	-1.9375	-1.4125	-1.25	-0.575	-0.3125	-0.087
5	-3.525	-3.675	-3.275	-2.8125	-2.4125	-1.925	-1.4	-1.2375	-0.5625	-0.3	-0.07
4	-3.5125	-3.3625	-3.2625	-2.8	-2.4	-1.9125		-1.225	-0.55	-0.2875	-0.062
3	-3.5	-3.65	-3.25	-2.7875	-2.3875	-1.9	-1.375	-1.2125	-0.5375	-0.275	-0.05
2	-3.4875	-3.3375	-3.2375	-2.775	-2.375	-1.8875		-1.2	-0.525	-0.2625	-0.037
11	-3.475	-3.625	-3.225	-2.7625	-2.3625	-1.875	-1.35	-1.1875	-0.5125	-0.25	-0.025
0	-3.4625	-3.3125	-3.2125	-2.75	-2.35	1 -1 8625	-1.3375	-1.175	-0.5	-0.2375	-0.012







VBP[1:0]: Positive GAMMAN bias current selection. VBN[1:0]: Negative GAMMAN bias current selection									
VBP/N[1]	VBP/N[0]	Gamma bias current							
0	0	80%							
0	1	100% (default)							
1	0	120%							
1	1	140%							

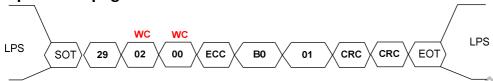




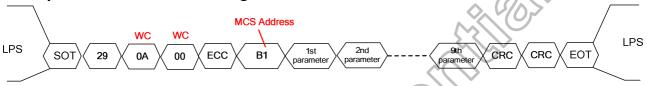
8.4.5 OTP Control register(page1 B1h)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set Gamma control register



Page	B1H				0	TP control regis	ster					
	Command	D7	D6	D5	D4	D3	D2	D1	D0	Hex		
	Command	1	0	1	1	0	0	0	1	B1		
	1st parameter		OTP_Group									
	2nd parameter		OTP_pwd									
	3rd parameter		OTP_PTM OTP_prog_sel OTP_re_Load OTP_RD OTP_WR									
1	4th parameter		NC NC									
	5th parameter		OTP ADDR									
	6th parameter				0	TP_PDOB				-		
	7th parameter					TP_PDIN				-		
	8th parameter	OTP_MANUAL										
	9th parameter	-	-	(-/	-	POR	PPROG	VPS	PWE	-		

Detial OTP program flow please refer section 10.3

OTP_GROUP[4:0]: OTP trimming group selection. The group range is from group1 to group27

OTP_PWD[7:0]: The OTP password enter auto program mode.
OTP_WR: OTP write control.
OTP_RD: OTP read control.

OTP_RE_LOAD: OTP auto re-load control.

OTP PTM[1:0]: OTP test mode.

OTP_ADDR[7:0]: OTP address set.

OTP_PDOB[7:0]: Read data from OTP.
OTP_PDIN[7:0]: Read data from OTP.
OTP_PDIN[7:0]: Write data to OTP.(for manual mode)
OTP_MANUAL[7:0]: OTP password enter manual program mode.
DISABLE_OTP[1:0]: OTP function disables. (for manual mode)

Description

DISABLE_OTP	Master OTP function	Slave OTP function
00b	Enable	Enable
01b	Enable	Disable
10b	Disable	Enable
11b	Disable	Disable

POR: OTP POR control signal. (for manual mode) PPROG: OTP PPROG control signal. (for manual mode)

VPS: OTP VPS control signal. (for manual mode)

PWE: OTP PWE control signal. (for manual mode)

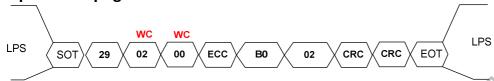
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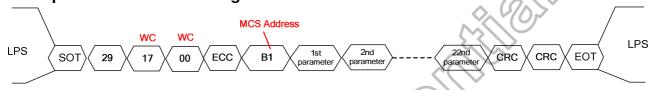
8.4.6 MUXL Control register(page2 B1h)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set MUXL control register



						10				
Page	B1H				MUXL Co	ntrol regis	ter			
	Command	D7	D6	D5	D4	D3	D2	D1	D0	Hex
	Command	1	0	1	1	0	0	0	1	B1
	1st parameter	GOUTL1_S	TBYB_MOD		(0)	GOUTL_	1_SEL	\mathcal{A}		-
	2nd parameter	GOUTL2_S	TBYB_MOD		57	GOUTL_2	2_SEL			-
	3rd parameter	GOUTL3_S	TBYB_MOD			GOUTL_	3_SEL			-
	4th parameter	GOUTL4_S	TBYB_MOD		(//)	GOUTL_4	4 SEL			-
	5th parameter	GOUTL5_S	TBYB_MOD			GOUTL !	5_SEL			-
	6th parameter	GOUTL6_S	TBYB_MOD			GOUTL (SEL			-
	7th parameter	GOUTL7_S	TBYB_MOD		/	GOUTL	7_SEL			-
	8th parameter	GOUTL8 S	TBYB MOD)	\sim	GOUTL 8	B SEL			-
	9th parameter	GOUTL9 S	TBYB MOD))	ζ,	GOUTL 9	9 SEL			-
2	10th parameter	GOUTL10 S	STBYB MOD			GOUTL 1	0 SEL			-
_	11th parameter				(())	GOUTL 1	1 SEL			-
	12th parameter	GOUTL12 S	TBYB MOD			GOUTL 1	2 SEL			-
	13th parameter	GOUTL13 S	TBYB_MOD			GOUTL_1	3_SEL			-
	14th parameter					GOUTL 1	4 SEL			-
	15th parameter				·	GOUTL 1	5 SEL			-
	16th parameter					GOUTL 1	6 SEL			-
	17th parameter					GOUTL 1	7 SEL			-
	18th parameter	GOUTL18 S	STBYB MOD			GOUTL 1	8 SEL			-
	19th parameter	GOUTL19 S	TBYB MOD			GOUTL 1	9 SEL			-
	20th parameter					GOUTL 2	0 SEL			-
	21st parameter	GOUTL21 S	STBYB MOD			GOUTL 2	1 SEL			-
	22nd parameter	GOUTL22 S	STBYB MOD			GOUTL_2				-
		GOUTL_1 S	SEL ~ GOUTL	_22_SEL	: Mux GOA	signal to C	GOUTL1	~ GOUTL22		
Ι.	Dogovintion		TBYB_MOD~							us
	Description	selection	_			=			•	
		00:VGL 01:V	GH 1X:GND							

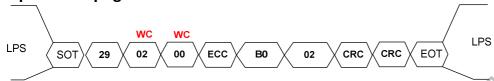
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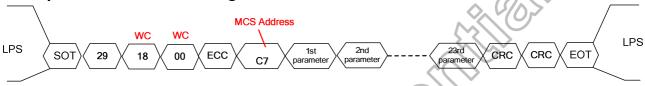
8.4.7 MUXR Control register(page2 C7h)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set MUXR control register



Page	C7H				MUXR	control registe	er				
g -		D7	De	3	D5	D4	D3	D2	D1	D0	Hex
	Command	1	1	,	0	0	0	1	1	1	C7
	1st parameter	•	STBYB	MOD			R 1 SEI		•		-
	2nd parameter		STBYB		53		R 2 SEI				_
	3rd parameter		STBYB				R 3 SEI				_
	4th parameter		STBYB			GOUT	R 4 SEI	\rightarrow			_
	5th parameter		STBYB				R 5 SEI				_
	6th parameter		STBYB				R 6 SEI				-
	7th parameter		STBYB		(())		R 7 SEI				-
	8th parameter	GOUTR	STBYB	MOD			R 8 SEI				-
	9th parameter		STBYB		7) 5		R 9 SEI				-
	10th parameter		0 STBYB				R 10 SE				-
2	11th parameter		1 STBYB		. (0		 ₹ 11 SE				-
	12th parameter		2 STBYB			GOUTF	12 SE	L			-
	13th parameter	GOUTR1	3_STBYB	MOD	\sim	GOUTF	13_SE	L			-
	14th parameter		4_STBYB		1		R_14_SE				-
	15th parameter	GOUTR1	5_STBYB	MOD		GOUTF	15_SE	L			-
	16th parameter		6_STBYB_				R_16_SE				-
	17th parameter		7 STBYB				R_17_SE				-
	18th parameter		8_STBYB_				R_18_SE				-
	19th parameter		9_STBYB_				R_19_SE				-
	20th parameter		0_STBYB_				R_20_SE				-
	21st parameter		1_STBYB				R_21_SE				-
	22nd parameter		2_STBYB				R_22_SE	L		r	-
	23rd parameter	VGL_GAS	GOA_VG	OFF_EN	GOA_PWROFF	GOA_HZ_EN					-
	~	GOUTR_1_	SEL ~ GO	UTR_22_	SEL: Mux GOA	signal to GOU	TR1~ GC	OUTR22			
		GOUTR1_S	IRAR WC	DD~ GOU	JTR22_STBYB_I			R22 stan	idby stai	us selec	tion.
		GOA HZ E	N. COALI	1 7 anahi		01:VGH 1X:GN	ID.				
		1: Enable G			е.						
		0: Disable.	OA sirigic	13 1 112.							
		o. Disable.									
		goa power	off: goa al	l on and	source pull to GN	ID when power	off phas	e.			
		1: Enable.	3			- 1	- 1				
	Description	0: Disable.									
	·										
			FF_EN:GC	A VGOF	F mode enable.						
		1: Enable.									
		0: Disable.									
		VOL CAS	204		ا مسلم ما						
		VGL_GAS:0 1:vgl tie to h									
		0:only VGL		S IS EADI	C						
		U.UIIIY VGL	υμιραι								



8.4.8 GOA Control register(page3 B1h)

GOA control register setting please refers Application Note.

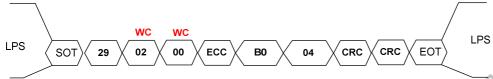




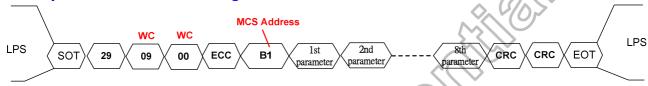
8.4.9 CABC Control register(page4 B1h)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set CABC control register



Page	B1H				C	ABC control re	gister				
	Command	D7	D6	D5	D4	D3	D2	_D1\	D0	Hex	
	Command	1	0	1	1		0	0	1	B1	
	1st parameter	-	-	DIM_EN	BL_EN	CABC_AGAIN	ام -	CABC_AGAIN	-	-	
	2nd parameter	-	-	-	-	DIM_STE	P	DIM_FM		-	
2	3rd parameter		DUTY_UD -								
۷	4th parameter		CABC_MB								
	5th parameter		PWM PRD								
	6th parameter				\bigcirc))	PWM_DIV		-	
	7th parameter			10		Reserve				-	
	8th parameter	eter MAX_DUTY									
		CABC_A	AGING_E	N: CABC	aging ena	ables.					
		1: Enable	е.								

- 0: Disable.

PWM POL: Poliarty of PWM control signal setting.

- PWM output is inversion.
 PWM output is non-inversion.

BL_EN: CABC back light control enables.

- 1: Enable.
- 0: Disable.

DIM_EN: CABC dimming enables.

- 1: Enable.
 - 0: Disable.

Description

DIM_FM[1:0]: CABC dimimng cycle settling

DIM_FM[1]	DIM_FM[0]	CABC dimimng cycle
0	0	1 frame per step
0	1	2 frame per step (default)
1	0	3 frame per step
1	1	4 frame per step

DIM STEPI1:01:CABC dimming step setting

DIM_FM[1]	DIM_FM[0]	CABC dimimng cycle
0	0	2 steps
0	1	4 steps
1	0	8 steps (default)
1	1	16 steps

2402 CH TFT LCD Source Driver with MIPI/LVDS TCON



DATASHEET V01

Internal VS						
	Current duty	i ———				Target duty
Gray means	Gray means =128	Gray means =136	Gray means =144	Gray means =152	Gray means =160	Gray means =168
DMIO	Duty = 50%	Duty = 53.13%	Duty = 56.25%	Duty = 59.38%	Duty = 62.50%	Duty = 65.63%

Note: (1) DIM_FRME[1:0]=01, DIM_STEP[1:0]=10, Max duty is 100%, Min duty is 0%.

DUTY_UD[7:0]: Set user-defined PWM duty on CABC bypass mode.

The CABC bypass mode is setting at 0xB6[3:2] of page0.

CABC_MB[7:0]: Set PWM minimum duty.

PWM_PRD[7:0]: CABC PWM period setting.

PWM DIV[2:0]: CABC PWM period divider

<u></u>	m_bri[E.o]. C/LBC i vim period divider										
PWM_DIV[2]	PWM_DIV[1]	PWM_DIV[0]	CABC PWM period divider								
0	0	0	DIV 1								
0	0	1	DIV 2								
0	1	0	DIV 4 (default)								
0	1		DIV 8								
1	0	0	DIV 16								
1	0		DIV 32								
1	1 (5)	0	DIV 64								
1	1	1	DIV 128								

MAX_DUTY[7:0]: Set PWM maximum duty.8'hff=100%,8'h00=0%.



8.4.10 MIPI Control register(page6 B1h)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set MIPI control register



Page	B1H			MIPI c	ontrol regist	er						
	Command	D7	D6	D5	D4	D3	D2 D1	D0	Hex			
	Command	1	0	1	(A)	0	0 0	1	B1			
	1st parameter	EoTp_EN	CRCEN	CRCErr_FilterOut	VC4FRAME	VC	CS VC	_m	-			
	2nd parameter		Reserved -									
5	3rd parameter		Reserved -									
	4th parameter		Reserved									
	6th parameter	-	RT3 RT2						-			
	7th parameter	-		RT1		RT0		-				
	8th parameter	TurnDisable	-		(- ()	-	RTC		-			
		VC_m[1:0]:	virtual cha	nnel ID setting of m	aster (for LP	tx).						
		VC_S[1:0]: \	irtual char	nnel ID setting of sla	ve (for LP/H	S rx).						
		VC4FRAME	: RX virtua	I channel filtering m	ode.	-						
		1: Enable.			\							
	0: Disable.											
			1	\wedge (())								
		CBCErr Filt	erOut: Fill	ter-out by CBC ched	ck result enab	او						

1: Enable.

0: Disable.

CRCEN: CRC check enable.

1: Enable.

0: Disable

EoTp_EN: Process of EoT packet enable.

1: Enable.

0: Disable.

RT0[2:0]: Lane0 termination resistance control. RT1[2:0]: Lane1 termination resistance control. RT2[2:0]: Lane2 termination resistance control. RT3[2:0]: Lane3 termination resistance control.

RTC[2:0]: Clock lane termination resistance control

RTx[2:0]	Ohm Ω
111	81
110	90
101	102 (default)
100	118
011	128
010	153
001	192
000	255

TurnDisable: BTA→TX procedure function enable.

1: Enable.

0: Disable.

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Description

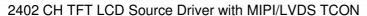
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8.5 Register Table (For LVDS input SPI mode)

8.5.1 Register of Page0

MIPI address	SPI address	Default	Bit name				Data	[7:0]			Description	Group
0xB0	0x30	0Fh	PAGE									Page setting.	
0xB1	0x31	80h	VCOMS	1	0	0	0	0	0	0	0	VCOM voltage select.	0
			STB		1							Standby mode select.	
			UPDNB			0						Veritical direction selection.	
			LR				0					Horizontal direction selection.	
0xB2	0x32	4bh	ZIGZAG_SEL					1				Panel type of selection.	
			DISP_ON						0			Disply on/off command.	
			NBW_SEL							1		Normal black/white panel selection.	
			BIST								1	TCON bist mode.	
			ZTYPE_SEL	0	0							Type of zigzag selection.	
0xB3	0x33	28h	PWRMD			1	0					Power mode selection.	
UXD3	0x33	2011	VRES_FIX					1				Vertical Line changeable selection.	
			RES							0	0	Vertical Line selection.	
0xB4	0x34	C0h	VRES	1	1	0	0	0	0	0	0	Vertical Resolution select.	1
0xB5	0x35	00h	ZDATA			0	0	0	0	0	0	ZigZag dummy data select.	
			LNSW	0	0							MIPI data lane swap.	Ī
			PNSW			0				4		MIPI lane P/N swap.	1
		0.01	HFRC INV				0				7,	HI-FRC function inversion.	Ī
0xB6	0x36	03h	CABC CTRL				_	0	0			CABC-Mode selection.	1
			DITHER_EN					-		1		Dithering enable.	1
			HFRC EN					(5		$\overline{}$	Hi-FRC enable.	1
			PCLK_SEL	0				>			<u> </u>	PCLK source seclect.	1
			RX DINT	Ť	1							LVDS 6bit/8bit input select.	1
0xB7	0x37	53h	RX_VB		Ė	0	1					LVDS bias currect selection.	1
O/LD/	OAO1	0011	LVDS_VB			Ů			0	1		LVDS DLL bias currect selection.	1
			LVDS FMT						_	Ė	1	LVDS JEIDA / VESA format select.	1
			LVDS_TD		0	0	0				1	LVDS datalanes skew tuning.	1
0xB8	0x38	00h	LVDS TC		0	-	0		0	0	0		1
			LVDS BW			0	1				-	LVDS DLL bandwidth select.	1
0xB9	0x39	12h	LVDS_CPB	-	-	U	-		0	1	0	LVDS DLL pump current select .	
			BLREV	7	0				0	10	U	Source output defines at Vblanking.	1
			BLREVONOFF	_	-	1/		/(_		Source output defines at Volariking. Source output defines at Power on/off.	1
0xBA	0x3A	a9h	SD ISSEL			-1<	0	4	7			Source Bias current.	1
			INV SEL				U	-	0	0	1	Inversion type select.	1
			BC CTRL	0		7		\rightarrow	U	U	-	BC CTRL output contrl.	1
			GOA EN	U	1	1						GOA enable.	1
0xBB	0x3B	68h	RB SWAP		ı	1	\Diamond				-	GOA enable.	-
UXDD	UX3D	0011	DPFM OSC SEL			-	_	1				R/B color swap.	1
		.6		\leftarrow	71		0	1	_	_		DPFM clcok selection.	1
		A ('(')	LNSEL		//				0	0		MIPI lane nunmber select.	1
0.00	0.00	\ \E_0\\\	GAS_GOA_EN	1								CKV/STV status select when GAS enable.	_
0xBC	0x3C	E0h	VRES_BLACK)	1							Send black pattern when change VRES.	_
			GCHL_Blanking			1						GCH/GCL output define at power on.	
0xBD	0x3D	aah	VSPS	1	0	1	0	<u> </u>	L.			VDDP voltage select.	_
_			VSNS					1	0	1	0	VDDN voltage select.	
0xBE	0x3E	23h	VGHS			1	0	0	0	1	1	VGH voltage select.	
0xBF	0x3F	14h	VGLS	ļ		0	1	0	1	0	0	VGL voltage select.	
0xC1	0x41	66h	VSPON	0	1	1	0					VSP PFM TON setting.	
50	57.11	5511	VSPOFF					0	1	1	0	VSP PFM TOFF setting.	





MIPI address	SPI address	Default	Bit name				Data	[7:C)]			Description	Group
0xC2	0x42	66h	VSNON	0	1	1	0					VSN PFM TON setting.	
UXC2	UX42	9911	VSNOFF					0	1	1	0	VSN PFM TOFFsetting.	
			VGLXSP		1							VGH boost function.	
000	040	701-	VGHXSP			1	1					VGH boost function.	
0xC3	0x43	70h	PFMFREN					0				PFM frequency randomizer enable.	
			T OFFSET					Ť	0			PFM Ton Toff offset.	
0xC4	0x44	04h	VPHS				0	0	1	0	0	Positive gamma_H select.	
UNU I	UM. I	•	CGPP INV	1			Ť	Ť		Ť	Ť	CGPP output invert enable.	
			SOFT EN			1						Charge Pump soft start enable.	
0xC5	0x45	adh	CLK SEL				0	1	1			Charge Pump clock select.	1
			CMD_SEL				Ť	·	<u> </u>	0	1	Charge Pump command select.	
0xC6	0x46	04h	VNHS				0	0	1	0	0	Negative gamma H select.	
OXOO	OXIO	0 111	VCL CPCTL			0	1	Ŭ	i i	<u> </u>	Ť	VCL charge pump frequency select.	
0xC7	0x47		VGL CPCTL				† ·	0	1			VGL charge pump frequency select.	
OXO1	OX 17		VGH_CPCTL					_	† ·	0	1	VGH charge pump frequency select.	-
			POCSD CTL	0	0					-		SD offset cancel method select.	_
0xC8	0x48	06h	EQ0W	Ů	Ů	0	0	0	1	1	0	EQ0 precharge pluse width select.	_
0xC9	0x49	00h	EQ1W				0	0	0	0	0	EQ1 precharge pluse width select.	
0xCA	0x4A	18h	EQ2W				1	1	0	0	0	EQ2 precharge pluse width select.	-
0xCB	0x4B	3fh	PVP1			1	1	1	1	1	1	2nd Positive gamma op's input voltage.	+
0xCC	0x4C	34h	PVP2			1	1	0	1	0	0	3nd Positive gamma op's input voltage.	
0xCD	0x4C 0x4D	2dh	PVP3			1	0	1	1	0	1	4dr Positive gamma op's input voltage.	_
0xCE	0x4E	2dh	PVP4			1	0		1	0	1		_
0XCE	0X4E	21h	PVP5			1	0	0	0	0	1	5th Positive gamma op's input voltage. 6th Positive gamma op's input voltage.	_
0XD0	0X4F 0X50	1bh	PVP6			0	1	1	0	1	7		2
0XD0	0X50 0X51	1eh	PVP7			0	1	1	1	2.0	ý	7th Positive gamma op's input voltage.	-
0XD1	0X51 0X52	25h	PVP7			1	0	0	4	0	0	8th Positive gamma op's input voltage.	
			PVP9								P	9th Positive gamma op's input voltage.	
0XD3	0X53	20h				1	0	0	0	0	0	10th Positive gamma op's input voltage.	_
0XD4	0X54	20h	PVP10			1	0	0	0	0	0	11th Positive gamma op's input voltage.	
0XD5	0X55	16h	PVP11			0	1	0	71	1	0	12th Positive gamma op's input voltage.	
0XD6	0X56	3fh	PVN1			_[1	1	1	1	1	2nd Negative gamma op's input voltage.	
0XD7	0X57	33h	PVN2		\sim	1	7	0	0	1	1	3nd Negative gamma op's input voltage.	
0XD8	0X58	2ch	PVN3	\mathcal{L}		1	0	1	1	0	0	4dr Negative gamma op's input voltage.	
0XD9	0X59	2eh	PVN4	//		<i>) 1)</i>	0	1	1	1	0	5th Negative gamma op's input voltage.	
0XDA	0X5A	21h	PVN5			1	0	0	0	0	7	6th Negative gamma op's input voltage.	
0XDB	0X5B	1bh	PVN6			0	1	1	0	1 1	1	7th Negative gamma op's input voltage.	
0XDC	0X5C	1dh	PVN7			0	1	1	1	0	1	8th Negative gamma op's input voltage.	3
0xDD	0x5D	24h	PVN8			_	0	0	1	0	0	9th Negative gamma op's input voltage.	
0XDE	0X5E	21h	PVN9			1	0	0	0	0	1	10th Negative gamma op's input voltage.	
0XDF	0X5F	1fh	PVN10			0	1	1	1	1	1	11th Negative gamma op's input voltage.	
0xE0	0x60	16h	PVN11			0	1	0	1	1	0	12th Negative gamma op's input voltage.	
0xE1	0x61	B5h	VBP					0	1			GAMMAP bias current select.	
OXL I	0.001	DOIL	VBN							0	1	GAMMAN bias current select.	
0xFA	0x7A	70h	VENDER_ID	0	H	1	1	0	0	0	0	Driver ID and module ID.	Х
0XFB	0X7B	01h	GRB	1							1	Global reset.	Х
0XFC	0X7C	82h	PRODUCT ID1	77	0	0	0	0	0	1	0	PRODUCT ID 1.	Х
0XFD	0X7D	60h	PRODUCT ID2	0	1	1	0	0	0	0	0	PRODUCT ID 2.	Х
0XFE	0X7E	0Ah	PRODUCT ID3				Ť	1	0	1	0	PRODUCT ID 3.	X
0xFF	0x7F	03h	VERSIONID	0	0	0	0	0	0	1	1	IC version ID.	X



8.5.2 Register of Page(OTP)

MIPI Address	SPI Address	Default	Bit name	Data[7:0]								Description
0xB1	0x31	00h	OTP_Group				0	0	0	0	0	OTP trimming group select.
0xB2	0x32	5Ah	OTP_pwd	0	1	0	1	1	0	1	0	OTP program password.
			OTP_PTM		0	0	0					Urer /margin read select.
			OTP_prog_sel					0				OTP program select.
0xB3	0x33	00h	OTP_re_Load						0			OTP auto load.
			OTP_RD							0		OTP read command.
			OTP_WR								0	OTP write command.
0xB5	0x35	00h	OTP_ADDR	0	0	0	0	0	0	0	0	OTP address.
0xB6	0x36	00h	OTP_PDOB	0	0	0	0	0	0	0	0	OTP read out data.
0xB7	0x37	00h	OTP_PDIN	0	0	0	0	0	0	0	0	OTP program data.
0xB8	0x38	5Ah	OTP_MANUAL	0	1	0	1	1	0	1	0	OTP manual program.
			POR					0				OTP POR control.
0xB9	0.430	00h	PPROG						0			OTP PPROG control.
UXD9	0x39 00h		VPS							0		OTP VPS control.
		PWE								0	OTP PWE control.	





8.5.3 Registers of Page2 (GOA MUX)

MIPI address	SPI address	Default	Bit name				Da	ata				Description	Group
0xB1	0x31	08h	GOUTL1_STBYB_MOD	0	0							GOUTL_1 standby staus select.	
UNDI	0,01	0011	GOUTL_1_SEL			0	0	1	0	0	0	Mux GOA signal to GINL1.	
0xB2	0x32	08h	GOUTL2_STBYB_MOD	0	0							GOUTL_2 standby staus select.	
UXDZ	0x32	UOII	GOUTL_2_SEL			0	0	1	0	0	0	Mux GOA signal to GINL2.	
0xB3	0x33	06h	GOUTL3_STBYB_MOD	0	0							GOUTL_3 standby staus select.	
UXDO	UXSS	0011	GOUTL_3_SEL			0	0	0	1	1	0	Mux GOA signal to GINL3.	
0xB4	0x34	06h	GOUTL4_STBYB_MOD	0	0							GOUTL_4 standby staus select.	
UXD4	0x34	UOII	GOUTL_4_SEL			0	0	0	1	1	0	Mux GOA signal to GINL4.	
0xB5	0x35	0Ch	GOUTL5_STBYB_MOD	0	0							GOUTL_5 standby staus select.	
UXDS	UXSS	UCII	GOUTL_5_SEL			0	0	1	1	0	0	Mux GOA signal to GINL5.	
0xB6	0x36	0Ch	GOUTL6_STBYB_MOD	0	0							GOUTL_6 standby staus select.	
UXDO	UXSO	UCII	GOUTL_6_SEL			0	0	1	1	0	0	Mux GOA signal to GINL6.	
0xB7	0x37	0Ah	GOUTL7_STBYB_MOD	0	0							GOUTL_7 standby staus select.	
UXD/	0x37	UAII	GOUTL 7 SEL			0	0	1	0	1	0	Mux GOA signal to GINL7.	
OvD0	0,20	016	GOUTL8_STBYB_MOD	0	0							GOUTL 8 standby staus select.	
0xB8	0x38	0Ah	GOUTL 8 SEL			0	0	1	0	1	0	Mux GOA signal to GINL8.	
0xB9	0x39	02h	GOUTL9 STBYB MOD	0	0							GOUTL 9 standby staus select.	
Охра	0x39	0211	GOUTL 9 SEL			0	0	0	0	1	0	Mux GOA signal to GINL9.	
0	004	004	GOUTL10 STBYB MOD	0	0						0	GOUTL_10 standby staus select.	
0xBA	0x3A	00h	GOUTL_10_SEL			0	0	0	0	0	0	Mux GOA signal to GINL10.	
0xBB	000	004	GOUTL11_STBYB_MOD	0	0							GOUTL_11 standby staus select.	
UXBB	0x3B	00h	GOUTL_11_SEL			0	0	0	0	0	0	Mux GOA signal to GINL11.	4
000	000	001-	GOUTL12_STBYB_MOD	0	0						/	GOUTL 12 standby staus select.	4
0xBC	0x3C	00h	GOUTL 12 SEL			0	0	0	0	0	0	Mux GOA signal to GINL12.	
000	000	0.01-	GOUTL13_STBYB_MOD	0	0							GOUTL_13 standby staus select.	
0xBD	0x3D	00h	GOUTL_13_SEL			0	0	0	0	0	0	Mux GOA signal to GINL13.	
0DE	00	0.01-	GOUTL14 STBYB MOD	0	0			17			7	GOUTL_14 standby staus select.	
0xBE	0x3E	00h	GOUTL 14 SEL			0	0	0	0	0	0	Mux GOA signal to GINL14.	
0.05	0.05	0.01	GOUTL15_STBYB_MOD	0	0							GOUTL_15 standby staus select.	
0xBF	0x3F	00h	GOUTL 15 SEL			0	0	0	0	0	0	Mux GOA signal to GINL15.	
	2.42	2.41	GOUTL16 STBYB MOD	0	0							GOUTL 16 standby staus select.	
0xC0	0x40	04h	GOUTL_16_SEL		7	0	0	0	\$ 1	0	0	Mux GOA signal to GINL16.	
		0.01	GOUTL17_STBYB_MOD	0	0			~				GOUTL_17 standby staus select.	
0xC1	0x41	00h	GOUTL 17 SEL)		0	0	0	0	0	0	Mux GOA signal to GINL17.	
	2.42	2.01	GOUTL18_STBYB_MOD	0	0		((() <u> </u>	_		GOUTL_18 standby staus select.	
0xC2	0x42	00h	GOUTL_18_SEL		_	0	0	0	0	0	0	Mux GOA signal to GINL18.	
			GOUTL19 STBYB MOD	0	0		1	_	Ť			GOUTL_19 standby staus select.	
0xC3	0x43	00h	GOUTL_19_SEL	_		0	0	0	0	0	0	Mux GOA signal to GINL19.	
			GOUTL20 STBYB MOD	0	0			Ŭ	Ť			GOUTL_20 standby staus select.	
0xC4	0x44	00h	GOUTL 20 SEL		Ů	0	0	0	0	0	0	Mux GOA signal to GINL20.	
			GOUTL21_STBYB_MOD	0	0		-	<u> </u>	<u> </u>		_	GOUTL_21 standby staus select.	\dashv
0xC5	0x45	00h	GOUTL 21 SEL	-) /	0	0	0	0	0	0	Mux GOA signal to GINL21.	=
		$-\phi_{\wedge}$	GOUTL22_STBYB_MOD	0	0	U	U			0	-	GOUTL_22 standby staus select.	=
0xC6	0x46	00h	GOUTL_22_SEL	0		0	0	0	0	0	0	Mux GOA signal to GINL22.	=
	l		GOOTL_ZZ_OEL		İ	U	U	U	U	U	U	Max GOA Signal to GITTLE.	

2402 CH TFT LCD Source Driver with MIPI/LVDS TCON



MIPI address	SPI address	Default	Bit name					D	ata			Description	Group
0xC7	0x47	07h	GOUTR1 STBYB MOD	0	0							GOUTR 1 standby staus select.	
UXC1	0.47	0711	GOUTR_1_SEL			0	0	0	1	1	1	Mux GOA signal to GINR_1.	
0xC8	0x48	07h	GOUTR2_STBYB_MOD	0	0							GOUTR_2 standby staus select.	
UXCO	UX40	0711	GOUTR_2_SEL			0	0	0	1	1	1	Mux GOA signal to GINR_2.	
0xC9	0x49	05h	GOUTR3_STBYB_MOD	0	0							GOUTR_3 standby staus select.	
0.03	0,43	0311	GOUTR_3_SEL			0	0	0	1	0	1	Mux GOA signal to GINR_3.	
0xCA	0x4A	05h	GOUTR4_STBYB_MOD	0	0							GOUTR_4 standby staus select.	
UXUA	0,47	0311	GOUTR_4_SEL			0	0	0	1	0	1	Mux GOA signal to GINR_4.	
0xCB	0x4B	0Bh	GOUTR5_STBYB_MOD	0	0							GOUTR_5 standby staus select.	
UXOD	0,40	ODII	GOUTR_5_SEL			0	0	1	0	1	1	Mux GOA signal to GINR_5.	
0xCC	0x4C	0Bh	GOUTR6_STBYB_MOD	0	0							GOUTR_6 standby staus select.	
0,00	0,40	ODII	GOUTR_6_SEL			0	0	1	0	1	1	Mux GOA signal to GINR_6.	
0xCD	0x4D	09h	GOUTR7_STBYB_MOD	0	0							GOUTR_7 standby staus select.	
UNOD	UNTD	0311	GOUTR_7_SEL			0	0	1	0	0	1	Mux GOA signal to GINR_7.	
0xCE	0x4E	09h	GOUTR8_STBYB_MOD	0	0							GOUTR 8 standby staus select.	
UXUL	UA4L	0311	GOUTR_8_SEL			0	0	1	0	0	1	Mux GOA signal to GINR_8.	
0xCF	0x4F	01h	GOUTR9_STBYB_MOD	0	0							GOUTR_9 standby staus select.	
UXCI	0,41	0111	GOUTR_9_SEL			0	0	0	0	0	1	Mux GOA signal to GINR_9.	
0xD0	0x40	00h	GOUTR10_STBYB_MOD	0	0							GOUTR_10 standby staus select.	
UXDU	0.40	0011	GOUTR_10_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_10.	
0xD1	0x41	00h	GOUTR11_STBYB_MOD	0	0							GOUTR_11 standby staus select.	
UXDT	UX4 I	UUII	GOUTR_11_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_11.	
0xD2	0x42		GOUTR12_STBYB_MOD	0	0							GOUTR_12 standby staus select.	
UXDZ	UX42	00h	GOUTR_12_SEL			0	0	0	0	0		Mux GOA signal to GINR 12.	4
OvD2	0.40		GOUTR13 STBYB MOD	0	0				5			GOUTR 13 standby staus select.	7 4
0xD3	0x43	00h	GOUTR_13_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_13.	
0D.4	044		GOUTR14_STBYB_MOD	0	0							GOUTR 14 standby staus select.	
0xD4	0x44	00h	GOUTR_14_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_14.	
0xD5	0x45		GOUTR15_STBYB_MOD	0	0					,		GOUTR_15 standby staus select.	
UXD5	UX45	00h	GOUTR_15_SEL			0	0	0	0	0	(0	Mux GOA signal to GINR_15.	
000	040		GOUTR16_STBYB_MOD	0	0							GOUTR_16 standby staus select.	
0xD6	0x46	03h	GOUTR_16_SEL			0	0	0	0.	1		Mux GOA signal to GINR 16.	
007	047		GOUTR17 STBYB MOD	0	0					5		GOUTR 17 standby staus select.	
0xD7	0x47	00h	GOUTR 17 SEL)	0	0	0	0	0	0	Mux GOA signal to GINR_17.	
000	010	0.01-	GOUTR18_STBYB_MOD	0	0						\mathcal{F}	GOUTR_18 standby staus select.	
0xD8	0x48	00h	GOUTR_18_SEL			0	0	0 (0	0	0	Mux GOA signal to GINR_18.	
0.00	0 40	201	GOUTR19_STBYB_MOD	0	0							GOUTR 19 standby staus select.	
0xD9	0x49	00h	GOUTR 19 SEL			0	0	0	0	0	0	Mux GOA signal to GINR 19.	
		201	GOUTR20 STBYB MOD	0	0	7					_	GOUTR_20 standby staus select.	1
0xDA	0x4A	00h	GOUTR 20 SEL			0	0	0	0	0	0	Mux GOA signal to GINR 20.	
			GOUTR21 STBYB MOD	0_	0		\rightarrow				_	GOUTR 21 standby staus select.	
0xDB	0x4B	00h	GOUTR 21 SEL		Ť	0	0	0	0	0	0	Mux GOA signal to GINR 21.	
			GOUTR22 STBYB MOD	0	0	Ŭ				Ť		GOUTR 22 standby staus select.	1
0xDC	0x4C	00h	GOUTR_22_SEL	-		0	0	0	0	0	0	Mux GOA signal to GINR_22.	1
		7,4	VGL GAS	0		Ť		Ŭ	Ŭ	Ŭ	Ĭ	GOAOUT status when GAS enable.	1
			GOA VGOFF EN	۲	1							GOA VGOFF mode enable.	-
0xDD	0x4D	40h	GOA_PWROFF		-	0						GOAOUT status when power off.	-
			GOA_FWHOIT			0	0					GOA HI Z enable.	1
L			GOA_HZ_LN	<u> </u>		l	U				l	GOATH & CHADIC.	



8.5.4 Registers of Page3 (GOA)

GOA register setting please refers Application Note.

8.5.5 Registers of Page4 (CABC)

MIPI address	SPI address	Default	Bit name				Da	ata				Description	Group	
			DIM_EN			1						Dimming function enable.		
0xB1	0x31	3Bh	BL_EN				1					Blacklight enable.		
UXDT	0,01	JDII	PWM_POL					1				PWM output polarity select.		
				CABC_AGAIN							1		CABC block aging enable.	
0xB2	0x32	09h	DIM_STEP					1	0			Dimming step setting.		
UXDZ	0,32	0911	DIM_FRME							0	1	Dimming cycle setting.	5	
0xB3	0x33	FFh	DUTY_UD	1	1	1	1	1	1	1	1	Bypass mode duty setting.		
0xB4	0x34	10h	CABC_MB	0	0	0	1	0	0	0	0	Minimun duty constraint.		
0xB5	0x35	00h	PWM_PRD	0	0	0	0	0	0	0	0	PWM period setting.		
0xB6	0x36	02h	PWM_DIV						0	1	0	PWM period divider setting.		
0xB8	0x38	FFh	MAX_DUTY	1	1	1	1	1	1	1	1	CABC max duty.		

8.5.6 Registers of Page6 (MIPI)

MIPI address	SPI address	Default	Bit name				Da	ata				Description	Group
			EoTp_EN	1					~~			Process of EoT packet enable.	
			CRCEN		1))				CRC check enable.	
			CRCErr_FilterOut			1	1					Filter-out by CRC check result enable.	
0xB1	0x31	E0h	VC4FRAME				0					RX virtual channel filtering mode.	6
OXBT	0.01	Lon	VC_S					0	0			virtual channel ID setting of slave (for LP/HS rx).	
			VC_m		7		2		^	0	0	virtual channel ID setting of master (for LP tx).	
0xB5	0x35	55h	RT3		1)	0	1		5			Lane3 termination resistance control.	
UXDO	UXSS	5511	RT2						1	0		Lane2 termination resistance control.	
0xB6	0x36	55h	RT1		1	0	1			,		Lane1 termination resistance control.	8
UXDO	UXSO	5511	RT0			~	/		7	0	1	Lane0 termination resistance control.	0
0vB7	0xB7 0x37	05h	TurnDisable	▶ 0								BTA->TX procedure function enable.	
0,07	0,37	0311	RTC		<	4			1	0	1	Clock lane termination resistance control.	



9. Register Description (for LVDS input SPI mode)

9.1 Registers of Page0

Address is 0xB1

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP	
Name		VCOMS								
Description		VCOM voltage select (step=10mV) (OTP 3 times)								
Default	1	1 0 0 0 0 0 0 0								

VCOMS[7:0]	VCOM Voltage
00000000	-0.2V
0000001	-0.21V
0000010	-0.22V
:	
10000000	-1.48V (default)
:	
11111111	-2.75V

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NA	STB	UPDNB	LR	ZIGZAG_SEL	DISP_ON	NBW_SEL	BIST	V
Default	0	1	0	0	1) / 0	1	1	V

Bit	Item	Description
6	STB	TCON sleep mode selection. MIPI DCS 0x10 (Enter sleep mode), and 0x11 (exit sleep mode). MIPI DCS command do XOR with SPI register.
5	UPDNB	Vertical direction selection. MIPI DCS 0x36 set_address_mode[7] command and SPI register do XOR operation.
4	LR	Horizontal direction selection. MIPI DCS 0x36 set_address_mode[6] command and SPI register do XOR operation.
3	ZIGZAG_SEL	Panel driving method selection.0:Strip panel ,1:Zigzag type panel
2	DISP_ON	MIPI DCS: 0x28 display on, 0x29 display off 0: Follow MIPI_DCS command. 1: Reverse MIPI_DCS command. (to MIPI_DCS command do "XOR" operation)
1	NBW_SEL	Normal Black and Normal white panel selection. 0:Normally white ,1:Normally black
0	BIST	TCON bist mode selection. 0:BIST mode ,1:Normal mode



Address is 0xB3

Bit #	B7	B6	B5	B4	В3	B2	B1	В0	OTP
Name	ZTYPE_SEL[1]	ZTYPE_SEL[0]	PWRMD[1]	PWRMD[0]	VRES_FIX	NC	RES[1]	RES[0]	V
Default	0	0	1	0	1	0	0	0	V

Bit	Item		Description						
7	ZTYPE_SEL[1]	Zigzag type slec	Zigzag type slection (panel type please refer section 6.3).						
6	ZTYPE_SEL[0]	0: Zigzag type 0	, 1: Zigzag typ	e 1 2:Zigzag type 2 3:Zigzag type3					
5	PWRMD[1]	POWR ON mode	e (to pin PWRM	ID do XOR operation).					
		PWRMD[1]	· · · · · · · · ·						
		0	0 0 Support HX5186-C power mode						
4	PWRMD[0]	0	1	Suppot PFM circuit power mode					
		1	0	External VSP, VSN, VGH, VGL power mode(default).					
		1	1	External VSP,VSN power mode					
3	VRES_FIX	Display vertical L	Display vertical Line decide by(1):RES[2:0] or (0) VRES (Register 0xB4)						
1	RES[1]	Resolution selection (to pin HW RES do XOR operation).							
0	RES[0]	Resolution settin	g please refer s	ection 6.1					

Address is 0xB4

Bit #	B7	В6	B5	B4	В3	B2	B1	В0	OTP
Name		VRES							
Description		Vertical Resolution selection, VRES[7:0], range=80~ 253, step= 8H							V
Default	1	1	0	0	0	0	0	0	

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC			ZDA	ATA			
Description			Zigz	Zag dummy	data selection	on			V
Default	0	0	0	0	0	0	0	0	



Address is 0xB6

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	LNSW[1]	LNSW[0]	PNSW	HFRC_INV	CABC_CTRL[1]	CABC_CTRL[0]	DITHER_EN	HFRC_EN	V
Default	0	0	0	0	0	0	1	1	v

Bit	Item		Description										
7	LNSW[1]	MIPI lane swa	MIPI lane swap (to pin LNSW do XOR operation).										
				D2P		D1P		CLKP	CLKN	D0P	D0N	D3P	D3N
		LNSW[1]	LNSW[1] LNSW[0]				MIPI	lanes m	napping	table			
6	LNCWIOI	0	0	D3P	D3N	D2P	D2N	CLKP	CLKN	D1P	D1N	D0P	D0N
6	LNSW[0]	0	1	D3P	D3N	D0P	D0N	CLKP	CLKN	D1P	D1N	D2P	D2N
		1	0	D0P	D0N	D1P	D1N	CLKP	CLKN	D2P	D2N	D3P	D3N
		1	1	D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N
5	PNSW	MIPI/LVDS	pin change p	olarity	(to pin	PNS	N do X	OR ope	ration) 1	:P/N s	wap.		
4	HFRC INV	HI-FRC funct										Defaul	t=0)
3	CABC_CTRL[1]	CABC-Mode	selection:					40	11		•		•
		CABC_CT		BC_CT	RL[0]				CABC	Mode			
		0		0				Вура	ass mod	e (def a	ault)		
2	CABC_CTRL[0]	0	0 1 Still-mode										
		1	1 0 UI-mode										
		1	1 1 Movingl-mode										
-	DITHER EN	Dithoring one	Dithering enable.1: dithering enable, 0: dithering disable.										
<u> </u>	_	Hi-FRC enable.1: differing enable, 0: differing disable.											
0	HFRC_EN	HI-FKC enab	ie.1:HFRC ei	nable 0	:HFRC	aisab	ıe.						

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	PCLK_SEL	RX_DINT	RX_VB[1]	RX_VB[0]	NC	LVDS_VB[1]	LVDS_VB[0]	LVDS_FMT	V
Default	0	1	0	1	0	0	1	1	V

Bit	Item	Description									
7	PCLK_SEL	TCON PCLK source 0:frome internal OSC25M 1:from EXT_CLK.									
6	RX_DINT	LVDS 8 bit mode 1:8bit mode 0	LVDS 8 bit mode 1:8bit mode 0:6 bit mode.								
5	RX_VB[1]	LVDS bias current selection.									
		LVDS_RX[1]	LVDS_RX[0]	LVDS bias current							
		0	0	75%							
4	RX_VB[0]	0	1	100%							
		1/	0	125%							
	\vee/\vee	\sim	1	150%							
2	LVDS_VB[1]	LVDS DLL bias current selection	on.								
		LVDS_VB[1]	LVDS_VB[0]	LVDS DLL bias current							
		0	0	82%							
1	LVDS_VB[0]	0	0 1 100%								
		1 0 137%									
		1 1 160%									
0	LVDS_FMT	LVDS data format select 0:NS	_VDS data format select 0:NS or JEIDA forma 1:Thine or VESA format								



Address is 0xB8

Bit #	B7	B6	B5	B4	В3	B2	B1	B0	OTP
Name	NC	LVDS_TD[2]	LVDS_TD[1]	LVDS_TD[0]	NC	LVDS_TC[2]	LVDS_TC[1]	LVDS_TC[0]	V
Default	0	0	0	0	0	0	0	0	V

Bit	Item	Description
6	LVDS_TD[2]	LVDS_TC skew tuning for LVDS Data lanes
5	LVDS_TD[1]	1setp delay 0.18 nsec.
	LVDS_TD[0]	, ,
2	LVDS_TC[2]	LVDS_TC skew tuning for LVDS Clock lanes
1	LVDS_TC[1]	1setp delay 0.18 nsec.
0	LVDS_TC[0]	Tocip uciay 0.10 fisco.

Bit #	B7	B6	B5	B4	В3	B2	B1	B0	OTP
Name	NC	NC	LVDS_BW[1]	LVDS_BW[0]	NC	LVDS_CPB[2]	LVDS_CPB[1]	LVDS_CPB[0]	V
Default	0	0	0	1	0	0	1	0	٧
						V (4/2			

Bit	Item	Description						
5	LVDS_BW[1]	LVDS DLL bandwidth selection						
		LVDS_BW[1]	LVDS_BW[0]	LVDS bias current				
	4 LVDS BW[0]	0	0	100%				
4		0	1	91%				
		1		83%				
		1		77%				
2	LVDS_CPB[2]	LVPO PLI						
1	LVDS CPB[1]	LVDS DLL pump current selection. I=20u*CPB[2]+10u*CPB[1]+5u*CPB[0]						
0	LVDS_CPB[0]	1=200 CPB[2]+100 CPB[1]+50	СРБ[0]					

2402 CH TFT LCD Source Driver with MIPI/LVDS TCON



DATASHEET V01

Address is 0xBA

Bit #	B7	B6	B5	B4	В3	B2	B1	В0	OTP
Name	BLREV[1]	BLREV[0]	BLREVONOFF	SD_ISSEL[1]	SD_ISSEL[0]	INV_SEL[2]	INV_SEL[1]	INV_SEL[0]	V
Default	1	0	1	0	1	0	0	1	V

Bit	Item		Descr	iption				
7	BLREV[1]	Source output at V-blar	Source output at V-blanking.					
6	BLREV[0]	00:SD keep output the 01: Hi-Z. 1X: GND.	• · · · · · - ·					
5	BLREVONOFF							
4	SD_ISSEL[1]	Source output bias current selection.						
3	SD_ISSEL[0]	Source output bias cur	rent selection.	\/\/\/				
2	INV_SEL[2]	Normal mode POL inve	ersion type selection (f o	or strip panel only).	•			
1	INV_SEL[1]	INV_SEL[2]	INV_SEL[1]	INV_SEL[0]	Inversion tpye			
		0	0	0	line inversion			
		0	0	1	2-line inversion			
0	INV_SEL[0]	0	1		4-line inversion			
		0	1		column inversion			
		1	0	0	8-line inversion			

Bit #	B7	В6	B5	B4	B3	B2	B1	В0	OTP
Name	BC_CTRL	GOA_EN	RB_SWAP	DPFM_OSC_SEL[1]	DPFM_OSC_SEL[0]	LNSEL[1]	LNSEL[0]	NC	V
Default	0	1	1	0		0	0	0	V

Bit	Item		Description				
7	BC_CTRL	H/W pin BC_CTRL control.	H/W pin BC CTRL control.				
6	GOA_EN	GOA function enables.1:enable	ole ,0:disable.				
5	RB_SWAP	Red and Blue color swap.1:R	Red and Blue color swap.1:R/B swap,0:non-swap.				
4	DPFM_OSC_SEL[1]	DPFM clock selection (for BIST mode use clock).					
		DPFM_OSC_SEL[1]	DPFM_OSC_SEL[0]	DPFM frequency			
		0	0	6.25MHz			
3	DPFM_OSC_SEL[0]	0	1	12.5MHz			
		1	0	25MHz			
))1	1	25MHz			
2	(I NOELM1						
	LNSEL[1]	MIPI lane number control. The register do XOR with LANE1_STBYB & LANE0_BISTB					
1	LNSEL[0]	pin.					



Address is 0xBC

Bit #	B7	B6	B5	B4	B3	B2	B1	В0	OTP
Name	GAS_GOA_EN	VRES_BLACK	GCHL_Blanking	NC	NC	NC	NC	NC	V
Default	1	1	1	0	0	0	0	0	V

Bit	Item Description				
7	GAS_GOA_EN	1: When enable gas function, GOA CKV/STV pulled to high level.			
6	VRES_BLACK	1: When user change VRES register, TCON will send two black pattern.			
5	GCHL_Blanking	1: CLR1 =GND, CLR2=High level ,when power on status. 0: CLR1/2 =GND, when power on status.			

Bit #	B7	B6	B5	B4	B3	B2	B1	В0	OTP
Name	VSPS[3]	VSPS[2]	VSPS[1]	VSPS[0]	VSNS[3]	VSNS[2]	VSNS[1]	VSNS[0]	
Description	VDDP v	voltage sele	ction (step=	0.1V)	VDDN voltage selection (step=0.1V)				V
Default	1	0	1	0	1	0	V 1	0	
							>		

VSPS [3:0]	Voltage
0000	4.5V
0001	4.6V
0010	4.7V
:	
1010	5.5V
1111	6V

VSNS [3:0]	Voltage
0000	-4.5V
0001	-4.6V
0010	-4.7V
	>
1010	-5.5V
	:
1,11	-6V



Address is 0xBE

Bit #	B7	B6	B5	B4	В3	B2	B1	B0	OTP
Name	NC	NC	VGHS[5]	VGHS[4]	VGHS[3]	VGHS[2]	VGHS[1]	VGHS[0]	
Description				VGH voltage selection				V	
Default	0	0	1	0	0	0	1	1	

VGHS [5:0]	Voltage
000000	8V
000001	8.2V
000010	8.4V
:	
100011	15V
: :	
111111	20.6V

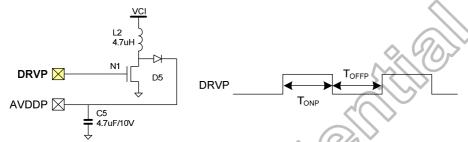
Bit #	B7	B6	B5	B4	B3	B2	B1	В0	OTP
Name	NC	NC	VGLS[5]	VGLS[4]	VGLS[3]	VGLS[2]	VGLS[1]	VGLS[0]	
Description					VGL voltage	e selection			V
Default	0	0	0	1	0) 1	0	0	

VGLS [5:0]	Voltage
000000	-6V
000001	-6.2V
000010	-6.4V
010100	-10V
25	
111111	-18.6V



Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	VSPON[3]	VSPON[2]	VSPON[1]	VSPON[0]	VSPOFF[3]	VSPOFF[2]	VSPOFF[1]	VSPOFF[0]	V
Default	0	1	1	0	0	1	1	0	V

ĺ	Bit	Item	Description
ſ	[7:4]	VSPON [3:0]	Select VSP PFM TON tonp = tpfmclk * (TONP[3:0]+ 4 + N) if PRMFREN=0 N=1.
	[3:0]	VSPOFF[3:0]	Select VSP PFM TOFF toffp = tpfmclk * (TOFFP[3:0]+ 5).



VSPON_T[3:0]	T _{ONP} (μs)
0	1.0
1	1.2
2	1.4
3	1.6
	ſ
13	3.6
14	3.8
15	4.0

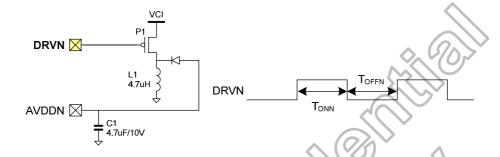
VSPOFF_T[3:0]	T _{OFFP} (μs)
0	1.0
	1.2
2	1.4
3	1.6
$\sim \sim $	
13	3.6
14	3.8
15	4.0



Address is 0xC2

Bit #	B7	B6	B5	B4	В3	B2	B1	B0	OTP
Name	VSNON[3]	VSNON[2]	VSNON[1]	VSNON[0]	VSNOFF[3]	VSNOFF[2]	VSNOFF[1]	VSNOFF[0]	W
Default	0	1	1	0	0	1	1	0	v

Bit	Item	Description
[7:4]	VSNON [3:0]	Select VSN PFM TON tonp = tpfmclk * (TONP[3:0]+ 4 + N) if PRMFREN=0 N=1.
[3:0]	VSNPOFF[3:0]	Select VSN PFM TOFF toffp = tpfmclk * (TOFFP[3:0]+ 5).



VSNON_T[3:0]	T _{ONN} (μs)
0	1.0
1	1.2
2	1.4
3	1.6
	J
13	3.6
14	3.8
15	4.0

VSNOFF_T[3:0]	T _{OFFN} (μs)
	1.0
1	1.2
2	1.4
37 (0)	1.6
13	3.6
14	3.8
15	4.0

• Address is 0xC3

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	VGLXSP	VGHXSP[1]	VGHXSP[0]	PFMFREN	T_OFFSET	NC	NC	NC	V
Default	1	7/	1	0	0	0	0	0	V

Bit	Item	Description
7	VGLXSP	VGL boost function selection. 0:VSN-VSP. 1:2VSN-VSP.
[6:5]	VGHXSP[1:0]	VGH boost function selection. 00: 2VSP. 01: 2VSP+(-VSN). 1x: 2VSP+2(-VSN).
4	PFMFREN	Enable frequency randomizer of both VDDP and VDDN PFM.
3	T_OFFSET	PFM ton / toff offset.



Bit #	B7	B6	B5	B4	B3	B2	B1	В0	OTP			
Name	NC	NC	NC	VPHS[4]	VPHS[3]	VPHS[2]	VPHS[1]	VPHS[0]				
Description		Positive gamma high selection										
Default	0	0	0	0	0	1	0	1				

VPHS [4:0]	Voltage
00000	4
00001	4.05V
00010	4.1V
00100	4.2V (default)
:	
11111	5.5V



Address is 0xC5

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	CGPP_INV[1]	CGPP_INV[0]	SOFT_EN	CLK_SEL[2]	CLK_SEL[1]	CLK_SEL[0]	CMD_SEL[1]	CMD_SEL[0]	W
Default	1	0	1	0	1	1	0	1	٧

Bit	Item		Desci	ription			
[7:6]	CGPP_INV	CGPP_INV [1] set the DRVN sig 1: Invert. 0: Non-invert.	gnal, CGPP_IN\	/ [0] set the DR\	/P signal.		
5	SOFT_EN	Power mode 00 Charge Pump s 0: Disable. 1: Enable.	oft start.				
		CLK_SEL[2:0]			Frequency		
		000			403kHz		
		001		595kHz			
	0114 051	010		781 kHz			
[4:2]	CLK_SEL	011			963kHz (default)		
		100		1136 kHz 1389kHz			
		110		1786kHz			
		111		2083kHz			
		Power mode 00: charge Pump of	ommand select				
		CMD_SEL[1]	CMD_	SEL[0]	Pump command		
[1:0]	CMD_SEL	0		0	x1.5		
[]	05_022	0		1	x2 (default)		
		1		0	x3		
) / \		х3		

• Address is 0xC6

					\ 1.1						
Bit #	B7	B6	B5	B4	B3	B2	B1	В0	OTP		
Name	NC	NC	NC	VNHS[4]	VNHS[3]	VNHS[2]	VNHS[1]	VNHS[0]			
Description		Negative gamma high selection									
Default	0	-00	0	0	0	1	0	0			

VNHS [4:0]	Voltage
00000	-4
00001	-4.05V
00010	-4.1V
	:
00100 (default)	-4.2V
:	:
:	:
11111	-5.5V



Address is 0xC7

Bit #	B 7	B6	B5	B4	B3	B2	B1	В0	OTP
Name	NC	NC	VCL_CPCTL[1]	VCL_CPCTL[0]	VGL_CPCTL[1]	VGL_CPCTL[0]	VGH_CPCTL[1]	VGH_CPCTL[0]	W
Default	0	0	0	1	0	1	0	1	v

Bit	Item	Description
[5:4]	VCL_CPCTL	VCL charge pump clock frequency. 00: X1. 01: X2. 10: X4. 11: X8. (unit=line frequency)
[3:2]	VGL_CPCTL	VGL charge pump clock frequency. 00: X1. 01: X2. 10: X4. 11: X8. (unit=line frequency)
[1:0]	VGH_CPCTL	VGH charge pump clock frequency. 00: X1. 01: X2. 10: X4. 11: X8. (unit=line frequency)

Address is 0xC8

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	POCSD_CTL[1]	POCSD_CTL[0]	EQ0W[5]	EQ0W[4]	EQ0W[3]	EQ0W[2]	EQ0W[1]	EQ0W[0]	V
Default	0	0	0	0	0	1	1	0	V

Bit Ite	m	Description								
[7:6] POCSD	O-CTL	Source output offset cancel method selection. POCSD_CTL=00b								
[5:0] EQ0W		Source EQ0 time setting. TEQ0=EQ0W[4:0]x4 DCLK (Min is 12DCLK).								

• Address is 0xC9

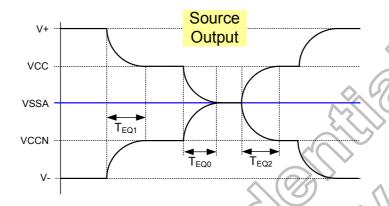
Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP		
Name	NC	NC	NC	EQ1W[4]	EQ1W[3]	EQ1W[2]	EQ1W[1]	EQ1W[0]			
Description	Source EQ1								V		
Description	TEQ1=EQ1V	EQ1=EQ1W[4:0]x4 DČLK.									
Default	0	0	0	0	0	0	0	0			

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Address is 0xCA

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP	
Name	NC	NC	NC	EQ2W[4]	EQ2W[3]	EQ2W[2]	EQ2W[1]	EQ2W[0]		
Possintian Source EQ2 time setting.									V	
Description	TEQ2=EQ2W[4:0]x4 DCLK (TEQ2≤TOEV-22DCLK satisfies gate driver settle time).									
Default	0	0	0	1	1	0	0	0		



• Address are 0xCB~E0

MIPI address	Default	Name	Description	OTP
0xCB	3fh	PVP1	Control 1st Positive gamma op's input voltage. Default: 3.462V~4.250V. Step=12.5mV.	
0xCC	34h	PVP2	Control 2nd Positive gamma op's input voltage. Default:3.312V~4.100V. Step=12.5mV.	
0xCD	2dh	PVP3	Control 3dr Positive gamma op's input voltage. Default:3.212V~4.000V. Step=12.5mV.	
0xCE	2dh	PVP4	Control 4th Positive gamma op's input voltage. Default:2.750V~3.537V. Step=12.5mV.	
0XCF	21h	PVP5	Control 5th Positive gamma op's input voltage. Default:2.350V~3.137V. Step=12.5mV.	
0XD0	1bh	PVP6	Control 6th Positive gamma op's input voltage. Default:1.862V~2.650V. Step=12.5mV.	
0XD1	1eh	PVP7	Control 7th Positive gamma op's input voltage. Default:1.337V~2.125V. Step=12.5mV.	
0XD2	25h	PVP8	Control 8th Positive gamma op's input voltage.Default:1.175V~1.962V. Step=12.5mV.	
0XD3	20h	PVP9	Control 9th Positive gamma op's input voltage. Default:0.500V~1.287V. Step=12.5mV.	
0XD4	20h	PVP10	Control 10th Positive gamma op's input voltage. Default:0.237V~1.025V. Step=12.5mV.	
0XD5	16h	PVP11	Control 11th Positive gamma op's input voltage. Default:0.012V~0.800V. Step=12.5mV.	
0XD6	3fh	PVN1	Control 1st Negative gamma op's input voltage.Default:-3.462V~-4.250V. Step=-12.5mV.	
0XD7	33h	PVN2	Control 2nd Negative gamma op's input voltage. Default:-3.312V~-4.100V. Step=-12.5mV.	
0XD8	2ch	PVN3	Control 3dr Negative gamma op's input voltage. Default:-3.212V~-4.000V. Step=-12.5mV.	٧
0XD9	2eh	PVN4	Control 4th Negative gamma op's input voltage. Default:-2.750V~-3.537V. Step=-12.5mV.	
0XDA	21h	PVN5	Control 5th Negative gamma op's input voltage. Default:-2.350V~-3.137V. Step=-12.5mV.	
0XDB	1bh	PVN6	Control 6th Negative gamma op's input voltage. Default:-1.862V~-2.650V. Step=-12.5mV.	
0XDC	1dh	PVN7	Control 7th Negative gamma op's input voltage. Default:-1.337V~-2.125V. Step=-12.5mV.	
0xDD	24h	PVN8	Control 8th Negative gamma op's input voltage. Default:-1.175V~-1.962V. Step=-12.5mV.	
0XDE	21h	PVN9	Control 9th Negative gamma op's input voltage. Default:-0.500V~-1.287V. Step=-12.5mV.	
0XDF	1fh	PVN10	Control 10th Negative gamma op's input voltage. Default:-0.237V~-1.025V. Step=-12.5mV.	
0xE0	16h	PVN11	Control 11th Negative gamma op's input voltage. Default:0.012V~0.800V. Step=-12.5mV.	



PVP1~ PVP11 gamma voltage mapping

Register setting	PVP1	PVP2	PVP3	PVP4	PVP5	PVP6	PVP7	PVP8	PVP9	PVP10	PVP11
3F	4.25	4.1	4	3.5375	3.1375	2.65	2.125	1.9625	1.2875	1.025	0.8
3E	4.2375	4.0875	3.9875	3.525	3.125	2.6375	2.1125	1.95	1.275	1.0125	0.7875
3D	4.225	4.075	3.975	3.5125	3.1125	2.625	2.1	1.9375	1.2625	1	0.775
3C	4.2125	4.0625	3.9625	3.5	3.1	2.6125	2.0875	1.925	1.25	0.9875	0.7625
3B	4.2	4.05	3.95	3.4875	3.0875	2.6	2.075	1.9125	1.2375 1.225	0.975	0.75
3A 39	4.1875 4.175	4.0375 4.025	3.9375 3.925	3.475 3.4625	3.075 3.0625	2.5875 2.575	2.0625 2.05	1.9 1.8875	1.225	0.9625 0.95	0.7375 0.725
38	4.175	4.025	3.9125	3.45	3.0625	2.5625	2.0375	1.875	1.2123	0.9375	0.725
37	4.1023	4.0123	3.9	3.4375	3.0375	2.55	2.025	1.8625	1.1875	0.9373	0.7123
36	4.1375	3.9875	3.8875	3.425	3.025	2.5375	2.0125	1.85	1.175	0.9125	0.6875
35	4.125	3.975	3.875	3.4125	3.0125	2.525	2	1.8375	1.1625	0.9	0.675
34	4.1125	3.9625	3.8625	3.4	3	2.5125	1.9875	1.825	1.15	0.8875	0.6625
33	4.1	3.95	3.85	3.3875	2.9875	2.5	1.975	1.8125	1.1375	0.875	0.65
32	4.0875	3.9375	3.8375	3.375	2.975	2.4875	1.9625	1.8	1.125	0.8625	0.6375
31	4.075	3.925	3.825	3.3625	2.9625	2.475	1.95	1.7875	1.1125	0.85	0.625
30	4.0625	3.9125	3.8125	3.35	2.95	2.4625	1.9375	1.775	1.1	0.8375	0.6125
2F	4.05	3.9	3.8	3.3375	2.9375	2.45	1.925	1.7625	1.0875	0.825	0.6
2E 2D	4.0375	3.8875	3.7875	3.325	2.925	2.4375	1.9125	1.75	1.075	0.8125	0.5875
2D 2C	4.025 4.0125	3.875 3.8625	3.775 3.7625	3.3125 3.3	2.9125 2.9	2.425 2.4125	1.9 1.8875	1.7375 1.725	1.0625 1.05	0.8 0.7875	0.575 0.5625
2B	4.0123	3.85	3.7625	3.2875	2.8875	2.4123	1.875	1.7125	1.0375	0.7875	0.5625
2A	3.9875	3.8375	3.7375	3.275	2.875	2.3875	1.8625	1.7 123	1.025	0.7625	0.5375
29	3.975	3.825	3.725	3.2625	2.8625	2.375	1.85	1.6875	1.0125	0.75	0.525
28	3.9625	3.8125	3.7125	3.25	2.85	2.3625	1.8375	1.675	10170	0.7375	0.5125
27	3.95	3.8	3.7	3.2375	2.8375	2.35	1.825	1.6625	0.9875	0.725	0.5
26	3.9375	3.7875	3.6875	3.225	2.825	2.3375	1.8125	1.65	0.975	0.7125	0.4875
25	3.925	3.775	3.675	3.2125	2.8125	2.325	1.8	1.6375	0.9625	0.7	0.475
24	3.9125	3.7625	3.6625	3.2	2.8	2.3125	1.7875	1.625	0.95	0.6875	0.4625
23	3.9	3.75	3.65	3.1875	2.7875	2.3	1.775	1.6125	0.9375	0.675	0.45
22	3.8875	3.7375	3.6375	3.175	2.775	2.2875	1.7625	1.6	0.925	0.6625	0.4375
21	3.875	3.725	3.625	3.1625	2.7625	2.275	1.75	1.5875	0.9125	0.65	0.425
20	3.8625	3.7125	3.6125	3.15	2.75	2.2625	1.7375	1.575	0.9	0.6375	0.4125
1F 1E	3.85 3.8375	3.7 3.6875	3.6 3.5875	3.1375 3.125	2.7375 2.725	2.25 2.2375	1.725	1.5625 1.55	0.8875 0.875	0.625 0.6125	0.4 0.3875
1D	3.825	3.675	3.575	3.125	2.7125	2.2375	1.7125 1.7	1.5375	0.8625	0.6125	0.375
1C	3.8125	3.6625	3.5625	3.1123	2.7123	2.2125	1.6875	1.525	0.85	0.5875	0.3625
1B	3.8	3.65	3.55	3.0875	2.6875	2.2	1.675	1.5125	0.8375	0.575	0.35
1A	3.7875	3.6375	3.5375	3.075	2.675	2.1875	1.6625	1.5	0.825	0.5625	0.3375
19	3.775	3.625	3.525	3.0625	2.6625	2.175	1.65	1.4875	0.8125	0.55	0.325
18	3.7625	3.6125	3.5125	3.05	2.65	2.1625	1.6375	1.475	0.8	0.5375	0.3125
17	3.75	3.6	3.5	3.0375	2.6375	2.15	1.625	1.4625	0.7875	0.525	0.3
16	3.7375	3.5875	3.4875	3.025	2.625	2.1375	1.6125	1.45	0.775	0.5125	0.2875
15	3.725	3.575	3.475	3.0125	2.6125	2.125	1.6	1.4375	0.7625	0.5	0.275
14	3.7125	3.5625	3.4625	3	2.6	2.1125	1.5875	1.425	0.75	0.4875	0.2625
13	3.7	3.55	3.45	2.9875	2.5875	2.1	1.575	1.4125	0.7375	0.475	0.25
12 11	3.6875	3.5375	3.4375	2.975	2.575	2.0875	1.5625	1.4	0.725	0.4625	0.2375
10	3.675 3.6625	3.525 3.5125	3.425 3.4125	2.9625 2.95	2.5625 2.55	2.075 2.0625	1.55 1.5375	1.3875 1.375	0.7125 0.7	0.45 0.4375	0.225 0.2125
IU	3.65	3.5125	3.4123	2.9375	2.5375	2.0625	1.525	1.3625	0.6875	0.4373	0.2123
E E	3.6375	3.4875	3.3875	2.925	2.525	2.0375	1.5125	1.35	0.675	0.4125	0.1875
<u>_</u>	3.625	3.475	3.375	2.9125	2.5125	2.025	1.5	1.3375	0.6625	0.4	0.175
C	3.6125	3.4625	3.3625	2.9	2.5	2.0125	1.4875	1.325	0.65	0.3875	0.1625
В	3.6	3.45	3.35	2.8875	2.4875	2	1.475	1.3125	0.6375	0.375	0.15
Α	3.5875	3.4375	3.3375	2.875	2.475	1.9875	1.4625	1.3	0.625	0.3625	0.1375
9	3.575	3.425	3.325	2.8625	2.4625	1.975	1.45	1.2875	0.6125	0.35	0.125
8	3.5625	3.4125	3.3125	2.85	2.45	1.9625	1.4375	1.275	0.6	0.3375	0.1125
7	3.55	3.4	3.3	2.8375	2.4375	1.95	1.425	1.2625	0.5875	0.325	0.1
6	3.5375	3.3875	3.2875	2.825	2.425	1.9375	1.4125	1.25	0.575	0.3125	0.0875
5	3.525	3.375	3.275	2.8125	2.4125	1.925	1.4	1.2375	0.5625	0.3	0.075
4	3.5125	3.3625	3.2625	2.8 2.7875	2.4 2.3875	1.9125	1.3875	1.225	0.55	0.2875	0.0625
<u>3</u> 2	3.5 3.4875	3.35 3.3375	3.25 3.2375	2.7875	2.3875	1.9 1.8875	1.375 1.3625	1.2125 1.2	0.5375 0.525	0.275 0.2625	0.05 0.0375
	3.475	3.325	3.2373	2.7625	2.3625	1.875	1.35	1.1875	0.525	0.2625	0.0375
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Note: (1) Blue marks are the default value. Unit: V.



PVN1~ PVN11 gamma voltage mapping

Register setting	PVN1	PVN2	PVN3	PVN4	PVN5	PVN6	PVN7	PVN8	PVN9	PVN10	PVN11
3F	-4.25	-4.1	-4	-3.5375	-3.1375	-2.65	-2.125	-1.9625	-1.2875	-1.025	-0.8
3E	-4.2375	-4.0875	-3.9875	-3.525	-3.125	-2.6375	-2.1125	-1.95	-1.275	-1.0125	-0.7875
3D	-4.225	-4.375	-3.975	-3.5125	-3.1125	-2.625	-2.1	-1.9375	-1.2625	-1	-0.775
3C	-4.2125	-4.0625	-3.9625	-3.5	-3.1	-2.6125	-2.0875	-1.925	-1.25	-0.9875	-0.7625
3B	-4.2	-4.35	-3.95	-3.4875	-3.0875	-2.6	-2.075	-1.9125	-1.2375	-0.975	-0.75
3A	-4.1875	-4.0375	-3.9375	-3.475	-3.075	-2.5875 -2.575	-2.0625	-1.9	-1.225	-0.9625	-0.7375
39 38	-4.175 -4.1625	-4.325 -4.0125	-3.925 -3.9125	-3.4625 -3.45	-3.0625 -3.05	-2.575 -2.5625	-2.05 -2.0375	-1.8875 -1.875	-1.2125 -1.2	-0.95 -0.9375	-0.725 -0.7125
37	-4.1625	-4.0125	-3.9123	-3.4375	-3.0375	-2.5625	-2.0375	-1.8625	-1.1875	-0.9375	-0.7123
36	-4.1375	-3.9875	-3.8875	-3.425	-3.025	-2.5375	-2.0125	-1.85	-1.175	-0.925	-0.6875
35	-4.125	-4.275	-3.875	-3.4125	-3.0125	-2.525	-2	-1.8375	-1.1625	-0.9	-0.675
34	-4.1125	-3.9625	-3.8625	-3.4	-3	-2.5125	-1.9875	-1.825	-1.15	-0.8875	-0.6625
33	-4.1	-4.25	-3.85	-3.3875	-2.9875	-2.5	-1.975	-1.8125	-1.1375	-0.875	-0.65
32	-4.0875	-3.9375	-3.8375	-3.375	-2.975	-2.4875	-1.9625	-1.8	-1.125	-0.8625	-0.6375
31	-4.075	-4.225	-3.825	-3.3625	-2.9625	-2.475	-1.95	-1.7875	-1.1125	-0.85	-0.625
30	-4.0625	-3.9125	-3.8125	-3.35	-2.95	-2.4625	-1.9375	-1.775	U -1.1	-0.8375	-0.6125
2F	-4.05	-4.2	-3.8	-3.3375	-2.9375	-2.45	-1.925	-1.7625	-1.0875	-0.825	-0.6
2E	-4.0375	-3.8875	-3.7875	-3.325	-2.925	-2.4375	-1.9125	-1.75	-1.075	-0.8125	-0.5875
2D	-4.025	-4.175	-3.775	-3.3125	-2.9125	-2.425	-1,9	-1.7375	-1.0625	-0.8	-0.575
2C	-4.0125	-3.8625	-3.7625	-3.3	-2.9	-2.4125	-1.8875	-1.725	-1.05	-0.7875	-0.5625
2B	-4	-4.15	-3.75	-3.2875	-2.8875	-2.4	-1.875	-1.7125	-1.0375	-0.775	-0.55
2A	-3.9875	-3.8375	-3.7375	-3.275	-2.875	-2.3875	-1.8625	-1.7	-1.025	-0.7625	-0.5375
29	-3.975	-4.125	-3.725	-3.2625	-2.8625	-2.375	-1.85	-1.6875	-1.0125	-0.75	-0.525
28	-3.9625	-3.8125	-3.7125	-3.25	-2.85	-2.3625	-1.8375	-1.675)) -1(/	-0.7375	-0.5125
27	-3.95	-4.1	-3.7	-3.2375	-2.8375	-2.35	-1.825	-1.6625	-0.9875	-0.725	-0.5
26	-3.9375	-3.7875	-3.6875	-3.225	-2.825	-2.3375	-1.8125	-1.65	-0.975	-0.7125	-0.4875
25	-3.925	-4.075	-3.675	-3.2125	-2.8125	-2.325	-1.8	-1.6375	-0.9625	-0.7	-0.475
24	-3.9125	-3.7625	-3.6625	-3.2	-2.8	-2.3125	-1.7875	-1.625	-0.95	-0.6875	-0.4625
23	-3.9	-4.05	-3.65	-3.1875	-2.7875	-2.3	-1.775	-1.6125	-0.9375	-0.675	-0.45
22	-3.8875	-3.7375	-3.6375	-3.175	-2.775	-2.2875	-1.7625	-1.6	-0.925	-0.6625	-0.4375
21	-3.875	-4.025	-3.625	-3.1625	-2.7625	-2.275	-1.75	-1.5875	-0.9125	-0.65	-0.425
20 1F	-3.8625	-3.7125 -4	-3.6125	-3.15	-2.75	-2.2625	-1.7375	-1.575	-0.9	-0.6375	-0.4125 -0.4
1E	-3.85		-3.6 -3.5875	-3.1375 -3.125	-2.7375	-2.25 -2.2375	-1.725	-1.5625 -1.55	-0.8875	-0.625	
1D	-3.8375 -3.825	-3.6875 -3.975	-3.575	-3.125	-2.725 -2.7125	-2.2375	-1.7125 -1.7	-1.5375	-0.875 -0.8625	-0.6125 -0.6	-0.3875 -0.375
1C	-3.8125	-3.6625	-3.5625	-3.1125	-2.7123	-2.225	-1.6875	-1.525	-0.85	-0.5875	-0.3625
1B	-3.8	-3.0023	-3.55	-3.0875	-2.6875	-2.2123	-1.675	-1.5125	-0.8375	-0.575	-0.3623
1A	-3.7875	-3.6375	-3.5375	-3.0675	-2.675	-2.1875	-1.6625	-1.5	-0.825	-0.5625	-0.3375
19	-3.775	-3.925	-3.525	-3.0625	-2.6625	-2.1075	-1.65	-1.4875	-0.8125	-0.55	-0.325
18	-3.7625	-3.6125	-3.5125	-3.05	-2.65	-2.1625	-1.6375	-1.475	-0.8	-0.5375	-0.3125
17	-3.75	-3.9	-3.5	-3.0375	-2.6375	-2.15	-1.625	-1.4625	-0.7875	-0.525	-0.3
16	-3.7375	-3.5875	-3.4875	-3.025	-2.625	-2.1375	-1.6125	-1.45	-0.775	-0.5125	-0.2875
15	-3.725	-3.875	-3.475	-3.0125	-2.6125	-2.125	-1.6	-1.4375	-0.7625	-0.5	-0.275
14	-3.7125	-3.5625	-3.4625	-3	-2.6	-2.1125	-1.5875	-1.425	-0.75	-0.4875	-0.2625
13	-3.7	-3.85	-3.45	-2.9875	-2.5875	-2.1	-1.575	-1.4125	-0.7375	-0.475	-0.25
12	-3.6875	-3.5375	-3.4375	-2.975	-2.575	-2.0875	-1.5625	-1.4	-0.725	-0.4625	-0.2375
11	-3.675	-3.825	-3.425	-2.9625	-2.5625	-2.075	-1.55	-1.3875	-0.7125	-0.45	-0.225
10	-3.6625	-3.5125	-3.4125	-2.95	-2.55	-2.0625	-1.5375	-1.375	-0.7	-0.4375	-0.2125
F	-3.65	-3.8	-3.4	-2.9375	-2.5375	-2.05	-1.525	-1.3625	-0.6875	-0.425	-0.2
Е	-3.6375	-3.4875	-3.3875	-2.925	-2.525	-2.0375	-1.5125	-1.35	-0.675	-0.4125	-0.1875
D	-3.625	-3.775	-3.375	-2.9125	-2.5125	-2.025	-1.5	-1.3375	-0.6625	-0.4	-0.175
С	-3.6125	-3.4625	-3.3625	-2.9	-2.5	-2.0125	-1.4875	-1.325	-0.65	-0.3875	-0.1625
В	-3.6	-3.75	-3.35	-2.8875	-2.4875	-2	-1.475	-1.3125	-0.6375	-0.375	-0.15
Α	-3.5875	-3.4375	-3.3375	-2.875	-2.475	-1.9875	-1.4625	-1.3	-0.625	-0.3625	-0.1375
9	-3.575	-3.725	-3.325	-2.8625	-2.4625	-1.975	-1.45	-1.2875	-0.6125	-0.35	-0.125
8	-3.5625	-3.4125	-3.3125	-2.85	-2.45	-1.9625	-1.4375	-1.275	-0.6	-0.3375	-0.1125
7	-3.55	-3.7	-3.3	-2.8375	-2.4375	-1.95	-1.425	-1.2625	-0.5875	-0.325	-0.1
6	-3.5375	-3.3875	-3.2875	-2.825	-2.425	-1.9375	-1.4125	-1.25	-0.575	-0.3125	-0.0875
5	-3.525	-3.675	-3.275	-2.8125	-2.4125	-1.925	-1.4	-1.2375	-0.5625	-0.3	-0.075
4	-3.5125	-3.3625	-3.2625	-2.8	-2.4	-1.9125	-1.3875	-1.225	-0.55	-0.2875	-0.0625
3	-3.5	-3.65	-3.25	-2.7875	-2.3875	-1.9	-1.375	-1.2125	-0.5375	-0.275	-0.05
2	-3.4875	-3.3375	-3.2375	-2.775	-2.375	-1.8875	-1.3625	-1.2	-0.525	-0.2625	-0.0375
1	-3.475	-3.625	-3.225	-2.7625	-2.3625	-1.875	-1.35	-1.1875	-0.5125	-0.25	-0.025
0	-3.4625	-3.3125	-3.2125	-2.75	-2.35	-1.8625	-1.3375	-1.175	-0.5	-0.2375	-0.0125

Note: (1) Blue marks are the default value. Unit: V.



Address is 0xE1

Bit #	B7	B6	B5	B4	B3	B2	B1	В0	OTP
Name	NC	NC	NC	NC	VBP[1]	VBP[0]	VBN[1]	VBN[0]	V
Default	0	0	0	0	0	1	0	1	V

Bit	Item	Description
[3:2]	VBP	GAMMAP bias current select. 00=80% 01=100% 10=120% 11=140%.
[1:0]	VBN	GAMMAN bias current select. 00=80% 01=100% 10=120% 11=140%.

Address is 0xFA

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	[f][J]	ID[0]	
Description				VENDE	R_ID		5.3		X
Default	0	1	1	1	0	0	0	0	

Address is 0xFB

		r		1			r	r	
Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	GRB							
Description				GR	B		$\langle \langle \rangle \rangle$	<i>'</i>	Х
Default	0	0	0	0	0	0	0	1	

Address is 0xFC

Bit #	B7	B6	B5	B4	В3	B2	B1	В0	OTP
Name	ID[7]	ID[6]	ID[5]	ID[4]	(ID[3]	ID[2]	ID[1]	ID[0]	
Description				PRODU	CT ID1				X
Default	1	0	0	0	0	0	1	0	

• Address is 0xFD

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	
Description	~ ~C			PRODU	CT ID2				Х
Default	0	1 //		0	0	0	0	0	

Address is 0xFE

Bit #	B7	B6	B5	B4	B3	B2	B1	В0	OTP
Name	NC	NC	NC	NC	ID[3]	ID[2]	ID[1]	ID[0]	
Description	PRODUCT ID3								
Default	0	0	0	0	1	0	0	1	

Address is 0xFF

Bit #	B7	В6	B 5	B4	B3	B2	B1	В0	OTP	
Name	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]		
Description		VERSIONID								
Default	0	0	0	0	0	0	1	1		

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9.2 Registers of Page1

Address is 0xB1

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NA			OTP_GROUP[4:0]					
Default	0	0	0	0	0	0	0	0	^

Bit	Item	Description
[4:0]	OTP_GROUP[4:0]	OTP trimming group select. The group range is from group1 to group27.

Address is 0xB2

Bit #	B7	B6	B5	B4	B3	B2	B1	В0	OTP	
Name	OTP_PWD[7:0]									
Default	0	1	0	1	1	0	1	0	^	

	Bit	Item	Description
Ī	[7:0]	OTP_PWD[7:0]	OTP enter auto program mode.

Address is 0xB3

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	N	С	OTP_P	TM[1:0]	NA	OTP_RE_LOAD	OTP_RD	OTP_WR	
Default	0	0	0	0	0	0	0	0	^
				$-(\bigcirc)$,				

Bit	Item	Description
[5:4]	OTP_PTM[1:0]	OTP test mode.
2	OTP_RE_LOAD	OTP auto re-load control.
1	OTP_RD	OTP read control.
0	OTP WR	OTP write control.

• Address is 0xB4

		1//							
Bit #	B7	B6	B5	B4	В3	B2	B1	В0	ОТР
Name	0,<			NA				OTP_ADDR[8]	Y
Default	0	0	0	0	0	0	0	0	_ ^

Address is 0xB5

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	ОТР	
Name	OTP_ADDR[7:0]									
Default	0	0	0	0	0	0	0	0		

Bit	Item	Description
0	OTP_ADDR[8]	OTP address set.
[7:0]	OTP_ADDR[7:0]	OTF address set.

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Address is 0xB6

Bit #	B7	B6	B5	B4	B3	B2	B1	В0	OTP		
Name		OTP_PDOB[7:0]									
Default	0	0	0	0	0	0	0	0	^		

Bit	Item	Description
[7:0]	OTP_PDOB[7:0]	Read data from OTP.

Address is 0xB7

Bit #	B7	B6	B5	B4	B3	B2	B1	В0	ОТР
Name				OTP_P	DIN[7:0]		0. 0/0.	>	V
Default	0	0	0	0	0	0	0	0	7 /

Bit	Item	Description
[7:0]	OTP_PDIN[7:0]	Write data to OTP.

Address is 0xB8

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name				OTP_MA	NUAL[7:0]	<,	\bigcirc) \vee		Y
Default	0	1	0	1	1	0	1	0	^
				7(~ (O)			

Bit	Item	Description
[7:0]	OTP_MANUAL[7:0]	OTP enter manual program mode.

Address is 0xB9

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	N	Α <	DISABLE	OTP[1:0]	POR	PPROG	VPS	PWE	V
Default	0	0	0	0	0	0	0	0	^

Bit	Item		Description						
0	PWE	OTP PWE control	signal.						
1	VPS	OTP VPS control s	signal.						
2	PPROG	OTP PPROG cont							
3	POR	OTP POR control	signal.						
	OTP function disables.								
		DISABLE_OTP	Master OTP function	Slave OTP function					
5:4	DISABLE OTP[1:0]	00b	Enable	Enable					
5.4	DISABLE_OTP[1.0]	01b	Enable	Disable					
	10b Disable Enable								
		11b	Disable	Disable					

9.3 Registers of Page2

Please refer application note

9.4 Registers of Page3

Please refer application note



9.5 Registers of Page4

Address is 0xB1

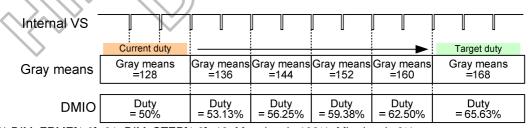
Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	DIM_EN	BL_EN	PWM_POL	NC	CABC_ AGING_EN	NC	V
Default	0	0	1	1	1	0	1	0	

Bit	Item	Description
		CABC aging enables.
1	CABC_AGING_EN	0: Disable.
		1: Enable.
		Poliarty of PWM control signal setting.
3	PWM_POL	0: PWM output is non-inversion.
		1: PWM output is inversion.
		CABC back light control enables.
4	BL_EN	0: Disable.
		1: Enable.
		CABC dimming enables.
5	DIM_EN	0: Disable.
		1: Enable.

Address is 0xB2

Bit #	B7	B6	B5	B4	B3	B2	B1	В0	OTP
Name	NC	NC	NC	NC		STEP	DIM_I	RME	V
Default	0	0	0	0	1 (0	1	0] '

Bit	Item	Description
[1:0]	DIM_FRME[1:0]	CABC dimimng cycle settling. 00b: 1 frame per step 01b: 2 frame per step. 10b: 3 frame per step. 11b: 4 frame per step.
[3:2]	DIM_STEP[1:0]	CABC dimming step setting. 00b: 2 steps. 01b: 4 steps. 10b: 8 steps. 11b: 16 steps.



Note: (1) DIM_FRME[1:0]=01, DIM_STEP[1:0]=10, Max duty is 100%, Min duty is 0%.

Figure 9.1: CABC dimming control

2402 CH TFT LCD Source Driver with MIPI/LVDS TCON



DATASHEET V01

Address is 0xB3

Bit #	B7	B6	B5	B4	В3	B2	B1	B0	OTP
Name		DUTY_UD							
Default	1	1	1	1	1	1	1	1	V

Bit	Item	Description
[7:0]	DUTY_UD[7:0]	Set user-defined PWM duty on CABC bypass mode. The CABC bypass mode is setting at 0xB6[3:2] of page0.

Address is 0xB4

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP	
Name		CABC_MB								
Default	0	0 0 0 1 0 0 0								

Bit	Item	Description
[7:0]	CABC_MB[7:0]	Set PWM minimum duty.

• Address is 0xB5

Bit #	B7	B6	B5	B4	В3	B2	B1	B0	OTP
Name	PWM_PRD								
Default	0	0	0	1 /(0	0()	0	0	v

ĺ	Bit	Item		Description
I	[7:0]	PWM_PRD[7:0]	CABC PWM period setting.	

Address is 0xB6

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	NC	NC	NC		PWM_DIV		V
Default	0	0(\$//	0	0	0	0	1	0	v

Bit	Item			Description				
		CABC PWM period divider.						
		PWM_DIV[2]	PWM_DIV[1]	PWM_DIV[0]	CABC PWM period divider			
[0,0]		0	0	0	DIV 1			
		0	0	1	DIV 2			
	PWM_DIV[2:0]	0	1	0	DIV 4			
[2:0]		0	1	1	DIV 8			
		1	0	0	DIV 16			
		1	0	1	DIV 32			
		1	1	0	DIV 64			
		1	1	1	DIV 128			
		_	l .	l .				

Address is 0xB8

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP	
Name	MAX_DUTY[7:0]									
Default	1	1 1 1 1 1 1 1 1 1 V								

Bit	Item	Description
[7:0]	MAX DUTY	Set PWM maximum duty.

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9.6 Registers of Page6

Address is 0xB0

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	EoTp_EN	CRCEN	CRCErr_FilterOut	VC4FRAME	VC_S[1]	VC_S[0]	VC_m[1]	VC_m[0]	V
Default	1	1	1	0	0	0	0	0	V

Bit	Item	Description
[7]	EoTp_EN	Process of EoT packet enable. 1: Enable. 0: Disable.
[6]	CRCEN	CRC check enable. 1: Enable. 0: Disable.
[5]	CRCErr_FilterOut	Filter-out by CRC check result enable. 1: Enable. 0: Disable.
[4]	VC4FRAME	RX virtual channel filtering mode. 1: Enable. 0: Disable.
[3:2]	VC_S	virtual channel ID setting of slave (for LP/HS rx).
[1:0]	VC_m	virtual channel ID setting of master (for LP tx).

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	RT3[2]	RT3[1]	RT3[0]	NC	RT2[2]	RT2[1]	RT2[0]	V
Default	0	1	0	U .	0	1	0	1	V

Bit	Item	Desc	ription
		Lane3 termination resistance control.	
		RT3[2:0]	Ohm Ω
		111	81
		110	90
[6:4]	RT3	101	102
[0.1]	1110	100	118
	~ ~((011)	128
		010	153
		001	192
		000	255
		Lane2 termination resistance control.	
		RT2[2:0]	Ohm Ω
		111	81
		110	90
[2:0]	RT2	101	102
[2.0]	1112	100	118
		011	128
		010	153
		001	192
		000	255



Address is 0xB4

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	RT1[2]	RT1[1]	RT1[0]	NC	RT0[2]	RT0[1]	RT0[0]	V
Default	0	1	0	1	0	1	0	1	V

Bit	Item	Descr	iption
		Lane1 termination resistance control.	
		RT3[2:0]	Ohm Ω
		111	81
		110	90
[6:4]	RT1	101	102
[0.4]	''''	100	118
		011	128
		010	153
		001	192
		000	255
		Lane0 termination resistance control.	
		RT2[2:0]	Ohm Ω
		111	81
		110	90
[2:0]	RT0	101	102
[2.0]	1110	100	118
		011	128
		010	153
		001	192
		000	255

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	TurnDisable	NC	NC	NC	NC	RTC[2]	RTC[1]	RTC[0]	W
Default	0	0	0	0	0	1	0	1	٧

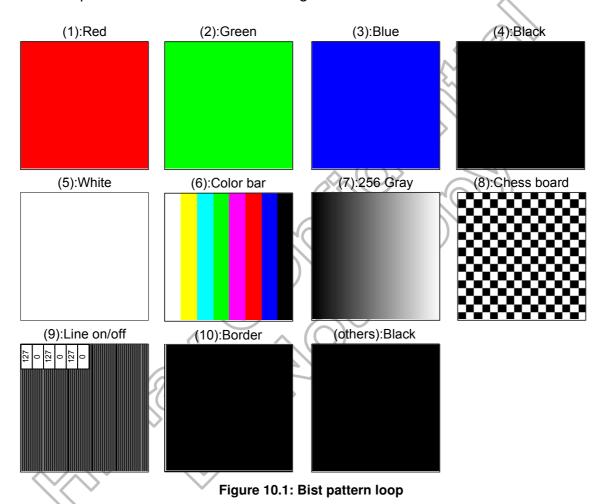
Bit	Item	Descripti	on
7	TurnDisable	BTA→TX procedure function enable. 1: Enable. 0: Disable.	
		Clock Lane termination resistance control.	
		RTC[2:0]	Ohm Ω
		111	81
		110	90
[2:0]	RT0	101	102
[2.0]	1110	100	118
		011	128
		010	153
		001	192
		000	255

10. Function Description

10.1 BIST pattern

When register BIST_EN is trigger to high, then HX8260-A will leave normal operation mode and starts to generate the BIST pattern to LCD panel without MIPI input signals.

The BIST pattern is illustrated as below figure.



10.2 CABC Function

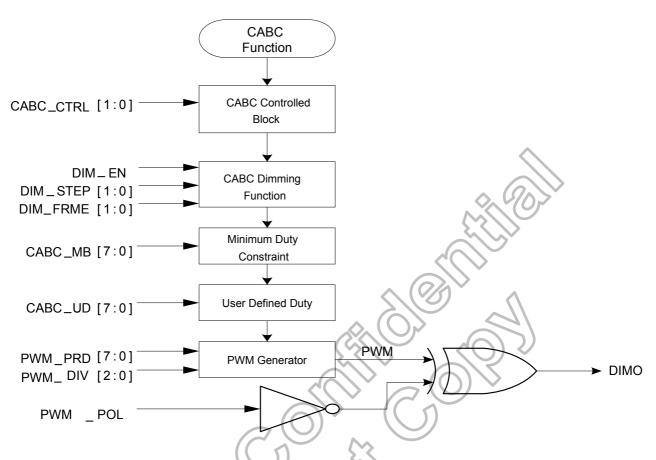


Figure 10.2: CABC flow chart

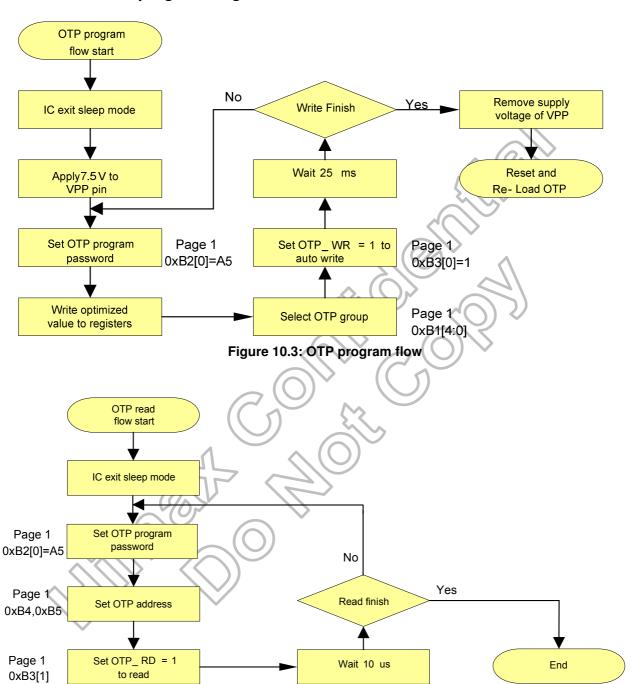
CABC controlled register:

- CABC_EN: CABC enable/ disable switch
- CABC CTRL[1:0]: UI / Still / Moving / Bypass mode selection
- CABC MB[7:0]: Minimum PWM duty constraint
- DUTY UD[7:0]: Fixed PWM duty by user-defined when operating on Bypass mode
- PWM POL: PWM duty polarity selection
- BL EN: back-light On/ Off switch
- DIM EN: Dimming function enable/ disable switch
- Dimming time selection : DIM STEP[1:0] / DIM FRME[1:0]
 - Total dimming time = DIM STEP[1:0] × DIM FRME[1:0]
- PWM duty frequency selection: PWM PRD[7:0] / PWM DIV[2:0]
 - PWM output period = CLK period × 256 × (PWM PRD[7:0]) / (PWM DIV[2:0] + 1)

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10.3 OTP function

10.3.1 OTP flow of programming and read





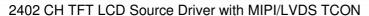
10.3.2 OTP table

OTP address[7:0]	В7	В6	B5	B4	В3	B2	B1	В0	Group
2	W1								
3		T_VCOMS[7:0]							
4	W2								GROUP0
5				T_VCO	MS[7:0]				GROOF
6	W3								
7	T_VCOMS[7:0]								

OTP address[7:0]	В7	В6	B5	B4	В3	B2	B1	В0	Group
8	W1	STB	UPDNB	LR	ZIGZAG_S EL	DISP_ON	NBW_SEL	BIST	
9	ZTYPI	SEL	PWF	RMD	VRES_FIX		RES		
10		<u></u>		VR					
11				ZDA	ATA	40			
12	LN	SW	PNSW	HFRC_IN V	CABC_	_CTRL	DITHER_E N	HFRC_EN	
13	PCLK_SE L	RX_DINT	RX_	VB	2	LVDS	_ ~ / /	LVDS_FM T	
14			LVDS_TD		\ (C		LVDS_TC		
15			LVDS	S_BW		J	LVDS_CPB		
16	BLF	REV	BLREVON FF		~ / / /	SSEL	NNV_	SEL	
17	BC_CTRL	GOA_EN	RB_SWAP	DPFM_C	SC_SEL	LNS	SEL		
18	GAS_GOA _EN	VRES_BL ACK	GCHL_Bla nking			oi_tmp03c[4:	0]		Group 1
19		VS	SPS			VS	NS		
20					VG	HS			
21			((VG	LS			
22				//					
23			PON			VSP			
24		VSI	NON			VSN	OFF		
25		VGLXSP	VGH	XSP	PFMFREN	T_OFFSE T			
26		U/Δ	>			VPHS			
27	CGPF	VIII_Y	SOFT_EN		CLK_SEL		CMD	SEL	
28						VNHS			
29	~ ~ ~ ~		VCL_C	PCTL	VGL_0		VGH_0	CPCTL	
30	POCS	D_CTL			EQ				
31						EQ1W			
32	///\		\\//			EQ2W			



OTP address[7:0]	В7	В6	B5	B4	В3	B2	B1	В0	Group
33	W1				PV	P1			
34						P2			
35					PV	P3			
36					PV	P4			
37						P5			
38					PV	'P6			Group 2
39					PV	'P7			
40					PV	'P8			
41					PV	'P9	<		
42					PV	P10			
43					PV	P11			
44	W1				PV	N1	0.07	7>	
45					PV	N2	7.77.0	7	
46					PV	N3	23/7		
47					PV	N4	1/1/2		
48					PV	N5	1/10		
49					PV	N6			
50					PV	N7	→		
51					PV	N8	7		
52					PV	N9			Group 3
53					PVI	V10			
54					PV	N11	$\langle \langle \rangle \rangle$)	
55					VI	3P	V V	BN	
56					~~ ~ ~	T_OSCT[4:	0]		
57				7(210)) 🗸		
58		•			V //	7 (
59		BIST	VFP		<i>?</i> ((BIST	ΓVBP		
60				$\frac{1}{2}$			_	MENU_EN	

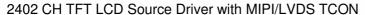




ОТР	B7	В6	B5	B4	B3	B2	B1	В0	Group
address[7:0] 61	W1								3 Gup
62		STBYB MOD			GOLITI	1 SEL[5:0]			=
63		STBYB MOD				2_SEL[5:0]			=
64		STBYB MOD				3 SEL[5:0]			-
65		STBYB MOD				4 SEL[5:0]			-
66		STBYB MOD				5 SEL[5:0]			┪
67		STBYB MOD				6_SEL[5:0]			-
68		STBYB_MOD				7 SEL[5:0]			
69		STBYB MOD				8 SEL[5:0]			
70		STBYB MOD				9 SEL[5:0]			
71		STBYB MOD				0 SEL[5:0]			
72	GOUTL11	STBYB MOD				1 SEL[5:0]			7
73		STBYB_MOD				2 SEL[5:0]			1
74		STBYB MOD				3 SEL[5:0]			7
75	GOUTL14	STBYB MOD			GOUTL 1	4 SEL[5:0]			7
76	GOUTL15	STBYB_MOD			GOUTL_1	5_SEL[5:0]			
77	GOUTL16	STBYB_MOD			GOUTL_1	6_SEL[5:0]			
78	GOUTL17	_STBYB_MOD			GOUTL_1	7_SEL[5:0]			
79	GOUTL18	_STBYB_MOD				8_SEL[5:0]			
80		_STBYB_MOD				9_SEL[5:0]			
81	GOUTL20	_STBYB_MOD			GOUTL_2	0_SEL[5:0]			
82		_STBYB_MOD				21_SEL[5:0]			
83		_STBYB_MOD				22_SEL[5:0]			
84		_STBYB_MOD				1_SEL[5:0]			Group 4
85		_STBYB_MOD				2_SEL[5:0]			
86		_STBYB_MOD				3_SEL[5:0]			
87		STBYB_MOD				4_SEL[5:0]			_
88		STBYB_MOD				5_SEL[5:0]			
89		_STBYB_MOD				6_SEL[5:0]			
90		STBYB_MOD				7_SEL[5:0]			4
91		STBYB_MOD				8_SEL[5:0]			4
92		STBYB_MOD				9_SEL[5:0]			4
93		STBYB_MOD				10_SEL[5:0]			4
94		_STBYB_MOD				11_SEL[5:0]			_
95 96		STBYB_MOD STBYB_MOD				12_SEL[5:0] 13_SEL[5:0]			4
96		STBYB MOD							_
98		STBYB MOD				4_SEL[5:0] 5 SEL[5:0]			_
	0.01175	0.777 (0.110.0			001170				-
100		STBYB MOD				6_SEL[5:0] 7_SEL[5:0]			-
101		STBYB MOD							-
102		STBYB MOD				18_SEL[5:0] 19_SEL[5:0]			-
103		STBYB MOD				20 SEL[5:0]			
104	_	STBYB MOD				21 SEL[5:0]			┥ !
105		STBYB MOD				22 SEL[5:0]			┥ !
		GOA VGOFF	GOA P	GOA HZ					1
106	VGL_GAS	EN EN	WROFF	EN					



OTP	В7	В6	B5	B4	В3	B2	B1	В0	Group		
107	W1		DAC_EN	SLC_DMY_	CPV_EN	CPV_4P_	AUO_EN	AUO_DC_	-		
107	VVI	CV/NC D	DAC_LIN	CLK_EN CLKV BLA		EN	AUU_LIN	4P_EN	-		
108		SYNC_P OL	UD_POL	NKON			CKV_PHASI	<u> </u>			
109											
110		STV_DELAY FACTOR HS_NUM									
111	CLR_PRI	EC_CNT	FLC_P	REC_CNT		STV_PR	EC_CNT				
112 113					DL T0						
114					T1						
115					T2						
116					T3						
117					T4						
118					T5 Г2В						
119 120					г <u>2В</u> ГЗВ						
121					T6				1		
122					T7	(0)	<u> </u>]		
123					Г6В						
124				7	77B	OT (
125						STV STV LEAD	_WD				
126 127					1	STV_LEAD CKV	WD				
128						CKV LEAD			1		
129					CKV [1		
130			•		PRC_CNT				- - -		
131					NO						
132				F	FLC				Group 5		
133					FLCA_LEAD	FLC BLA			Group 5		
134						NKON_S					
						EL	FLC_NON-	OVERLAP			
135					(_START						
136				BLAN	VK_WD		CLDO LEA		-		
137			CI	R DL	CLR1_LEA D	AD	CLR3_LEA D	AD			
			OL.	II_DL	CLR1234 F	AD.	l D	AD	1		
138		spi_goa_r	eserve50		P SEL	CLI	R1234_WD[1	0:8]			
139					R1_WD						
140	OLD4 DO			CLR2	234_WD						
141	CLR1_PO L				CLR1_STAR	т					
1.10	CLR2_PO				<u> </u>	•					
142	L				CLR2_STAR	Т					
143	CLR3_PO				0.00.07.5	-					
0	CL D4 DO				CLR3_STAR	Τ					
144	CLR4_PO CLR4_START										
145	CLR234_START_MSB CLR1_START_MSB								1		
146		_	_	М	ASKSTART[6	6:0]		1			
147	MARK_LE		·		MARK_CKV						
148	AD			R	5	KV7	V9	KVA	-		
149									1		
150				CKV PF	REC_CNT2				-		
151		CLR1	_SEL			CLR2	_SEL]		
152											





OTP address[7:0]	B7	В6	B5	B4	В3	B2	B1	В0	Group
153	W1		DIM_EN	BL_EN	PWM_PO L		CABC_AG AIN		
154					DIM	STEP	DIM	FM]
155				DUTY	_UD[7:0]				
156				CABC_	_MB[7:0]				Group 6
157				PWM	I_PRD				
158						F	WM_DIV[2:0	0]	
159									
160				MAX_D	UTY[7:0]				
176	W1								
177	EoTp_EN	CRCEN	CRCErr_ FilterOut	VC4FRA ME	V	C_S	VC	<u></u> m	
178	PCLK_Refi ne_Auto	PCLK_Man ual_On			PC	CLK_Manual	_Freq	9	
179							1/1/2		Group 8
180						\dagger{\langle}{\rightarrow}			
181			RT3[2:0]				RT2[2:0]		
182			RT1[2:0]			(0)	RT0[2:0]	•	
183	TurnDisabl e						RTC[2:0]		



10.4 No signal detect function

HX8260-A keeps detect input signals (HS, VS) for MIPI mode input and DCLK for LVDS mode input. If deticting of signals is missing, HX8260-A will enter no signal mode.

No signal mode:

- A. All GOA signals will keep running.
- B. Keep PFM and charge pump running.
- C. Panel display will show black pattern.



10.5 GAS function

When power is removed from an electronic device during display, the image still keeps on the LCD panel for a long time. GAS function can speed the process that image disappears.

The GAS function is a voltage detector. By GAS circuit, HX8260 can detect low voltage of power and send control signal to discharge residual potential in LCD panel and remove image.

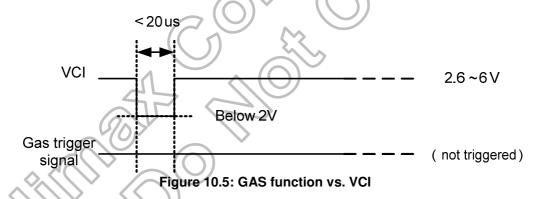
In any one of the following case, the chip will entry GAS function.

- A. VCI is lower than 2V (Case 1)
- B. VSP is lower than 3V (Case 2)

GAS function:

- A. Source output pull to VSSA.
- B. All GOA signals will be set to gas mode (setting by register).
- C. Stop PFM and charge pump function.
- D. VCOM output pull to VSSA.

The GAS function has debounce protection circuit. EX: If the duration of voltage drop on VCI is less than 20us (Ex: induced by ESD pulse), the GAS function will not be active even the VCI voltage level is less than 2V.



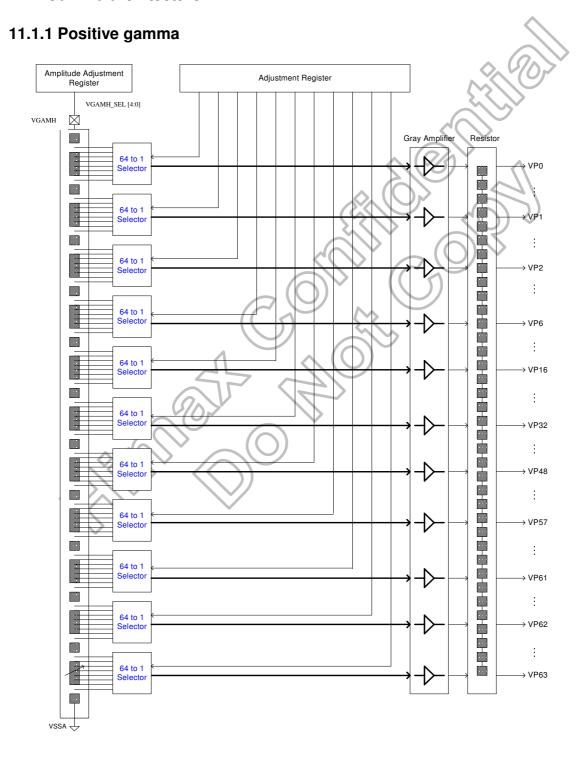


11. Gamma Adjustment Function

HX8260-A supports 11gamma correction reference point:

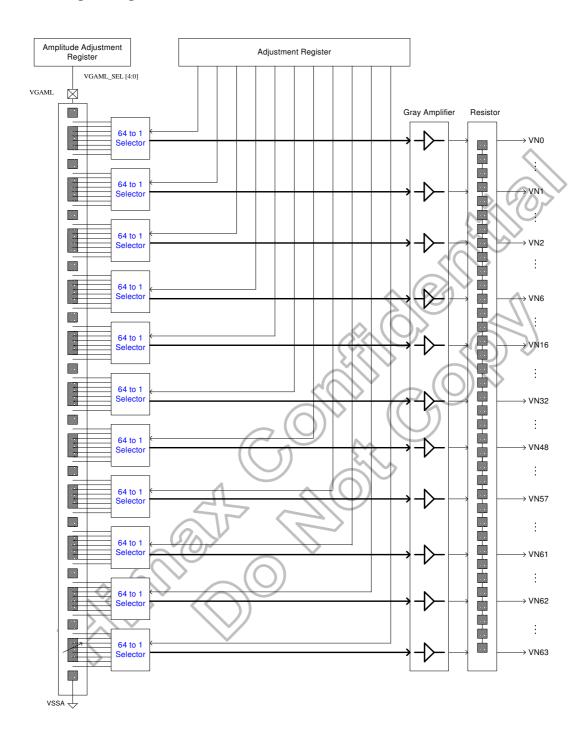
VP0/VP2/VP6/VP16/VP32/VP48/VP57/VP61/VP62/VP63 are generated within driver IC and adjustable by register setting.

11.1 Gamma architecture





11.1.2 Negative gamma





11.2 Gamma resistor table

Positive gamn	na resistor (Ω)		Negative gamı	ma resistor (Ω)
RV0	1050		RV0	1050
RV1	826		RV1	826
RV2	525		RV2	525
RV3	217		RV3	217
RV4	126		RV4	126
RV5	378		RV5	378
RV6	462		RV6	462
RV7	315		RV7	315
RV8	266		RV8	266
RV9	336		RV9	336
RV10	161		RV10	161
RV11	161		RV11	161
RV12	161		RV12	161
RV13	140		RV13	140
RV14	140		RV14	140
RV15	140		RV15	140
RV16	140		RV16	140
RV17	140		RV17	140
RV18	140		RV18	140
RV19	133		RV19	133
RV20	105		RV20	105
RV21	105		RV21	105
RV22	105		RV22	105
RV23	105		RV23	105
RV24	105		RV24	105
RV25	98		RV25	98
RV26	98	1	RV26	98
RV27	98		RV27	98
RV28	98		RV28	98
RV29	126	.)	RV29	126
RV30	105	\vee	RV30	105
RV31	112	ĺ	RV31	112
RV32	91		RV32	91
RV33 RV34	91 91		RV33 RV34	91 91
RV35	105		RV35	105
RV36	77,	\setminus	RV36	77
RV37	84		RV37	84
RV38	91		RV38	91
RV39	112		RV39	112
RV40	91		RV40	91
RV41	91		RV41	91
RV42	91		RV42	91
RV43	91		RV43	91
RV44	105		RV44	105
RV45	105		RV45	105
RV46	105		RV46	105
RV47	105		RV47	105
RV48	105		RV48	105
RV49	154		RV49	154
RV50	189		RV50	189
RV51	189		RV51	189
RV52	196		RV52	196
RV53	210		RV53	210
RV54	210		RV54	210
RV55	224		RV55	224
RV56	280		RV56	280
RV57	294		RV57	294
RV58	343		RV58	343
RV59	539		RV59	539
RV60	525		RV60	525
RV61	406		RV61	406
RV62	476		RV62	476

Table 11.1: Gamma resistor table



12. DC Characteristics

12.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit
	Symbol	Min.	Typ.	Max.	Oilit
I/O voltage	VDDI_RX	-0.3	-	3.96	٧
	VDDI_D				
Power input	VCI	-0.3	-	6.5	V
VSP voltage	VSP	-0.3	-	6.5	V
VSN voltage	VSN	-6.5	-	0.3	V
VPP (OTP power)	VPP	-0.3	-	8.64	V
Operating temperature ⁽¹⁾	Topr	-20	- 0	+ 85	$^{\circ}\mathbb{C}$
Storage temperature ⁽¹⁾	Tstg	-55	-(^)	125	$^{\circ}\mathbb{C}$

Note: (1) Do not let condensation for low temperature.

12.2 Typical operating condition

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	Offic
IOVCC voltage	VDDI_RX		1.8	1.9	V
	VDDI_D	8(1)	1.0) 1.9	٧
Power input	VCI	2.6	3.3	6	V
VSP voltage	VSP (4.5		6	V
VSN voltage	VSN	-6	1	-4.5	V
VPP (OTP power)	VPP	7.4	7.6	7.8	V



12.3 DC electrical characteristics

(Test condition: VCI=1.6~3.6V, T_A=-20℃~+85℃.VSS=VSSA=0V)

D	arameter	Symbol		Spec.		Unit
F	arameter	Syllibol	Min.	Typ.	Max.	Offic
VDDI_D Input high level voltage1		VIH1	0.8 x VDDI_D	-	VDDI_D	V
VDDI_D input lo	w level voltage1	VIL1	VSS	1	0.2 x VDDI_D	V
Input Leakage C	Gurrent	IL1	(-1)	ı	(+1)	μΑ
VGLO2 output v		VGLO2	-15	-	-5	V
VGMAH output v	O .	VGMAH	4	-	5.5	V
VGMAL output v	roltage	VGMAL	-5.5	-	-4	V
VCI_REG output	t voltage	VCI_REG	2.1	- 🔷	3.0	V
VGL output volta		VGL	-16	-(>>)	-6	V
VGH output volta	age	VGH	8	-	19	V
VCL output volta	ige	VCL	-2.1	-2.4	-3.0	V
VOM output volt	age	VOM	-2.75	-1.48	-0.2	V
Input terminal pu	ıll-high resistance	RPU	(300		ΚΩ
Input terminal pu	ıll-low resistance	RPD	-(///	300	^ -	ΚΩ
Source output	Graycode= 0 ~ 14 Graycode= 241 ~ 255	Sdev1	40	, ,	-	mV
level deviation	Graycode= 15 ~ 31 Graycode= 208 ~ 240	Sdev2	30))	mV
	Graycode= 32 ~ 207	Sdev3	25	(C)	-	mV
Source output	Graycode= 0 ~ 14 Graycode= 241 ~ 255	Sdev4	40		-	mV
offset deviation	Graycode= 15 ~ 31 Graycode= 208 ~ 240	Sdev5	30	_	-	mV
	Graycode= 32 ~ 207	Sdev6	25	•	-	mV
Current	Normal mode ⁽²⁾	lvdd		17.6	-	mΑ
consumption	Standby mode	lvdd	O) -	1.1	-	mA
Rush current ⁽¹⁾	47	lvddpeak	<i>-</i>	60	-	mA
VPP operation c	urrent	I _{VRP}	-	-	8	mA

Note: (1) IC internal only, excluded PFM circuit's peak current of VCI (2) Condition: 800RGBx1280 white pattern

12.4 MIPI DC electrical characteristics

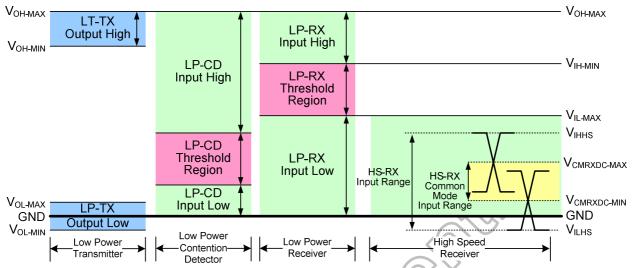


Figure 12.1: MIPI signaling and contention voltage levels

DC characteristics for MIPI LP mode

Parameter	Symbol		Spec.		Unit
raidilielei	Symbol	Min.	Тур.	Max.	Offic
Logic 1 input voltage	V _{IH}	880	~ (3)	-	mV
Logic 0 input voltage	V _{IL}	0	5) -	550	mV
Logic 1 output voltage	V _{OH}	7) 1,1	1.2	1.3	V
Logic 0 output voltage	V _{OL}	-50	•	50	mV

DC characteristics for MIPI HS mode

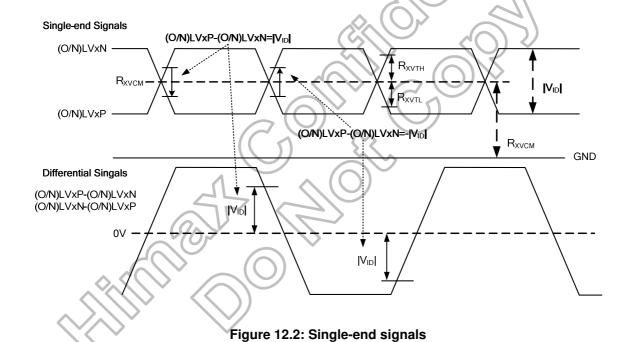
Parameter	Symbol		Spec.		Unit
Faranietei	Syllibol	Min.	Тур.	Max.	Offic
Common-mode voltage HS Receive mode	V _{CMRXDC}	70	-	330	mV
Differential input high threshold	V_{IDTH}	-	-	70	mV
Differential input low threshold	V_{IDTL}	70	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Differential input impedance	Z_{ID}	80	100	125	Ω
HS transmit differential voltage (VDP-VDN)	VOD	140	200	270	mV

Note: (1) V_{IDTH} and V_{IDTL} only for reference, related to power and ground noise, this spec need to check on panel performance to fine tune



12.5 LVDS mode DC electrical characteristics

Parameter	Symbol		Spec.		Unit	Condition
Farameter	Syllibol	Min.	Тур.	Max.	Offic	Condition
Differential input high threshold voltage	R _{XVTH}	+0.1	-	-	٧	R _{XVCM} =1.2V
Differential input low threshold voltage	R _{XVTL}	-	-	-0.1	٧	
Input voltage range (singled-end)	R _{XVIN}	0	-	VDD-1.2+ V _{ID} /2	٧	-
Differential input common Mode voltage	R _{XVCM}	V _{ID} /2	-	VDD-1.2	V	-
Differential input voltage	V _{ID}	0.2	-	0.6	V	(0,\\\-
Differential input leakage Current	RV_{Xliz}	-10	-	+10	μА	- ·
LVDS digital operating current	lddlvds	-	15	30	mA	Fclk=65MHz, VDD=3.3V
LVDS digital stand-by current	Istlvds	•	10	50	μA	Clock & all Functions are stopped



13. AC Characteristics

13.1 MIPI AC characteristics

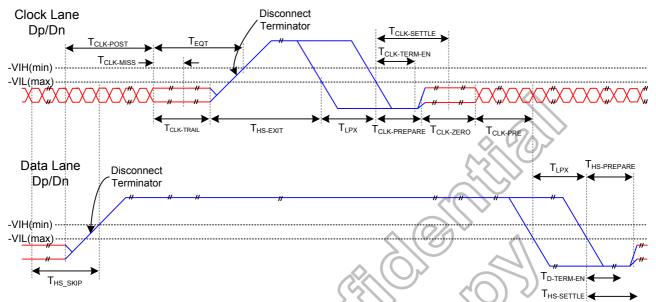


Figure 13.1: Switching the clock lane between clock transmission and low-power mode

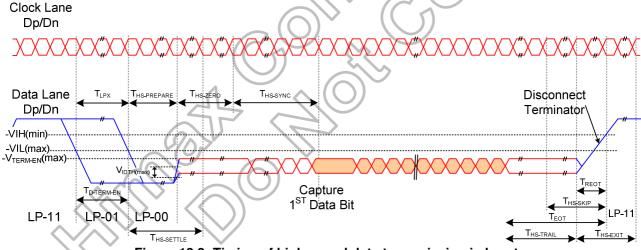


Figure 13.2: Timing of high-speed data transmission in bursts



MIPI AC Characteristics

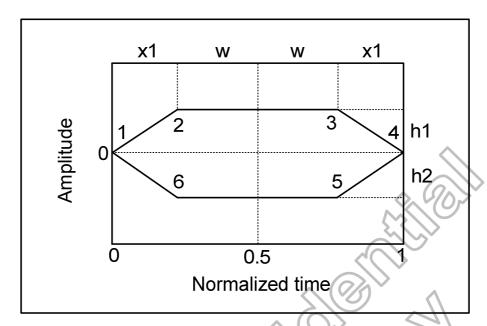
Parameter	Doggrintion		Spec.		Unit
Parameter	Description	Min	Тур	Max	Ollit
T _{REOT}	30%-85% rise time and fall time	-	-	35	ns
T _{CLK-MISS}	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
T _{CLK-POST} *1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of T _{CLK-TRAIL} .	60 ns + 52*Ul (For DCS)	-		ns
T _{CLK-PRE}	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8		0,7	ns
T _{CLK-SETTLE}	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{\text{CLK-PRE}}$.	95	> -	300	ns
T _{CLK-TERM-EN}	Dn crosses V _{IL,MAX} .	Time for Dn to reach V _{TERM-EN}	SW	38	ns
T _{HS-SETTLE}	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of T _{HSPREPARE} .	85 ns + 6*UI		145 ns + 10*UI	ns
T _{EOT}	Time from start of $T_{\text{HS-TRAIL}}$ or $T_{\text{CLK-TRAIL}}$ period to start of LP-11 state	20	-	105ns+48*UI	-
T _{HS-EXIT} ⁽¹⁾	time to drive LP-11 after HS burst	100	-	-	ns
T _{HS-PREPARE}	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
T _{HS-PREPARE} + T _{HS-ZERO}	T _{HS-PREPARE} + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-		ns
T _{HS-SKIP}	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
T _{HS-TRAIL}	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T _{LPX}	Ratio of T _{LPX(MASTER)} /T _{LPS(SLAVE)} between Master and Slave side	2/3	-	3/2	-
T _{TA-GET}	Time to drive LP-00 by new TX		5*T _{LPX}		ns
T _{TA-GO}	Time to drive LP-00 after Turnaround Request		4*T _{LPX}		ns
T _{TA-SURE}	Time-out before new TX side starts driving	T _{LPX}	-	2*T _{LPX}	ns

Note: (1) For image transmission:

 $T_{\text{CLK-POST}}$ min value =164 when MIPI max frequency per lane = 0.53Gbps. $T_{\text{CLK-POST}}$ min value =112 when MIPI max frequency per lane = 1Gbps



13.2 MIPI data-clock timing specification



Symbol	Time (UI)	Voltage
1	0	0
2	0.2	+70mV (Min.)
3	0.8	+70mV (Min.)
4	1	0
5	0.8	-70mV (Min.)
6	0.2	-70mV (Min.)
x1	0.2	-
W	0.3	-
h1	\ \(\lambda\)	+70mV (Min.)
h2	5 ~ [[0]	-70mV (Min.)

13.3 LVDS mode AC electrical characteristics

Parameter	Symbol		Spec.		Unit	Condition
Farameter	Syllibol	Min.	Тур.	Max.	Offic	Condition
Clock frequency	R _{XFCLK}	20	-	85	MHz	-
Input data skew margin	T _{RSKM}	500	-	-	pS	V _{ID} =400mV R _{XVCM} =1.2V R _{XFCLK} =71MHz
Clock high time	T _{LVCH}	1	4/(7* R _{XFCLK})	ı	ns	-
Clock low time	T _{LVCL}	1	3/(7* R _{XFCLK})	ı	ns	-
PLL wake-up time	T _{emPLL}	-	-	150	μs	-

Table 13.1: LVDS mode AC electrical characteristics

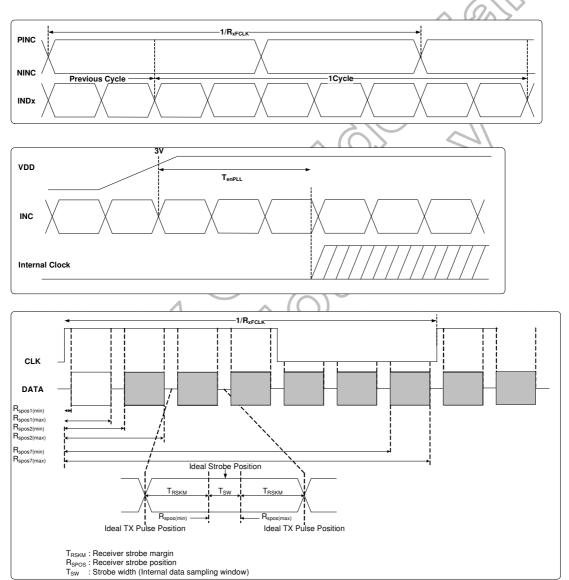


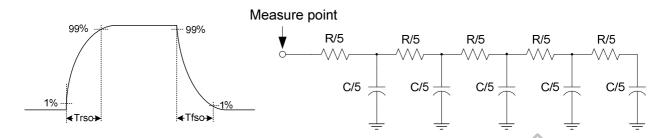
Figure 13.3: LVDS figure

Parameter	Symbol		Spec.		Unit	Condition
Faranietei	Syllibol	Min.	Тур.	Max.	Offic	Condition
Modulation frequency	SSC_{MF}	23	-	93	KHz	-
Modulation rate	SSC _{MR}	-	-	±3	%	LVDS clock =71MHz center spread

Table 13.2: SSC table



13.4 Source output timing (SOUT1 ~ SOUT2400, SL1, SR1)

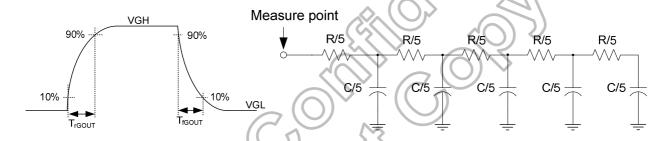


Parameter	Symbol	Condition		Spec.		Unit
Farameter	Syllibol	Condition	Min.	Тур.	Max.	Offic
Source driver rising time	trSO	R=6.3kohm, C=105.2pF	X	/ <u>(</u> 0)	3.01	μs
Source driver falling time	tfSO	t=0.5k01 11,	-5.7		4.2	μs

Note: (1) Himax can support simulation for customer design.

Table 13.3: Source output timing

Panel control signal output 1(GOUT1_L~GOUT16_L, GOUT1_R~GOUT16_R)



Parameter	Symbol	Condition		Spec.		Unit
Farameter	Syllibol	Condition	Min.	Тур.	Max.	Oilit
Panel control signal rising time	T_{rGOUT}	R=4.42kohm, C=156pF	-	-	1.74	μs
Panel control signal falling time	T_{fGOUT}	11=4.42K011111, U=130p1	-	-	1.3	μs

Note: (1) Himax can support simulation for customer design.

Table 13.4: GOA output timing

13.5 Serial interface characteristics

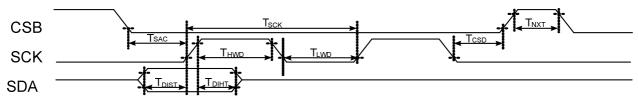


Figure 13.4: Serial interface characteristics

(VDDIO=1.65V~3.6V, VSS=0V, T_A=-20℃~+85℃)

Parameter	Symbol	Condition		Spec.		Unit
Farameter	Syllibol	Condition	Min.	Тур.	Max.	Oill
CSB assertion to first clock edge	T_{SAC}	-	120	2	<i>'UK</i> -	ns
CSB deassertion frome last clock edge	T _{CSD}	ı	120	(>)//	-	ns
CSB next control enable	T_E	ı	200	7-6	-	ns
SCK period time	T _{SCK}	ı	200	11-	-	ns
SCK high period time	T_{HWD}	ı	100	\ <u>\</u>	-	ns
SCK low period time	T_LWD	-	100	V -	-	ns
SDA input data setup time	T_{DIST}	-	50	- (-	ns
SDA input data hold time	T_{DIHT}	- ((50	-	-	ns

Table 13.5: AC characteristic of SPI interface





13.6 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

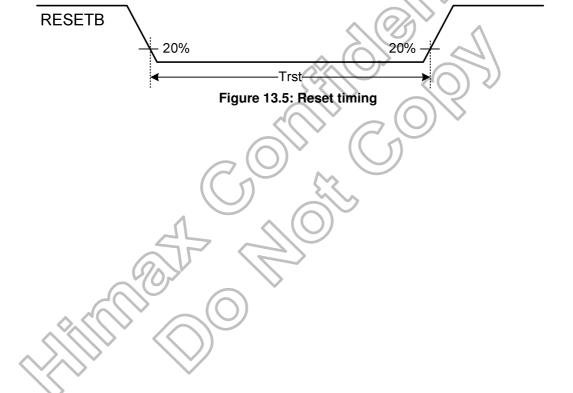
However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(VDDIO=1.65V \sim 3.6V, VSS=0V, T_A =-20 $^{\circ}$ \sim +85 $^{\circ}$)

Parameter	Symbol	Condition		Spec.		Unit
Parameter	Syllibol	Condition		Тур.	Max.	Uill
Reset low pulse width	Trst	-	20	\$? - \ >	-	μs

Table 13.6: Reset timing



Himax

14. Pin Assignment (IC Face View)

14.1 PAD sequence

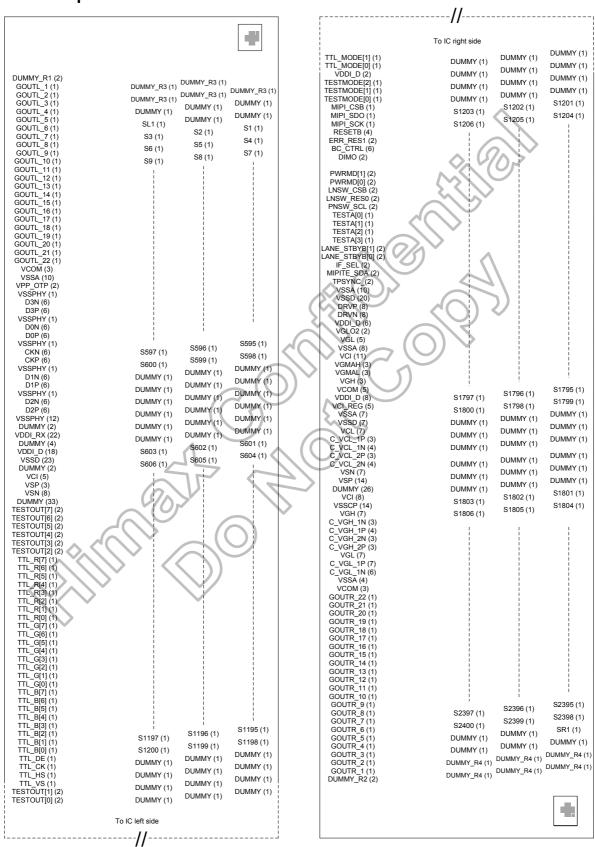
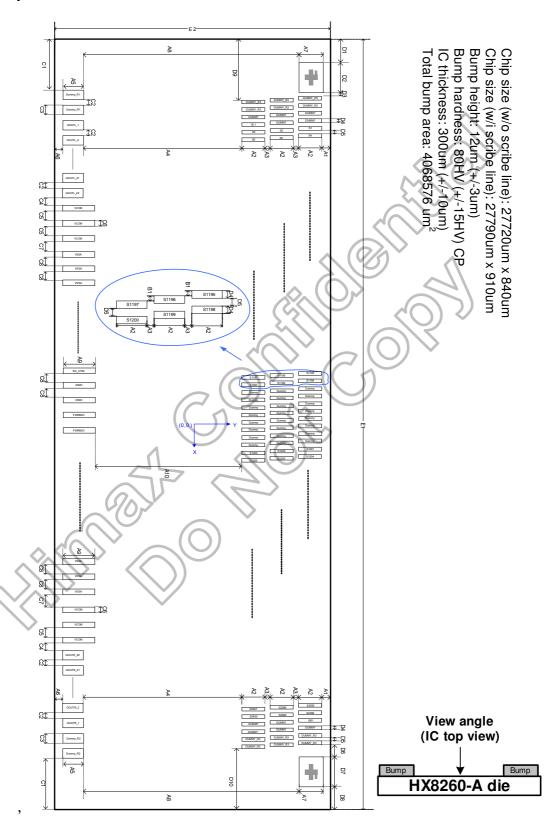


Figure 14.1: Pad sequence



14.2 Bump information

14.2.1 Chip outline dimension





14.2.2 Pad information

Symbol	Dimension (µm)	Symbol	Dimension (µm)	Symbol	Dimension (μm)	Symbol	Dimension (μm)	Symbol	Dimension (µm)
A1	9	B1	11	C1	177.5	D1	104	E1	27720
A2	73	-	1	C2	15	D2	89.5	E2	840
А3	17	-	ı	C3	30	D3	6.1	-	-
A4	519	-	-	C4	20	D4	16	-	-
A5	50	-	-	C5	25	D5	17	-	-
A6	9	-	-	C6	20	D6	17.6	-	-
A7	78	-	-	C7	35	D7	100	(-	-
A8	697	-	-	C8	25	D8	104	1-1	-
A9	100	-	1	-	ı	D9	221.6	7.\-	-
A10	469	-		-	ı	D10	199.6	<u> </u>	-

Table 14.1: Pad information

14.2.3 Alignment mark

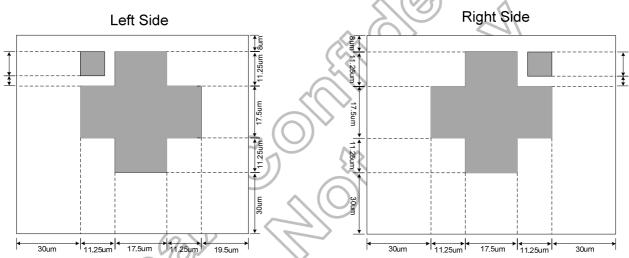


Figure 14.2: Alignment mark





14.3 Pad coordinates

No.	Name	Х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)
1	DUMMY_R1	-13667.5	-386	30X50	81	D1N	-10057.5	-361	20X100	161	VDDI_D	-6457.5	-361	20X100
2	DUMMY_R1	-13622.5	-386	30X50	82	D1N	-10012.5	-361	20X100	162	VDDI_D	-6412.5	-361	20X100
3	GOUTL_1	-13577.5	-386	30X50	83	D1N	-9967.5	-361	20X100	163	VSSD	-6367.5	-361	20X100
4	GOUTL_2	-13532.5	-386	30X50	84	D1N	-9922.5	-361	20X100	164	VSSD	-6322.5	-361	20X100
5 6	GOUTL_3 GOUTL 4	-13487.5 -13442.5	-386 -386	30X50 30X50	85 86	D1N D1P	-9877.5 -9832.5	-361 -361	20X100 20X100	165 166	VSSD VSSD	-6277.5 -6232.5	-361 -361	20X100 20X100
7	GOUTL 5	-13397.5	-386	30X50	87	D1P	-9787.5	-361	20X100	167	VSSD	-6187.5	-361	20X100
8	GOUTL 6	-13352.5	-386	30X50	88	D1P	-9742.5	-361	20X100	168	VSSD	-6142.5	-361	20X100
9	GOUTL_7	-13307.5	-386	30X50	89	D1P	-9697.5	-361	20X100	169	VSSD	-6097.5	-361	20X100
10	GOUTL_8	-13262.5	-386	30X50	90	D1P	-9652.5	-361	20X100	170	VSSD	-6052.5	-361	20X100
11 12	GOUTL_9 GOUTL 10	-13217.5 -13172.5	-386 -386	30X50 30X50	91 92	D1P VSSPHY	-9607.5 -9562.5	-361 -361	20X100 20X100	171 172	VSSD VSSD	-6007.5 -5962.5	-361 -361	20X100 20X100
13	GOUTL_10	-13172.5	-386	30X50	93	D2N	-9502.5	-361	20X100 20X100	173	VSSD	-5917.5	-361	20X100
14	GOUTL 12	-13082.5	-386	30X50	94	D2N	-9472.5	-361	20X100	174	VSSD	-5872.5	-361	20X100
15	GOUTL_13	-13037.5	-386	30X50	95	D2N	-9427.5	-361	20X100	175	VSSD	-5827.5	-361	20X100
16	GOUTL_14	-12992.5	-386	30X50	96	D2N	-9382.5	-361	20X100	176	VSSD	-5782.5	-361	20X100
17	GOUTL_15	-12947.5	-386	30X50	97	D2N	-9337.5	-361	20X100	177	VSSD	-5737.5	-361	20X100
18 19	GOUTL_16 GOUTL 17	-12902.5 -12857.5	-386 -386	30X50 30X50	98 99	D2N D2P	-9292.5 -9247.5	-361 -361	20X100 20X100	178 179	VSSD VSSD	-5692.5 -5647.5	-361 -361	20X100 20X100
20	GOUTL 18	-12812.5	-386	30X50	100	D2P	-9202.5	-361	20X100	180	VSSD	-5602.5	-361	20X100
21	GOUTL_19	-12767.5	-386	30X50	101	D2P	-9157.5	-361	20X100	181	VSSD	-5557.5	-361	20X100
22	GOUTL_20	-12722.5	-386	30X50	102	D2P	-9112.5	-361	20X100	182	VSSD	-5512.5	-361	20X100
23	GOUTL_21	-12677.5	-386	30X50	103	D2P	-9067.5	-361	20X100	183	VSSD	-5467.5	-361	20X100
24	GOUTL_22	-12632.5	-386	30X50 20X100	104	D2P	-9022.5 -8977.5	-361	20X100	184	VSSD	-5422.5	-361	20X100
25 26	VCOM	-12587.5 -12542.5	-361 -361	20X100 20X100	105 106	VSSPHY VSSPHY	-8977.5	-361 -361	20X100 20X100	185 186	VSSD DUMMY	-5377.5 -5332.5	-361 -361	20X100 20X100
27	VCOM	-12497.5	-361	20X100	107	VSSPHY	-8887.5	-361	20X100	187	DUMMY	-5287.5	-361	20X100
28	VSSA	-12442.5	-361	20X100	108	VSSPHY	-8842.5	-361	20X100	188	VCI	-5242.5	-361	20X100
29	VSSA	-12397.5	-361	20X100	109	VSSPHY	-8797.5	-361	20X100	189	ACI	-5197.5	-361	20X100
30	VSSA	-12352.5	-361	20X100	110	VSSPHY	-8752.5	-361	20X100	190	VCI	-5152.5	-361	20X100
31 32	VSSA VSSA	-12307.5	-361	20X100	111	VSSPHY VSSPHY	-8707.5 -8662.5	-361	20X100 20X100	191 192	VCI VCI	-5107.5 -5062.5	-361 -361	20X100
33	VSSA	-12262.5 -12217.5	-361 -361	20X100 20X100	113	VSSPHY	-8617.5	-361 -361	20X100 20X100	192	VSP	-5062.5	-361	20X100 20X100
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35	VSSA	-12127.5	-361	20X100	115	VSSPHY	-8527.5	-361	20X100	195	VSP	-4927.5	-361	20X100
36	VSSA	-12082.5	-361	20X100	116	VSSPHY	-8482.5	-361	20X100	196	VSN	-4882.5	-361	20X100
37	VSSA	-12037.5	-361	20X100	117	DUMMY	-8437.5	-361	20X100	197	VSN	-4837.5	-361	20X100
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40	VSSPHY	-11947.5	-361	20X100 20X100	120	VDDI_RX	-8302.5	-361	20X100	200	VSN	-4747.5	-361	20X100
41	D3N	-11857.5	-361	20X100	121	VDDI RX	-8257.5	-361	20X100	201	VSN	-4657.5	-361	20X100
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45 46	D3N D3N	-11677.5 -11632.5	-361 -361	20X100 20X100	125 126	VDDI_RX VDDI_RX	-8077.5 -8032.5	-361 -361	20X100 20X100	205 206	DUMMY DUMMY	-4477.5 -4432.5	-361 -361	20X100 20X100
47	D3P	-11587.5	-361	20X100	127	VDDI_RX	-7987.5	-361	20X100	207	DUMMY	-4387.5	-361	20X100
48	D3P	-11542.5	-361	20X100	128	VDDI_RX	-7942.5	-361	20X100	208	DUMMY	-4342.5	-361	20X100
49	D3P	-11497.5	-361	20X100	129	VDDI_RX	-7897.5	-361	20X100	209	DUMMY	-4297.5	-361	20X100
50	D3P	-11452.5	-361	20X100	130	VDDI_RX	-7852.5	-361	20X100	210	DUMMY	-4252.5	-361	20X100
51 52	D3P D3P	-11407.5 -11362.5	-361 -361	20X100 20X100	131	VDDI_RX VDDI_RX	-7807.5 -7762.5	-361 -361	20X100 20X100	211	DUMMY DUMMY	-4207.5 -4162.5	-361 -361	20X100 20X100
53	VSSPHY	-11317.5	-361	20X100	133	VDDI_RX	-7717.5	-361	20X100 20X100	213	DUMMY	-4117.5	-361	20X100
54	DON	-11272.5	-361	20X100	134	VDDI RX	-7672.5	-361	20X100	214	DUMMY	-4072.5	-361	20X100
55	D0N	-11227.5	-361	20X100	135	VDDI_RX	-7627.5	-361	20X100	215	DUMMY	-4027.5	-361	20X100
56	D0N	-11182.5	-361	20X100	136	VDDI_RX	-7582.5	-361	20X100	216	DUMMY	-3982.5	-361	20X100
57 58	D0N D0N	-11137.5 -11092.5	-361 -361	20X100 20X100	137	VDDI_RX VDDI_RX	-7537.5 -7492.5	-361 -361	20X100 20X100	217 218	DUMMY DUMMY	-3937.5 -3892.5	-361 -361	20X100 20X100
58 59	DON DON	-11092.5	-361 -361	20X100 20X100	138	VDDI_RX VDDI_RX	-7492.5 -7447.5	-361 -361	20X100 20X100	218	DUMMY	-3892.5 -3847.5	-361 -361	20X100 20X100
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61	D0P	-10957.5	-361	20X100	141	DUMMY	-7357.5	-361	20X100	221	DUMMY	-3757.5	-361	20X100
62	D0P	-10912.5	-361	20X100	142	DUMMY	-7312.5	-361	20X100	222	DUMMY	-3712.5	-361	20X100
63	D0P	-10867.5	-361	20X100	143	DUMMY	-7267.5	-361	20X100	223	DUMMY	-3667.5	-361	20X100
64	D0P	-10822.5	-361	20X100	144	DUMMY VDDI D	-7222.5	-361	20X100	224	DUMMY	-3622.5	-361	20X100
65 66	D0P VSSPHY	-10777.5 -10732.5	-361 -361	20X100 20X100	145 146	VDDI_D VDDI_D	-7177.5 -7132.5	-361 -361	20X100 20X100	225 226	DUMMY DUMMY	-3577.5 -3532.5	-361 -361	20X100 20X100
67	CKN	-10687.5	-361	20X100	147	VDDI D	-7087.5	-361	20X100	227	DUMMY	-3487.5	-361	20X100
68	CKN	-10642.5	-361	20X100	148	VDDI_D	-7042.5	-361	20X100	228	DUMMY	-3442.5	-361	20X100
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70	CKN	-10552.5	-361	20X100	150	VDDI_D	-6952.5	-361	20X100	230	DUMMY	-3352.5	-361	20X100
71 72	CKN CKN	-10507.5 -10462.5	-361 -361	20X100 20X100	151 152	VDDI_D VDDI_D	-6907.5 -6862.5	-361 -361	20X100 20X100	231	DUMMY DUMMY	-3307.5 -3262.5	-361 -361	20X100 20X100
73	CKN	-10462.5	-361	20X100 20X100	153	VDDI_D	-6862.5	-361	20X100 20X100	232	DUMMY	-3262.5	-361	20X100 20X100
74	CKP	-10417.5	-361	20X100	154	VDDI_D	-6772.5	-361	20X100	234	DUMMY	-3172.5	-361	20X100
75	CKP	-10327.5	-361	20X100	155	VDDI_D	-6727.5	-361	20X100	235	TESTOUT7	-3127.5	-361	20X100
76	CKP	-10282.5	-361	20X100	156	VDDI_D	-6682.5	-361	20X100	236	TESTOUT7	-3082.5	-361	20X100
77	CKP	-10237.5	-361	20X100	157	VDDI_D	-6637.5	-361	20X100	237	TESTOUT6	-3037.5	-361	20X100
78 79	CKP VSSPHY	-10192.5	-361 -361	20X100 20X100	158 159	VDDI_D VDDI_D	-6592.5 -6547.5	-361 -361	20X100	238	TESTOUT6 TESTOUT5	-2992.5 -2947.5	-361 -361	20X100 20X100
80	D1N	-10147.5 -10102.5	-361	20X100 20X100	160	VDDI_D	-6547.5 -6502.5	-361	20X100 20X100	239	TESTOUTS	-2947.5	-361	20X100 20X100
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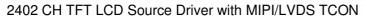


241 242 243 244 245 246 247 248 249 250	TESTOUT4 TESTOUT4 TESTOUT3 TESTOUT3 TESTOUT2 TESTOUT2	-2857.5 -2812.5 -2767.5	-361 -361	size(μm) 20X100	321	LANGO DIOTO			size(µm)					size(µm)
242 243 244 245 246 247 248 249 250	TESTOUT4 TESTOUT3 TESTOUT3 TESTOUT2 TESTOUT2	-2767.5	-361			LANE0 BISTB	742.5	-361	20X100	401	VCI	4342.5	-361	20X100
244 245 246 247 248 249 250	TESTOUT3 TESTOUT2 TESTOUT2			20X100	322	LANE0_BISTB	787.5	-361	20X100	402	VCI	4387.5	-361	20X100
245 246 247 248 249 250	TESTOUT2 TESTOUT2		-361	20X100	323	IF_SEL	832.5	-361	20X100	403	VCI	4432.5	-361	20X100
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247 248 249 250		-2677.5 -2632.5	-361 -361	20X100 20X100	325 326	MIPITE_SDA MIPITE SDA	922.5 967.5	-361 -361	20X100 20X100	405 406	VCI VCI	4522.5 4567.5	-361 -361	20X100 20X100
248 249 250	TTL R7	-2587.5	-361	20X100	327	TPSYNC	1012.5	-361	20X100	406	VGMAH	4612.5	-361	20X100
249 250	TTL R6	-2542.5	-361	20X100	328	TPSYNC	1057.5	-361	20X100	408	VGMAH	4657.5	-361	20X100
	TTL_R5	-2497.5	-361	20X100	329	VSSA	1102.5	-361	20X100	409	VGMAH	4702.5	-361	20X100
	TTL_R4	-2452.5	-361	20X100	330	VSSA	1147.5	-361	20X100	410	VGMAL	4747.5	-361	20X100
251	TTL_R3	-2407.5	-361	20X100	331	VSSA	1192.5	-361	20X100	411	VGMAL	4792.5	-361	20X100
252 253	TTL_R2 TTL_R1	-2362.5 -2317.5	-361 -361	20X100 20X100	332 333	VSSA VSSA	1237.5 1282.5	-361 -361	20X100 20X100	412 413	VGMAL VGH	4837.5 4882.5	-361 -361	20X100 20X100
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258 259	TTL_G6 TTL G5	-2092.5 -2047.5	-361 -361	20X100 20X100	338	VSSA VSSD	1507.5 1552.5	-361 -361	20X100 20X100	418 419	VCOM	5107.5 5152.5	-361 -361	20X100 20X100
260	TTL G4	-2047.5	-361	20X100	340	VSSD	1597.5	-361	20X100	420	VCOM	5197.5	-361	20X100
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262	TTL_G2	-1912.5	-361	20X100	342	VSSD	1687.5	-361	20X100	422	VDDI_D	5287.5	-361	20X100
263	TTL_G1	-1867.5	-361	20X100	343	VSSD	1732.5	-361	20X100	423	VDDI_D	5332.5	-361	20X100
264	TTL_G0	-1822.5	-361	20X100	344	VSSD	1777.5	-361	20X100	424	VDDI_D	5377.5	-361	20X100
265 266	TTL_B7 TTL_B6	-1777.5 -1732.5	-361 -361	20X100 20X100	345 346	VSSD VSSD	1822.5 1867.5	-361 -361	20X100 20X100	425 426	VDDI_D VDDI_D	5422.5 5467.5	-361 -361	20X100 20X100
267	TTL B5	-1/32.5	-361	20X100 20X100	346	VSSD	1912.5	-361	20X100	426	VDDI_D	5512.5	-361	20X100 20X100
268	TTL B4	-1642.5	-361	20X100	348	VSSD	1957.5	-361	20X100	428	VDDI_D	5557.5	-361	20X100
269	TTL_B3	-1597.5	-361	20X100	349	VSSD	2002.5	-361	20X100	429	VCI_REG	5602.5	-361	20X100
270	TTL_B2	-1552.5	-361	20X100	350	VSSD	2047.5	-361	20X100	430	VCI_REG	5647.5	-361	20X100
271	TTL_B1	-1507.5	-361	20X100	351	VSSD	2092.5	-361	20X100	431	VCI_REG	5692.5	-361	20X100
272 273	TTL_B0 TTL_DE	-1462.5	-361 -361	20X100 20X100	352 353	VSSD VSSD	2137.5	-361 -361	20X100 20X100	432 433	VCI_REG VCI_REG	5737.5	-361 -361	20X100 20X100
274	TTL_DE	-1417.5 -1372.5	-361	20X100 20X100	353	VSSD	2182.5 2227.5	-361	20X100 20X100	434	VSSA VSSA	5782.5 5827.5	-361	20X100 20X100
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276	TTL_VS	-1282.5	-361	20X100	356	VSSD	2317.5	-361	20X100	436	VSSA	5917.5	-361	20X100
277	TESTOUT1	-1237.5	-361	20X100	357	VSSD	2362.5	-361	20X100	437	VSSA	5962.5	-361	20X100
278	TESTOUT1	-1192.5	-361	20X100	358	VSSD	2407.5	-361	20X100	438	VSSA	6007.5	-361	20X100
279 280	TESTOUT0 TESTOUT0	-1147.5 -1102.5	-361 -361	20X100 20X100	359 360	DRVP DRVP	2452.5 2497.5	-361 -361	20X100 20X100	439 440	VSSA VSSA	6052.5 6097.5	-361 -361	20X100 20X100
281	TTL MODE1	-1102.5	-361	20X100	361	DRVP	2542.5	-361	20X100	441	VSSD	6142.5	-361	20X100 20X100
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285	TESTMODE2	-877.5	-361	20X100	365	DRVP	2722.5	-361	20X100	445	VSSD	6322.5	-361	20X100
286 287	TESTMODE1 TESTMODE0	-832.5 -787.5	-361 -361	20X100 20X100	366 367	DRVP DRVN	2767.5 2812.5	-361 -361	20X100 20X100	446 447	VSSD VSSD	6367.5 6412.5	-361 -361	20X100 20X100
288	MIPI CSB	-742.5	-361	20X100	368	DRVN	2857.5	-361	20X100	448	VCL	6457.5	-361	20X100
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291	RESETB	-607.5	-361	20X100	371	DRVN	2992.5	-361	20X100	451	VCL	6592.5	-361	20X100
292	RESETB	-562.5 -517.5	-361 -361	20X100	372 373	DRVN DRVN	3037.5	-361 -361	20X100	452	VCL VCL	6637.5	-361	20X100 20X100
293 294	RESETB RESETB	-317.5 -472.5	-361	20X100 20X100	373	DRVN	3082.5 3127.5	-361	20X100 20X100	453 454	VCL	6682.5 6727.5	-361 -361	20X100 20X100
295	ERR RES1	-427.5	-361	20X100	375	VDDI D	3172.5	-361	20X100	455	C VCL 1P	6772.5	-361	20X100
296	ERR_RES1	-382.5	-361	20X100	376	VDDI_D	3217.5	-361	20X100	456	C_VCL_1P	6817.5	-361	20X100
297	BC_CTRL	-337.5	-361	20X100	377	VDDI_D	3262.5	-361	20X100	457	C_VCL_1P	6862.5	-361	20X100
298	BC_CTRL	-292.5	-361	20X100	378	VDDI_D	3307.5	-361	20X100	458	C_VCL_1N	6907.5	-361	20X100
299 300	BC_CTRL BC_CTRL	-247.5 -202.5	-361 -361	20X100 20X100	379 380	VDDI_D VDDI_D	3352.5 3397.5	-361 -361	20X100 20X100	459 460	C_VCL_1N C_VCL_1N	6952.5 6997.5	-361 -361	20X100 20X100
300	BC_CTRL	-202.5 -157.5	-361	20X100	380	VGLO2	3442.5	-361	20X100 20X100	461	C VCL_IN	7042.5	-361	20X100 20X100
302	BC_CTRL	-112.5	-361	20X100	382	VGLO2	3487.5	-361	20X100	462	C_VCL_2P	7087.5	-361	20X100
303	DIMO	-67.5	-361	20X100	383	VGL	3532.5	-361	20X100	463	C_VCL_2P	7132.5	-361	20X100
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305	PWRMD1	22.5	-361	20X100	385	VGL	3622.5	-361	20X100	465	C_VCL_2N	7222.5	-361	20X100
306 307	PWRMD1 PWRMD0	67.5	-361	20X100 20X100	386	VGL VGL	3667.5 3712.5	-361	20X100 20X100	466 467	C_VCL_2N C_VCL_2N	7267.5 7312.5	-361	20X100 20X100
307	PWRMD0	112.5 157.5	-361 -361	20X100 20X100	387 388	VGL VSSA	3712.5	-361 -361	20X100 20X100	467	C VCL_2N	7312.5	-361 -361	20X100 20X100
309	LNSW CSB	202.5	-361	20X100	389	VSSA	3802.5	-361	20X100	469	VSN	7402.5	-361	20X100
310	LNSW_CSB	247.5	-361	20X100	390	VSSA	3847.5	-361	20X100	470	VSN	7447.5	-361	20X100
311	LNSW_RES0	292.5	-361	20X100	391	VSSA	3892.5	-361	20X100	471	VSN	7492.5	-361	20X100
312	LNSW_RES0	337.5	-361	20X100	392	VSSA	3937.5	-361	20X100	472	VSN	7537.5	-361	20X100
313	PNSW_SCL	382.5	-361	20X100	393	VSSRC	3982.5	-361	20X100	473	VSN	7582.5	-361	20X100
314 315	PNSW_SCL TESTA0	427.5 472.5	-361 -361	20X100 20X100	394 395	VSSRC VSSRC	4027.5 4072.5	-361 -361	20X100 20X100	474 475	VSN VSN	7627.5 7672.5	-361 -361	20X100 20X100
316	TESTA1	517.5	-361	20X100	396	VSSNC	4117.5	-361	20X100	476	VSP	7717.5	-361	20X100 20X100
317	TESTA2	562.5	-361	20X100	397	VCI	4162.5	-361	20X100	477	VSP	7762.5	-361	20X100
318	TESTA3	607.5	-361	20X100	398	VCI	4207.5	-361	20X100	478	VSP	7807.5	-361	20X100
	LANE1_STBYB	652.5	-361	20X100	399	VCI	4252.5	-361	20X100	479	VSP	7852.5	-361	20X100
320 I	LANE1_STBYB	697.5	-361	20X100	400	VCI	4297.5	-361	20X100	480	VSP	7897.5	-361	20X100



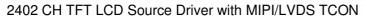


No.	Name	х	Υ	Bump	No.	Name	х	Υ	Bump	No.	Name	х	Υ	Bump
				size(µm)					size(µm)					size(µm)
481	VSP VSP	7942.5	-361	20X100	561	VGL	11542.5	-361	20X100	641	S2380	13304.5	374.5	16X73
482 483	VSP	7987.5 8032.5	-361 -361	20X100 20X100	562 563	VGL VGL	11587.5 11632.5	-361 -361	20X100 20X100	642 643	S2379 S2378	13293.5 13282.5	194.5 284.5	16X73 16X73
484	VSP	8077.5	-361	20X100	564	VGL	11677.5	-361	20X100	644	S2377	13271.5	374.5	16X73
485	VSP	8122.5	-361	20X100	565	C_VGL_1P	11722.5	-361	20X100	645	S2376	13260.5	194.5	16X73
486	VSP	8167.5	-361	20X100	566	C_VGL_1P	11767.5	-361	20X100	646	S2375	13249.5	284.5	16X73
487 488	VSP VSP	8212.5 8257.5	-361 -361	20X100 20X100	567 568	C_VGL_1P C VGL 1P	11812.5 11857.5	-361 -361	20X100 20X100	647 648	S2374	13238.5 13227.5	374.5 194.5	16X73 16X73
489	VSP	8302.5	-361	20X100 20X100	569	C VGL_IP	11902.5	-361	20X100 20X100	649	S2373 S2372	13227.5	284.5	16X73
490	DUMMY	8347.5	-361	20X100	570	C VGL 1P	11947.5	-361	20X100	650	S2371	13205.5	374.5	16X73
491	DUMMY	8392.5	-361	20X100	571	C_VGL_1P	11992.5	-361	20X100	651	S2370	13194.5	194.5	16X73
492	DUMMY	8437.5	-361	20X100	572	C_VGL_1N	12037.5	-361	20X100	652	S2369	13183.5	284.5	16X73
493 494	DUMMY DUMMY	8482.5 8527.5	-361 -361	20X100 20X100	573 574	C_VGL_1N C_VGL_1N	12082.5 12127.5	-361 -361	20X100 20X100	653 654	S2368 S2367	13172.5 13161.5	374.5 194.5	16X73 16X73
494	DUMMY	8572.5	-361	20X100	575	C VGL 1N	12172.5	-361	20X100 20X100	655	S2366	13150.5	284.5	16X73
496	DUMMY	8617.5	-361	20X100	576	C_VGL_1N	12217.5	-361	20X100	656	S2365	13139.5	374.5	16X73
497	DUMMY	8662.5	-361	20X100	577	C_VGL_1N	12262.5	-361	20X100	657	S2364	13128.5	194.5	16X73
498	DUMMY	8707.5	-361	20X100	578	VSSA	12307.5	-361	20X100	658	S2363	13117.5	284.5	16X73
499 500	DUMMY DUMMY	8752.5 8797.5	-361 -361	20X100 20X100	579 580	VSSA VSSA	12352.5 12397.5	-361 -361	20X100 20X100	659 660	S2362 S2361	13106.5 13095.5	374.5 194.5	16X73 16X73
501	DUMMY	8842.5	-361	20X100	581	VSSA	12442.5	-361	20X100	661	S2360	13084.5	284.5	16X73
502	DUMMY	8887.5	-361	20X100	582	VCOM	12497.5	-361	20X100	662	S2359	13073.5	374.5	16X73
503	DUMMY	8932.5	-361	20X100	583	VCOM	12542.5	-361	20X100	663	S2358	13062.5	194.5	16X73
504	DUMMY	8977.5	-361	20X100	584	VCOM	12587.5	-361	20X100	664	S2357	13051.5	284.5	16X73
505 506	DUMMY DUMMY	9022.5 9067.5	-361 -361	20X100 20X100	585 586	GOUTR_22 GOUTR 21	12632.5 12677.5	-386 -386	30X50 30X50	665 666	S2356 S2355	13040.5 13029.5	374.5 194.5	16X73 16X73
507	DUMMY	9112.5	-361	20X100	587	GOUTR 20	12722.5	-386	30X50	667	S2354	13018.5	284.5	16X73
508	DUMMY	9157.5	-361	20X100	588	GOUTR_19	12767.5	-386	30X50	668	S2353	13007.5	374.5	16X73
509	DUMMY	9202.5	-361	20X100	589	GOUTR_18	12812.5	-386	30X50	669	S2352	12996.5	194.5	16X73
510	DUMMY	9247.5	-361	20X100	590	GOUTR_17	12857.5	-386	30X50	670	S2351	12985.5	284.5	16X73
511 512	DUMMY DUMMY	9292.5 9337.5	-361 -361	20X100 20X100	591 592	GOUTR_16 GOUTR 15	12902.5 12947.5	-386 -386	30X50 30X50	671 672	S2350 S2349	12974.5 12963.5	374.5 194.5	16X73 16X73
513	DUMMY	9382.5	-361	20X100	593	GOUTR 14	12992.5	-386	30X50	673	S2348	12952.5	284.5	16X73
514	DUMMY	9427.5	-361	20X100	594	GOUTR_13	13037.5	-386	30X50	674	S2347	12941.5	374.5	16X73
515	DUMMY	9472.5	-361	20X100	595	GOUTR_12	13082.5	-386	30X50	675	S2346	12930.5	194.5	16X73
516	VCI	9517.5	-361	20X100	596	GOUTR_11	13127.5	-386	30X50	676	\$2345	12919.5	284.5	16X73
517 518	VCI VCI	9562.5 9607.5	-361 -361	20X100 20X100	597 598	GOUTR_10 GOUTR 9	13172.5 13217.5	-386 -386	30X50 30X50	677 678	S2344 S2343	12908.5 12897.5	374.5 194.5	16X73 16X73
519	VCI	9652.5	-361	20X100	599	GOUTR 8	13262.5	-386	30X50	679	S2342	12886.5	284.5	16X73
520	VCI	9697.5	-361	20X100	600	GOUTR_7	13307.5	-386	30X50	680	S2341	12875.5	374.5	16X73
521	VCI	9742.5	-361	20X100	601	GOUTR_6	13352.5	-386	30X50	681	S2340	12864.5	194.5	16X73
522 523	VCI VCI	9787.5 9832.5	-361 -361	20X100 20X100	602	GOUTR_5 GOUTR 4	13397.5 13442.5	-386 -386	30X50 30X50	682 683	S2339 S2338	12853.5 12842.5	284.5 374.5	16X73 16X73
524	VSSCP	9877.5	-361	20X100	604	GOUTR 3	13487.5	-386	30X50	684	S2337	12831.5	194.5	16X73
525	VSSCP	9922.5	-361	20X100	605	GOUTR_2	13532.5	-386	30X50	685	S2336	12820.5	284.5	16X73
526	VSSCP	9967.5	-361	20X100	606	GOUTR_1	13577.5	-386	30X50	686	S2335	12809.5	374.5	16X73
527	VSSCP	10012.5	-361	20X100	607	DUMMY_R2	13622.5	-386	30X50	687	S2334	12798.5	194.5	16X73
528 529	VSSCP VSSCP	10057.5 10102.5	-361 -361	20X100 20X100	608	DUMMY_R2 DUMMY_R4	13667.5 13656.5	-386 194.5	30X50 16X73	688 689	S2333 S2332	12787.5 12776.5	284.5 374.5	16X73 16X73
530	VSSCP	10147.5	-361	20X100	610	DUMMY R4	13645.5	284.5	16X73	690	S2331	12765.5	194.5	16X73
531	VSSCP	10192.5	-361	20X100	611	DUMMY_R4	13634.5	374.5	16X73	691	S2330	12754.5	284.5	16X73
532	VSSCP	10237.5	-361	20X100	612	DUMMY_R4	13623.5	194.5	16X73	692	S2329	12743.5	374.5	16X73
533 534	VSSCP VSSCP	10282.5 10327.5	-361 -361	20X100 20X100	613 614	DUMMY_R4 DUMMY_R4	13612.5 13601.5	284.5 374.5	16X73 16X73	693 694	S2328 S2327	12732.5 12721.5	194.5 284.5	16X73 16X73
535	VSSCP	10327.5	-361	20X100	615	DUMMY DUMMY	13590.5	194.5	16X73	695	S2326	12710.5	374.5	16X73
536	VSSCP	10417.5	-361	20X100	616	DUMMY	13579.5	284.5	16X73	696	S2325	12699.5	194.5	16X73
537	VSSCP	10462.5	-361	20X100	617	DUMMY	13568.5	374.5	16X73	697	S2324	12688.5	284.5	16X73
538	VGH	10507.5	-361	20X100	618	DUMMY	13557.5	194.5	16X73	698	S2323	12677.5	374.5	16X73
539 540	VGH VGH	10552.5 10597.5	-361 -361	20X100 20X100	619 620	SR1	13546.5 13535.5	284.5 374.5	16X73 16X73	699 700	S2322 S2321	12666.5 12655.5	194.5 284.5	16X73 16X73
541	VGH	10642.5	-361	20X100	621	S2400	13524.5	194.5	16X73	700	S2320	12633.3	374.5	16X73
542	VGH	10687.5	-361	20X100	622	S2399	13513.5	284.5	16X73	702	S2319	12633.5	194.5	16X73
543	VGH	10732.5	-361	20X100	623	S2398	13502.5	374.5	16X73	703	S2318	12622.5	284.5	16X73
544	VGH	10777.5	-361	20X100	624	S2397	13491.5	194.5	16X73	704	S2317	12611.5	374.5	16X73
545 546	C_VGH_1N C_VGH_1N	10822.5 10867.5	-361 -361	20X100 20X100	625 626	S2396 S2395	13480.5 13469.5	284.5 374.5	16X73 16X73	705 706	S2316 S2315	12600.5 12589.5	194.5 284.5	16X73 16X73
547	C VGH 1N	10912.5	-361	20X100	627	S2394	13458.5	194.5	16X73	707	S2314	12578.5	374.5	16X73
548	C_VGH_1P	10957.5	-361	20X100	628	S2393	13447.5	284.5	16X73	708	S2313	12567.5	194.5	16X73
549	C_VGH_1P	11002.5	-361	20X100	629	S2392	13436.5	374.5	16X73	709	S2312	12556.5	284.5	16X73
550 551	C_VGH_1P C_VGH_1P	11047.5	-361 -361	20X100 20X100	630	S2391 S2390	13425.5	194.5	16X73	710	S2311	12545.5	374.5 194.5	16X73 16X73
551	C_VGH_1P C_VGH_2N	11092.5 11137.5	-361 -361	20X100 20X100	631 632	S2390 S2389	13414.5 13403.5	284.5 374.5	16X73 16X73	711 712	S2310 S2309	12534.5 12523.5	194.5 284.5	16X/3 16X73
553	C_VGH_2N	11182.5	-361	20X100	633	S2388	13392.5	194.5	16X73	713	S2308	12512.5	374.5	16X73
554	C_VGH_2N	11227.5	-361	20X100	634	S2387	13381.5	284.5	16X73	714	S2307	12501.5	194.5	16X73
555	C_VGH_2P	11272.5	-361	20X100	635	S2386	13370.5	374.5	16X73	715	S2306	12490.5	284.5	16X73
556 557	C_VGH_2P	11317.5	-361	20X100 20X100	636	S2385 S2384	13359.5	194.5	16X73	716 717	S2305 S2304	12479.5	374.5	16X73
557	C_VGH_2P VGL	11362.5 11407.5	-361 -361	20X100 20X100	637 638	S2384 S2383	13348.5 13337.5	284.5 374.5	16X73 16X73	717	S2304 S2303	12468.5 12457.5	194.5 284.5	16X73 16X73
559	VGL	11452.5	-361	20X100	639	S2382	13326.5	194.5	16X73	719	S2302	12446.5	374.5	16X73
560	VGL	11497.5	-361	20X100	640	S2381	13315.5	284.5	16X73	720	S2301	12435.5	194.5	16X73



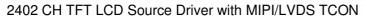


122 1220 1221 1	No.	Name	Х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)
222 22298 124625 1445 16672 1693 22215 11525 7745 16672 1683 35718 106425 28445 16673 7755 22297 129125 2845 16673 1683 28297 11525 2745 16673 28298 18998 18998 28445 18978 28458 18998 18998 189	721	S2300	12424.5	284.5		801	S2220	11544.5	194.5		881	S2140	10664.5	374.5	
\$\frac{1}{2}\$ \$\frac{1}{2}															
Texas 1988															
1.00	726	S2295	12369.5	194.5	16X73	806	S2215	11489.5	374.5	16X73	886	S2135	10609.5	284.5	16X73
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200 20214 20225 204.5 107.73 810 502211 11446.5 104.5 106.73 800 \$52131 1066.6 104.5 104.73 107.7															
S2290 12914 6 374.5 1073 811 S2210 1144.5 284.5 1073 881 S2190 10654.5 184.5 1073 1072 2293 1293.5 1294.5 1073 1294.5 1073 1294.5 1073 1294.5 1294.5 1073 1294.5 1294.5 1073 1294.5 1294.5 1073 1294.5 1294.5 1073 1294.5 1294.5 1073 1294.5 129															
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757 S2264 12026.5 284.5 16X73 837 S2184 11/138.6 194.5 16X73 91 2620.2 11/7 S21.6 S21.7 S21.6 S21.7 S21.6 11/7 S21.6															
758 \$2262 12017.5 374.5 16X73 838 \$2183 4173.6 294.5 16X73 919 \$2102 10264.5 284.5 16X73 760 \$22261 11196.5 284.5 16X73 840 \$2181 11115.6 194.5 16X73 919 \$2101 10264.5 284.5 16X73 761 \$22261 11945.5 1847.3 841 \$2180 11903.5 374.5 16X73 762 \$22258 11915.5 174.5 16X73 842 \$2179 11093.5 374.5 16X73 764 \$22256 11940.5 194.5 16X73 844 \$2177 11071.5 284.5 16X73 922 \$2099 10213.5 284.5 16X73 766 \$22256 11945.5 1873.3 844 \$2177 11091.5 194.5 16X73 922 \$2099 10191.5 194.5 16X73 766 \$22256 1194.5 16X73 846															
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	800	S2221	11555.5	374.5	16X73	880	S2141	10675.5	284.5	16X73	960	S2061	9795.5	194.5	16X73





No.	Name	х	Υ	Bump size(µm)	No.	Name	х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)
961	S2060	9784.5	284.5	16X73	1041	S1980	8904.5	194.5	16X73	1121	S1900	8024.5	374.5	16X73
962	S2059	9773.5	374.5	16X73	1042	S1979	8893.5	284.5	16X73	1122	S1899	8013.5	194.5	16X73
963	S2058	9762.5	194.5	16X73	1043	S1978	8882.5	374.5	16X73	1123	S1898	8002.5	284.5	16X73
964	S2057	9751.5	284.5	16X73	1044	S1977	8871.5	194.5	16X73	1124	S1897	7991.5	374.5	16X73
965 966	S2056 S2055	9740.5 9729.5	374.5 194.5	16X73 16X73	1045	S1976 S1975	8860.5 8849.5	284.5 374.5	16X73 16X73	1125 1126	S1896 S1895	7980.5 7969.5	194.5 284.5	16X73 16X73
967	S2054	9718.5	284.5	16X73	1047	S1973	8838.5	194.5	16X73	1127	S1894	7958.5	374.5	16X73
968	S2053	9707.5	374.5	16X73	1048	S1973	8827.5	284.5	16X73	1128	S1893	7947.5	194.5	16X73
969	S2052	9696.5	194.5	16X73	1049	S1972	8816.5	374.5	16X73	1129	S1892	7936.5	284.5	16X73
970	S2051	9685.5	284.5	16X73	1050	S1971	8805.5	194.5	16X73	1130	S1891	7925.5	374.5	16X73
971 972	S2050 S2049	9674.5 9663.5	374.5 194.5	16X73 16X73	1051 1052	S1970 S1969	8794.5 8783.5	284.5 374.5	16X73 16X73	1131	S1890 S1889	7914.5 7903.5	194.5 284.5	16X73 16X73
973	S2048	9652.5	284.5	16X73	1053	S1968	8772.5	194.5	16X73	1133	S1888	7892.5	374.5	16X73
974	S2047	9641.5	374.5	16X73	1054	S1967	8761.5	284.5	16X73	1134	S1887	7881.5	194.5	16X73
975	S2046	9630.5	194.5	16X73	1055	S1966	8750.5	374.5	16X73	1135	S1886	7870.5	284.5	16X73
976 977	S2045 S2044	9619.5	284.5 374.5	16X73 16X73	1056 1057	S1965	8739.5 8728.5	194.5	16X73 16X73	1136	S1885 S1884	7859.5 7848.5	374.5 194.5	16X73
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979	S2042	9586.5	284.5	16X73	1059	S1962	8706.5	194.5	16X73	1139	S1882	7826.5	374.5	16X73
980	S2041	9575.5	374.5	16X73	1060	S1961	8695.5	284.5	16X73	1140	S1881	7815.5	194.5	16X73
981	S2040	9564.5	194.5	16X73	1061	S1960	8684.5	374.5	16X73	1141	S1880	7804.5	284.5	16X73
982	S2039	9553.5	284.5	16X73	1062	S1959	8673.5	194.5	16X73	1142	S1879	7793.5	374.5	16X73
983 984	S2038 S2037	9542.5 9531.5	374.5 194.5	16X73 16X73	1063 1064	S1958 S1957	8662.5 8651.5	284.5 374.5	16X73 16X73	1143	S1878 S1877	7782.5 7771.5	194.5 284.5	16X73 16X73
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994 995	S2027 S2026	9421.5 9410.5	284.5 374.5	16X73 16X73	1074 1075	S1947 S1946	8541.5 8530.5	194.5 284.5	16X73 16X73	1154 1155	S1867 S1866	7661.5 7650.5	374.5 194.5	16X73 16X73
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1007	S2014	9278.5	374.5	16X73	1087	S1934	8398.5	284.5	16X73	1167	S1854	7518.5	194.5	16X73
1008	S2013	9267.5	194.5	16X73	1088	S1933	8387.5	374.5	16X73	1168	S1853	7507.5	284.5	16X73
1009	S2012	9256.5	284.5	16X73	1089	S1932	8376.5	194.5	16X73	1169	S1852	7496.5	374.5	16X73
1010 1011	S2011 S2010	9245.5 9234.5	374.5 194.5	16X73 16X73	1090	S1931 S1930	8365.5 8354.5	284.5 374.5	16X73 16X73	1170 1171	S1851 S1850	7485.5 7474.5	194.5 284.5	16X73 16X73
1012	S2009	9223.5	284.5	16X73	1092	S1929	8343.5	194.5	16X73	1172	S1849	7463.5	374.5	16X73
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1040	S1981	8915.5	374.5	16X73	1120	S1901	8035.5	284.5	16X73	1200	S1821	7155.5	194.5	16X73
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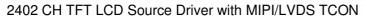


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1222 DUMMY 6913.5 284.5 16X73 1302 S1737 6033.5 194.5 16X73 1382 S1657 1223 DUMMY 6902.5 374.5 16X73 1303 S1736 6022.5 284.5 16X73 1383 S1656 1224 DUMMY 6891.5 194.5 16X73 1304 S1735 6011.5 374.5 16X73 1384 S1655 1225 DUMMY 6890.5 284.5 16X73 1305 S1734 6000.5 194.5 16X73 1386 S1654 1226 DUMMY 6890.5 284.5 16X73 1306 S1733 5990.5 284.5 16X73 1386 S1653 1227 DUMMY 6895.5 194.5 16X73 1306 S1733 5998.5 284.5 16X73 1386 S1653 1227 DUMMY 6887.5 284.5 16X73 1306 S1731 5967.5 194.5 16X73 1388 S1656 1228 DUMMY 6887.5 284.5 16X73 1308 S1731 5967.5 194.5 16X78 1388 S1651 1229 DUMMY 6836.5 374.5 16X73 1309 S1730 5966.5 284.5 16X78 1389 S1660 1230 DUMMY 682.5 194.5 16X73 1310 S1729 5945.5 374.5 16X73 1399 S1660 1230 DUMMY 6803.5 374.5 16X73 1311 S1728 5934.5 194.5 16X73 1399 S1649 1232 DUMMY 6803.5 374.5 16X73 1312 S1727 5923.5 284.5 16X73 1391 S1648 1232 DUMMY 6781.5 284.5 16X73 1313 S1726 5912.5 374.5 16X73 1392 S1647 1234 DUMMY 6770.5 374.5 16X73 1315 S1724 5890.5 284.5 16X73 1399 S1646 1236 DUMMY 6781.5 284.5 16X73 1316 S1723 5879.5 374.5 16X73 1399 S1646 1236 DUMMY 6787.5 284.5 16X73 1316 S1723 5879.5 374.5 16X73 1399 S1644 1236 DUMMY 678.5 284.5 16X73 1316 S1723 5890.5 284.5 16X73 1399 S1644 1236 DUMMY 6781.5 284.5 16X73 1316 S1723 5890.5 284.5 16X73 1399 S1644 1236 DUMMY 6785.5 284.5 16X73 1316 S1723 5890.5 284.5 16X73 1399 S1640 1239 S1800 6726.5 194.5 16X73 1316 S1723 5890.5 284.5 16X73 1399 S1640 1239 S1800 6726.5 194.5 16X73 1318 S1721 5867.5 284.5 16X73 1399 S1640 1399 S1640 S1799 6615.5 284.5 16X73 132	5164.5	284.5	16X73
1223 DUMMY 6890.5 374.5 16X73 1303 S1736 6022.5 284.5 16X73 1384 S1656 1225 DUMMY 6880.5 194.5 16X73 1304 S1735 6011.5 374.5 16X73 1384 S1655 1226 DUMMY 6880.5 284.5 16X73 1306 S1733 5989.5 284.5 16X73 1386 S1653 1227 DUMMY 6897.5 284.5 16X73 1307 S1732 5976.5 374.5 16X73 1388 S1651 1228 DUMMY 6897.5 284.5 16X73 1309 S1730 5956.5 284.5 16X73 1388 S1651 1230 DUMMY 6825.5 194.5 16X73 1310 S1729 5945.5 374.5 16X73 1390 S1649 1231 DUMMY 6804.5 284.5 16X73 1311 S1728 5934.5 194.5 16X73 1391 S1648 1233 DUMMY 6893.5 374.5 16X73 1312 S1727 5923.5 284.5 16X73 1391 S1648 1233 DUMMY 6792.5 194.5 16X73 1314 S1725 5901.5 194.5 16X73 1394 S1645 1235 DUMMY 6792.5 194.5 16X73 1314 S1725 5901.5 194.5 16X73 1394 S1646 1235 DUMMY 6795.5 194.5 16X73 1315 S1724 5990.5 284.5 16X73 1394 S1645 1236 DUMMY 6795.5 194.5 16X73 1315 S1724 5990.5 284.5 16X73 1394 S1646 1236 DUMMY 6795.5 194.5 16X73 1316 S1722 5868.5 194.5 16X73 1396 S1644 1236 DUMMY 6795.5 194.5 16X73 1316 S1722 5868.5 194.5 16X73 1396 S1644 1236 DUMMY 6795.5 194.5 16X73 1316 S1721 5879.5 374.5 16X73 1396 S1644 1236 DUMMY 6795.5 194.5 16X73 1316 S1721 5879.5 374.5 16X73 1396 S1644 1236 DUMMY 6795.5 194.5 16X73 1316 S1721 5879.5 374.5 16X73 1396 S1644 1236 DUMMY 6795.5 194.5 16X73 1316 S1721 5879.5 574.5 16X73 1396 S1644 1236 DUMMY 6795.5 194.5 16X73 1316 S1721 5879.5 574.5 16X73 1396 S1644 1236 DUMMY 6795.5 194.5 16X73 1326 S1718 5879.5 574.5 16X73 1400 S1639 1244 S1798 6695.5	5153.5	374.5	16X73
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1226 DUMMY 6869.5 374.5 16X73 1306 S1733 5989.5 284.5 16X73 1386 S1653 1227 DUMMY 6847.5 284.5 16X73 1308 S1731 5967.5 134.5 16X73 1388 S1651 1229 DUMMY 6847.5 284.5 16X73 1308 S1731 5967.5 134.5 16X73 1388 S1651 1229 DUMMY 6836.5 374.5 16X73 1309 S1730 5956.5 284.5 16X73 1389 S1650 1230 DUMMY 6814.5 284.5 16X73 1310 S1729 5945.5 374.5 16X73 1399 S1649 1232 DUMMY 6814.5 284.5 16X73 1311 S1728 S934.5 194.5 16X73 1391 S1648 1232 DUMMY 6792.5 194.5 16X73 1312 S1727 5923.5 284.5 16X73 1392 S1647 1233 DUMMY 6781.5 284.5 16X73 1314 S1725 5991.5 5912.5 374.5 16X73 1393 S1648 1234 DUMMY 6781.5 284.5 16X73 1315 S1724 5890.5 284.5 16X73 1395 S1644 1236 DUMMY 6759.5 194.5 16X73 1316 S1723 5879.5 374.5 16X73 1395 S1644 1239 DUMMY 6781.5 284.5 16X73 1316 S1723 5879.5 374.5 16X73 1395 S1644 1239 S1800 6726.5 194.5 16X73 1318 S1721 5865.5 284.5 16X73 1396 S1641 1239 S1800 6726.5 194.5 16X73 1318 S1721 5865.5 284.5 16X73 1398 S1641 1240 S1799 6715.5 284.5 16X73 1322 S1718 5824.5 16X73 1398 S1641 1242 S1797 6693.5 194.5 16X73 1322 S1718 5824.5 16X73 1401 S1638 1242 S1797 6693.5 194.5 16X73 1322 S1718 5824.5 16X73 1401 S1638 1242 S1794 6660.5 194.5 16X73 1324 S1716 5805.5 374.5 16X73 1324 S1716 5805.5 374.5 16X73 1404 S1635 1248 S1794 6660.5 194.5 16X73 1324 S1716 5805.5 374.5 16X73 1404 S1635 1248 S1791 6627.5 194.5 16X73 1324 S1716 5780.5 374.5 16X73 1404 S1635 1248 S1794 6660.5 194.5 16X73 1324 S1716 5780.5 374.5 16X73 1406 S1633 1248 S1794 6660.5 194.5 16X73 1324 S1716 5780.5 374.5 16X73 1406 S1633 1248 S1791 6627.5	5131.5	284.5	16X73
1227 DUMMY 6858.5 194.5 16X73 1307 S1732 5978.5 374.5 16X73 1388 S1652 1228 DUMMY 6847.5 284.5 16X73 1308 S1731 5967.5 194.5 16X73 1389 S1650 1230 DUMMY 6825.5 194.5 16X73 1310 S1729 5945.5 374.5 16X73 1399 S1649 1231 DUMMY 6814.5 284.5 16X73 1311 S1728 5934.5 194.5 16X73 1391 S1648 1322 DUMMY 6792.5 194.5 16X73 1312 S1727 5923.5 284.5 16X73 1391 S1648 13234 DUMMY 6781.5 284.5 16X73 1313 S1726 5912.5 374.5 16X73 1393 S1646 13235 DUMMY 6781.5 284.5 16X73 1314 S1725 5901.5 194.5 16X73 1393 S1646 13236 DUMMY 6795.5 194.5 16X73 1316 S1723 5879.5 374.5 16X73 1394 S1645 13237 DUMMY 6781.5 284.5 16X73 1316 S1723 5879.5 374.5 16X73 1394 S1645 13237 DUMMY 6781.5 284.5 16X73 1316 S1723 5879.5 374.5 16X73 1394 S1645 13238 DUMMY 6737.5 374.5 16X73 1316 S1723 5879.5 374.5 16X73 1396 S1644 13239 S1800 6726.5 194.5 16X73 1318 S1721 5857.5 284.5 16X73 1398 S1641 1324 S1799 6715.5 284.5 16X73 1322 S1719 5835.5 194.5 16X73 1398 S1640 1324 S1799 6688.5 294.5 16X73 1322 S1719 5835.5 194.5 16X73 1400 S1639 1444 S1795 6671.5 374.5 16X73 1322 S1716 5802.5 194.5 16X73 1400 S1639 1244 S1795 6671.5 374.5 16X73 1322 S1716 5802.5 194.5 16X73 1402 S1637 1245 S1794 6660.5 194.5 16X73 1326 S1714 5780.5 374.5 16X73 1405 S1634 1404 S1635 1244 S1795 6638.5 374.5 16X73 1326 S1714 5780.5 374.5 16X73 1405 S1634 1404 S1635 1248 S1791 6627.5 194.5 16X73 1328 S1716 5802.5 194.5 16X73 1405 S1634 1405 S1634 1404 S1635 1406 S1633 1406	5120.5	374.5	16X73
1228 DUMMY 6847.5 284.5 16X73 1308 S1731 5967.5 194.5 16X73 1398 S1651 1229 DUMMY 6836.5 374.5 16X73 1310 S1729 594.5 374.5 16X73 1310 S1729 594.5 374.5 16X73 1390 S1649 1311 S1728 S934.5 194.5 16X73 1391 S1648 1392 S1649 1311 S1728 S934.5 194.5 16X73 1391 S1648 1392 S1649 1311 S1728 S934.5 194.5 16X73 1392 S1647 1312 S1727 S923.5 284.5 16X73 1392 S1647 1312 S1727 S923.5 284.5 16X73 1392 S1647 1314 S1725 S901.5 194.5 16X73 1392 S1647 1314 S1725 S901.5 194.5 16X73 1394 S1645 1323 DUMMY 6792.5 194.5 16X73 1314 S1725 S901.5 194.5 16X73 1394 S1645 1323 DUMMY 6770.5 374.5 16X73 1315 S1724 S890.5 284.5 16X73 1394 S1645 1323 DUMMY 6779.5 194.5 16X73 1316 S1723 S879.5 374.5 16X73 1395 S1644 13238 DUMMY 6737.5 374.5 16X73 1318 S1722 S686.5 194.5 16X73 1396 S1643 1397 S1642 13239 S1800 6726.5 194.5 16X73 1318 S1721 S857.5 284.5 16X73 1398 S1641 1329 S1800 6726.5 194.5 16X73 1318 S1721 S857.5 284.5 16X73 1398 S1641 1324 S1798 6704.5 374.5 16X73 1322 S1719 S835.5 194.5 16X73 1398 S1641 1324 S1796 6682.5 284.5 16X73 1322 S1717 S813.5 374.5 16X73 1400 S1639 1424 S1795 6671.5 374.5 16X73 1322 S1716 5802.5 194.5 16X73 1402 S1637 1245 S1794 6660.5 194.5 16X73 1324 S1715 5791.5 284.5 16X73 1404 S1635 1424 S1795 6671.5 374.5 16X73 1324 S1716 5780.5 374.5 16X73 1405 S1634 1404 S1635 1424 S1795 6671.5 374.5 16X73 1324 S1716 5780.5 374.5 16X73 1404 S1638 1424 S1795 6671.5 374.5 16X73 1324 S1716 5780.5 374.5 16X73 1404 S1636 1424 S1795 6671.5 374.5 16X73 1324 S1716 5780.5 374.5 16X73 1406 S1633 1406 S1633 1424 S1799 6668.5	5109.5	194.5	16X73
1229 DUMMY 6836.5 374.5 16X73 1309 S1730 S956.5 284.5 16X73 1390 S1649 1391 S1648 1322 DUMMY 6814.5 284.5 16X73 1311 S1728 S934.5 194.5 16X73 1391 S1648 1322 DUMMY 6803.5 374.5 16X73 1312 S1727 S923.5 284.5 16X73 1392 S1647 1323 DUMMY 6792.5 194.5 16X73 1313 S1726 S912.5 374.5 16X73 1393 S1646 13234 DUMMY 6707.5 374.5 16X73 1314 S1725 S901.5 194.5 16X73 1394 S1645 1236 DUMMY 6770.5 374.5 16X73 1315 S1724 S890.5 284.5 16X73 1394 S1645 1236 DUMMY 6770.5 374.5 16X73 1316 S1723 S890.5 284.5 16X73 1394 S1645 1237 DUMMY 6748.5 284.5 16X73 1316 S1723 S879.5 374.5 16X73 1396 S1643 1237 DUMMY 6748.5 284.5 16X73 1317 S1722 S868.5 194.5 16X73 1398 S1641 1398 S1641 1398 S1644 1398 S1645 1399 S1644 1399 S1645 1399 S1644 139	5098.5	284.5	16X73
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1231 DUMMY 6814.5 284.5 16X73 1311 S1728 5934.5 194.5 16X73 1392 S1648 1232 DUMMY 6792.5 194.5 16X73 1312 S1726 5912.5 284.5 16X73 1392 S1647 1393 S1646 1393 1234 DUMMY 6792.5 194.5 16X73 1314 S1725 5901.5 194.5 16X73 1394 S1645 1234 DUMMY 6770.5 374.5 16X73 1314 S1725 5901.5 194.5 16X73 1394 S1645 1235 DUMMY 6770.5 374.5 16X73 1316 S1724 5890.5 284.5 16X73 1395 S1644 1392 S1647 1393 S1646 1394 S1645 1394 S1646 1394 S1647 1394 S1646 S1647 S1646 S	5076.5 5065.5	194.5 284.5	16X73 16X73
1232 DUMMY 6803.5 374.5 16X73 1312 S1727 5923.5 284.5 16X73 1392 S1647 1233 DUMMY 6792.5 194.5 16X73 1313 S1726 5912.5 374.5 16X73 1393 S1646 1393 S1647 1394 S1645 1395 S1644 1395 S1	5053.5	374.5	16X73
1233 DUMMY 679.5 194.5 16X73 1313 S1726 S912.5 374.5 16X73 1394 S1646 1234 DUMMY 6770.5 374.5 16X73 1314 S1725 S90.5 S44.5 16X73 1394 S1645 1236 DUMMY 6770.5 374.5 16X73 1316 S1724 S890.5 284.5 16X73 1395 S1644 1395 S1645 1395 S1644 1395 S1645 S16473 S1646 S16473	5043.5	194.5	16X73
1234 DUMMY 6781.5 284.5 16X73 1314 S1725 S901.5 194.5 16X73 1395 S1644 1395 S1645 S16473 S1725	5032.5	284.5	16X73
1236 DUMMY 6759.5 194.5 16X73 1316 S1723 5879.5 374.5 16X73 1396 S1643 1237 DUMMY 6748.5 284.5 16X73 1317 S1722 5868.5 194.5 16X73 1397 S1642 1338 DUMMY 6737.5 374.5 16X73 1318 S1721 5857.5 284.5 16X73 1398 S1641 1398 S1800 6726.5 194.5 16X73 1319 S1720 5846.5 374.5 16X73 1399 S1640 1319 S1720 5846.5 374.5 16X73 1399 S1640 1319 S1720 5846.5 374.5 16X73 1399 S1640 1324 S1799 6715.5 284.5 16X73 1320 S1719 5835.5 194.5 16X73 1400 S1639 1241 S1798 6704.5 374.5 16X73 1321 S1718 S824.5 284.5 16X73 1401 S1638 1242 S1797 6693.5 194.5 16X73 1322 S1717 S813.5 374.5 16X73 1401 S1638 1244 S1795 6671.5 374.5 16X73 1322 S1716 5802.5 194.5 16X73 1402 S1637 1244 S1795 6671.5 374.5 16X73 1324 S1716 5802.5 194.5 16X73 1403 S1636 1244 S1793 6649.5 284.5 16X73 1324 S1715 5791.5 284.5 16X73 1404 S1635 1246 S1793 6649.5 284.5 16X73 1326 S1714 5780.5 374.5 16X73 1406 S1633 1247 S1792 6638.5 374.5 16X73 1326 S1713 5769.5 194.5 16X73 1406 S1633 1248 S1791 6627.5 194.5 16X73 1328 S1711 5747.5 374.5 16X73 1408 S1631 1249 S1790 6616.5 284.5 16X73 1329 S1710 5736.5 194.5 16X73 1408 S1631 1249 S1790 6616.5 284.5 16X73 1329 S1710 5736.5 194.5 16X73 1409 S1630 1250 S1789 6605.5 374.5 16X73 1329 S1710 5736.5 194.5 16X73 1409 S1630 1251 S1788 6594.5 194.5 16X73 1331 S1708 5714.5 374.5 16X73 1411 S1628 1251 S1788 6594.5 194.5 16X73 1331 S1708 5714.5 374.5 16X73 1411 S1628	5021.5	374.5	16X73
1237 DUMMY 6748.5 284.5 16X73 1238 DUMMY 6737.5 374.5 16X73 1239 S1800 6726.5 194.5 16X73 1240 S1799 6715.5 284.5 16X73 1241 S1798 6704.5 374.5 16X73 1241 S1798 6704.5 374.5 16X73 1242 S1797 6693.5 194.5 16X73 1242 S1796 6682.5 194.5 16X73 1244 S1796 6682.5 284.5 16X73 1244 S1796 6682.5 284.5 16X73 1244 S1796 6682.5 284.5 16X73 1245 S1794 6660.5 194.5 16X73 1245 S1794 6660.5 194.5 16X73 1246 S1794 6660.5 194.5 16X73 1246 S1794 6660.5 194.5 16X73 1246	5010.5	194.5	16X73
1238 DUMMY 6737.5 374.5 16X73 1318 S1721 5857.5 284.5 16X73 1398 S1641 1239 S1800 6726.5 194.5 16X73 1319 S1720 5846.5 374.5 16X73 1399 S1640 1240 S1798 6704.5 374.5 16X73 1320 S1718 5824.5 16X73 1400 S1639 1241 S1798 6704.5 374.5 16X73 1321 S1718 5824.5 284.5 16X73 1400 S1639 1242 S1797 6693.5 194.5 16X73 1322 S1717 5813.5 374.5 16X73 1401 S1638 1244 S1796 6682.5 284.5 16X73 1322 S1717 5813.5 374.5 16X73 1402 S1637 1244 S1795 6671.5 374.5 16X73 1324 S1716 5802.5 194.5	4999.5	284.5	16X73
1239 \$1800 6726.5 194.5 16X73 1319 \$1720 \$5846.5 374.5 16X73 1399 \$1640 \$1739 \$1799 6715.5 284.5 16X73 1320 \$1719 \$683.5 194.5 16X73 1320 \$1719 \$683.5 194.5 16X73 1400 \$1639 . \$16273 1401 \$1639 . \$16273 1401 \$1639 . . \$16273 1401 \$1639 . . \$16273 1400 \$1639 . . \$16273 1401 \$1639 . . \$16273 1400 \$1639 . . . \$16273 1400 \$1639 . <td< td=""><td>4988.5</td><td>374.5</td><td>16X73</td></td<>	4988.5	374.5	16X73
1240 \$1799 6715.5 284.5 16X73 1320 \$1719 \$6835.5 194.5 16X73 1400 \$1639 1241 \$1798 6704.5 374.5 16X73 1321 \$1718 \$824.5 284.5 16X73 1401 \$1638 1401 \$1633 1402 \$1637 1402 \$1637 1402 \$1637 1403 \$1638 1401 \$1633 1402 \$1637 1403 \$1636 1402 \$1637 1403 \$1636 1401 \$1633 1403 \$1636 1401 \$1633 1403 \$1636	4977.5	194.5	16X73
1241 S1798 6704.5 374.5 16X73 1321 S1718 5824.5 284.5 16X73 1401 S1638 1402 S1637 1403 S1638 1402 S1637 1402 S1637 1402 S1637 1403 S1638 1403 S1638 1404 S1637 1403 S1638 1403 S1638 1404 S1634 1404 S1634 1404 S1634 1404 S1634 1404 S1634 1404 S1634	4966.5	284.5 374.5	16X73 16X73
1242 \$1797 \$6693.5 194.5 16X73 1322 \$1717 \$813.5 374.5 16X73 1402 \$1637 1243 \$1796 \$6682.5 284.5 16X73 1323 \$1716 5802.5 194.5 16X73 1403 \$1636 . 1244 \$1795 \$6661.5 374.5 16X73 1324 \$1715 5791.5 284.5 16X73 1403 \$1636 . 1246 \$1794 \$6660.5 194.5 16X73 1325 \$1714 5780.5 374.5 16X73 1404 \$1635 . 1246 \$1793 \$6649.5 284.5 16X73 1326 \$1714 5780.5 94.5 16X73 1405 \$1634 . 1247 \$1792 \$6638.5 374.5 16X73 1327 \$1712 \$758.5 284.5 16X73 1406 \$1632 1248 \$1791 \$6627.5 194.5 16X73 1328 \$1711 5747.5	4955.5 4944.5	194.5	16X73
1243 \$1796 6682.5 284.5 16X73 1323 \$1716 5802.5 194.5 16X73 1403 \$1636 1403 \$1636 1403 \$1636 1403 \$1636 1403 \$1636 1403 \$1636 1403 \$1636 1403 \$1636 1403 \$1636 1404 \$1635 1404 \$1635 1404 \$1635 1404 \$1635 1404 \$1635 1404 \$1635 1404 \$1635 1404 \$1635 1405 \$1634 1405 \$1634 1405 \$1634 1405 \$1634 1405 \$1634 1405 \$1634 1405 \$1634 1406 \$1634 1406 \$1633 1406 \$1633 1406 \$1633 1406 \$1633 1406 \$1633 1406 \$1633 1407 \$1632 1406 \$1633 1406 \$1633 1407 \$1632 1407 \$1632 1407 \$1632 1407 \$1632 1407 \$1632 1407 \$1632	4933.5	284.5	16X73
1244 \$1795 \$6671.5 \$374.5 \$16X73 \$1324 \$\$1715 \$5791.5 \$284.5 \$16X73 \$1404 \$\$1635 1245 \$1794 \$660.5 \$194.5 \$16X73 \$1325 \$\$1714 \$5780.5 \$374.5 \$16X73 \$1405 \$\$1634 \$\$1793 \$649.5 \$284.5 \$16X73 \$1326 \$\$1718 \$5769.5 \$194.5 \$16X73 \$1406 \$\$1633 \$\$16273 <	4922.5	374.5	16X73
1246 \$1793 \$6649.5 \$284.5 \$16X73 \$1326 \$1713 \$5769.5 \$194.5 \$16X73 \$1406 \$\$1633 \$1247 \$1792 \$6638.5 \$374.5 \$16X73 \$1327 \$1712 \$5759.5 \$284.5 \$16X73 \$1407 \$1632 \$1633 \$1248 \$1790 \$661.5 \$194.5 \$16X73 \$1328 \$1711 \$574.5 \$374.5 \$16X73 \$1408 \$1631 \$1633	4911.5	194.5	16X73
1247 \$1792 \$6638.5 \$374.5 \$16X73 \$1327 \$5758.5 \$284.5 \$16X73 \$1407 \$\$1632 \$1248 \$1791 \$6627.5 \$194.5 \$16X73 \$1328 \$1711 \$574.5 \$374.5 \$16X73 \$1408 \$1631 \$1632 </td <td>4900.5</td> <td>284.5</td> <td>16X73</td>	4900.5	284.5	16X73
1248 \$1791 6627.5 194.5 16X73 1328 \$1711 5747.5 374.5 16X73 1408 \$1631 1249 \$1790 6616.5 284.5 16X73 1329 \$1710 5786.5 194.5 16X73 1409 \$1630 1251 \$1789 6695.5 374.5 16X73 1330 \$1709 \$725.5 284.5 16X73 1410 \$1629 1251 \$1788 6594.5 194.5 16X73 1331 \$1708 \$714.5 374.5 16X73 1411 \$1628	4889.5	374.5	16X73
1249 \$1790 6616.5 284.5 16X73 1329 \$1710 \$5736.5 194.5 16X73 1409 \$1630 \$1250 \$1789 6605.5 374.5 16X73 1330 \$1709 \$725.5 284.5 16X73 1410 \$1629 \$1629 \$1620 <td< td=""><td>4878.5</td><td>194.5</td><td>16X73</td></td<>	4878.5	194.5	16X73
1250 S1789 6605.5 374.5 16X73 1330 S1709 5725.5 284.5 16X73 1410 S1629 1251 S1788 6594.5 194.5 16X73 1331 S1708 5714.5 374.5 16X73 1411 S1628	4867.5	284.5	16X73
1251 S1788 6594.5 194.5 16X73 1331 S1708 5714.5 374.5 16X73 1411 S1628	4856.5 4845.5	374.5 194.5	16X73 16X73
	4834.5	284.5	16X73
	4823.5	374.5	16X73
	4812.5	194.5	16X73
1254 S1785 6561.5 194.5 16X73 1334 S1705 5681.5 374.5 16X73 1414 S1625	4801.5	284.5	16X73
	4790.5	374.5	16X73
	4779.5	194.5	16X73
1050 04704 0547.5 0.0045 (0)/70 4000 04704 5007.5 404.5 40//70 4440 04004	4768.5	284.5	16X73
	4757.5	374.5	16X73
	4746.5 4735.5	194.5 284.5	16X73 16X73
	4735.5	374.5	16X73
	4713.5	194.5	16X73
	4702.5	284.5	16X73
	4691.5	374.5	16X73
1265 S1774 6440.5 374.5 16X73 1345 S1694 5560.5 284.5 16X73 1425 S1614	4680.5	194.5	16X73
	4669.5	284.5	16X73
	4658.5	374.5	16X73
	4647.5	194.5	16X73
	4636.5	284.5	16X73
	4625.5 4614.5	374.5 194.5	16X73 16X73
	4603.5	284.5	16X73
	4592.5	374.5	16X73
	4581.5	194.5	16X73
	4570.5	284.5	16X73
	4559.5	374.5	16X73
1277 S1762 6308.5 374.5 16X73 1357 S1682 5428.5 284.5 16X73 1437 S1602	4548.5	194.5	16X73
	4537.5	284.5	16X73
	4526.5	374.5	16X73
1280 S1759 6275.5 374.5 16X73 1360 S1679 5395.5 284.5 16X73 1440 S1599	4515.5	194.5	16X73



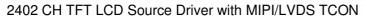


No.	Name	Х	Υ	Bump	No.	Name	х	Υ	Bump	No.	Name	Х	Υ	Bump
1441	S1598	4504.5	284.5	size(μm) 16X73	1521	S1518	3624.5	194.5	size(μm) 16X73	1601	S1438	2744.5	374.5	size(μm) 16X73
1442	S1597	4493.5	374.5	16X73	1522	S1517	3613.5	284.5	16X73	1602	S1437	2733.5	194.5	16X73
1443	S1596	4482.5	194.5	16X73	1523	S1516	3602.5	374.5	16X73	1603	S1436	2722.5	284.5	16X73
1444	S1595	4471.5	284.5	16X73	1524	S1515	3591.5	194.5	16X73	1604	S1435	2711.5	374.5	16X73
1445 1446	S1594	4460.5 4449.5	374.5 194.5	16X73	1525	S1514	3580.5 3569.5	284.5 374.5	16X73	1605	S1434	2700.5	194.5	16X73
1445	S1593 S1592	4449.5	284.5	16X73 16X73	1526 1527	S1513 S1512	3558.5	194.5	16X73 16X73	1606 1607	S1433 S1432	2689.5 2678.5	284.5 374.5	16X73 16X73
1448	S1591	4427.5	374.5	16X73	1528	S1512	3547.5	284.5	16X73	1608	S1431	2667.5	194.5	16X73
1449	S1590	4416.5	194.5	16X73	1529	S1510	3536.5	374.5	16X73	1609	S1430	2656.5	284.5	16X73
1450	S1589	4405.5	284.5	16X73	1530	S1509	3525.5	194.5	16X73	1610	S1429	2645.5	374.5	16X73
1451	S1588	4394.5	374.5	16X73	1531	S1508	3514.5	284.5	16X73	1611	S1428	2634.5	194.5	16X73
1452 1453	S1587 S1586	4383.5 4372.5	194.5 284.5	16X73 16X73	1532 1533	S1507 S1506	3503.5 3492.5	374.5 194.5	16X73 16X73	1612 1613	S1427 S1426	2623.5 2612.5	284.5 374.5	16X73 16X73
1454	S1585	4361.5	374.5	16X73	1534	S1505	3481.5	284.5	16X73	1614	S1425	2601.5	194.5	16X73
1455	S1584	4350.5	194.5	16X73	1535	S1504	3470.5	374.5	16X73	1615	S1424	2590.5	284.5	16X73
1456	S1583	4339.5	284.5	16X73	1536	S1503	3459.5	194.5	16X73	1616	S1423	2579.5	374.5	16X73
1457 1458	S1582 S1581	4328.5 4317.5	374.5 194.5	16X73 16X73	1537 1538	S1502 S1501	3448.5 3437.5	284.5 374.5	16X73 16X73	1617 1618	S1422 S1421	2568.5 2557.5	194.5 284.5	16X73 16X73
1459	S1580	4317.5	284.5	16X73	1539	S1501	3426.5	194.5	16X73	1619	S1421	2546.5	374.5	16X73
1460	S1579	4295.5	374.5	16X73	1540	S1499	3415.5	284.5	16X73	1620	S1419	2535.5	194.5	16X73
1461	S1578	4284.5	194.5	16X73	1541	S1498	3404.5	374.5	16X73	1621	S1418	2524.5	284.5	16X73
1462	S1577	4273.5	284.5	16X73	1542	S1497	3393.5	194.5	16X73	1622	S1417	2513.5	374.5	16X73
1463 1464	S1576 S1575	4262.5 4251.5	374.5 194.5	16X73 16X73	1543 1544	S1496 S1495	3382.5 3371.5	284.5 374.5	16X73 16X73	1623 1624	S1416 S1415	2502.5 2491.5	194.5 284.5	16X73 16X73
1465	S1574	4240.5	284.5	16X73	1545	S1493	3360.5	194.5	16X73	1625	S1413	2480.5	374.5	16X73
1466	S1573	4229.5	374.5	16X73	1546	S1493	3349.5	284.5	16X73	1626	S1413	2469.5	194.5	16X73
1467	S1572	4218.5	194.5	16X73	1547	S1492	3338.5	374.5	16X73	1627	S1412	2458.5	284.5	16X73
1468	S1571	4207.5	284.5	16X73	1548	S1491	3327.5	194.5	16X73	1628	S1411	2447.5	374.5	16X73
1469 1470	S1570 S1569	4196.5 4185.5	374.5 194.5	16X73 16X73	1549 1550	S1490 S1489	3316.5 3305.5	284.5 374.5	16X73 16X73	1629 1630	S1410 S1409	2436.5 2425.5	194.5 284.5	16X73 16X73
1471	S1568	4174.5	284.5	16X73	1551	S1488	3294.5	194.5	16X73	1631	S1409 S1408	2414.5	374.5	16X73
1472	S1567	4163.5	374.5	16X73	1552	S1487	3283.5	284.5	16X73	1632	S1407	2403.5	194.5	16X73
1473	S1566	4152.5	194.5	16X73	1553	S1486	3272.5	374.5	16X73	1633	S1406	2392.5	284.5	16X73
1474	S1565	4141.5	284.5	16X73	1554	S1485	3261.5	194.5	16X73	1634	S1405	2381.5	374.5	16X73
1475 1476	S1564 S1563	4130.5 4119.5	374.5 194.5	16X73 16X73	1555 1556	S1484 S1483	3250.5 3239.5	284.5 374.5	16X73 16X73	1635 1636	\$1404 \$1403	2370.5 2359.5	194.5 284.5	16X73 16X73
1477	S1562	4108.5	284.5	16X73	1557	S1482	3228.5	194.5	16X73	1637	\$1402	2348.5	374.5	16X73
1478	S1561	4097.5	374.5	16X73	1558	S1481	3217.5	284.5	16X73	1638	S1401	2337.5	194.5	16X73
1479	S1560	4086.5	194.5	16X73	1559	S1480	3206.5	374.5	16X73	1639	S1400	2326.5	284.5	16X73
1480	S1559	4075.5	284.5	16X73	1560	S1479	3195.5	194.5	16X73	1640	S1399	2315.5	374.5	16X73
1481 1482	S1558 S1557	4064.5 4053.5	374.5 194.5	16X73 16X73	1561 1562	S1478 S1477	3184.5 3173.5	284.5 374.5	16X73 16X73	1641 1642	S1398 S1397	2304.5 2293.5	194.5 284.5	16X73 16X73
1483	S1556	4042.5	284.5	16X73	1563	S1476	3162.5	194.5	16X73	1643	S1396	2282.5	374.5	16X73
1484	S1555	4031.5	374.5	16X73	1564	S1475	3151.5	284.5	16X73	1644	S1395	2271.5	194.5	16X73
1485	S1554	4020.5	194.5	16X73	1565	S1474	3140.5	374.5	16X73	1645	S1394	2260.5	284.5	16X73
1486 1487	S1553 S1552	4009.5 3998.5	284.5 374.5	16X73 16X73	1566 1567	S1473 S1472	3129.5 3118.5	194.5 284.5	16X73 16X73	1646 1647	S1393 S1392	2249.5 2238.5	374.5 194.5	16X73 16X73
1488	S1551	3987.5	194.5	16X73	1568	S1471	3107.5	374.5	16X73	1648	S1391	2227.5	284.5	16X73
1489	S1550	3976.5	284.5	16X73	1569	S1470	3096.5	194.5	16X73	1649	S1390	2216.5	374.5	16X73
1490	S1549	3965.5	374.5	16X73	1570	S1469	3085.5	284.5	16X73	1650	S1389	2205.5	194.5	16X73
1491 1492	S1548 S1547	3954.5	194.5 284.5	16X73	1571	S1468 S1467	3074.5	374.5	16X73 16X73	1651	S1388	2194.5	284.5	16X73
1492	S1547 S1546	3943.5 3932.5	374.5	16X73 16X73	1572 1573	S1467 S1466	3063.5 3052.5	194.5 284.5	16X73	1652 1653	S1387 S1386	2183.5 2172.5	374.5 194.5	16X73 16X73
1494	S1545	3921.5	194.5	16X73	1574	S1465	3041.5	374.5	16X73	1654	S1385	2161.5	284.5	16X73
1495	S1544	3910.5	284.5	16X73	1575	S1464	3030.5	194.5	16X73	1655	S1384	2150.5	374.5	16X73
1496	S1543	3899.5	374.5	16X73	1576	S1463	3019.5	284.5	16X73	1656	S1383	2139.5	194.5	16X73
1497 1498	S1542 S1541	3888.5 3877.5	194.5 284.5	16X73 16X73	1577 1578	S1462 S1461	3008.5 2997.5	374.5 194.5	16X73 16X73	1657 1658	S1382 S1381	2128.5 2117.5	284.5 374.5	16X73 16X73
1499	S1540	3866.5	374.5	16X73	1579	S1460	2986.5	284.5	16X73	1659	S1380	2106.5	194.5	16X73
1500	S1539	3855.5	194.5	16X73	1580	S1459	2975.5	374.5	16X73	1660	S1379	2095.5	284.5	16X73
1501	S1538	3844.5	284.5	16X73	1581	S1458	2964.5	194.5	16X73	1661	S1378	2084.5	374.5	16X73
1502	S1537	3833.5	374.5	16X73	1582	S1457	2953.5 2942.5	284.5	16X73	1662	S1377	2073.5	194.5	16X73
1503 1504	S1536 S1535	3822.5 3811.5	194.5 284.5	16X73 16X73	1583 1584	S1456 S1455	2942.5	374.5 194.5	16X73 16X73	1663 1664	S1376 S1375	2062.5 2051.5	284.5 374.5	16X73 16X73
1505	S1534	3800.5	374.5	16X73	1585	S1454	2920.5	284.5	16X73	1665	S1374	2040.5	194.5	16X73
1506	S1533	3789.5	194.5	16X73	1586	S1453	2909.5	374.5	16X73	1666	S1373	2029.5	284.5	16X73
1507	S1532	3778.5	284.5	16X73	1587	S1452	2898.5	194.5	16X73	1667	S1372	2018.5	374.5	16X73
1508	S1531	3767.5	374.5	16X73	1588	S1451	2887.5	284.5	16X73	1668	S1371	2007.5	194.5	16X73
1509 1510	S1530 S1529	3756.5 3745.5	194.5 284.5	16X73 16X73	1589 1590	S1450 S1449	2876.5 2865.5	374.5 194.5	16X73 16X73	1669 1670	S1370 S1369	1996.5 1985.5	284.5 374.5	16X73 16X73
1511	S1528	3734.5	374.5	16X73	1591	S1448	2854.5	284.5	16X73	1671	S1368	1974.5	194.5	16X73
1512	S1527	3723.5	194.5	16X73	1592	S1447	2843.5	374.5	16X73	1672	S1367	1963.5	284.5	16X73
1513	S1526	3712.5	284.5	16X73	1593	S1446	2832.5	194.5	16X73	1673	S1366	1952.5	374.5	16X73
1514	S1525	3701.5	374.5	16X73	1594	S1445	2821.5	284.5	16X73	1674	S1365	1941.5	194.5	16X73
1515 1516	S1524 S1523	3690.5 3679.5	194.5 284.5	16X73 16X73	1595 1596	S1444 S1443	2810.5 2799.5	374.5 194.5	16X73 16X73	1675 1676	S1364 S1363	1930.5 1919.5	284.5 374.5	16X73 16X73
1517	S1523	3668.5	374.5	16X73	1596	S1443 S1442	2788.5	284.5	16X73	1677	S1362	1908.5	194.5	16X73
1518	S1521	3657.5	194.5	16X73	1598	S1441	2777.5	374.5	16X73	1678	S1361	1897.5	284.5	16X73
1519	S1520	3646.5	284.5	16X73	1599	S1440	2766.5	194.5	16X73	1679	S1360	1886.5	374.5	16X73
1520	S1519	3635.5	374.5	16X73	1600	S1439	2755.5	284.5	16X73	1680	S1359	1875.5	194.5	16X73





No.	Name	х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)
1681	S1358	1864.5	284.5	16X73	1761	S1278	984.5	194.5	16X73	1841	DUMMY	104.5	374.5	16X73
1682	S1357	1853.5	374.5	16X73	1762	S1277	973.5	284.5	16X73	1842	DUMMY	93.5	194.5	16X73
1683	S1356	1842.5	194.5	16X73	1763	S1276	962.5	374.5	16X73	1843	DUMMY	82.5	284.5	16X73
1684	S1355	1831.5	284.5	16X73	1764	S1275	951.5	194.5	16X73	1844	DUMMY	71.5	374.5	16X73
1685 1686	S1354 S1353	1820.5 1809.5	374.5 194.5	16X73 16X73	1765 1766	S1274 S1273	940.5 929.5	284.5 374.5	16X73 16X73	1845 1846	DUMMY DUMMY	60.5 49.5	194.5 284.5	16X73 16X73
1687	S1352	1798.5	284.5	16X73	1767	S1273	918.5	194.5	16X73	1847	DUMMY	38.5	374.5	16X73
1688	S1351	1787.5	374.5	16X73	1768	S1271	907.5	284.5	16X73	1848	DUMMY	27.5	194.5	16X73
1689	S1350	1776.5	194.5	16X73	1769	S1270	896.5	374.5	16X73	1849	DUMMY	16.5	284.5	16X73
1690	S1349	1765.5	284.5	16X73	1770	S1269	885.5	194.5	16X73	1850	DUMMY	5.5	374.5	16X73
1691	S1348	1754.5	374.5	16X73	1771	S1268	874.5	284.5	16X73	1851	DUMMY	-5.5	194.5	16X73
1692 1693	S1347 S1346	1743.5 1732.5	194.5 284.5	16X73 16X73	1772 1773	S1267 S1266	863.5 852.5	374.5 194.5	16X73 16X73	1852 1853	DUMMY DUMMY	-16.5 -27.5	284.5 374.5	16X73 16X73
1694	S1345	1721.5	374.5	16X73	1774	S1265	841.5	284.5	16X73	1854	DUMMY	-38.5	194.5	16X73
1695	S1344	1710.5	194.5	16X73	1775	S1264	830.5	374.5	16X73	1855	DUMMY	-49.5	284.5	16X73
1696	S1343	1699.5	284.5	16X73	1776	S1263	819.5	194.5	16X73	1856	DUMMY	-60.5	374.5	16X73
1697	S1342	1688.5	374.5	16X73	1777	S1262	808.5	284.5	16X73	1857	DUMMY	-71.5	194.5	16X73
1698	S1341	1677.5	194.5	16X73	1778	S1261	797.5	374.5	16X73	1858	DUMMY	-82.5	284.5	16X73
1699 1700	S1340 S1339	1666.5 1655.5	284.5 374.5	16X73 16X73	1779 1780	S1260 S1259	786.5 775.5	194.5 284.5	16X73 16X73	1859 1860	DUMMY DUMMY	-93.5 -104.5	374.5 194.5	16X73 16X73
1700	S1338	1644.5	194.5	16X73	1781	S1258	764.5	374.5	16X73	1861	DUMMY	-115.5	284.5	16X73
1702	S1337	1633.5	284.5	16X73	1782	S1257	753.5	194.5	16X73	1862	DUMMY	-126.5	374.5	16X73
1703	S1336	1622.5	374.5	16X73	1783	S1256	742.5	284.5	16X73	1863	S1200	-137.5	194.5	16X73
1704	S1335	1611.5	194.5	16X73	1784	S1255	731.5	374.5	16X73	1864	S1199	-148.5	284.5	16X73
1705	S1334	1600.5	284.5	16X73	1785	S1254	720.5	194.5	16X73	1865	S1198	-159.5	374.5	16X73
1706	S1333	1589.5	374.5	16X73	1786	S1253	709.5	284.5	16X73	1866	S1197	-170.5	194.5	16X73
1707 1708	S1332 S1331	1578.5 1567.5	194.5 284.5	16X73 16X73	1787 1788	S1252 S1251	698.5 687.5	374.5 194.5	16X73 16X73	1867 1868	S1196 S1195	-181.5 -192.5	284.5 374.5	16X73 16X73
1709	S1330	1556.5	374.5	16X73	1789	S1250	676.5	284.5	16X73	1869	S1193	-203.5	194.5	16X73
1710	S1329	1545.5	194.5	16X73	1790	S1249	665.5	374.5	16X73	1870	S1193	-214.5	284.5	16X73
1711	S1328	1534.5	284.5	16X73	1791	S1248	654.5	194.5	16X73	1871	S1192	-225.5	374.5	16X73
1712	S1327	1523.5	374.5	16X73	1792	S1247	643.5	284.5	16X73	1872	S1191	-236.5	194.5	16X73
1713	S1326	1512.5	194.5	16X73	1793	S1246	632.5	374.5	16X73	1873	\$1190	-247.5	284.5	16X73
1714 1715	S1325 S1324	1501.5 1490.5	284.5 374.5	16X73 16X73	1794 1795	S1245 S1244	621.5 610.5	194.5 284.5	16X73 16X73	1874 1875	S1189 S1188	-258.5 -269.5	374.5 194.5	16X73 16X73
1716	S1323	1479.5	194.5	16X73	1796	S1243	599.5	374.5	16X73	1876	S1187	-280.5	284.5	16X73
1717	S1322	1468.5	284.5	16X73	1797	S1242	588.5	194.5	16X73	1877	S1186	-291.5	374.5	16X73
1718	S1321	1457.5	374.5	16X73	1798	S1241	577.5	284.5	16X73	1878	S1185	-302.5	194.5	16X73
1719	S1320	1446.5	194.5	16X73	1799	S1240	566.5	374.5	16X73	1879	S1184	-313.5	284.5	16X73
1720	S1319	1435.5	284.5	16X73	1800	S1239	555.5	194.5	16X73	1880	S1183	-324.5	374.5	16X73
1721 1722	S1318 S1317	1424.5 1413.5	374.5 194.5	16X73 16X73	1801	S1238 S1237	544.5 533.5	284.5 374.5	16X73 16X73	1881 1882	S1182 S1181	-335.5 -346.5	194.5 284.5	16X73 16X73
1723	S1316	1402.5	284.5	16X73	1803	S1237	522.5	194.5	16X73	1883	S1180	-357.5	374.5	16X73
1724	S1315	1391.5	374.5	16X73	1804	S1235	511.5	284.5	16X73	1884	S1179	-368.5	194.5	16X73
1725	S1314	1380.5	194.5	16X73	1805	S1234	500.5	374.5	16X73	1885	S1178	-379.5	284.5	16X73
1726	S1313	1369.5	284.5	16X73	1806	S1233	489.5	194.5	16X73	1886	S1177	-390.5	374.5	16X73
1727	S1312	1358.5	374.5	16X73	1807	S1232	478.5	284.5	16X73	1887	S1176	-401.5	194.5	16X73
1728 1729	S1311 S1310	1347.5 1336.5	194.5 284.5	16X73 16X73	1808 1809	S1231 S1230	467.5 456.5	374.5 194.5	16X73 16X73	1888 1889	S1175 S1174	-412.5 -423.5	284.5 374.5	16X73 16X73
1730	S1309	1325.5	374.5	16X73	1810	S1230	445.5	284.5	16X73	1890	S1174 S1173	-423.5	194.5	16X73
1731	S1308	1314.5	194.5	16X73	1811	S1228	434.5	374.5	16X73	1891	S1172	-445.5	284.5	16X73
1732	S1307	1303.5	284.5	16X73	1812	S1227	423.5	194.5	16X73	1892	S1171	-456.5	374.5	16X73
1733	S1306	1292.5	374.5	16X73	1813	S1226	412.5	284.5	16X73	1893	S1170	-467.5	194.5	16X73
1734	S1305	1281.5	194.5	16X73	1814	S1225	401.5	374.5	16X73	1894	S1169	-478.5	284.5	16X73
1735 1736	S1304 S1303	1270.5 1259.5	284.5 374.5	16X73 16X73	1815 1816	\$1224 \$1223	390.5 379.5	194.5 284.5	16X73 16X73	1895 1896	S1168 S1167	-489.5 -500.5	374.5 194.5	16X73 16X73
1737	S1303	1239.5	194.5	16X73	1817	\$1223 \$1222	368.5	374.5	16X73	1897	S1167 S1166	-511.5	284.5	16X73
1738	S1301	1237.5	284.5	16X73	1818	S1221	357.5	194.5	16X73	1898	S1165	-522.5	374.5	16X73
1739	S1300	1226.5	374.5	16X73	1819	S1220	346.5	284.5	16X73	1899	S1164	-533.5	194.5	16X73
1740	S1299	1215.5	194.5	16X73	1820	S1219	335.5	374.5	16X73	1900	S1163	-544.5	284.5	16X73
1741	S1298	1204.5	284.5	16X73	1821	S1218	324.5	194.5	16X73	1901	S1162	-555.5	374.5	16X73
1742 1743	S1297 S1296	1193.5 1182.5	374.5 194.5	16X73 16X73	1822 1823	S1217 S1216	313.5 302.5	284.5 374.5	16X73	1902 1903	S1161 S1160	-566.5 -577.5	194.5 284.5	16X73
1743	S1296 S1295	1171.5	284.5	16X73	1823	S1216 S1215	291.5	194.5	16X73 16X73	1903	S1150 S1159	-577.5	374.5	16X73 16X73
1745	S1294	1160.5	374.5	16X73	1825	S1213	280.5	284.5	16X73	1905	S1158	-599.5	194.5	16X73
1746	S1293	1149.5	194.5	16X73	1826	S1213	269.5	374.5	16X73	1906	S1157	-610.5	284.5	16X73
1747	S1292	1138.5	284.5	16X73	1827	S1212	258.5	194.5	16X73	1907	S1156	-621.5	374.5	16X73
1748	S1291	1127.5	374.5	16X73	1828	S1211	247.5	284.5	16X73	1908	S1155	-632.5	194.5	16X73
1749	S1290	1116.5	194.5	16X73	1829	S1210	236.5	374.5	16X73	1909	S1154	-643.5	284.5	16X73
1750 1751	S1289 S1288	1105.5 1094.5	284.5 374.5	16X73 16X73	1830	S1209 S1208	225.5 214.5	194.5 284.5	16X73 16X73	1910 1911	S1153 S1152	-654.5 -665.5	374.5 194.5	16X73 16X73
1751	S1287	1094.5	194.5	16X73	1832	S1206 S1207	203.5	374.5	16X73	1912	S1152 S1151	-676.5	284.5	16X73
1753	S1286	1072.5	284.5	16X73	1833	S1206	192.5	194.5	16X73	1913	S1150	-687.5	374.5	16X73
1754	S1285	1061.5	374.5	16X73	1834	S1205	181.5	284.5	16X73	1914	S1149	-698.5	194.5	16X73
1755	S1284	1050.5	194.5	16X73	1835	S1204	170.5	374.5	16X73	1915	S1148	-709.5	284.5	16X73
1756	S1283	1039.5	284.5	16X73	1836	S1203	159.5	194.5	16X73	1916	S1147	-720.5	374.5	16X73
1757 1758	S1282	1028.5 1017.5	374.5	16X73	1837	S1202	148.5 137.5	284.5 374.5	16X73	1917	S1146 S1145	-731.5 -742.5	194.5	16X73
1758	S1281 S1280	1017.5	194.5 284.5	16X73 16X73	1838	S1201 DUMMY	126.5	194.5	16X73 16X73	1918 1919	S1145 S1144	-742.5 -753.5	284.5 374.5	16X73 16X73
1760	S1279	995.5	374.5	16X73	1840	DUMMY	115.5	284.5	16X73	1920	S1143	-764.5	194.5	16X73
	3.2.0	300.0		. 3, ., 0	.540				. 3, 0		30			. 57.17 0





922 9114 775 2815 1672 900 9104 11855 1677 900 9104 11855 1677 900 9812 2415 1677 9102 9114 1677 9102 9115 1677 9102 9115 1677 9102 9115 9115 9115 9115 9115 9115 9115 911	No.	Name	Х	Υ	Bump size(µm)	No.	Name	х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)
1922 1914	1921	S1142	-775.5	284.5		2001	S1062	-1655.5	194.5		2081	S982	-2535.5	374.5	
1924 1913 368 5 294.5 196.77 2004 51909 -1888.5 194.5 196.77 2004 51979 299.85 274.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196.77 196.5 196															
1852 18119															
1902 1512															
1927 1913 1915															
1995 1915	1927		-841.5		16X73		S1056		194.5	16X73	2087	S976	-2601.5	374.5	
1990 1912 1915															
1951 1952 1965															
1932 STIST 4996.5 1945.5 10773 2015 ST0501 1777.5 374.5 10773 2006 SST01 2006.5 294.5 10773 10713 10															
1934 1912	1932	S1131	-896.5	194.5	16X73	2012	S1051	-1776.5	374.5	16X73	2092	S971	-2656.5	284.5	16X73
1996 1912 999 5 194.5 16773 2016 51074 1920.5 194.5 16773 2006 5997. 2006 5997. 2006 1977. 1920.5 197.5 16773 197.5															
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1939 S1124 973.5 284.5 1687.3 2010 S1044 1853.5 194.5 1687.3 2010 S894 273.5 374.5 1687.3 194															
1940 S1123															
1942 1912 -996.5 194.5 1967.3 2021 51042 -1975.5 374.5 1967.3 2106 5896. 2775.5 294.5 1967.3 1949 1912 191															
94-6 S112															
1944 S1119 1028 1945 1073 2023 S1040 -1897.5 284.5 18X73 2024 S1073 1945 18X73 1945 18X73 1945 18X73 1945 18X73 1945 18X73 1945 18X73 1945 1947 S1118 -1039.5 284.5 16X73 2025 S1039 -1918.5 184.5 18X73 -1808 2799.5 274.5 10473 1947 S1118 -1039.5 284.5 16X73 2025 S1039 -1918.5 184.5 18X73 -1808 2799.5 274.5 10473 1947 S1118 -1039.5 284.5 16X73 2027 S1039 -1918.5 184.5 18X73 -1808 -1808.5 -1808 -1808.5 -1808 -1808.5 -1808 -1808.5 -1808 -1808.5 -1808 -1808.5 -1808 -1808.5 -1808 -1808.5 -1808															
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1946 S1116															
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1953 Si110															
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1998 S1104															
1999															
1960 S1102															
1982 S1100	1960	S1103	-1204.5	284.5	16X73	2040	S1023	-2084.5	194.5	16X73	2120		-2964.5	374.5	16X73
1988 S1100															
1984 S1099															
1966 51098															
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	2000	S1063	-1644.5	374.5	16X73	2080	S983	-2524.5	284.5	16X73	2160	S903	-3404.5	194.5	16X73



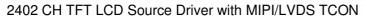


Fig. Sept.	No.	Name	Х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)	No.	Name	х	Υ	Bump size(µm)
\$\frac{1}{2} \frac{1}{2} \fr	2161	S902	-3415.5	284.5		2241	S822	-4295.5	194.5		2321	S742	-5175.5	374.5	
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1966 S899															
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2226 S837 -4130.5 194.5 16x73 2306 S757 -5010.5 374.5 16X73 2386 S677 -5890.5 284.5 16x73 2227 S836 -4141.5 284.5 16x73 2307 S756 -5021.5 194.5 16X73 2387 S676 -5901.5 374.5 16X73 2228 S835 -4163.5 194.5 16x73 2308 S755 -5032.5 284.5 16X73 2388 S676 -5901.5 374.5 16X73 2230 S833 -4174.5 284.5 16x73 2310 S753 -5054.5 194.5 16X73 2389 S674 -5923.5 284.5 16X73 2231 S832 -4185.5 374.5 16x73 2311 S752 -5065.5 284.5 16X73 2390 S673 -5934.5 194.5 16X73 2232 S831 -4196.5 194.5 16x73 2311 S752 -5065.5 284.5															
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2237 S826 -4251.5 374.5 16x73 2317 S746 -5131.5 284.5 16X73 2397 S666 -6011.5 194.5 16X73 2238 S825 -4262.5 194.5 16x73 2318 S745 -5142.5 374.5 16X73 2398 S665 -6022.5 284.5 16X73 2239 S824 -4273.5 284.5 16x73 2319 S744 -5153.5 194.5 16X73 2399 S664 -6033.5 374.5 16X73															
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No.	Name	Х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)
2401	S662	-6055.5	284.5	16X73	2481	S600	-6935.5	194.5	16X73	2561	S520	-7815.5	374.5	16X73
2402	S661	-6066.5	374.5	16X73	2482	S599	-6946.5	284.5	16X73	2562	S519	-7826.5	194.5	16X73
2403	S660	-6077.5	194.5	16X73	2483	S598	-6957.5	374.5	16X73	2563	S518	-7837.5	284.5	16X73
2404 2405	S659 S658	-6088.5 -6099.5	284.5 374.5	16X73 16X73	2484 2485	S597 S596	-6968.5 -6979.5	194.5 284.5	16X73 16X73	2564 2565	S517 S516	-7848.5 -7859.5	374.5 194.5	16X73 16X73
2406	S657	-6110.5	194.5	16X73	2486	S595	-6990.5	374.5	16X73	2566	S515	-7870.5	284.5	16X73
2407	S656	-6121.5	284.5	16X73	2487	S594	-7001.5	194.5	16X73	2567	S514	-7881.5	374.5	16X73
2408	S655	-6132.5	374.5	16X73	2488	S593	-7012.5	284.5	16X73	2568	S513	-7892.5	194.5 284.5	16X73
2409 2410	S654 S653	-6143.5 -6154.5	194.5 284.5	16X73 16X73	2489 2490	S592 S591	-7023.5 -7034.5	374.5 194.5	16X73 16X73	2569 2570	S512 S511	-7903.5 -7914.5	374.5	16X73 16X73
2411	S652	-6165.5	374.5	16X73	2491	S590	-7045.5	284.5	16X73	2571	S510	-7925.5	194.5	16X73
2412	S651	-6176.5	194.5	16X73	2492	S589	-7056.5	374.5	16X73	2572	S509	-7936.5	284.5	16X73
2413	S650	-6187.5	284.5	16X73	2493	S588	-7067.5	194.5	16X73	2573	S508 S507	-7947.5	374.5	16X73
2414 2415	S649 S648	-6198.5 -6209.5	374.5 194.5	16X73 16X73	2494 2495	S587 S586	-7078.5 -7089.5	284.5 374.5	16X73 16X73	2574 2575	S507 S506	-7958.5 -7969.5	194.5 284.5	16X73 16X73
2416	S647	-6220.5	284.5	16X73	2496	S585	-7100.5	194.5	16X73	2576	S505	-7980.5	374.5	16X73
2417	S646	-6231.5	374.5	16X73	2497	S584	-7111.5	284.5	16X73	2577	S504	-7991.5	194.5	16X73
2418	S645	-6242.5	194.5	16X73	2498	S583	-7122.5	374.5	16X73	2578	S503	-8002.5	284.5	16X73
2419 2420	S644 S643	-6253.5 -6264.5	284.5 374.5	16X73 16X73	2499 2500	S582 S581	-7133.5 -7144.5	194.5 284.5	16X73 16X73	2579 2580	\$502 \$501	-8013.5 -8024.5	374.5 194.5	16X73 16X73
2421	S642	-6275.5	194.5	16X73	2501	S580	-7155.5	374.5	16X73	2581	S500	-8035.5	284.5	16X73
2422	S641	-6286.5	284.5	16X73	2502	S579	-7166.5	194.5	16X73	2582	S499	-8046.5	374.5	16X73
2423	S640	-6297.5	374.5	16X73	2503	S578	-7177.5	284.5	16X73	2583	S498	-8057.5	194.5	16X73
2424 2425	S639 S638	-6308.5 -6319.5	194.5 284.5	16X73 16X73	2504 2505	S577 S576	-7188.5 -7199.5	374.5 194.5	16X73 16X73	2584 2585	S497 S496	-8068.5 -8079.5	284.5 374.5	16X73 16X73
2426	S637	-6330.5	374.5	16X73	2506	S575	-7210.5	284.5	16X73	2586	S495	-8090.5	194.5	16X73
2427	S636	-6341.5	194.5	16X73	2507	S574	-7221.5	374.5	16X73	2587	S494	-8101.5	284.5	16X73
2428	S635	-6352.5	284.5	16X73	2508	S573	-7232.5	194.5	16X73	2588	S493	-8112.5	374.5	16X73
2429 2430	S634 S633	-6363.5 -6374.5	374.5 194.5	16X73 16X73	2509 2510	S572 S571	-7243.5 -7254.5	284.5 374.5	16X73 16X73	2589 2590	S492 S491	-8123.5 -8134.5	194.5 284.5	16X73 16X73
2431	S632	-6385.5	284.5	16X73	2511	S570	-7265.5	194.5	16X73	2591	S490	-8145.5	374.5	16X73
2432	S631	-6396.5	374.5	16X73	2512	S569	-7276.5	284.5	16X73	2592	S489	-8156.5	194.5	16X73
2433	S630	-6407.5	194.5	16X73	2513	S568	-7287.5	374.5	16X73	2593	S488	-8167.5	284.5	16X73
2434 2435	S629 S628	-6418.5 -6429.5	284.5 374.5	16X73 16X73	2514 2515	S567 S566	-7298.5 -7309.5	194.5 284.5	16X73 16X73	2594 2595	\$487 \$486	-8178.5 -8189.5	374.5 194.5	16X73 16X73
2436	S627	-6440.5	194.5	16X73	2516	S565	-7309.5	374.5	16X73	2596	S485	-8200.5	284.5	16X73
2437	S626	-6451.5	284.5	16X73	2517	S564	-7331.5	194.5	16X73	2597	S484	-8211.5	374.5	16X73
2438	S625	-6462.5	374.5	16X73	2518	S563	-7342.5	284.5	16X73	2598	S483	-8222.5	194.5	16X73
2439 2440	S624 S623	-6473.5 -6484.5	194.5 284.5	16X73 16X73	2519 2520	S562	-7353.5	374.5 194.5	16X73	2599	S482 S481	-8233.5 -8244.5	284.5 374.5	16X73 16X73
2440	S622	-6495.5	374.5	16X73	2520	S561 S560	-7364.5 -7375.5	284.5	16X73 16X73	2600 2601	S480	-8244.5	194.5	16X73
2442	S621	-6506.5	194.5	16X73	2522	S559	-7386.5	374.5	16X73	2602	S479	-8266.5	284.5	16X73
2443	S620	-6517.5	284.5	16X73	2523	S558	-7397.5	194.5	16X73	2603	S478	-8277.5	374.5	16X73
2444 2445	S619	-6528.5 -6539.5	374.5	16X73 16X73	2524 2525	S557 S556	-7408.5	284.5 374.5	16X73 16X73	2604	S477 S476	-8288.5 -8299.5	194.5 284.5	16X73 16X73
2445	S618 S617	-6550.5	194.5 284.5	16X73	2526	S555	-7419.5 -7430.5	194.5	16X73	2605 2606	S475	-8299.5	374.5	16X73
2447	S616	-6561.5	374.5	16X73	2527	S554	-7441.5	284.5	16X73	2607	S474	-8321.5	194.5	16X73
2448	S615	-6572.5	194.5	16X73	2528	S553	-7452.5	374.5	16X73	2608	S473	-8332.5	284.5	16X73
2449 2450	S614 S613	-6583.5 -6594.5	284.5 374.5	16X73 16X73	2529 2530	S552 S551	-7463.5 -7474.5	194.5 284.5	16X73 16X73	2609 2610	S472 S471	-8343.5 -8354.5	374.5 194.5	16X73 16X73
2450	S612	-6605.5	194.5	16X73	2531	S550	-7474.5	374.5	16X73	2611	S471	-8365.5	284.5	16X73
2452	S611	-6616.5	284.5	16X73	2532	S549	-7496.5	194.5	16X73	2612	S469	-8376.5	374.5	16X73
2453	S610	-6627.5	374.5	16X73	2533	S548	-7507.5	284.5	16X73	2613	S468	-8387.5	194.5	16X73
2454	S609	-6638.5	194.5	16X73	2534	S547	-7518.5	374.5	16X73	2614	S467	-8398.5	284.5	16X73
2455 2456	S608 S607	-6649.5 -6660.5	284.5 374.5	16X73 16X73	2535 2536	S546 S545	-7529.5 -7540.5	194.5 284.5	16X73 16X73	2615 2616	S466 S465	-8409.5 -8420.5	374.5 194.5	16X73 16X73
2457	S606	-6671.5	194.5	16X73	2537	S544	-7551.5	374.5	16X73	2617	S464	-8431.5	284.5	16X73
2458	S605	-6682.5	284.5	16X73	2538	\$543	-7562.5	194.5	16X73	2618	S463	-8442.5	374.5	16X73
2459	S604	-6693.5	374.5	16X73	2539	S542	-7573.5	284.5	16X73	2619	S462	-8453.5	194.5	16X73
2460 2461	S603 S602	-6704.5 -6715.5	194.5 284.5	16X73 16X73	2540 2541	S541 S540	-7584.5 -7595.5	374.5 194.5	16X73 16X73	2620 2621	S461 S460	-8464.5 -8475.5	284.5 374.5	16X73 16X73
2462	S601	-6726.5	374.5	16X73	2542	S539	-7606.5	284.5	16X73	2622	S459	-8486.5	194.5	16X73
2463	DUMMY	-6737.5	194.5	16X73	2543	S538	-7617.5	374.5	16X73	2623	S458	-8497.5	284.5	16X73
2464	DUMMY	-6748.5	284.5	16X73	2544	S537	-7628.5	194.5	16X73	2624	S457	-8508.5 -8519.5	374.5	16X73
2465 2466	DUMMY DUMMY	-6759.5 -6770.5	374.5 194.5	16X73 16X73	2545 2546	S536 S535	-7639.5 -7650.5	284.5 374.5	16X73 16X73	2625 2626	S456 S455	-8519.5 -8530.5	194.5 284.5	16X73 16X73
2467	DUMMY	-6781.5	284.5	16X73	2547	S534	-7650.5	194.5	16X73	2627	S454	-8541.5	374.5	16X73
2468	DUMMY	-6792.5	374.5	16X73	2548	S533	-7672.5	284.5	16X73	2628	S453	-8552.5	194.5	16X73
2469	DUMMY	-6803.5	194.5	16X73	2549	S532	-7683.5	374.5	16X73	2629	S452	-8563.5	284.5	16X73
2470 2471	DUMMY	-6814.5 -6825.5	284.5 374.5	16X73 16X73	2550 2551	S531 S530	-7694.5 -7705.5	194.5 284.5	16X73 16X73	2630 2631	S451 S450	-8574.5 -8585.5	374.5 194.5	16X73 16X73
2471	DUMMY	-6836.5	194.5	16X73	2552	S529	-7716.5	374.5	16X73	2632	S449	-8596.5	284.5	16X73
2473	DUMMY	-6847.5	284.5	16X73	2553	S528	-7727.5	194.5	16X73	2633	S448	-8607.5	374.5	16X73
2474	DUMMY	-6858.5	374.5	16X73	2554	S527	-7738.5	284.5	16X73	2634	S447	-8618.5	194.5	16X73
2475	DUMMY	-6869.5	194.5	16X73	2555	S526	-7749.5	374.5	16X73	2635	S446	-8629.5	284.5	16X73
2476 2477	DUMMY DUMMY	-6880.5 -6891.5	284.5 374.5	16X73 16X73	2556 2557	S525 S524	-7760.5 -7771.5	194.5 284.5	16X73 16X73	2636 2637	S445 S444	-8640.5 -8651.5	374.5 194.5	16X73 16X73
2477	DUMMY	-6902.5	194.5	16X73	2558	S523	-7782.5	374.5	16X73	2638	S443	-8662.5	284.5	16X73
2479	DUMMY	-6913.5	284.5	16X73	2559	S522	-7793.5	194.5	16X73	2639	S442	-8673.5	374.5	16X73
2480	DUMMY	-6924.5	374.5	16X73	2560	S521	-7804.5	284.5	16X73	2640	S441	-8684.5	194.5	16X73





No.	Name	х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)	No.	Name	Х	Υ	Bump size(µm)
2641	S440	-8695.5	284.5	16X73	2721	S360	-9575.5	194.5	16X73	2801	S280	-10455.5	374.5	16X73
2642	S439	-8706.5	374.5	16X73	2722	S359	-9586.5	284.5	16X73	2802	S279	-10466.5	194.5	16X73
2643	S438	-8717.5	194.5	16X73	2723	S358	-9597.5	374.5	16X73	2803	S278	-10477.5	284.5	16X73
2644 2645	S437 S436	-8728.5 -8739.5	284.5 374.5	16X73 16X73	2724 2725	S357 S356	-9608.5 -9619.5	194.5 284.5	16X73 16X73	2804 2805	S277 S276	-10488.5 -10499.5	374.5 194.5	16X73 16X73
2646	S435	-8750.5	194.5	16X73	2726	S355	-9630.5	374.5	16X73	2806	S275	-10499.5	284.5	16X73
2647	S434	-8761.5	284.5	16X73	2727	S354	-9641.5	194.5	16X73	2807	S274	-10521.5	374.5	16X73
2648	S433	-8772.5	374.5	16X73	2728	S353	-9652.5	284.5	16X73	2808	S273	-10532.5	194.5	16X73
2649	S432	-8783.5	194.5	16X73	2729	S352	-9663.5	374.5	16X73	2809	S272	-10543.5	284.5	16X73
2650 2651	S431 S430	-8794.5 -8805.5	284.5 374.5	16X73 16X73	2730 2731	S351 S350	-9674.5 -9685.5	194.5 284.5	16X73 16X73	2810	S271 S270	-10554.5 -10565.5	374.5 194.5	16X73 16X73
2652	S429	-8816.5	194.5	16X73	2732	S349	-9696.5	374.5	16X73	2812	S269	-10576.5	284.5	16X73
2653	S428	-8827.5	284.5	16X73	2733	S348	-9707.5	194.5	16X73	2813	S268	-10587.5	374.5	16X73
2654	S427	-8838.5	374.5	16X73	2734	S347	-9718.5	284.5	16X73	2814	S267	-10598.5	194.5	16X73
2655	S426	-8849.5	194.5	16X73	2735	S346	-9729.5	374.5	16X73	2815	S266	-10609.5	284.5	16X73
2656 2657	S425 S424	-8860.5 -8871.5	284.5 374.5	16X73 16X73	2736 2737	S345 S344	-9740.5 -9751.5	194.5 284.5	16X73 16X73	2816 2817	S265 S264	-10620.5 -10631.5	374.5 194.5	16X73 16X73
2658	S423	-8882.5	194.5	16X73	2738	S343	-9762.5	374.5	16X73	2818	S263	-10642.5	284.5	16X73
2659	S422	-8893.5	284.5	16X73	2739	S342	-9773.5	194.5	16X73	2819	S262	-10653.5	374.5	16X73
2660	S421	-8904.5	374.5	16X73	2740	S341	-9784.5	284.5	16X73	2820	S261	-10664.5	194.5	16X73
2661	S420	-8915.5	194.5	16X73	2741	S340	-9795.5	374.5	16X73	2821	S260	-10675.5	284.5	16X73
2662 2663	S419 S418	-8926.5 -8937.5	284.5 374.5	16X73 16X73	2742 2743	S339 S338	-9806.5 -9817.5	194.5 284.5	16X73 16X73	2822	S259 S258	-10686.5 -10697.5	374.5 194.5	16X73 16X73
2664	S417	-8948.5	194.5	16X73	2744	S337	-9828.5	374.5	16X73	2824	S257	-10708.5	284.5	16X73
2665	S416	-8959.5	284.5	16X73	2745	S336	-9839.5	194.5	16X73	2825	S256	-10719.5	374.5	16X73
2666	S415	-8970.5	374.5	16X73	2746	S335	-9850.5	284.5	16X73	2826	S255	-10730.5	194.5	16X73
2667	S414	-8981.5	194.5	16X73	2747	S334	-9861.5	374.5	16X73	2827	S254	-10741.5	284.5	16X73
2668 2669	S413 S412	-8992.5 -9003.5	284.5 374.5	16X73 16X73	2748 2749	S333 S332	-9872.5 -9883.5	194.5 284.5	16X73 16X73	2828	S253 S252	-10752.5 -10763.5	374.5 194.5	16X73 16X73
2670	S411	-9014.5	194.5	16X73	2750	S331	-9894.5	374.5	16X73	2830	S251	-10774.5	284.5	16X73
2671	S410	-9025.5	284.5	16X73	2751	S330	-9905.5	194.5	16X73	2831	S250	-10785.5	374.5	16X73
2672	S409	-9036.5	374.5	16X73	2752	S329	-9916.5	284.5	16X73	2832	S249	-10796.5	194.5	16X73
2673	S408	-9047.5	194.5	16X73	2753	S328	-9927.5	374.5	16X73	2833	\$248	-10807.5	284.5	16X73
2674 2675	S407 S406	-9058.5 -9069.5	284.5 374.5	16X73 16X73	2754 2755	S327 S326	-9938.5 -9949.5	194.5 284.5	16X73 16X73	2834 2835	\$247 \$246	-10818.5 -10829.5	374.5 194.5	16X73 16X73
2676	S405	-9080.5	194.5	16X73	2756	S325	-9960.5	374.5	16X73	2836	S245	-10840.5	284.5	16X73
2677	S404	-9091.5	284.5	16X73	2757	S324	-9971.5	194.5	16X73	2837	S244	-10851.5	374.5	16X73
2678	S403	-9102.5	374.5	16X73	2758	S323	-9982.5	284.5	16X73	2838	S243	-10862.5	194.5	16X73
2679 2680	S402 S401	-9113.5 -9124.5	194.5 284.5	16X73 16X73	2759 2760	S322 S321	-9993.5 -10004.5	374.5 194.5	16X73 16X73	2839 2840	S242 S241	-10873.5 -10884.5	284.5 374.5	16X73 16X73
2681	S400	-9124.5	374.5	16X73	2760	S320	-10004.5	284.5	16X73	2841	S241	-10895.5	194.5	16X73
2682	S399	-9146.5	194.5	16X73	2762	S319	-10026.5	374.5	16X73	2842	S239	-10906.5	284.5	16X73
2683	S398	-9157.5	284.5	16X73	2763	S318	-10037.5	194.5	16X73	2843	S238	-10917.5	374.5	16X73
2684	S397	-9168.5	374.5	16X73	2764	S317	-10048.5	284.5	16X73	2844	S237	-10928.5	194.5	16X73
2685 2686	S396 S395	-9179.5 -9190.5	194.5 284.5	16X73 16X73	2765 2766	S316 S315	-10059.5 -10070.5	374.5 194.5	16X73 16X73	2845 2846	S236 S235	-10939.5 -10950.5	284.5 374.5	16X73 16X73
2687	S394	-9201.5	374.5	16X73	2767	S314	-10070.5	284.5	16X73	2847	S234	-10961.5	194.5	16X73
2688	S393	-9212.5	194.5	16X73	2768	S313	-10092.5	374.5	16X73	2848	S233	-10972.5	284.5	16X73
2689	S392	-9223.5	284.5	16X73	2769	S312	-10103.5	194.5	16X73	2849	S232	-10983.5	374.5	16X73
2690 2691	S391 S390	-9234.5 -9245.5	374.5 194.5	16X73 16X73	2770 2771	S311 S310	-10114.5 -10125.5	284.5 374.5	16X73 16X73	2850 2851	S231 S230	-10994.5 -11005.5	194.5 284.5	16X73 16X73
2692	S389	-9256.5	284.5	16X73	2772	S309	-10125.5	194.5	16X73	2852	S229	-11005.5	374.5	16X73
2693	S388	-9267.5	374.5	16X73	2773	S308	-10147.5	284.5	16X73	2853	S228	-11027.5	194.5	16X73
2694	S387	-9278.5	194.5	16X73	2774	S307	-10158.5	374.5	16X73	2854	S227	-11038.5	284.5	16X73
2695	S386	-9289.5	284.5	16X73	2775	S306	-10169.5	194.5	16X73	2855	S226	-11049.5	374.5	16X73
2696 2697	S385 S384	-9300.5 -9311.5	374.5 194.5	16X73 16X73	2776 2777	\$305 \$304	-10180.5 -10191.5	284.5 374.5	16X73 16X73	2856 2857	S225 S224	-11060.5 -11071.5	194.5 284.5	16X73 16X73
2698	S383	-9322.5	284.5	16X73	2778	S303	-10202.5	194.5	16X73	2858	S223	-11071.5	374.5	16X73
2699	S382	-9333.5	374.5	16X73	2779	S302	-10213.5	284.5	16X73	2859	S222	-11093.5	194.5	16X73
2700	S381	-9344.5	194.5	16X73	2780	S301	-10224.5	374.5	16X73	2860	S221	-11104.5	284.5	16X73
2701 2702	S380 S379	-9355.5	284.5 374.5	16X73 16X73	2781 2782	S300 S299	-10235.5 -10246.5	194.5 284.5	16X73 16X73	2861 2862	S220 S219	-11115.5 -11126.5	374.5 194.5	16X73 16X73
2702	S379 S378	-9366.5 -9377.5	194.5	16X73 16X73	2782	S299 S298	-10246.5	374.5	16X73	2862	S219 S218	-11126.5	284.5	16X73 16X73
2704	S377	-9388.5	284.5	16X73	2784	S297	-10268.5	194.5	16X73	2864	S217	-11148.5	374.5	16X73
2705	S376	-9399.5	374.5	16X73	2785	S296	-10279.5	284.5	16X73	2865	S216	-11159.5	194.5	16X73
2706	S375	-9410.5	194.5	16X73	2786	S295	-10290.5	374.5	16X73	2866	S215	-11170.5	284.5	16X73
2707 2708	S374 S373	-9421.5 -9432.5	284.5	16X73	2787	S294	-10301.5	194.5	16X73	2867	S214 S213	-11181.5	374.5	16X73
2708	S373 S372	-9432.5 -9443.5	374.5 194.5	16X73 16X73	2788 2789	S293 S292	-10312.5 -10323.5	284.5 374.5	16X73 16X73	2868 2869	S213 S212	-11192.5 -11203.5	194.5 284.5	16X73 16X73
2710	S371	-9454.5	284.5	16X73	2790	S291	-10323.5	194.5	16X73	2870	S211	-11214.5	374.5	16X73
2711	S370	-9465.5	374.5	16X73	2791	S290	-10345.5	284.5	16X73	2871	S210	-11225.5	194.5	16X73
2712	S369	-9476.5	194.5	16X73	2792	S289	-10356.5	374.5	16X73	2872	S209	-11236.5	284.5	16X73
2713 2714	S368 S367	-9487.5 -9498.5	284.5	16X73	2793 2794	S288 S287	-10367.5 -10378.5	194.5	16X73	2873 2874	S208 S207	-11247.5	374.5	16X73
2714	S367 S366	-9498.5 -9509.5	374.5 194.5	16X73 16X73	2794	S287 S286	-10378.5	284.5 374.5	16X73 16X73	2874	S207 S206	-11258.5 -11269.5	194.5 284.5	16X73 16X73
2716	S365	-9520.5	284.5	16X73	2796	S285	-10400.5	194.5	16X73	2876	S205	-11280.5	374.5	16X73
2717	S364	-9531.5	374.5	16X73	2797	S284	-10411.5	284.5	16X73	2877	S204	-11291.5	194.5	16X73
2718	S363	-9542.5	194.5	16X73	2798	S283	-10422.5	374.5	16X73	2878	S203	-11302.5	284.5	16X73
2719 2720	S362	-9553.5 9564.5	284.5	16X73	2799 2800	S282	-10433.5	194.5	16X73	2879 2880	S202 S201	-11313.5	374.5	16X73
Z1ZU	S361	-9564.5	374.5	16X73	2000	S281	-10444.5	284.5	16X73	2000	3201	-11324.5	194.5	16X73





No.	Name	х	Υ	Bump size(µm)	1	No.	Name	Х	Υ	Bump size(µm)
2881	S200	-11335.5	284.5	16X73		2961	S120	-12215.5	194.5	16X73
2882	S199	-11346.5	374.5	16X73 16X73		962	S119	-12226.5	284.5	16X73
2883 2884	S198 S197	-11357.5 -11368.5	194.5 284.5	16X73		963 964	S118 S117	-12237.5 -12248.5	374.5 194.5	16X73 16X73
2885	S196	-11379.5	374.5	16X73		2965	S116	-12259.5	284.5	16X73
2886	S195	-11390.5	194.5	16X73		2966	S115	-12270.5	374.5	16X73
2887	S194	-11401.5	284.5	16X73		967	S114	-12281.5	194.5	16X73
2888 2889	S193 S192	-11412.5 -11423.5	374.5 194.5	16X73 16X73		968 969	S113 S112	-12292.5 -12303.5	284.5 374.5	16X73 16X73
2890	S192	-11434.5	284.5	16X73		2970	S112	-12314.5	194.5	16X73
2891	S190	-11445.5	374.5	16X73		2971	S110	-12325.5	284.5	16X73
2892	S189	-11456.5	194.5	16X73		2972	S109	-12336.5	374.5	16X73
2893 2894	S188 S187	-11467.5 -11478.5	284.5 374.5	16X73 16X73		973 2974	S108 S107	-12347.5 -12358.5	194.5 284.5	16X73 16X73
2895	S186	-11476.5	194.5	16X73		975	S107	-12369.5	374.5	16X73
2896	S185	-11500.5	284.5	16X73		2976	S105	-12380.5	194.5	16X73
2897	S184	-11511.5	374.5	16X73		2977	S104	-12391.5	284.5	16X73
2898	S183	-11522.5	194.5	16X73		2978	S103	-12402.5	374.5	16X73
2899 2900	S182 S181	-11533.5 -11544.5	284.5 374.5	16X73 16X73		979 980	S102 S101	-12413.5 -12424.5	194.5 284.5	16X73 16X73
2901	S180	-11555.5	194.5	16X73		2981	S100	-12435.5	374.5	16X73
2902	S179	-11566.5	284.5	16X73	2	982	S99	-12446.5	194.5	16X73
2903	S178	-11577.5	374.5	16X73		983	S98	-12457.5	284.5	16X73
2904 2905	S177 S176	-11588.5 -11599.5	194.5 284.5	16X73 16X73		984 985	S97 S96	-12468.5 -12479.5	374.5 194.5	16X73 16X73
2905	S176	-11610.5	374.5	16X73	_	986	S95	-12479.5	284.5	16X73
2907	S174	-11621.5	194.5	16X73		987	S94	-12501.5	374.5	16X73
2908	S173	-11632.5	284.5	16X73		2988	S93	-12512.5	194.5	16X73
2909 2910	S172 S171	-11643.5 -11654.5	374.5 194.5	16X73 16X73		2989 2990	S92 S91	-12523.5 -12534.5	284.5 374.5	16X73 16X73
2910	S171	-11665.5	284.5	16X73		2990	S90	-12534.5	194.5	16X73
2912	S169	-11676.5	374.5	16X73		992	S89	-12556.5	284.5	16X73
2913	S168	-11687.5	194.5	16X73	2	2993	S88	-12567.5	374.5	16X73
2914	S167	-11698.5	284.5	16X73		2994	S87	-12578.5	194.5	16X73
2915 2916	S166 S165	-11709.5 -11720.5	374.5 194.5	16X73 16X73		995 1996	S86 S85	-12589.5 -12600.5	284.5 374.5	16X73 16X73
2916	S164	-11720.5	284.5	16X73		2996	S84	-12611.5	194.5	16X73
2918	S163	-11742.5	374.5	16X73		2998	S83	-12622.5	284.5	16X73
2919	S162	-11753.5	194.5	16X73		2999	S82	-12633.5	374.5	16X73
2920 2921	S161 S160	-11764.5 -11775.5	284.5 374.5	16X73 16X73		3000 3001	S81 S80	-12644.5 -12655.5	194.5 284.5	16X73 16X73
2921	S159	-11775.5	194.5	16X73		3002	S79	-12666.5	374.5	16X73
2923	S158	-11797.5	284.5	16X73		3003	S78	-12677.5	194.5	16X73
2924	S157	-11808.5	374.5	16X73		3004	S77	-12688.5	284.5	16X73
2925	S156	-11819.5	194.5	16X73		3005	S76	-12699.5	374.5	16X73
2926 2927	S155 S154	-11830.5 -11841.5	284.5 374.5	16X73 16X73		3006 3007	\$75 \$74	-12710.5 -12721.5	194.5 284.5	16X73 16X73
2928	S153	-11852.5	194.5	16X73		8008	\$73	-12732.5	374.5	16X73
2929	S152	-11863.5	284.5	16X73		3009	S72	-12743.5	194.5	16X73
2930	S151	-11874.5	374.5	16X73		3010	S71	-12754.5	284.5	16X73
2931 2932	S150 S149	-11885.5 -11896.5	194.5 284.5	16X73 16X73		011 012	S70 S69	-12765.5 -12776.5	374.5 194.5	16X73 16X73
2933	S148	-11907.5	374.5	16X73	_	012	S68	-12787.5	284.5	16X73
2934	S147	-11918.5	194.5	16X73		014	S67	-12798.5	374.5	16X73
2935	S146	-11929.5	284.5	16X73		015	S66	-12809.5	194.5	16X73
2936 2937	S145 S144	-11940.5 -11951.5	374.5 194.5	16X73 16X73	_	8016 8017	S65 S64	-12820.5 -12831.5	284.5 374.5	16X73 16X73
2938	S144 S143	-11962.5	284.5	16X73		017	S63	-12842.5	194.5	16X73
2939	S142	-11973.5	374.5	16X73	3	019	S62	-12853.5	284.5	16X73
2940	S141	-11984.5	194.5	16X73		020	S61	-12864.5	374.5	16X73
2941 2942	S140 S139	-11995.5 -12006.5	284.5 374.5	16X73 16X73		3021 3022	S60 S59	-12875.5 -12886.5	194.5 284.5	16X73 16X73
2942	S139	-12006.5	194.5	16X73		3023	S58	-12897.5	374.5	16X73
2944	S137	-12028.5	284.5	16X73	3	8024	S57	-12908.5	194.5	16X73
2945	S136	-12039.5	374.5	16X73		025	S56	-12919.5	284.5	16X73
2946	S135	-12050.5	194.5	16X73		026	S55	-12930.5	374.5	16X73
2947 2948	S134 S133	-12061.5 -12072.5	284.5 374.5	16X73 16X73		3027 3028	S54 S53	-12941.5 -12952.5	194.5 284.5	16X73 16X73
2949	S132	-12083.5	194.5	16X73		3029	S52	-12963.5	374.5	16X73
2950	S131	-12094.5	284.5	16X73	3	3030	S51	-12974.5	194.5	16X73
2951	S130	-12105.5	374.5	16X73		031	S50	-12985.5	284.5	16X73
2952 2953	S129 S128	-12116.5 -12127.5	194.5 284.5	16X73 16X73		3032 3033	S49 S48	-12996.5 -13007.5	374.5 194.5	16X73 16X73
2954	S126	-12127.5	374.5	16X73		3034	S47	-13007.5	284.5	16X73
2955	S126	-12149.5	194.5	16X73	3	3035	S46	-13029.5	374.5	16X73
2956	S125	-12160.5	284.5	16X73	_	036	S45	-13040.5	194.5	16X73
2957 2958	S124 S123	-12171.5 -12182.5	374.5 194.5	16X73 16X73		3037 3038	S44 S43	-13051.5 -13062.5	284.5 374.5	16X73 16X73
2959	S123	-12193.5	284.5	16X73		8039	S43	-13062.5	194.5	16X73
2960	S121	-12204.5	374.5	16X73		3040	S41	-13084.5	284.5	16X73
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				Bump
No.	Name	Х	Υ	size(µm)
3041	C40	10005.5	074.5	
3041	S40	-13095.5	374.5	16X73 16X73
3042	S39	-13106.5	194.5	
	S38	-13117.5	284.5	16X73
3044	S37	-13128.5	374.5	16X73
3045	S36	-13139.5	194.5	16X73
3046	S35	-13150.5	284.5	16X73
3047	S34	-13161.5	374.5	16X73
3048	S33	-13172.5	194.5	16X73
3049	S32	-13183.5	284.5	16X73
3050	S31	-13194.5	374.5	16X73
3051	S30	-13205.5	194.5	16X73
3052	S29	-13216.5	284.5	16X73
3053	S28	-13227.5	374.5	16X73
3054	S27	-13238.5	194.5	16X73
3055	S26	-13249.5	284.5	16X73
3056	S25	-13260.5	374.5	16X73
3057	S24	-13271.5	194.5	16X73
3058	S23	-13282.5	284.5	16X73
3059	S22	-13293.5	374.5	16X73
3060	S21 /	-13304.5	194.5	16X73
3061	S20	-13315.5	284.5	16X73
3062	S19	-13326.5	374.5	16X73
3063	S18	-13337.5	194.5	16X73
3064	S17	-13348.5	284.5	16X73
3065	S16	-13359.5	374.5	16X73
3066	S15	-13370.5	194.5	16X73
3067	S14	-13381.5	284.5	16X73
3068	S13	-13392.5	374.5	16X73
3069	S12	-13403.5	194.5	16X73
3070	S1.1	-13414.5	284.5	16X73
3071	S10	-13425.5	374.5	16X73
3072	S9	-13436.5	194.5	16X73
3073	S8	-13447.5	284.5	16X73
3074	S7	-13458.5	374.5	16X73
3075	S6	-13469.5	194.5	16X73
3076	S5	-13480.5	284.5	16X73
3077	S4	-13491.5	374.5	16X73
3078	S3	-13502.5	194.5	16X73
3079	S2	-13513.5	284.5	16X73
3080	S1	-13524.5	374.5	16X73
3081	SL1	-13535.5	194.5	16X73
3082	DUMMY	-13546.5	284.5	16X73
3083	DUMMY	-13557.5	374.5	16X73
3084	DUMMY	-13568.5	194.5	16X73
3085	DUMMY	-13579.5	284.5	16X73
3086	DUMMY	-13590.5	374.5	16X73
3087	DUMMY R3	-13601.5	194.5	16X73
3088	DUMMY R3	-13612.5	284.5	16X73
3089	DUMMY R3	-13623.5	374.5	16X73
3090	DUMMY R3	-13634.5	194.5	16X73
3091	DUMMY R3	-13645.5	284.5	16X73
3092	DUMMY R3	-13645.5	374.5	16X73
*	Alignment (L)	-13636.3	386	10///0
*	Alignment (R)	+13706	386	
	Angrinent (R)	+13/00	300	

Table 14.2: Pad coordinates



15. Ordering Information

Part no.	Package type					
HX8260-Ax <u>PDxxx</u>	X : meab fab code PD : mean COG xxx : mean chip thickness (μm)					

