DATA SHEET

(DOC No. HX8260-A-DS)

HX8260-A

2402CH TFT LCD Source Driver
with MIPI/LVDS TCON

Version 01 October, 2014

Himax Technologies, Inc.
http://www.himax.com.tw

Revision History

October, 2014

Version	Date	Description of changes
01	2014/4/18	New setup
	2014/4/23	Page 10~12 1. Modified pin function and pin name ERR_CSB →ERR_RES1 LNSW_RES1 →LNSW_CSB PNSW →PNSW_SCL MIPITE_SCL →MIPITE_SDA TPSYNC_SDA →TPSYNC Page 11, .28 and 75 2. Resolution selection 768RGBx1280→768x1024 Page 156 3. Updated section 14.2 chip outline dimension. Paeg 104 4. Updated Gamma PVP/N 8, PVP/N 9, and PVP/N 10 default value. Page 76 5. Updated video timing table.
	2014/5/15	Page 81~102 1. Updated section 8.4 User define command for MIPI interface.
	2014/5/29	Page 156 1. Updated Chip size **(w/i scribe line)**.
	2014/6/10	Page 142 1. Modified VDDI_RX and VDDI_D operation voltage 1.65~1.95V.
	2014/6/19	Page 131 1. Updated OTP read flow chart.
	2014/7/1	Page 142 1. Modified VDDI_RX and VDDI_D operation voltage 1.7~1.9V.
	2014/10/14	Page 14 1. Updadated section 4.2 Value of wiring resistance to each pin. Page 15~19 2. Updated section 5.1~5.4 example circuit. Page 29 3. Updated section 6.2 figure 6.1 GOA connection. Page 32 4. Updated section 6.4 input interface and pin mapping.

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1. General Description

The HX8260-A is a single-chip solution that combines source driver control, gate driver control and power supply circuit to drive TFT LCD.

The HX8260-A supports the resolution of 800RGBx1280, 768RGBx1024, 720RGBx1280, and 600RGBx1024 and with 6bit+2bit dithering in color depth.

The HX8260-A supports several interface modes, including MIPI DSI interface mode LVDS interface mode.

2. Features

- Interface: LVDS **(85MHz)**; MIPI 4 lane **(480Mbps/lane)**
- Channel Number: 2402 channel output, build in source driver and TCON
- Resolution :800RGBx1280,768RGBx1024,720RGBx1280,600RGBx1024
- Color : 6bits +2-bit dithering
- SPI interface
- VCOM is programmable adjustment by OTP
- Support GOA gate control signal
- Inversion :1/2/4/8 dot inversion, column inversion
- Support Zigzag panel
- Support CABC function
- Build-in PFM Booster controller to drive DC/DC converter circuit -- VSP & VSN
- Build-in Charge Pump controller to drive DC/DC converter circuit – VGH, VGL & VCL

3. Block Diagram

3.1 Function block diagram

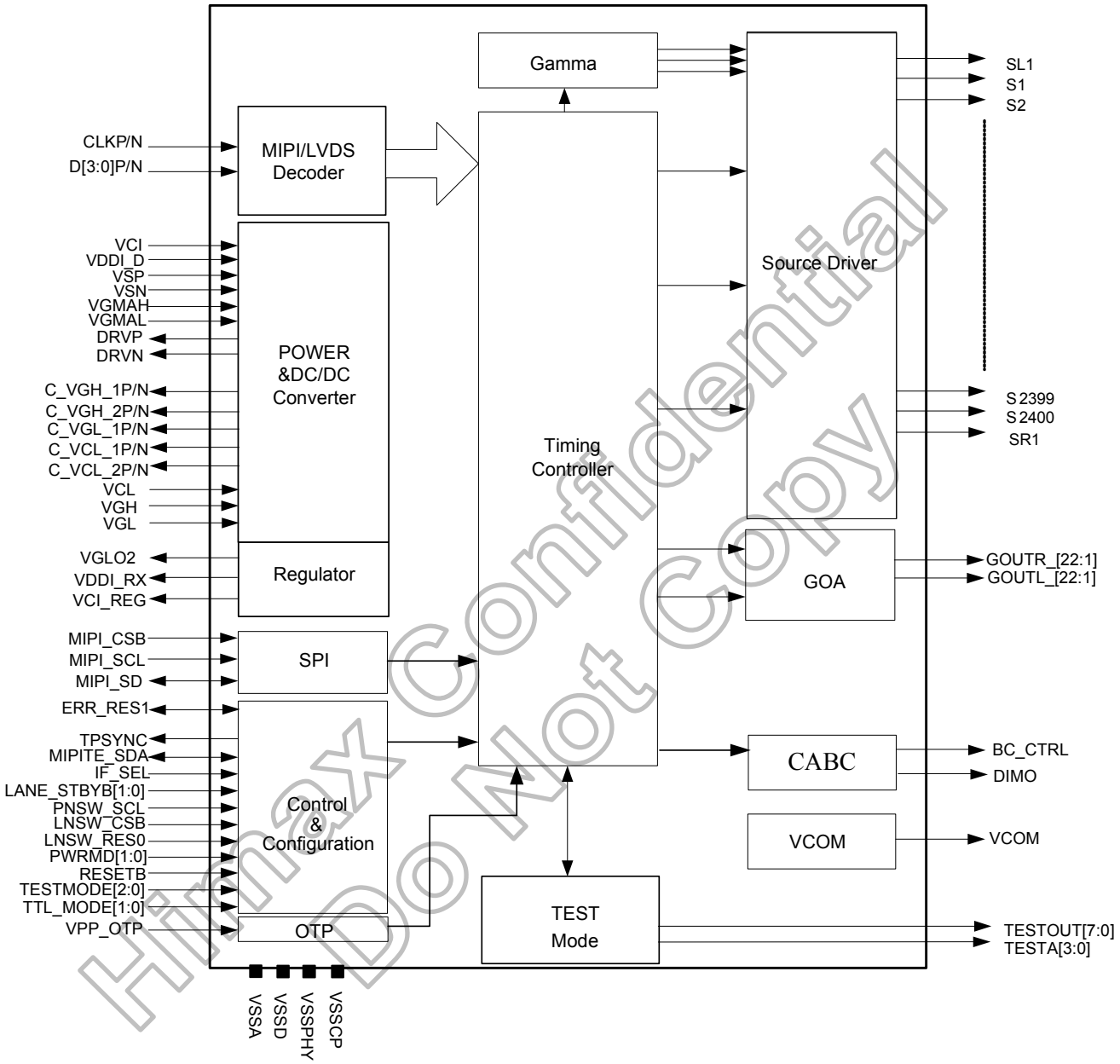


Figure 3.1: Function block diagram

4. Pin Description

Pin Types: **I**=Input, **O**=Output, **I/O**= Input/Output, **P**=Power, **G**=Ground, **N**=No Connection.

4.1 Pin description

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th></tr>
<tr><td>RESETB</td><td>I</td><td>Global reset.(VSSD~IOVCC)</td></tr>
<tr><td>IF_SEL</td><td>I</td><td>IF_SEL=1: MIPI mode (default)
IF_SEL=0: LVDS mode</td></tr>
<tr><td>LNSW_CSB</td><td>I</td><td>MIPI mode (IF_SEL=1): MIPI LANE swap function pin.
LVDS mode (IF_SEL=0): SPI CSB signal pin.
Default LNSW_CSB pulled H.</td></tr>
<tr><td>LNSW_RES0</td><td>I</td><td>MIPI mode (IF_SEL=1): MIPI LANE swap function pin (default=11).
<table>
<tr><th>Pad</th><th>D2P</th><th>D2N</th><th>D1P</th><th>D1N</th><th>CLKP</th><th>CLKN</th><th>D0P</th><th>D0N</th><th>D3P</th><th>D3N</th></tr>
<tr><th>LNSW_CSB</th><th>LNSW_RES0</th><th colspan="9">MIPI lanes mapping table</th></tr>
<tr><td>0</td><td>0</td><td>D3P</td><td>D3N</td><td>D2P</td><td>D2N</td><td>CLKP</td><td>CLKN</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td></tr>
<tr><td>0</td><td>1</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td><td>CLKP</td><td>CLKN</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td></tr>
<tr><td>1</td><td>0</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>CLKP</td><td>CLKN</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr>
<tr><td>1</td><td>1</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>CLKP</td><td>CLKN</td><td>D0P</td><td>D0N</td><td>D3P</td><td>D3N</td></tr>
</table>
LVDS mode (IF_SEL=0): Resolution selection pin
<table>
<tr><th>ERR_RES1</th><th>LNSW_RES0</th><th>Resolution</th></tr>
<tr><td>0</td><td>0</td><td>600RGBx1024</td></tr>
<tr><td>0</td><td>1</td><td>720RGBx1280</td></tr>
<tr><td>1</td><td>0</td><td>768RGBx1024</td></tr>
<tr><td>1</td><td>1</td><td>800RGBx1280</td></tr>
</table>
(Default LNSW_RES0 pulled H)</td></tr>
<tr><td>PWRMD[1]
PWRMD[0]</td><td>I</td><td>Power mode contorl pin.
<table>
<tr><th>PWRMD[1]</th><th>PWRMD[0]</th><th>Driving mode</th></tr>
<tr><td>0</td><td>0</td><td>Support HX5186-C power mode.</td></tr>
<tr><td>0</td><td>1</td><td>Suppot PFM circuit power mode.</td></tr>
<tr><td>1</td><td>0</td><td>External VSP,VSN, VGH,VGL power mode.</td></tr>
<tr><td>1</td><td>1</td><td>External VSP,VSN power mode (default).</td></tr>
</table></td></tr>
<tr><td>LANE1_STBYB</td><td>I</td><td>MIPI mode (IF_SEL=1): MIPI LANE number control pin
LVDS mode (IF_SEL=0): Standby mode signal (L :standby mode)
<table>
<tr><th>LANE1_STBYB</th><th>LANE0_BISTB</th><th>MIPI lane</th></tr>
<tr><td colspan="2">Others</td><td>Reserved</td></tr>
<tr><td>1</td><td>1</td><td>4-lane</td></tr>
</table>
LANE1_STBYB default pulled H.</td></tr>
<tr><td>LANE0_BISTB</td><td>I</td><td>MIPI mode (IF_SEL=1): MIPI LANE number control pin.
LVDS mode (IF_SEL=0): BIST mode signal (L: BIST mode).
LANE0_BISTB default pulled H.</td></tr>
<tr><td>MIPITE_SDA</td><td>I/O</td><td>MIPI mode (IF_SEL=1): TE output signal.
LVDS mode (IF_SEL=0): SPI SDA signal.
MIPITE_SDA default pulled H.</td></tr>
<tr><td>TPSYNC</td><td>O</td><td>TPSYNC output signal</td></tr>
<tr><td>PNSW_SCL</td><td>I</td><td>MIPI mode (IF_SEL=1): MIPI and LVDS PN swap function pin.
LVDS mode (IF_SEL=0): SPI clock signal.
Default pulled H.</td></tr>
<tr><td>BC_CTRL</td><td>O</td><td>ON/OFF LED Backlight driver</td></tr>
<tr><td>DIMO</td><td>O</td><td>CABC PWM output</td></tr>
<tr><td>ERR_RES1</td><td>I/O</td><td>MIPI mode (IF_SEL=1): ERR report
LVDS mode (IF_SEL=0): Resolution selection pin
ERR_RES1 default pulled H.</td></tr>
</table>

Table 4.1: Global pin

<table>
<tr><th>Pin name</th><th>I/O</th><th>Description</th></tr>
<tr><td>CLKP/CLKN</td><td>I</td><td>MIPI/LVDS clock input pin.</td></tr>
<tr><td>D0P/D0N
D1P/D1N
D2P/D2N
D3P/D3N</td><td>I</td><td>MIPI/LVDS data input pin.
<table>
<tr><th>Pad name</th><th>MIPI mode Pin mapping (default)</th><th>LVDS pin mapping</th></tr>
<tr><td>D0P/D0N</td><td>D0P/D0N</td><td>D2P/D2N</td></tr>
<tr><td>D1P/D1N</td><td>D1P/D1N</td><td>D1P/D1N</td></tr>
<tr><td>D2P/D2N</td><td>D2P/D2N</td><td>D0P/D0N</td></tr>
<tr><td>D3P/D3N</td><td>D3P/D3N</td><td>D3P/D3N</td></tr>
</table>
MIPI data lane could be swapped by LNSW_RES0 and LNSW_CSB pin,but LVDS data lane could not be swapped.</td></tr>
</table>

Table 4.2: MIPI interface

Pin name	I/O	Description
MIPI_CSB	I	MIPI mode SPI CHIP enable signal.default pulled H.
MIPI_SD	I/O	MIPI mode SPI DAT signal.default pulled H.
MIPI_SCK	I	MIPI mode SPI clock signal.default pulled H.

Table 4.3: SPI interface

Pin name	I/O	Description
GOUT_R[22:1]	O	GOA control signal at right side.**(VGL~VGH)**
GOUT_L[22:1]	O	GOA control signal at left side. **(VGL~VGH)**

Note: (1) IO cell voltage is between VGH and VGL.

Table 4.4: Gate driver (GOA) control pin

Pin name	I/O	Description
S1 ∫ S2400	O	Source output pin.
SL1,SR1	O	Source output pin. It is available when zigzag function enable.

Note: (1) IO cell voltage is between VSP and VSN.

Table 4.5: Source output pin

Pin name	I/O	Description
VCI	P	Power input 2.6V ~ 6V.
VSP	P	Positive power input for source driver and power circuits **(4.5V ~ 6V)**.
VSN	P	Negative power input for source driver and power circuits **(-4.5V ~ -6V)**.
VDDI_D	P	Power input 1.8V for TCON and Logic.
VDDI_RX	P	Power input 1.8V for MIPI & LVDS RX.
VPP_OTP	P	Power input for OTP programming **(7.6V)**.Leave this pin open or connect it to VSP when not programming OTP.
DRVP	O	CLK for VSP PFM and HX5186-C.
DRVN	O	CLK for VSN PFM and HX5186-C.
VGLO2	P	VGLO Regulator output 2.
VGMAH	P	Positive gamma high voltage.
VGMAL	P	Negative gamma high voltage.
VCI_REG	P	Regulator output for internal reference.
VCL	P	VCL charge pump output.
C_VCL_1P C_VCL_1N C_VCL_2P C_VCL_2N	O	VCL flying cap. pin.
VGH	P	VGH charge pump output.
C_VGH_1P C_VGH_1N C_VGH_2P C_VGH_2N	O	VGH flying cap. pin.

Pin name	I/O	Description
VGL	P	VGL charge pump output.
C_VGL_1P C_VGL_1N	O	GL flying cap. pin.
VCOM	P	VCOM Regulator output.
VSSD	G	Digital circuit ground **(0V)**.
VSSA	G	Analog circuit ground **(0V)**.
VSSPHY	G	Analog circuit ground **(0V)**.
VSSCP	G	Ground for charge pump circuit **(0V)**.

Table 4.6: Power and ground pin

Pin name	I/O	Description
TESTOUT[7:0]	O	Test pin. Float these pin for normal operation.
TESTA[3:0]	O	Test pin. Float these pin for normal operation.
DUMMY	NC	No connection.

Table 4.7: Others

4.2 Value of wiring resistance to each pin

The input wiring resistance values affect power or signal integrity and the display quality. So be sure to design using values that do not exceed those recommendations as below.

Pin type	Pin name	Resistance value(Ω)	Capacitance value(pF)
Power & Ground	VSSD	< 3	-
	VDD_ID	< 5	-
	VDD_RX	< 5	-
	VCI	< 5	-
	VSSA	< 3	-
	VSP	< 5	-
	VSN	< 5	-
	VSSCP	<5	-
	VPP_OTP	<10	-
	VSSPHY	<5	-

Pin type	Pin name	Resistance value(Ω)	Capacitance value(pF)
PFM & Charge Pump & Regulator	VCOM	< 5	
	VCI_REG	<5	
	VGLO2	<5	
	VGL	< 10	
	VGH	< 10	
	VCOM	< 10	-
	VGAMP	< 10	-
	VGAMN	< 10	-
	VCL	< 5	-
	C_VCL_1P,C_VCL_1N C_VCL_2P,C_VCL_2N	< 5	-
	C_VGH_1P,C_VGH_1N C_VGH_2P,C_VGH_2N	< 5	-
	DRVN,DRVP	< 5	-
	C_VGL_1P,C_VGL_1N	< 3	-

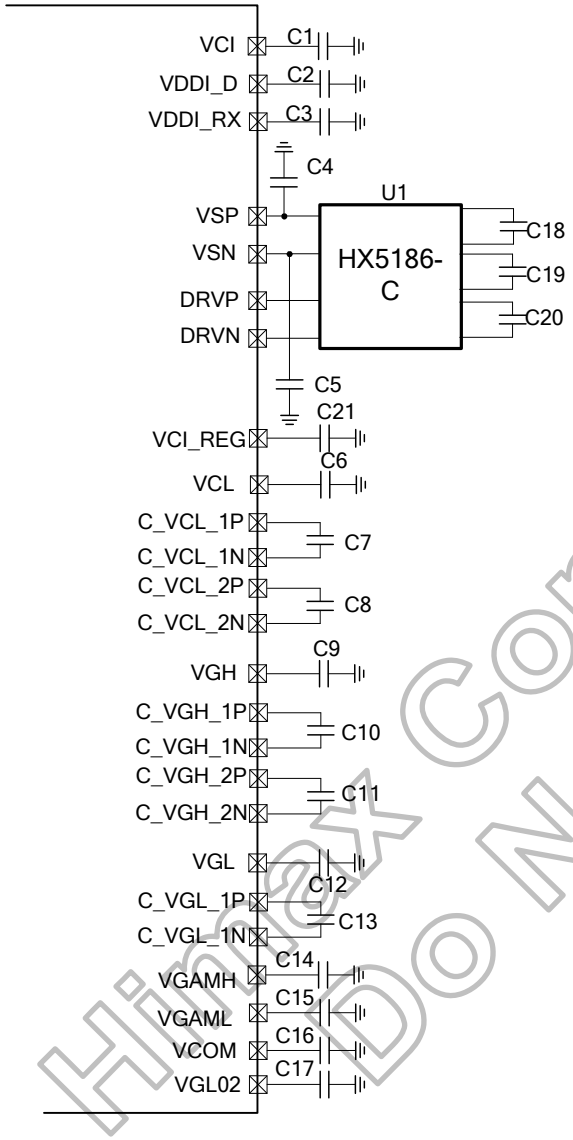
Pin type	Pin name	Resistance value(Ω)	Capacitance value(pF)
GOA	GOUT1_R~GOUT22_R	<100	-
	GOUT1_L~GOUT22_L	<100	-

Pin type	Pin name	Resistance value(Ω)	Capacitance value(pF)
MIPI/LVDS Interface	CKP, CLKN	< 10	< 0.9
	D0P, D0N		
	D1P, D1N		
	D2P, D2N		
	D3P, D3N		

5. Power Application

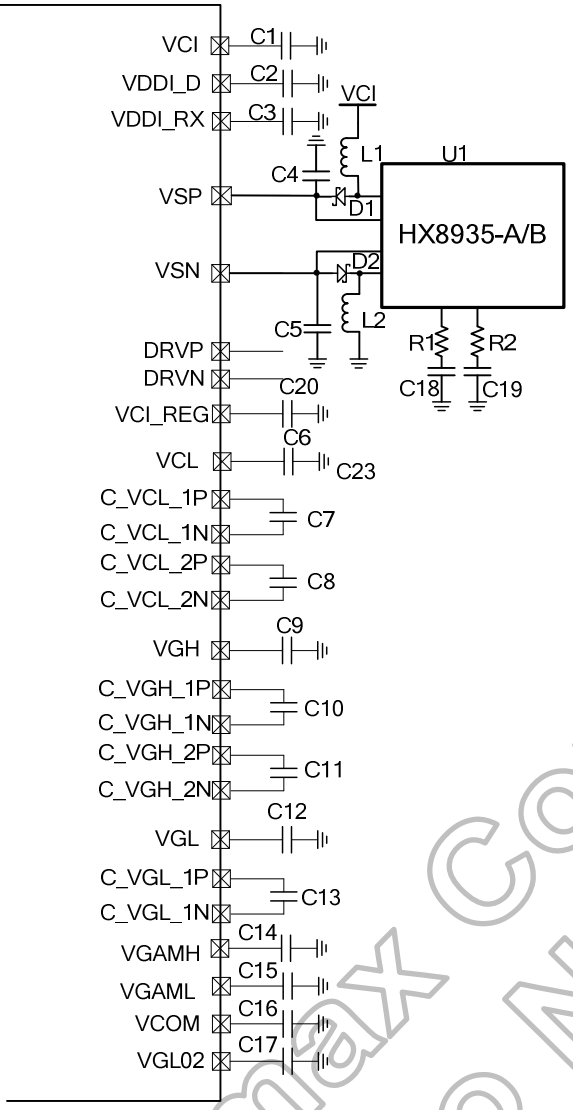
5.1 PWRMD [1:0] =00b

- **HX5186-C example circuit**



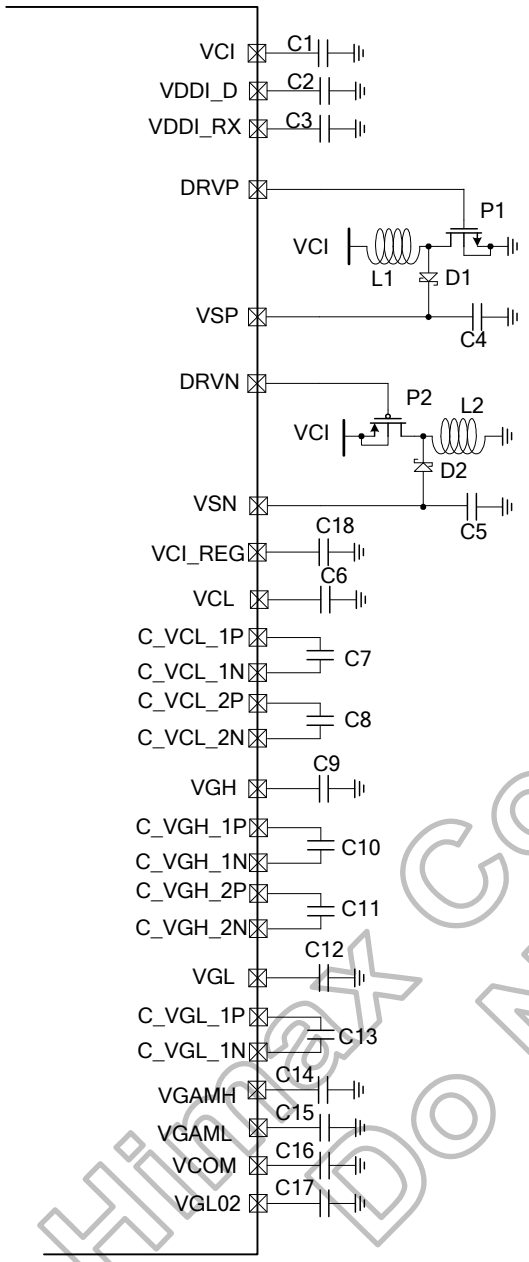
Component	Value
C1	2.2uF/10V
C2	2.2uF/6V
C3	2.2uF/6V
C4	2.2uF/10V
C5	2.2uF/10V
C6	1uF/6V
C7	1uF/6V
C8	1uF/6V
C9	1uF/25V
C10	1uF/16V
C11	1uF/16V
C12	1uF/25V
C13	1uF/16V
C14	1uF/10V
C15	1uF/10V
C16	1uF/6V
C17	1uF/25V
C18	Please refer HX5186-C datasheet
C19	Please refer HX5186-C datasheet
C20	Please refer HX5186-C datasheet
C21	1uF/6V
U1	HX5186-C

- **HX8935-A/B example circuit**



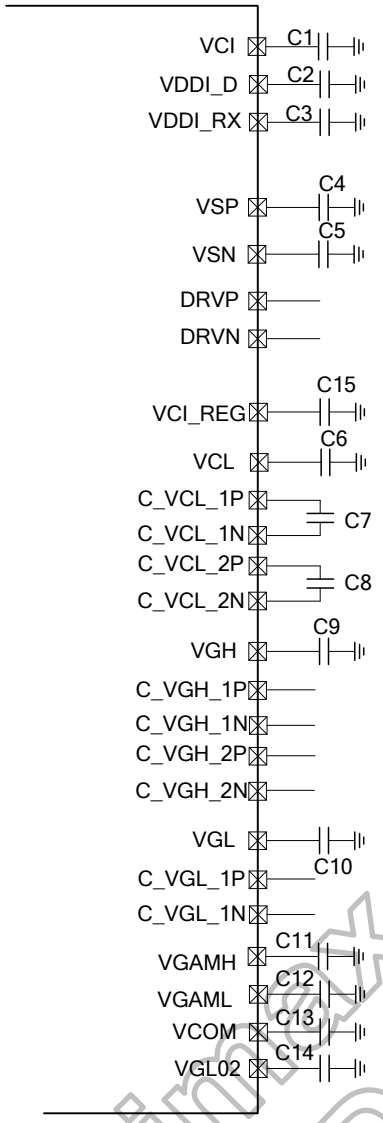
Component	Value
C1	2.2uF/10V
C2	2.2uF/6V
C3	2.2uF/6V
C4	2.2uF/10V
C5	2.2uF/10V
C6	1uF/6V
C7	1uF/6V
C8	1uF/6V
C9	1uF/25V
C10	1uF/16V
C11	1uF/16V
C12	1uF/25V
C13	1uF/16V
C14	1uF/10V
C15	1uF/10V
C16	1uF/6V
C17	1uF/25V
C18,C19	1nF/6.3V
C20	1uF/6V
R1,R2	100K
D1,D2	VF<0.4V /20mA, VR>30V recommand diode :RB521S-30
L1,L2	4.7uH
U1	HX8935-A/B

5.2 PWRMD [1:0] =01b



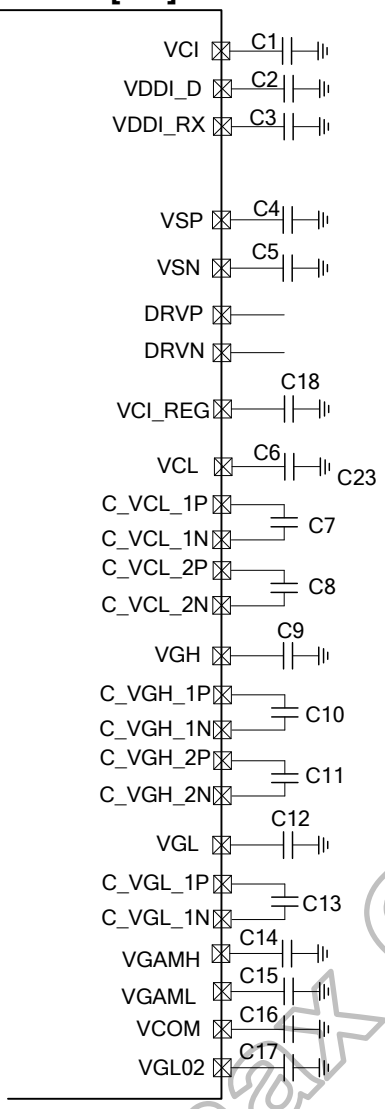
Component	Value
C1	2.2uF/10V
C2	2.2uF/6V
C3	2.2uF/6V
C4	2.2uF/10V
C5	2.2uF/10V
C6	1uF/6V
C7	1uF/6V
C8	1uF/6V
C9	1uF/25V
C10	1uF/16V
C11	1uF/16V
C12	1uF/25V
C13	1uF/16V
C14	1uF/10V
C15	1uF/10V
C16	1uF/6V
C17	1uF/25V
C18	1uF/6V
D1,D2	VF<0.4V /20mA, VR>30V recommand diode :RB521S-30
P1	NMOS
P2	PMOS
L1	TBD
L2	TBD

5.3 PWRMD [1:0] =10b



Component	Value
C1	2.2uF/10V
C2	2.2uF/6V
C3	2.2uF/6V
C4	2.2uF/10V
C5	2.2uF/10V
C6	1uF/6V
C7	1uF/6V
C8	1uF/6V
C9	1uF/25V
C10	1uF/25V
C11	1uF/10V
C12	1uF/10V
C13	1uF/6V
C14	1uF/25V
C15	1uF/6V

5.4 PWRMD [1:0] =11b



Component	Value
C1	2.2uF/10V
C2	2.2uF/6V
C3	2.2uF/6V
C4	2.2uF/10V
C5	2.2uF/10V
C6	1uF/6V
C7	1uF/6V
C8	1uF/6V
C9	1uF/25V
C10	1uF/16V
C11	1uF/16V
C12	1uF/25V
C13	1uF/16V
C14	1uF/10V
C15	1uF/10V
C16	1uF/6V
C17	1uF/25V
C18	1uF/6V

5.5 Power on/off sequence

5.5.1 Power on sequence PWRMD [1:0] =00b

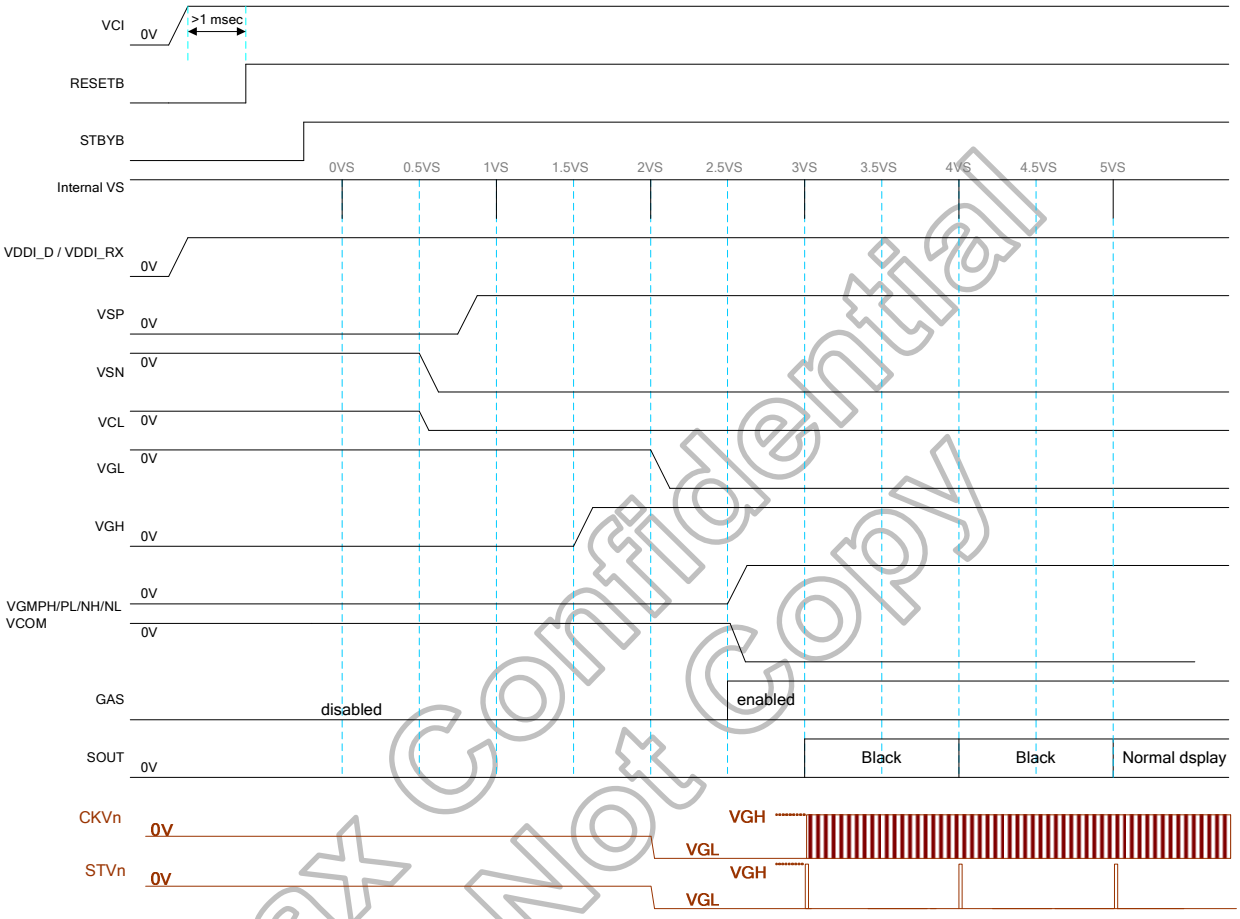


Figure 5.1: Power on sequence with PWRMD[1:0]=00b

5.5.2 Power off sequence PWRMD [1:0] =00b

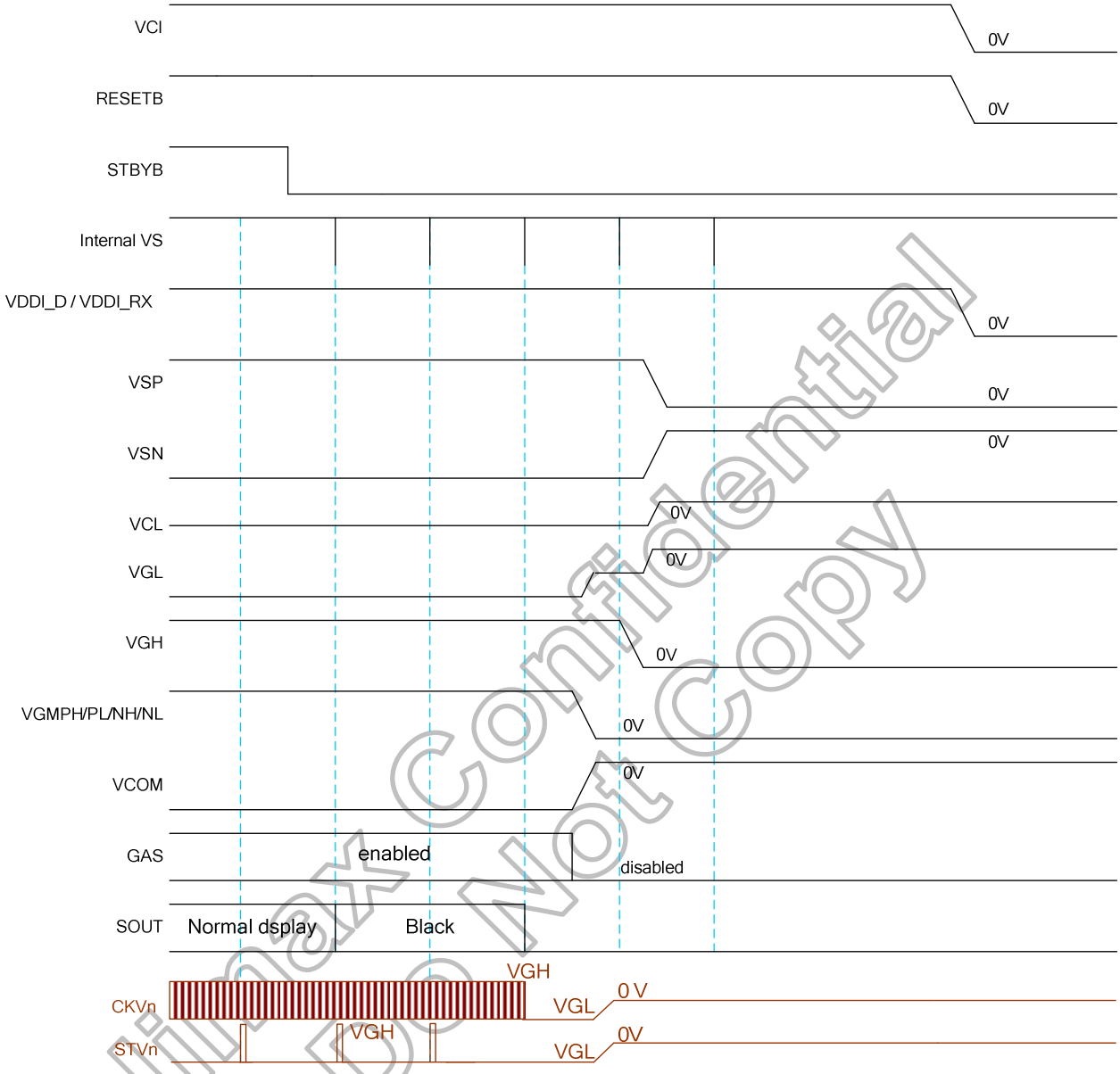


Figure 5.2: Power sequence in power off or standby mode with PWRMD[1:0]=00b

5.5.3 Power on sequence PWRMD [1:0]=01b

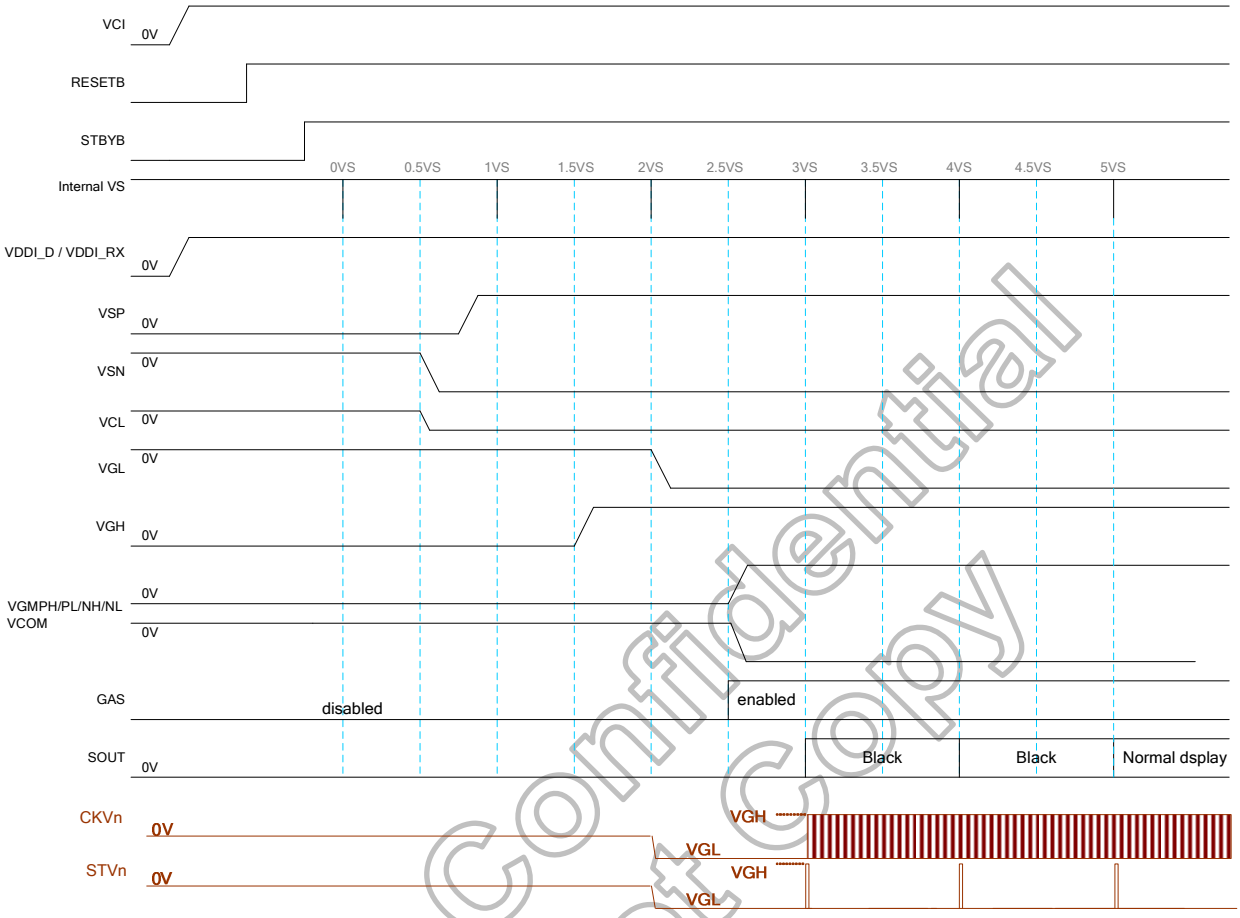


Figure 5.3: Power on sequence with PWRMD[1:0]=01b

5.5.4 Power off sequence PWRMD [1:0]=01b

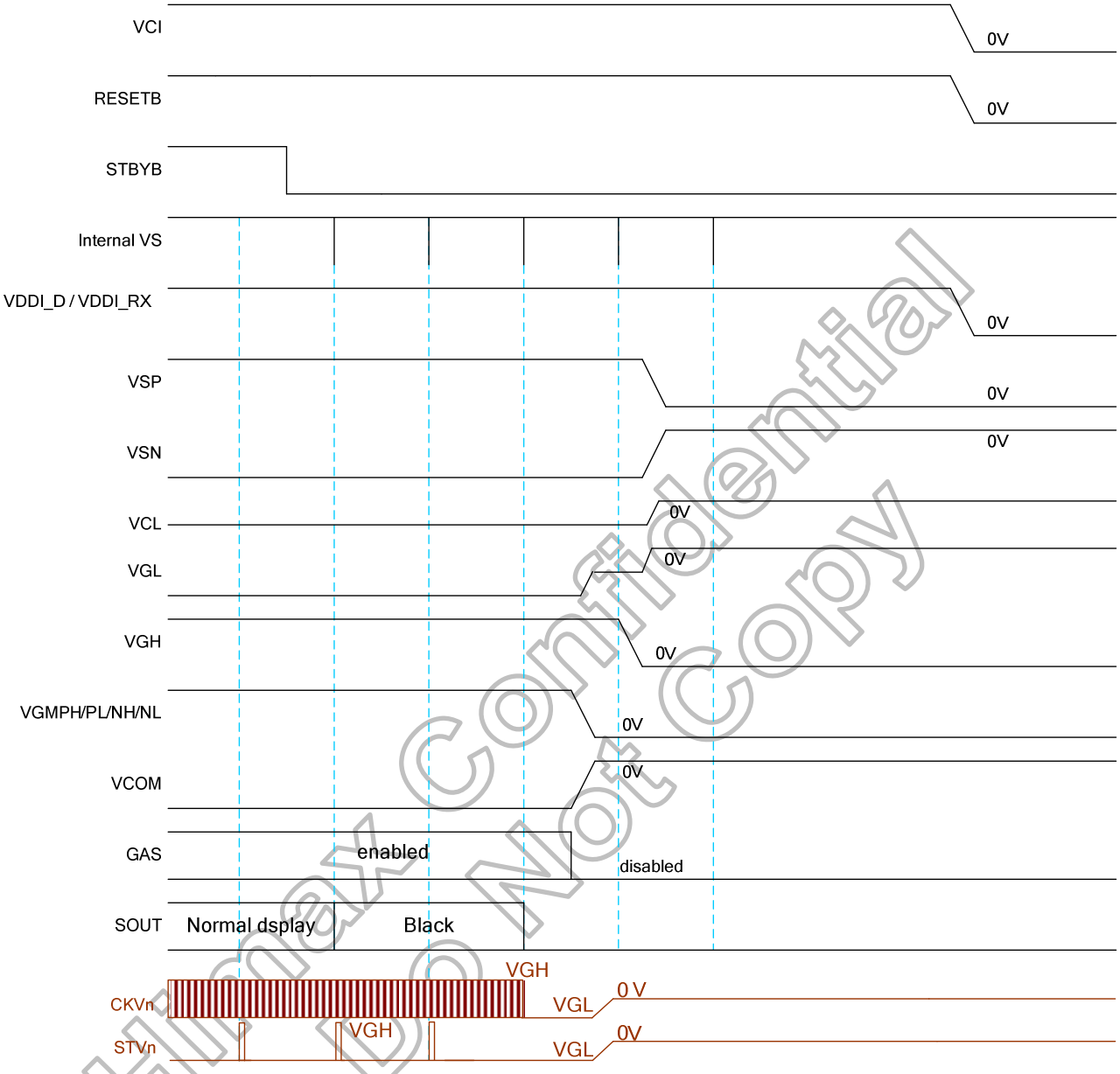


Figure 5.4: Power sequence in power off or standby mode with PWRMD[1:0]=01b

5.5.5 Power on sequence PWRMD [1:0]=10b

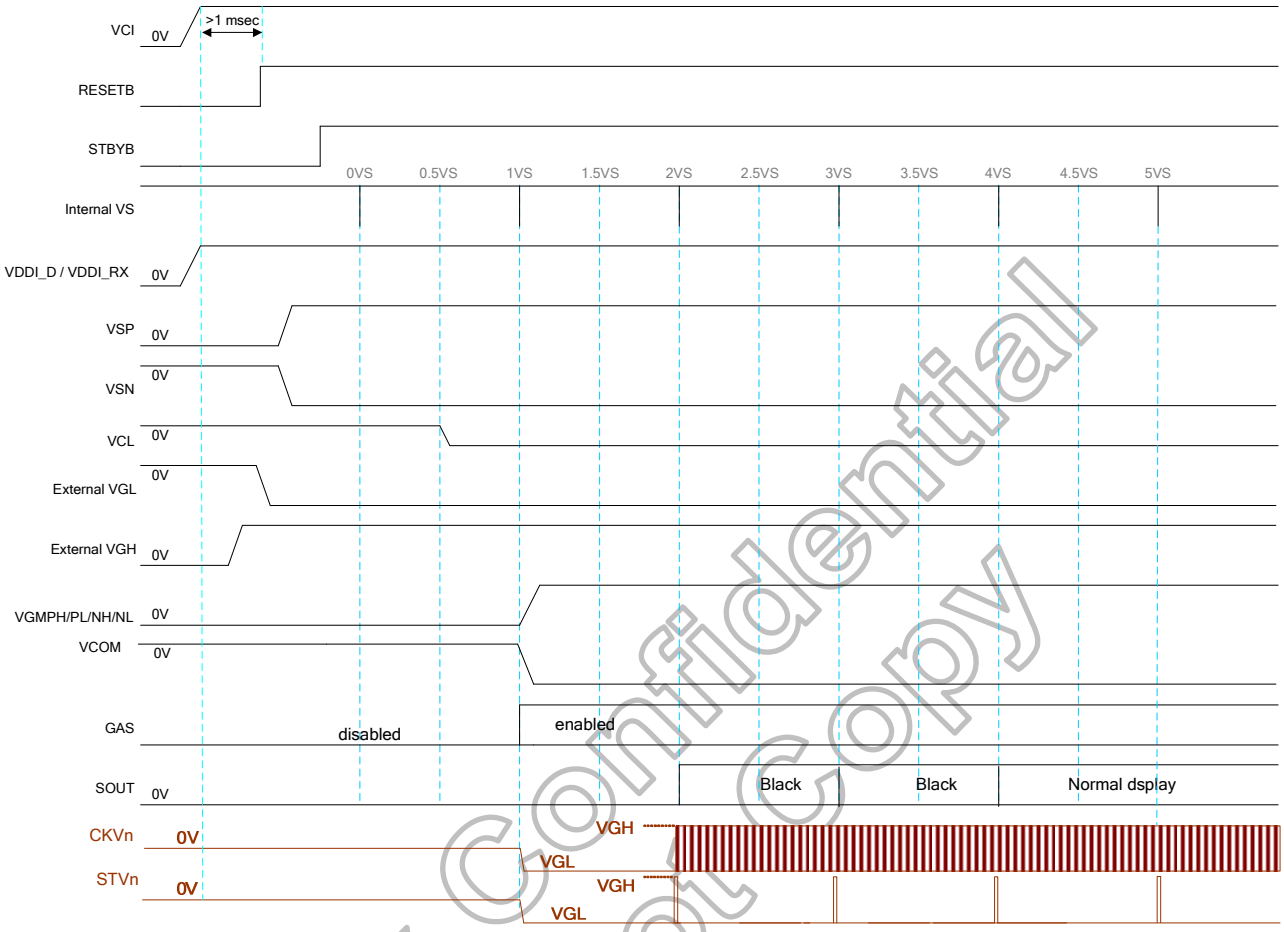


Figure 5.5: Power on sequence with PWRMD[1:0]=10b

5.5.6 Power off sequence PWRMD[1:0]=10b

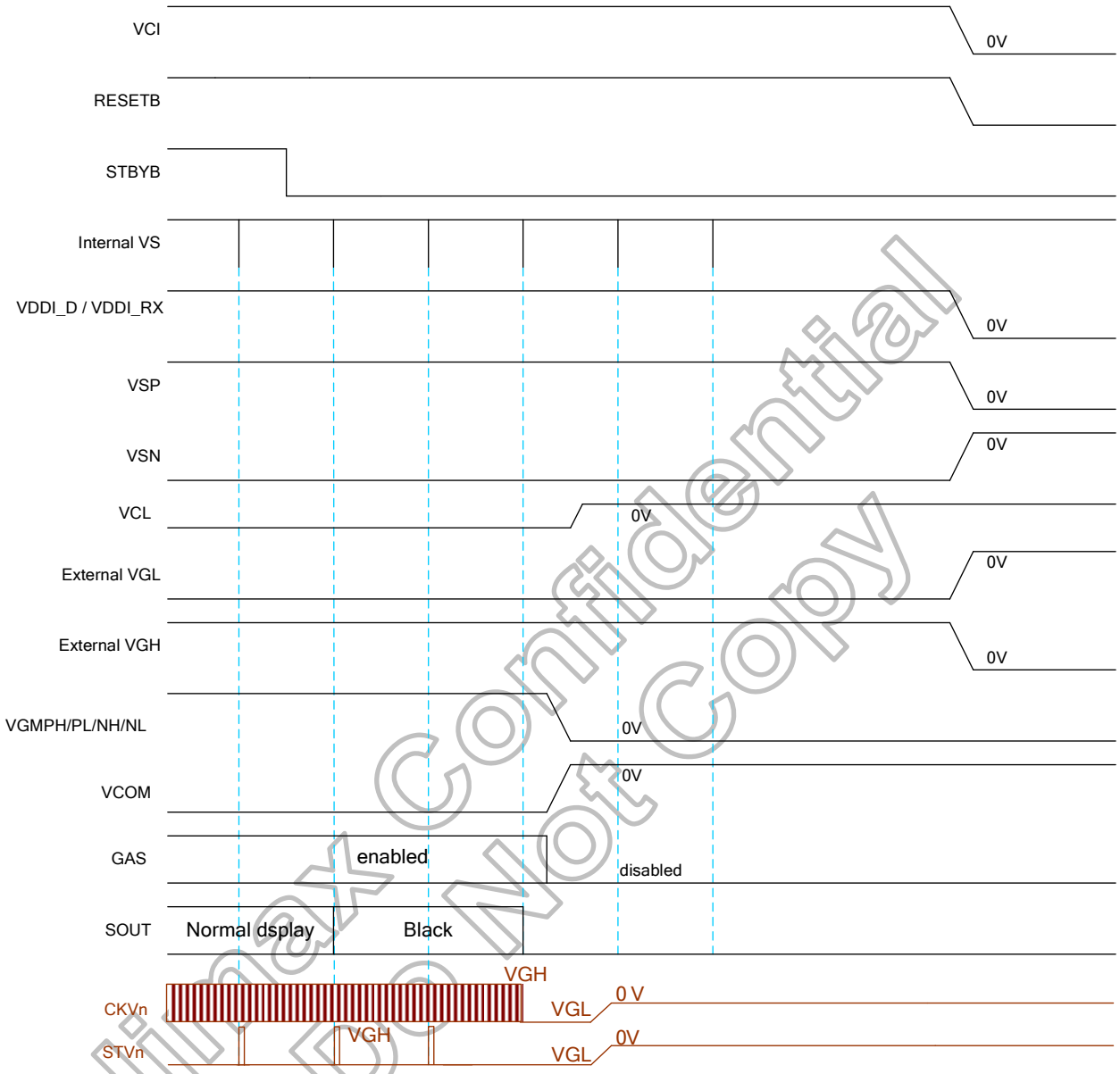


Figure 5.6: Power sequence in power off or Standby mode with PWRMD[1:0]=10b

5.5.7 Power on sequence PWRMD[1:0]=11b

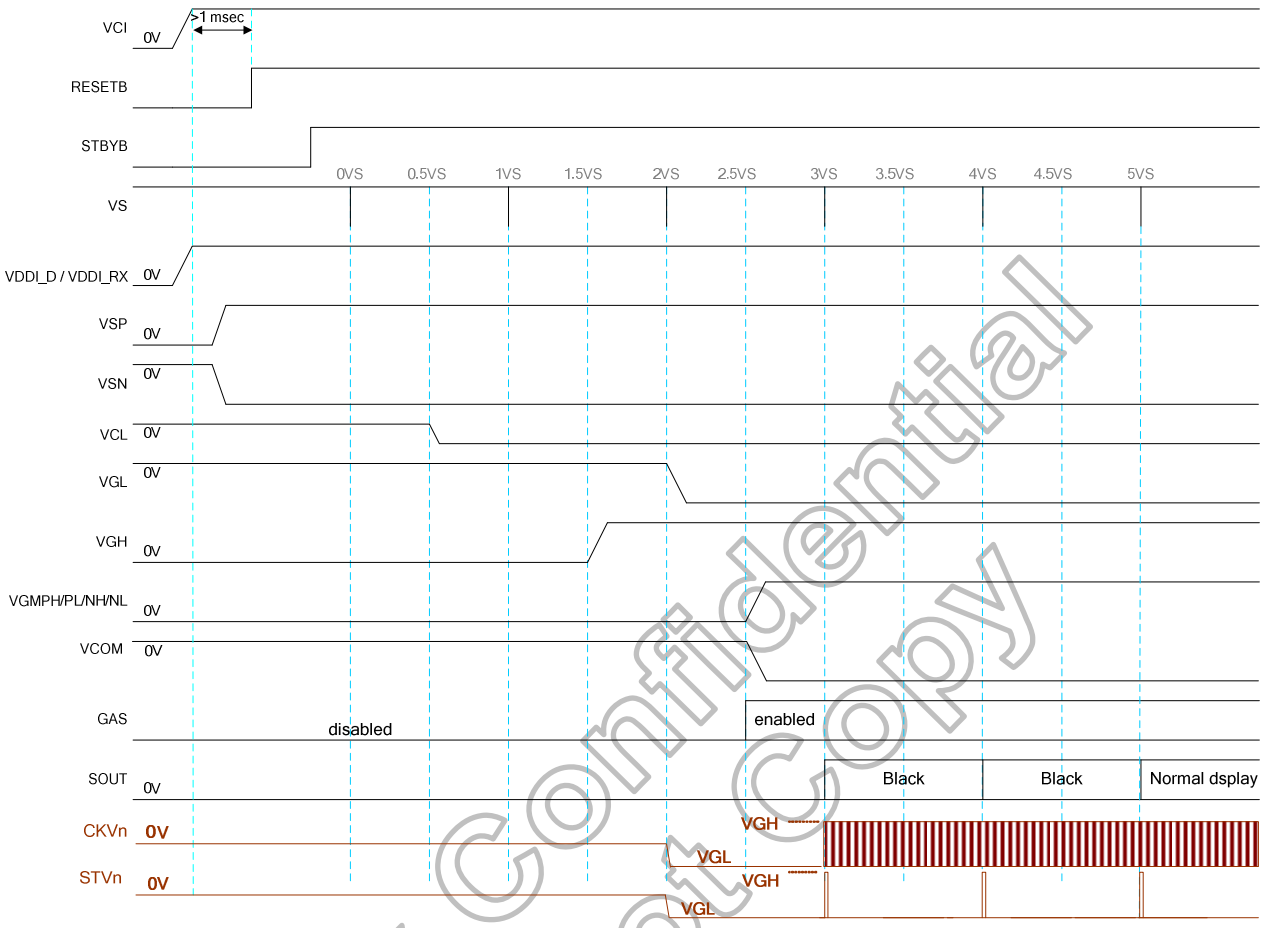


Figure 5.7: Power on sequence with PWRMD[1:0]=11b

5.5.8 Power off sequence PWRMD[1:0]=11b

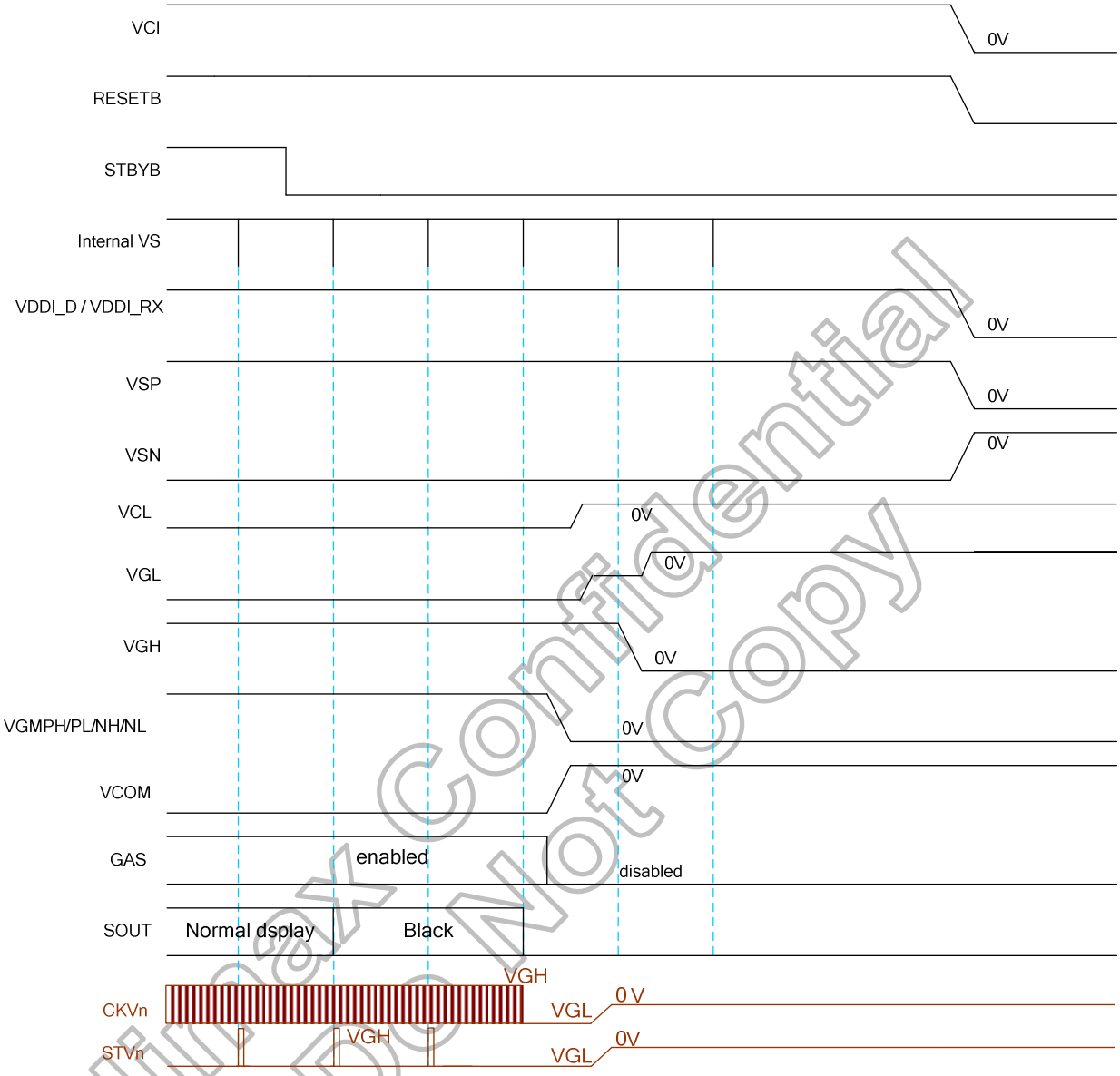


Figure 5.8: Power sequence in power off or Standby mode with PWRMD[1:0]=11b

6. Panel Application

The HX8260-A supports the resolution of 800RGBx1280, 768RGBx1024 720RGBx1280, and 600RGBx1024

The TCON also can generate gate controller timing. These signals can support for general gate driver or GOA **(Gate driver on Array)**.

6.1 Display resolution

6.1.1 Display resolution configuration

Resolution selection can set by hardware or register. Hardware pin name is ERR_RES1 and LNSW_RES0. Register address is locates 0xB3 at page0. The relationship between pin and register is shows below.

ERR_RES1	LNSW_RES0	Resolution	Valid source channel		Disable channel
0	0	600RGBx1024	1**(SL1)**~900	1501 ~2400**(SR1)**	901~1500
0	1	720RGBx1280	1**(SL1)**~1080	1321 ~2400**(SR1)**	1081~1321
1	0	768RGBx1024	1**(SL1)**~1152	1249 ~2400**(SR1)**	1153~1248
1	1	800RGBx1280	1**(SL1)**~1200	1201 ~2400**(SR1)**	-

Note: (1) Blue mark is typical application.
(2) For zigzag panel type, TCON will enable SR1 and SL1 channel.
For strip panel type, TCON will disable SR1 and SL1 channel.

Table 6.1 : Display resolution setting

6.2 GOA connection

The HX8260-A can support GOA/GIP **(Gate driver on array)** function.

GOA output pin define can set by register. A multiplexer is built in GOA function that selects one of several GOA signals. GOA function showed as below.The detail GOA output signal setting please refer application note.

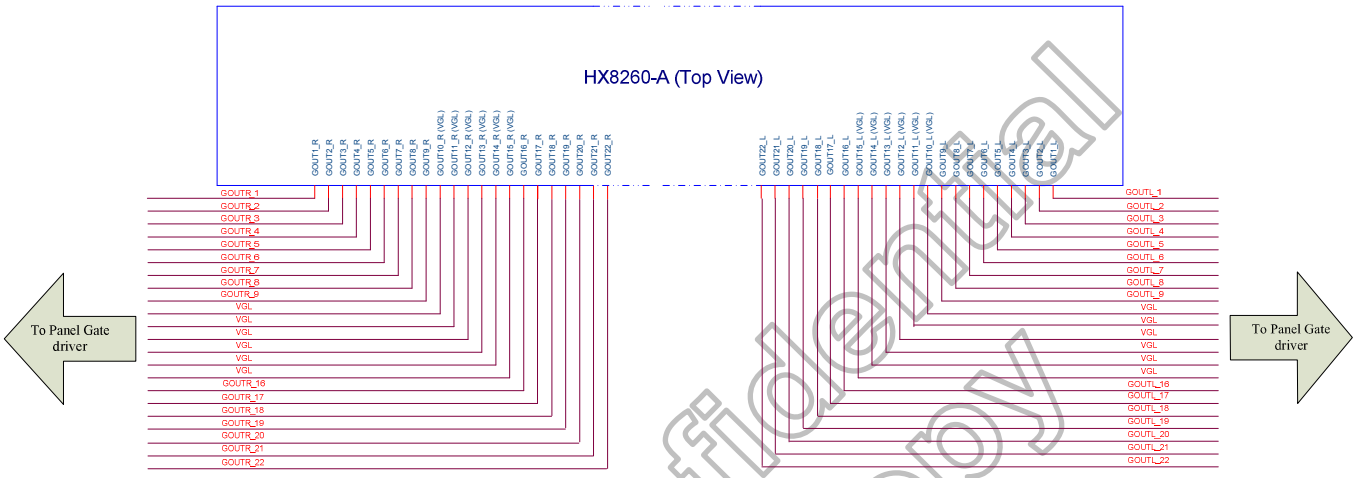


Figure 6.1: GOA wire example

6.3 Panel Structure

6.3.1 Driving method for panel structure

HX8260-A can support 2 types of driving method – stripe and zigzag. User could control Register: ZIGZAG_SEL and ZTYPE_SEL [1:0] select Panel type as following Figure:

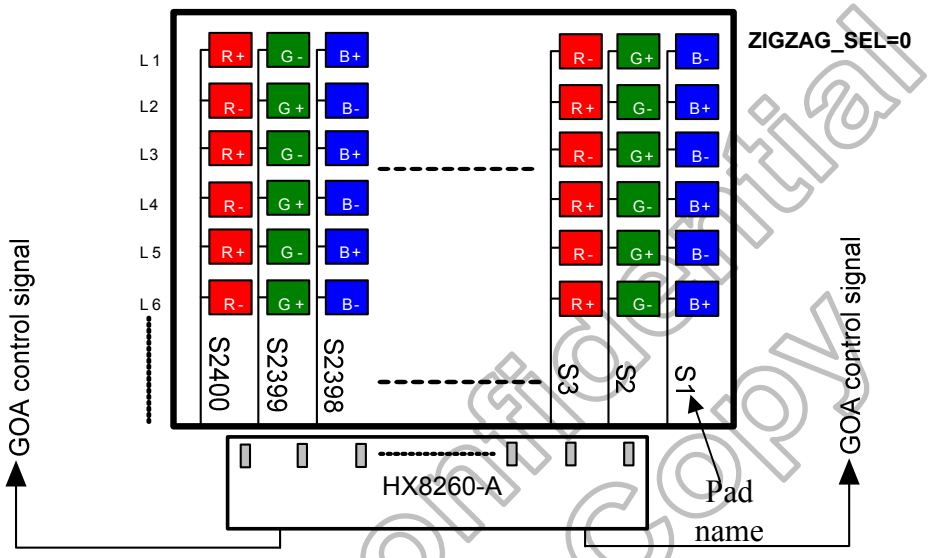


Figure 6.2 : Stripe driving method

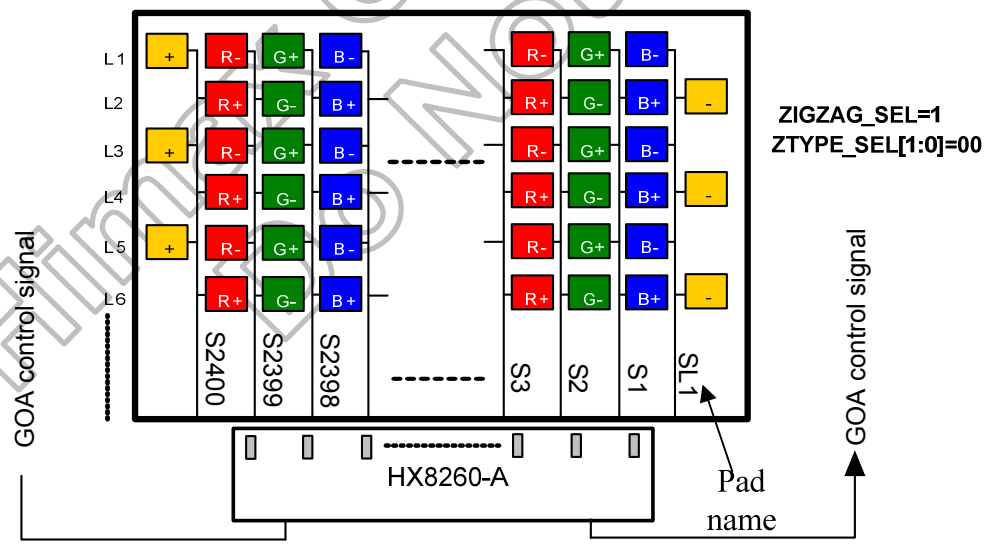


Figure 6.3: Zigzag type0 driving method

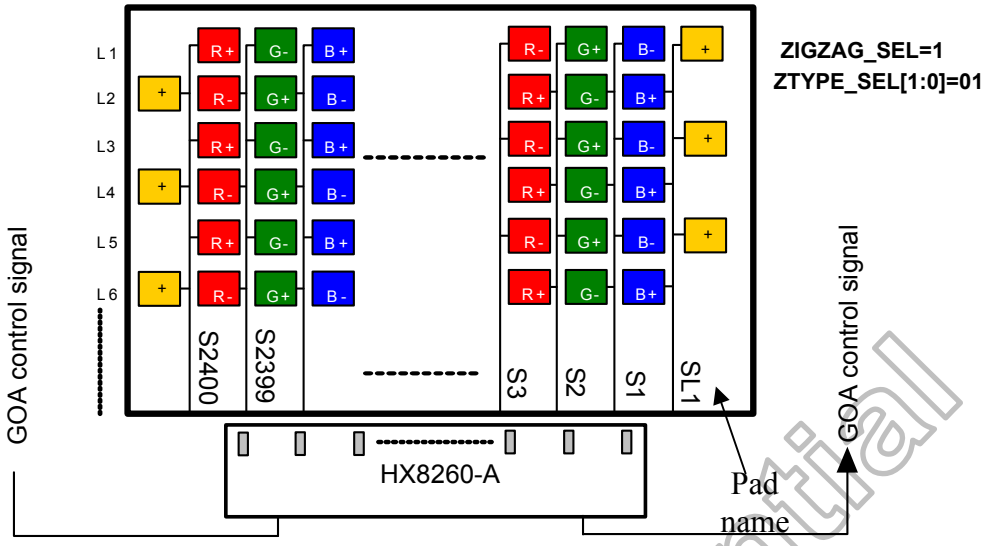


Figure 6.4: Zigzag type1 driving method

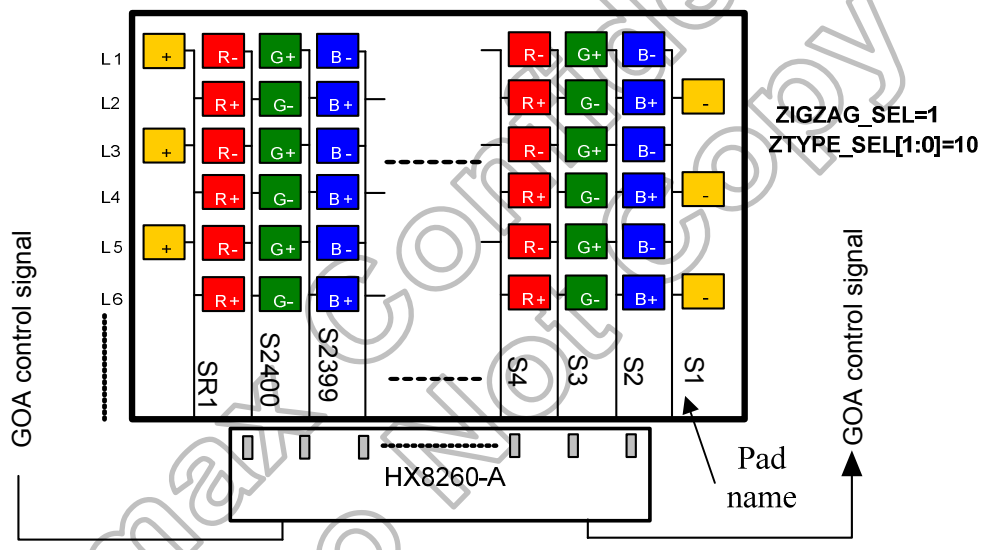


Figure 6.5: Zigzag type2 driving method

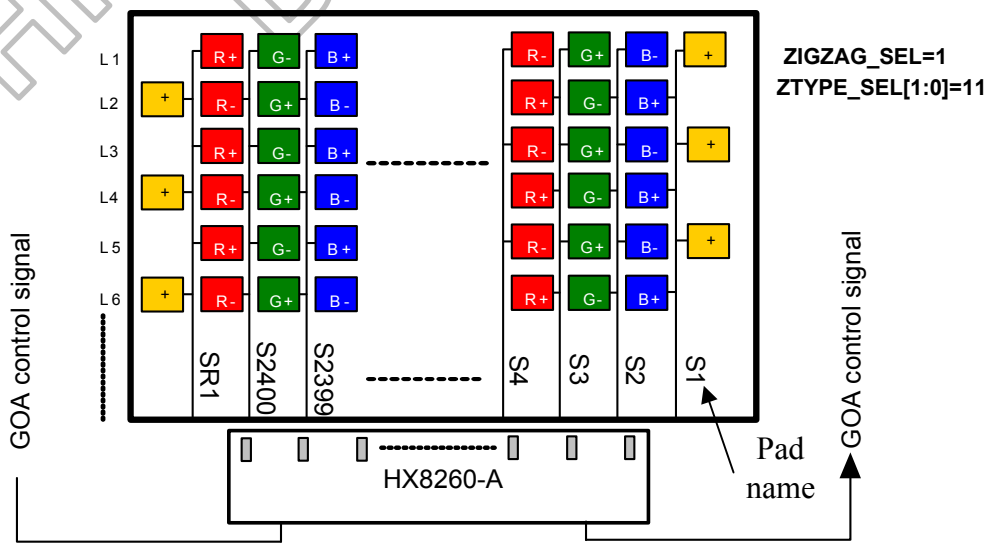


Figure 6.6: Zigzag type3 driving method

6.4 Input interface and pin mapping

HX8260-A support MIPI and LVDS interface,user can select input interface by IF_SEL pin

6.4.1 MIPI interface (IF_SEL=1)

When IF_SEL=1 HX8260-A set to MIPI interface,user could configure data lane arrangement by hardware pin PNSW_SCL, LNSW_CSB and LNSW_RES0.

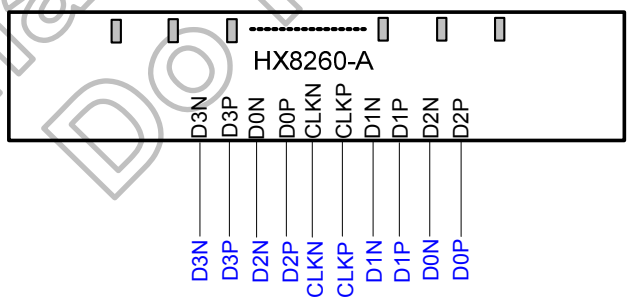
- PNSW_SCL is for swap differencial pair polarity.
- LNSW_RES0 and LNSW_CSB are for swap MIPI data pair.

Following table showed the MIPI lane swap pin mapping:

Configuration \ Pad name			D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N
PNSW_SCL	LNSW_CSB	LNSW_RES0	MIPI lanes mapping table									
0	0	0	D3P	D3N	D2P	D2N	CLKP	CLKN	D1P	D1N	D0P	D0N
0	0	1	D3P	D3N	D0P	D0N	CLKP	CLKN	D1P	D1N	D2P	D2N
0	1	0	D0P	D0N	D1P	D1N	CLKP	CLKN	D2P	D2N	D3P	D3N
0	1	1	D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N
1	0	0	D3N	D3P	D2N	D2P	CLKN	CLKP	D1N	D1P	D0N	D0P
1	0	1	D3N	D3P	D0N	D0P	CLKN	CLKP	D1N	D1P	D2N	D2P
1	1	0	D0N	D0P	D1N	D1P	CLKN	CLKP	D2N	D2P	D3N	D3P
1	1	1	D2N	D2P	D1N	D1P	CLKN	CLKP	D0N	D0P	D3N	D3P

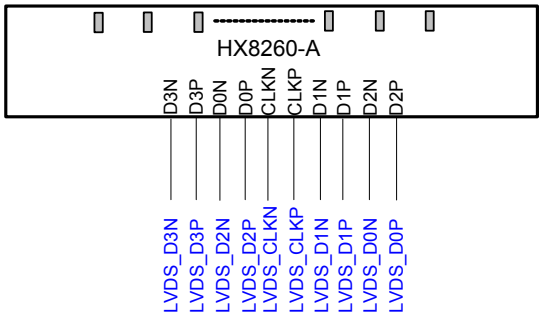
Setting Example:

PNSW_SCL=0, LNSW_CSB=1, LNSW_RES0



6.4.2 LVDS interface (IF_SEL=0)

When IF_SEL=0 HX8260-A set to LVDS interface, data lane could not be swapped.Please connection as following figure:



7. Interface

7.1 LVDS interface

The HX8260-A has a built-in single pixel LVDS receiver that converts data from differential serialized format to parallel output.

LVDS mode data input format

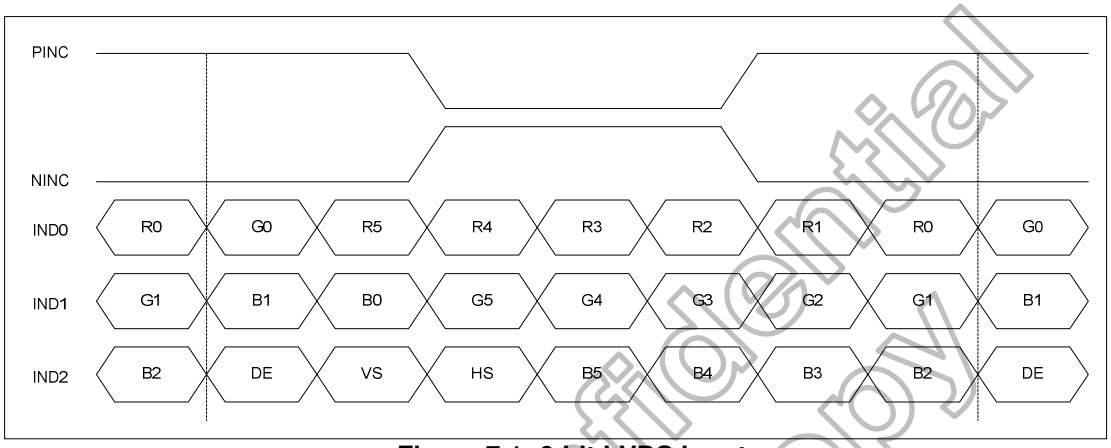


Figure 7.1: 6-bit LVDS input

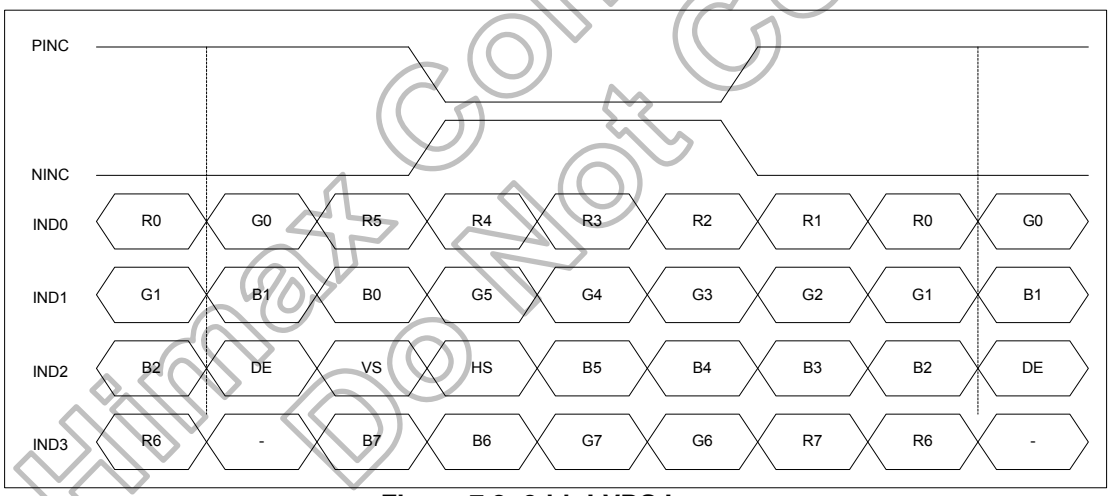
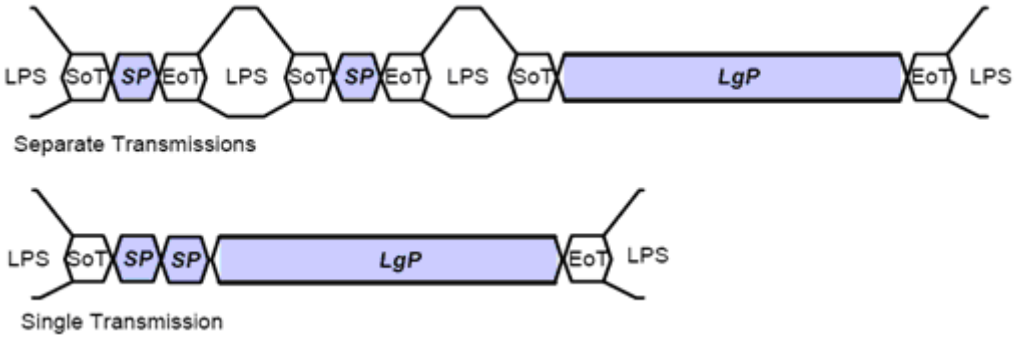


Figure 7.2: 8-bit LVDS Input

7.2 MIPI interface

7.2.1 DSI protocol

The protocol layer appends packet-protocol information and headers. The receiver side of a DSI Link performs the converse of the transmitter side, decomposing the packet into parallel data, signal events and commands. The DSI protocol permits multiple packets which is useful for events such as peripheral initialization, where many registers may be loaded separate write commands at system startup. Figure 7.3 illustrates multiple HS Transmission packets.

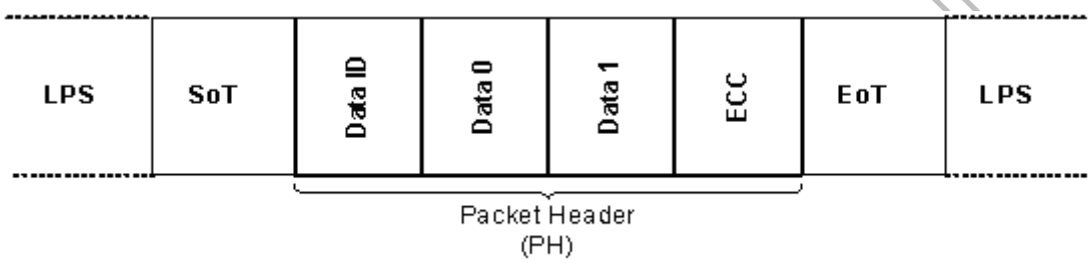


Note: (1) LPS: Low power state
SoT: Start of Transmission
SP: Short Packet
LgP: Long Packet
EoT: End of Transmission

Figure 7.3: Multiple packets transmission

The packet includes two types which are Long packet and Short packet. The first byte of the packet, the Data Identifier **(DI)**, includes information specifying the type of the packet. Command Mode systems send commands and an associated set of parameters, with the number of parameters depending on the command type.

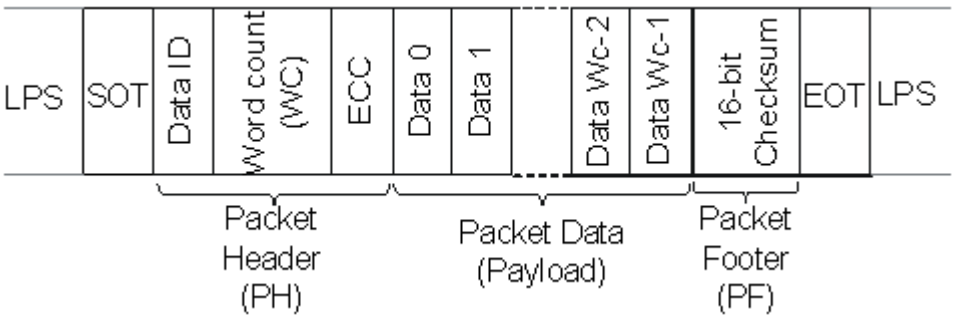
Short packets are four bytes in length including the ECC. Short packet is used for most Command Mode commands and associated parameters. Where Short packets format include an 8-bit Data ID followed by two command or data bytes and an 8-bit ECC. Figure 7.4 shows the structure of the Short packet.



Note: (1) DI **(Data ID)**: Contain Virtual Channel Identifier and Data Type.
ECC **(Error Correction Code)**: The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Short Packet.

Figure 7.4: Structure of the short packet

Long packets specify the payload length using a two-byte Word Count field and then the payload maybe from 0 to 65,535 bytes in length. Thus Long packets permit transmission of large blocks of pixel or other data.. Figure 7.5 shows the structure of the Long packet. Long Packet Header composed of three elements: an 8-bit Data Identifier, a 16-bit Word Count, and 8-bit ECC. An application-specific Data Payload has Word Count * bytes following the Packet Header. The Packet Footer has one element, a 16-bit checksum. Long packets can be from 6 to 65,541 bytes in length.
Where 65,541 bytes = 4 bytes PH + (2^{16}-1) bytes Payload + 2 bytes PF



Note: (1) DI **(Data ID)**: Contain Virtual Channel Identifier and Data Type.
WC **(Word Count)**: The receiver uses WC to determine the packet end.
ECC **(Error Correction Code)**: The Error Correction Code allows single-bit errors to be corrected and 2-bit errors to be detected in the Packet Header.
PF **(Packet Footer)**: Mean 16-bit Checksum.

Figure 7.5: Structure of the long packet

According to packet form, basic elements include DI and ECC. Table 7.1 shows format of Data ID.

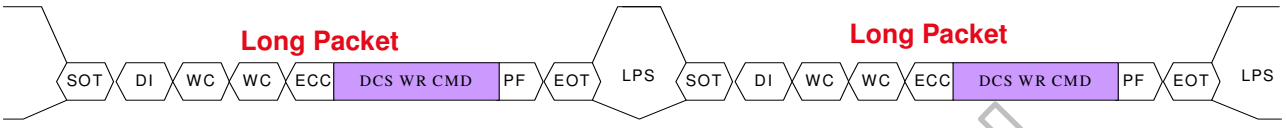
DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0
VC **(Virtual channel)**		DT **(Data type)**					

Table 7.1: Format of data ID

DI[7:6] ➔ These two bits identify the data as directed to one of four virtual channels.
DI[5:0] ➔These six bits specify the Data Type, which specifies the size, format and, in some cases, the interpretation of the packet contents.

Due to Data Type **(DT)** mean format of transmission type, following figure Short- / Long-packet transmission command sequence.
Long packet writes Command / Parameters / Pixel Data

Using Long Packet to access Command



Short packet writes Command / Parameters

Using Short Packet to access Command

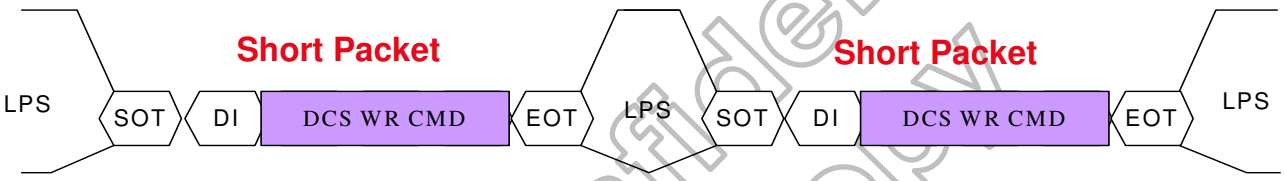
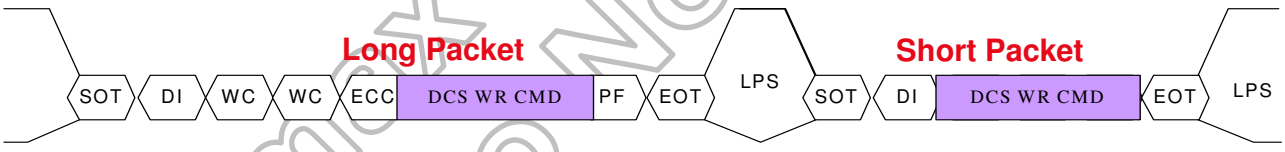
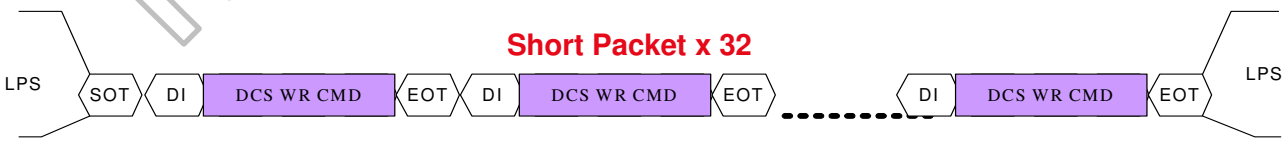


Figure 7.6: Show short- / long-packet transmission command sequence

Using Long Packet and Short Packet to access Command



Don’t send more 32 command in one HS



Brust write

7.2.2 Processor to peripheral (forward direction) packets data types

The set of transaction types sent from the host processor to a peripheral, such as a display module, are shown in Table 7.2 Data Types for Processor-sourced Packets.

Data type, hex	Data type, binary	Description packet	Size
01h	00 0001	Sync event, V Sync start.	Short
11h	01 0001	Sync event, V Sync end.	Short
21h	10 0001	Sync event, H Sync start.	Short
31h	11 0001	Sync event, H Sync end.	Short
08h	00 1000	End of transmission packet **(EoTp)**.	Short
02h	00 0010	Color Mode **(CM)** off command.	Short
12h	01 0010	Color Mode **(CM)** on command.	Short
22h	10 0010	Shut down peripheral command.	Short
32h	11 0010	Turn on peripheral command.	Short
03h	00 0011	Generic short WRITE, no parameter.	Short
13h	01 0011	Generic short WRITE, 1 parameter.	Short
23h	10 0011	Generic short WRITE, 2 parameter.	Short
04h	00 0100	Generic READ, no parameter.	Short
14h	01 0100	Generic READ, 1 parameter.	Short
24h	10 0100	Generic READ, 2 parameters.	Short
05h	00 0101	DCS short WRITE, no parameter.	Short
15h	01 0101	DCS short WRITE, 1 parameter.	Short
06h	00 0110	DCS READ, no parameters.	Short
37h	11 0111	Set maximum return packet size.	Short
09h	00 1001	Null packet, no data.	Long
19h	01 1001	Blanking packet, no data.	Long
29h	10 1001	Generic long write.	Long
39h	11 1001	DCS long write/write_LUT command packet.	Long
0Eh	00 1110	Packed pixel stream, 16-bit RGB, 5-6-5 format.	Long
1Eh	01 1110	Packed pixel stream, 18-bit RGB, 6-6-6 format.	Long
2Eh	10 1110	Loosely packed pixel stream, 18-bit RGB, 6-6-6 format.	Long
3Eh	11 1110	Packed pixel stream, 24-bit RGB, 8-8-8 format.	Long
X0h and XFh, unspecified	xx 0000 xx 1111	DO NOT USE. All unspecified codes are reserved.	-

Table 7.2: Data types for processor-sourced packets

Under tables list all detail function of all data types

Sync event (H start, H end, V start, V end), data type=xx 0001 (x1h)		
Data type, hex	**Function description**	**Number of bytes**
01h	V Sync start, start of VSA pulse.	4 bytes **(DI + 00h + 00h + ECC)**
11h	V Sync end, end of VSA pulse.	
21h	H Sync start, start of HSA pulse.	
31h	H Sync end, end of HSA pulse.	

Note: (1) V Sync start and V Sync end event represents the start and end of the VSA, respectively. Similarly H Sync start and H Sync end event represents the start and end of the HSA, respectively.

End of Transmission packet (EoTp)		
Data type, hex	**Function description**	**Number of bytes**
08h	End of transmission packet **(EoTp)**.	4 bytes **(DI + 00h + 00h + ECC)**

Color mode status (Color Mode On, Color Mode Off)		
Data type, hex	**Function description**	**Number of bytes**
02h	Color mode on that switches a video mode display module to a low-color mode for power saving.	4 bytes **(DI + 00h + 00h + ECC)**
12h	Color mode off that switches a video mode display module from low-color display to normal display.	

Display status (shutdown command, turn-on command)		
Data type, hex	**Function description**	**Number of bytes**
22h	Shutdown peripheral command that turns off the display in a video mode display for power saving.	4 bytes **(DI + 00h + 00h + ECC)**
32h	Turn on peripheral command that turns on the display in video mode display for normal display.	

Note: (1) When use shutdown command; interface shall remain powered in order to receive the turn-on, or wake-up, command.

Generic Short WRITE Packet with 0,1,2 parameter		
Data type, hex	**Function description**	**Number of bytes**
03h	Generic Short WRITE, no parameter.	**(DI + 00h + 00h + ECC)**
13h	Generic Short WRITE, 1 parameter.	**(DI + P1 + 00h + ECC)**
23h	Generic Short WRITE, 2 parameters. **(P1=Addr, P2=Data)**	**(DI + P1 + P2 + ECC)**

Note: (1) P1=parameter1, P2=parameter2.

Generic READ Request with 0,1,2 parameter		
Data type, hex	**Function description**	**Number of bytes**
04h	Generic READ, no parameter.	**(DI + 00h + 00h + ECC)**
14h	Generic READ, 1 parameter. **(P1=Addr)** only read 1 Data.	**(DI + P1 + 00h + ECC)**
24h	Generic READ, 2 parameters. **(P1=Addr, P2=Burst read length)**	**(DI + P1 + P2 + ECC)**

Note: (1) P1=parameter1, P2=parameter2.

DCS Show WRITE Command with 0,1 parameter		
Data type, hex	**Function description**	**Number of bytes**
05h	DCS Short WRITE, no parameter.	**(DI + DCS + 00h + ECC)**
15h	DCS Short WRITE, 1 parameter. **(P1=DCS's data)**	**(DI + DCS + P1 + ECC)**

Note: (1) P1=parameter1, DCS=DCS command.

DCS command setting		
Data type, hex	**Function description**	**Number of bytes**
06h	DCS Read command, the returned data may be of Short or Long packet format.	4 bytes **(DI + DCS CMD.+00h + ECC)**
39h	DCS Long Write/ Write _ LUT Command is used to send larger blocks of data to a display module that implements the Display Command Set.	Up to 65535 bytes **(DI + WC + ECC + DCS CMD. + Payload DATA(WC-1) + PF)**

Note: (1) For write part, If DCS Short Write command is followed by BTA, the peripheral shall respond with ACK when no error was detected in the transmission **(Host → Slave)**. Unless an error was detected, the peripheral shall respond with Acknowledge with Error Report.
(2) When use DCS Read Command, the Set Max Return Packet Size command will limit the size of returning packets.
(3) The peripheral shall respond to DCS Read Command Request in one of the following ways:
- ◆ If an error was detected and corrected in Packet Header field by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
- ◆ If no error was detected by the peripheral, it shall send the requested READ packet **(Short or Long)** with appropriate ECC and Checksum, if either or both features are enabled.

(4) One byte <= Length of payload DATA <= 2^{16}-1

Generic Long Write		
Data type, hex	**Function description**	**Number of bytes**
29h	Generic Long Write Packek is used to transmit arbitrary blocks of data from a host processor to peripheral in a Long packet. Support Burst Write : Parameter_1->MCS Addr**(p1>B0)** Parameter_2->Address's data Parameter_3->Address+1 's data Parameter_4->Address+2 's data : Parameter_N->Address+N-1 's data	Up to 65535 bytes **(DI + WC + ECC + Payload DATA(WC) + PF)**

Note: (1) For write part, If Short Write command is followed by BTA, the peripheral shall respond with ACK when no error was detected in the transmission **(Host → Slave)**. Unless an error was detected, the peripheral shall respond with Acknowledge with Error Report.
(2) When use Read Command, the Set Max Return Packet Size command will limit the size of returning packets.
(3) The peripheral shall respond to Read Command Request in one of the following ways:
- ◆ If an error was detected and corrected in Packet Header field by the peripheral, it shall send *Acknowledge with Error Report*. So the peripheral shall transmit the requested READ data packet with suitable ECC in the same transmission.
- ◆ If no error was detected by the peripheral, it shall send the requested READ packet **(Short or Long)** with appropriate ECC and Checksum, if either or both features are enabled.

(4) One byte <= Length of payload DATA <= 2^{16}-1

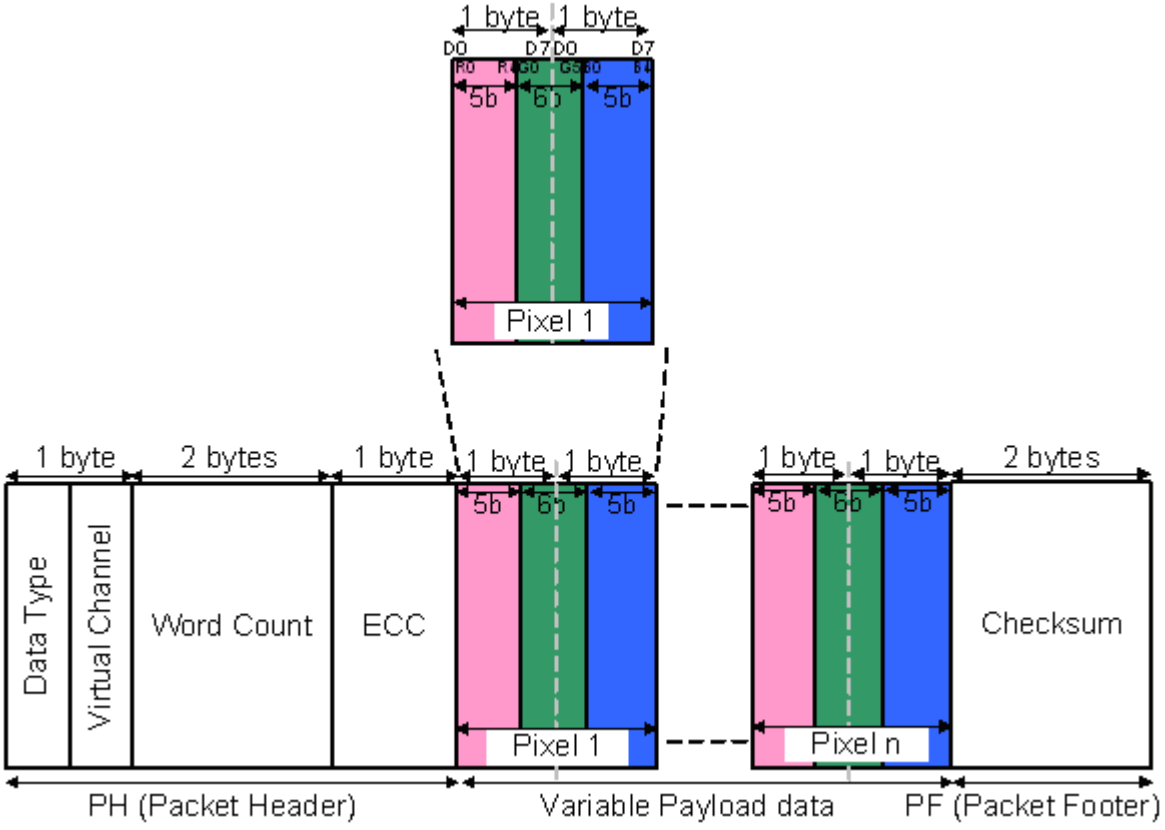
Return packet size setting		
Data type, hex	**Function description**	**Number of bytes**
37h	Set Maximum Return Packet Size that specifies the maximum size of the payload in a Long packet transmitted from peripheral back to the host processor.	4 bytes **(DI + Maximum Return Packet Size + ECC)**

Note: (1) The two-byte value is transmitted with LS byte first. And during a power-on or Reset sequence, the Maximum Return Packet Size shall be set by the peripheral to a default value of one.

Variable data packet		
Data type, hex	**Function description**	**Number of bytes**
09h	Null Packet is a mechanism for keeping the serial Data Lane**(s)** in High-Speed mode while sending dummy data.	Up to 65535 bytes **(DI + WC + ECC + DCS CMD. + Payload DATA + PF)**
19h	Blanking packet is used to convey blanking timing information in a Long packet.	

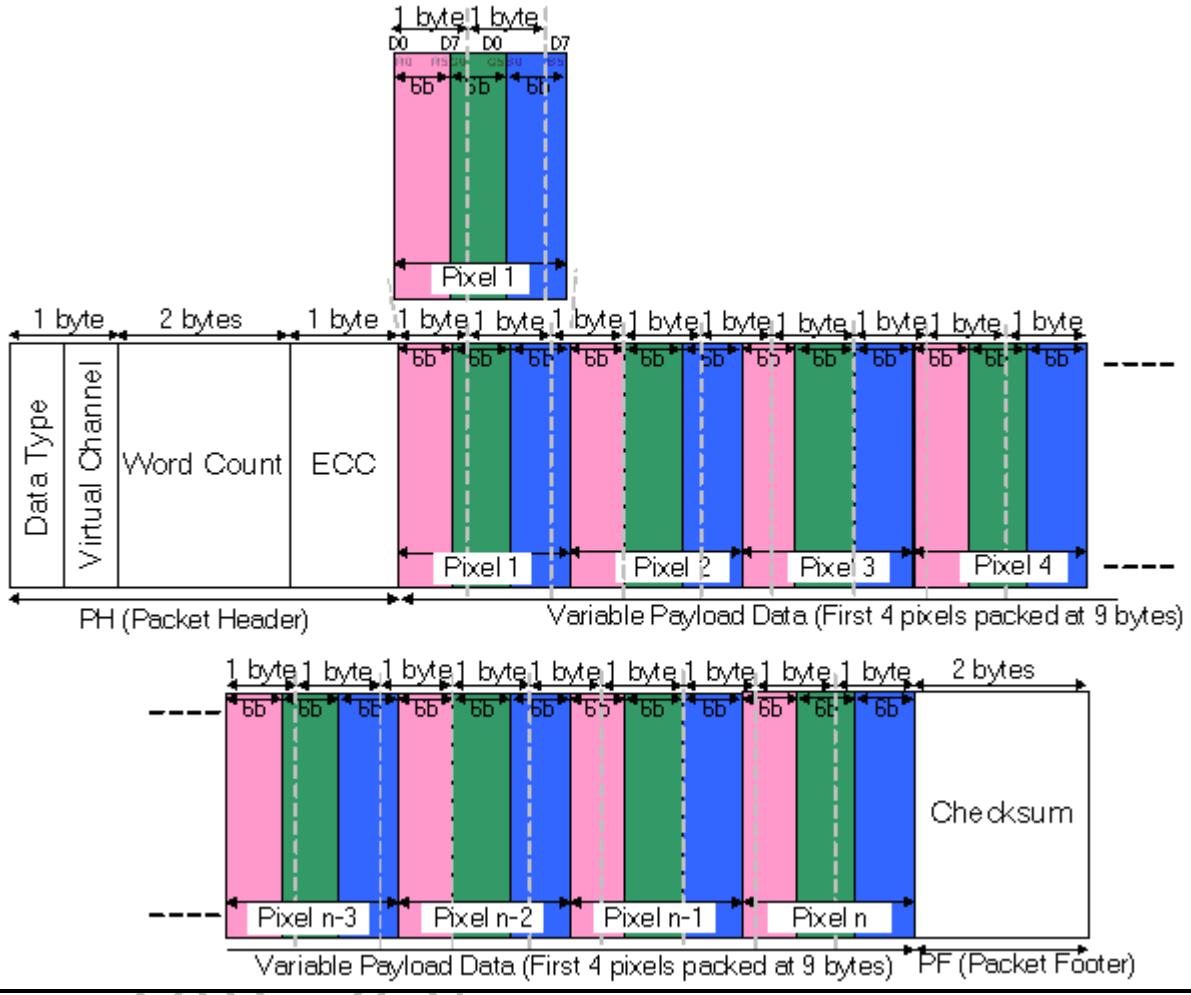
Note: (1) When Null Packet, the Payload Data belong "null" Data, actual data values sent are irrelevant because the peripheral does not capture or store the data.
(2) When Blanking packet, the packet represents a period between active scan lines of a Video Mode display.

Data stream format – 16bit Format		
Data type, hex	**Function description**	**Number of bytes**
0Eh	Packed Pixel Stream 16-Bit Format is used to transmit image data formatted as 16-bit pixels to a Video Mode display module. Pixel format is "**(5 bits)** red, **(6 bits)** green and **(5 bits)** blue".	Up to 65535 bytes **(DI + WC + ECC + DCS CMD. + Payload DATA + PF)**



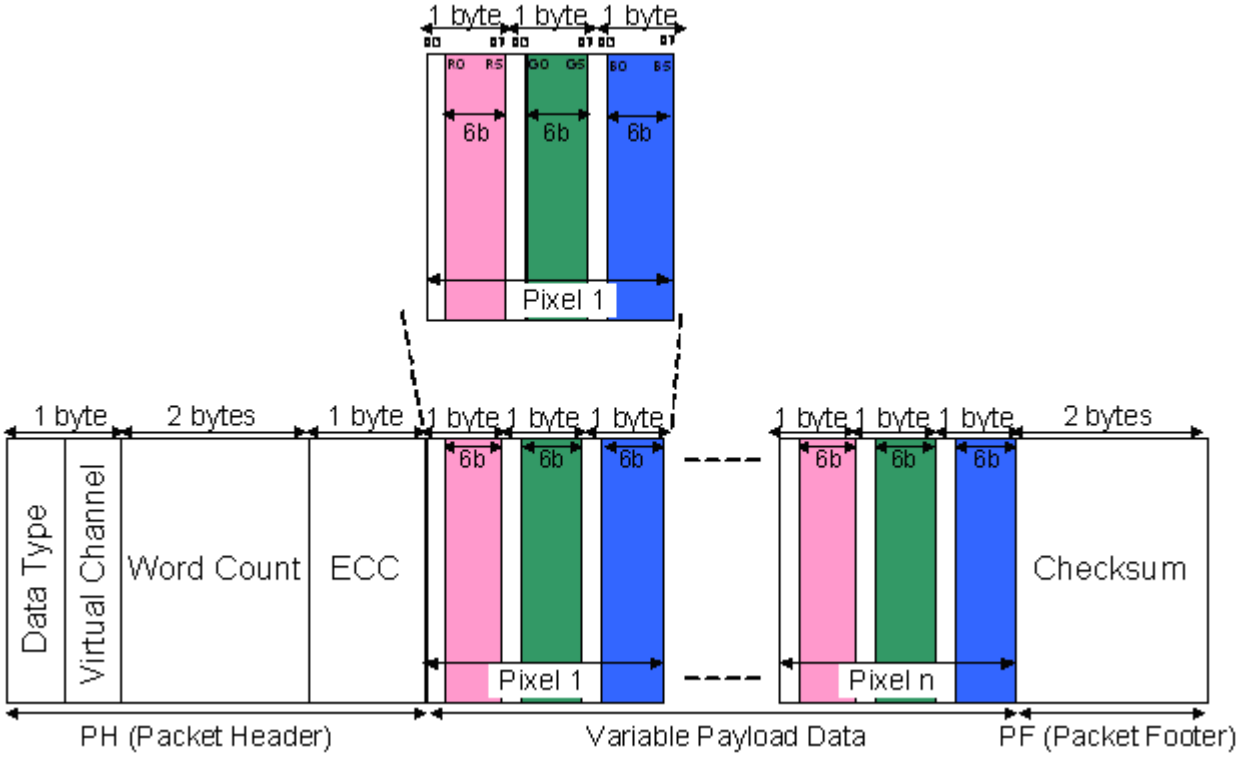
Note: (1) Within a color component, the "LSB is sent first, the MSB last ".

Data stream format – 18bit Format		
Data type, hex	**Function description**	**Number of bytes**
1Eh	Packed Pixel Stream 18-Bit Format is used to transmit image data formatted as 18-bit pixels to a Video Mode display module. Pixel format is "**(6 bits)** red, **(6 bits)** green and **(6 bits)** blue".	Up to 65535 bytes **(DI + WC + ECC + DCS CMD. + Payload DATA + PF)**



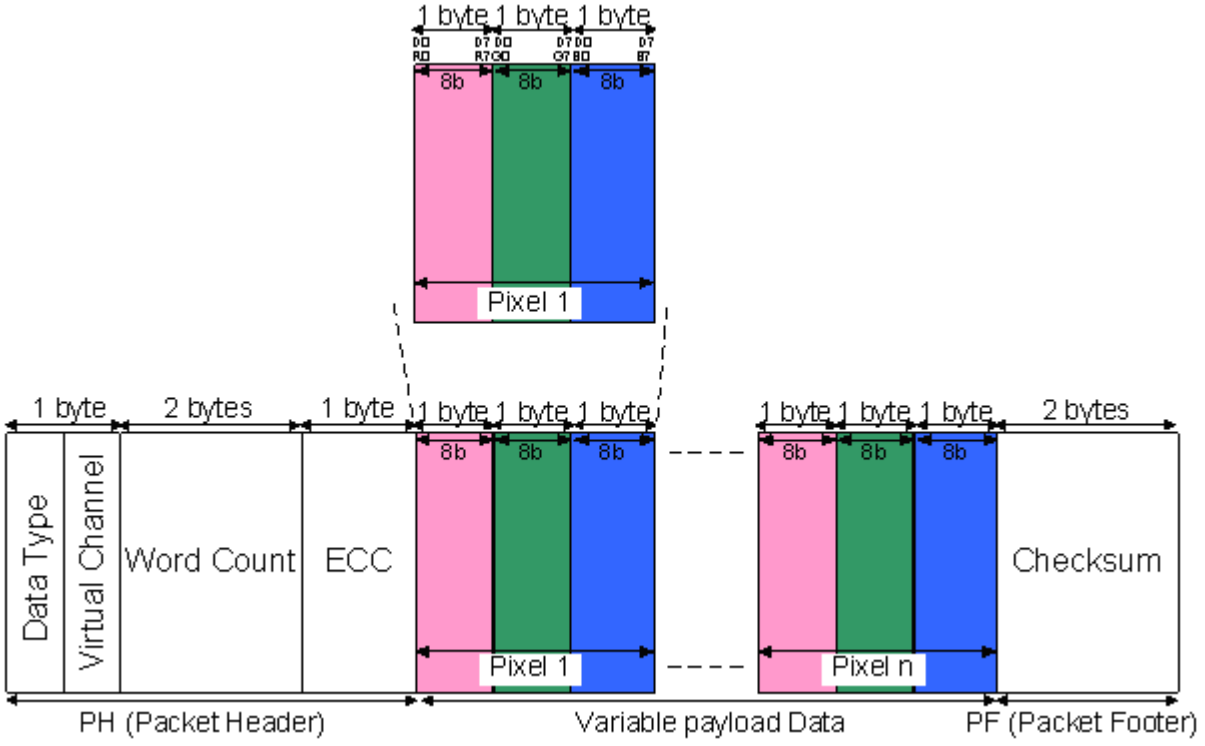
Note: (1) Within a color component, the LSB is sent first and the MSB last and pixel boundaries only line up with byte boundaries every four pixels **(nine bytes)**. Preferably, display modules employing this format have a horizontal extent **(width in pixels)** evenly divisible by four, so no partial bytes remain at the end of the display line data. It is possible to send pixel data that represent a line width that is not a multiple of four pixels, but display logic on the receiver end shall dispose of the extra bits of the partial byte at the end of active display and ensure a "clean start" for the next line.

Data stream format – 18bit Format		
Data type, hex	**Function description**	**Number of bytes**
2Eh	Packed Pixel Stream 18-Bit Format, each R, G, or B color component is one byte form, but the valid pixel bits occupy bits [7:2] and bits [1:0] of are ignored. Pixel format is "**(6 bits)** red, **(6 bits)** green and **(6 bits)** blue".	Up to 65535 bytes **(DI + WC + ECC** **+ DCS CMD.** **+ Payload DATA + PF)**



Note: (1) Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

Data stream format – 24bit Format		
Data Type, Hex	**Function Description**	**Number of bytes**
3Eh	Packed Pixel Stream 24-Bit Format is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. Pixel format is **(8 bits)** red, **(8 bits)** green and **(8 bits)** blue.	Up to 65535 bytes **(DI + WC + ECC + DCS CMD. + Payload DATA + PF)**



Note: (1) Within a color component, the LSB is sent first, the MSB last and With this format, pixel boundaries line up with byte boundaries every three bytes.

7.2.3 Peripheral to processor (reverse direction) packet data type

Table 7.3 present the complete set of peripheral-to-processor Data Types

Data type, hex	Data type, binary	Description packet	Size
0x02	00 0010	Acknowledge and error report.	Short
0x08	00 1000	End of transmission packet **(EoTp)**.	Short
0x11	01 0001	Generic short read response, 1 byte returned.	Short
0x12	01 0010	Generic short read response, 2 byte returned.	Short
0x1A	01 1010	Generic long read response.	Long
0x1C	01 1100	DCS long read response.	Long
0x21	10 0001	DCS short read response, 1 byte returned.	Short
0x22	10 0010	DCS short read response, 2 byte returned.	Short

Table 7.3: Data types for peripheral-sourced packets

Acknowledge types		
Data type, hex	**Function description**	**Number of bytes**
02h	Get Acknowledge with Error report when Error occurs from processor transmission.	4 bytes **(DI + bit0 ~ bit15 + ECC)**

Note: (1) When processor transmits complete Payload, following signal by BTA, peripheral must respond to processor. With error➔Acknowledge with error report **(Short packet)**, Without error➔ request READ data or Acknowledge **(trigger message)**.

Bit	Description
0	SoT error.
1	SoT Sync error.
2	EoT Sync error.
3	Escape mode entry command error.
4	Low-power transmit Sync error.
5	Peripheral timeout error.
6	False control error.
7	Contention detected.
8	ECC error, single-bit **(detected and corrected)**.
9	ECC error, multi-bit **(detected, not corrected)**.
10	Checksum error **(long packet only)**.
11	DSI data type not recognized.
12	DSI VC ID invalid.
13	Invalid transmission length.
14	Reserved.
15	DSI protocol violation.

Generic Short Read Response (1 byte returned)		
Data type, hex	**Function description**	**Number of bytes**
11h	This is the short-packet to Generic Read Request. **(1 byte returned)**.	4 bytes **(DI + R1 + 00h + ECC)**

Note: (1) R1=returned byte 1.

Generic Short Read Response (1 byte returned)		
Data type, hex	**Function description**	**Number of bytes**
12h	This is the short-packet to Generic Read Request. **(1 byte returned)**.	4 bytes **(DI + R1 + R2 + ECC)**

Note: (1) R1=returned byte 1, R2=returned byte 2.

Generic Long Read Response		
Data type, hex	**Function description**	**Number of bytes**
1Ah	This is the long-packet response to Generic Long Read Request.	Up to 65535 bytes **(DI + WC + ECC + DCS CMD. + Payload DATA + PF)**

Note: (1) If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h.
If the command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge with Error Report packet shall be sent.

DCS Read Response		
Data type, hex	**Function description**	**Number of bytes**
1Ch	This is the long-packet response to DCS Long Read Request.	Up to 65535 bytes **(DI + WC + ECC + DCS CMD. + Payload DATA + PF)**

Note: (1) If the peripheral is Checksum capable, is shall return a calculated two-byte Checksum appended to the N-byte payload data. If the peripheral does not support Checksum, it shall return 0000h.
If the DCS command itself is possibly corrupt, due to an uncorrectable ECC error, SoT or SoT Sync error, the requested READ data packet shall not be sent and only the Acknowledge with Error Report packet shall be sent.

DCS Short Read Response (1 byte returned)		
Data type, hex	**Function description**	**Number of bytes**
21h	This is the short-packet to DCS Read Request. **(1 byte returned)**.	4 bytes **(DI + R1 + 00h + ECC)**

Note: (1) R1=returned byte 1.

DCS Short Read Response (2 byte returned)		
Data type, hex	**Function description**	**Number of bytes**
22h	This is the short-packet to DCS Read Request. **(2 byte returned)**.	4 bytes **(DI + R1 + R2 + ECC)**

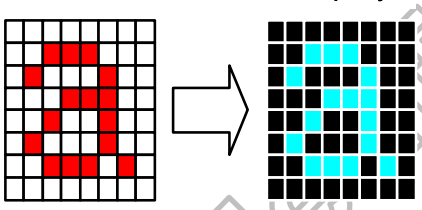
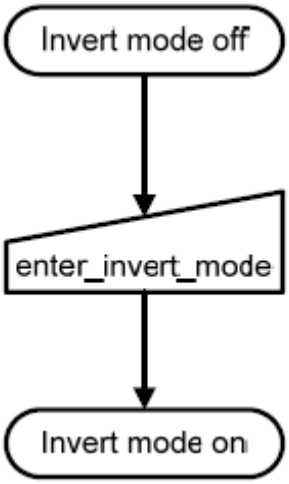
Note: (1) R1=returned byte 1, R2=returned byte 2.

7.3 Display command set (DCS)

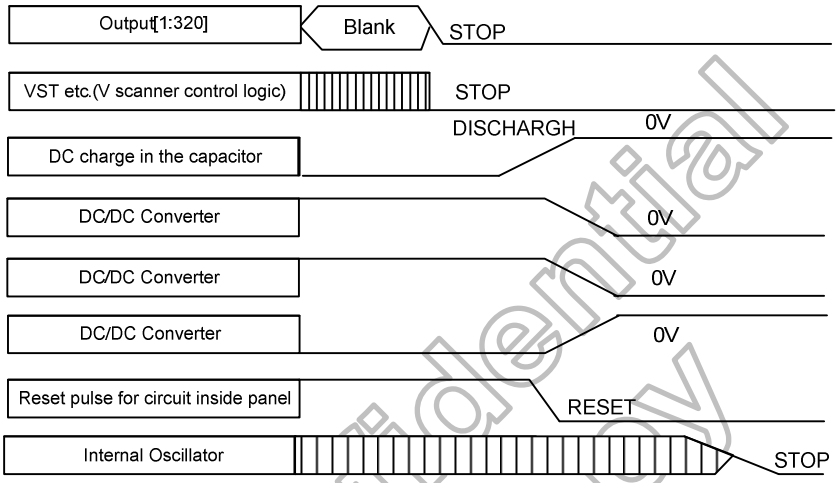
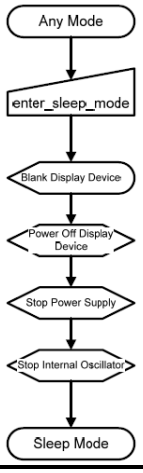
Command	Hex Code	Description	Number of parameters
Enter invert mode	21h	Displayed image colors are inverted.	0
Enter sleep mode	10h	Power for the display panel is off.	0
Exit invert mode	20h	Displayed image colors are not inverted.	0
Exit sleep mode	11h	Power for the display panel is on.	0
Get address mode	0Bh	Get data order for transfers from the Host to the display module and from the frame memory to the display device.	1
Get display mode	0Dh	Get the current display mode from the peripheral.	1
Get pixel format	0Ch	Get the current pixel format.	1
Get power mode	0Ah	Get the current power mode.	1
Get signal mode	0Eh	Get display module signaling mode.	1
Nop	00h	No operation.	0
Read DDB continue	A8h	Continue reading the DDB from the last read location.	variable
Read DDB start	A1h	Read the DDB from the provided location.	variable
Set address mode	36h	Set the data order for transfers from the host to the display module and from the frame memory to the display device.	1
Set display off	28h	Blanks the display device.	0
Set display on	29h	Show the image on the display device.	0
Set pixel format	3Ah	Defines how many bits per pixel are used in the interface.	1
Set tear off	34h	Synchronization information is not sent from the display module to the host processor.	0
Set tear on	35h	Synchronization information is sent from the display module to the host processor at the start of VFP	1
Set tear scan line	44h	Synchronization information is sent from the display module to the host processor when the display device refresh reaches the provided scan line.	2
Soft reset	01h	Software Reset.	0
Enter_idle_mode	39h	Reduced color depth is used on the display panel.	0
Exit_idle_mode	38h	Full color depth is used on the display panel.	0
Get diagnostic_result	0Fh	Get Peripheral Self-Diagnostic Reslut.	1
RDNUMED	05h	RDNUMED (**Read Number of the Errors on DSI**).	1

Table 7.4: DCS command list

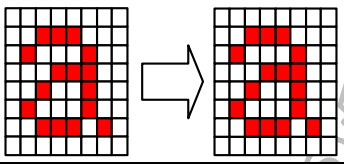
7.3.1 Enter_invert_mode (21h)

<table>
<tr><td rowspan="2">21 H</td><td colspan="10">Enter_invert_mode (Display Inversion On)→INVON</td></tr>
<tr><td>Direction</td><td>D7</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td><td>HEX</td></tr>
<tr><td>Command</td><td>H→D</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>21</td></tr>
<tr><td>Parameter</td><td colspan="10">No parameter.</td></tr>
<tr><td>Description</td><td colspan="10">This command is used to enter into display inversion mode.
This command makes no change of contents of frame memory. Every bit is inverted from the frame memory to the display.
This command does not change any other status.
(Example)
Host display
  </td></tr>
<tr><td>Restriction</td><td colspan="10">This command has no effect when module is already in inversion on mode.</td></tr>
<tr><td>Register Availability</td><td colspan="10"><table><tr><th>Status</th><th>Availability</th></tr><tr><td>Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table></td></tr>
<tr><td>Default</td><td colspan="10"><table><tr><th>Status</th><th>Default value</th></tr><tr><td>Power On Sequence</td><td>Display Inversion Off</td></tr><tr><td>S/W Reset</td><td>Display Inversion Off</td></tr><tr><td>H/W Reset</td><td>Display Inversion Off</td></tr></table></td></tr>
<tr><td>Flow Chart</td><td colspan="10"> 
</td></tr>
</table>

7.3.2 Enter_sleep_mode (10h)

10 H	Enter_sleep_mode (Sleep In)→SLPIN									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	1	0	0	0	0	10
Parameter	No parameter.									
Description	This command causes the LCD module to enter the minimum power consumption mode. In this mode the DC/DC converter is stopped, Internal oscillator is stopped, and panel scanning is stopped.  MCU interface and memory are still working and the memory keeps its contents.									
Restriction	This command has no effect when module is already in sleep in mode. Sleep In Mode can only be left by the Sleep Out Command **(11h)**. It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. It will be necessary to wait 120msec after sending Sleep Out command **(when in Sleep In Mode)** before Sleep In command can be sent.									
Register Availability	**Status** | **Availability** Sleep Out | Yes Sleep In | Yes									
Default	**Status** | **Default value** Power On Sequence | Sleep In Mode S/W Reset | Sleep In Mode H/W Reset | Sleep In Mode									
Flow Chart	It takes 120msec to get into Sleep In mode after SLPIN command issued.  									

7.3.3 Exit_invert_mode (20h)

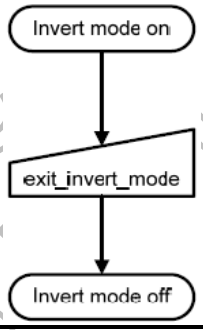
20 H	Exit_invert_mode (Display Inversion Off) →INVOFF									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	0	0	0	0	0	20
Parameter	No parameter.									
Description	This command is used to recover from display inversion mode. This command makes no change of contents of frame memory. This command does not change any other status. (Example) Host display 									
Restriction	This command has no effect when module is already in inversion off mode.									
Register Availability										

Status	Availability
Sleep Out	Yes
Sleep In	Yes

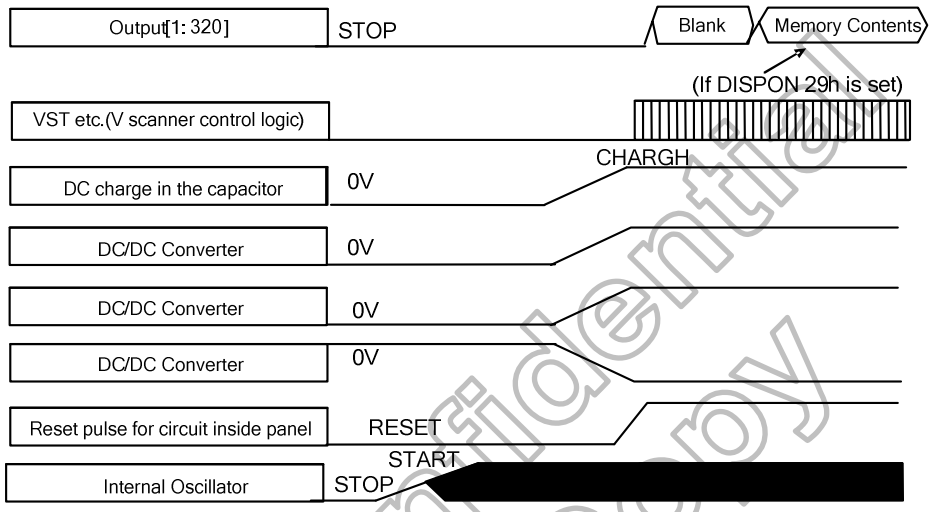
Default	

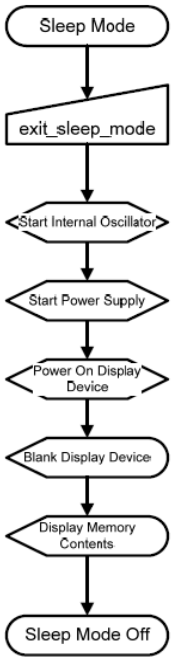
Status	Default value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



7.3.4 Exit_sleep_mode (11h)

11 H	Exit_sleep_mode (Sleep Out)→SLPOUT									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	1	0	0	0	1	11
Parameter	No parameter.									
Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal oscillator is started, and panel scanning is started.  									
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be left by the Sleep In Command **(10h)**. It will be necessary to wait 5msec before sending next command, this is to allow time for the supply voltages and clock circuits to stabilize. The display module loads all display supplier's factory default values to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if factory default and register values are same when this load is done and when the display module is already Sleep Out –mode. The display module is doing self-diagnostic functions during this 5msec. It will be necessary to wait 120msec after sending Sleep In command **(when in Sleep Out mode)** before Sleep Out command can be sent.									
Register Availability	**Status** / **Availability** Sleep Out / Yes Sleep In / Yes									
Default	**Status** / **Default value** Power On Sequence / Sleep In Mode S/W Reset / Sleep In Mode H/W Reset / Sleep In Mode									

Flow Chart	It takes 120msec to become Sleep Out mode after SLPOUT command issued. 

7.3.5 Get_address _mode (0Bh)

0B H	Get_address_mode (Read Display MADCTL) →RDDMADCTL									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	1	0	1	1	0B
1st parameter	D→H	D7	D6	0	0	D3	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Not Defined	-
D6	Not Defined	-
D5	Not Defined	Set to '0'
D4	Not Defined	Set to '0'
D3	RGB/BGR Order	-
D2	Not Defined	Set to '0'
D1	Flip Horizontal	Set to '0'
D0	Flip Vertical	Set to '0'

Bit D3 – RGB/BGR Order
'0' = RGB **(When MADCTL B3 = '0')**.
'1' = BGR **(When MADCTL B3 = '1')**.
Bit D1 – Flip Horizontal
'0' = Display from Left to Right
'1' = Display from Right to Left.
Bit D0 – Flip Vertical
'0' = Display from Top to Bottom
'1' = Display from Bottom to Top.

Restrictions

-

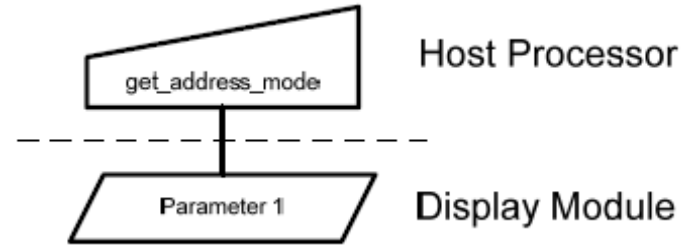
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

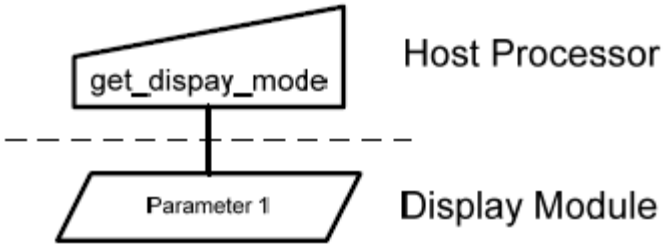
Default

Status	Default value
Power On Sequence	00h
S/W Reset	No Change
H/W Reset	00h

Flow Chart



7.3.6 Get_display _mode (0Dh)

0D H	Get_display_mode (Read Display Image Mode→RDDIM									
	Direction	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	H→D	0	0	0	0	1	1	0	1	0D
1st parameter	D→H	0	0	D5	0	0	0	0	0	xx
Description	This command indicates the current status of the display as described in the table below: **Bit D5 – Inversion On/Off** '0' = Inversion is Off. '1' = Inversion is On. **Bit D7,D6,D4,D3,D2,D1,D0- Not Defined** Set to '0'									
Restrictions	-									
Register Availability	**Status** / **Availability** Sleep Out / Yes Sleep In / Yes									
Default	**Status** / **Default value** Power On Sequence / 00h S/W Reset / No change H/W Reset / 00h									
Flow Chart										

7.3.7 Get_pixel_format (0Ch)

0C H	Get_pixel_format (Read Display COLMOD)→RDDCOLMOD									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	1	1	0	0	0C
1st parameter	D→H	0	D6	D5	D4	0	0	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Reserved	Set to '0'
D6	DPI Interface Pixel format	-
D5		-
D4		-
D3	Reserved	Set to '0'
D2	DBI Interface Pixel format -> Not Defined	Set to '0'
D1		Set to '0'
D0		Set to '0'

Bits D6, D5, D4 – DPI Pixel Format Definition
Bits D2, D1, D0 – DBI Pixel Format Definition-> Not Defined.

Interface Color Format	D6	D5	D4
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 bit/pixel	1	0	1
18 bit/pixel	1	1	0
24 bit/pixel	1	1	1

If a particular interface, either DSI or DPI, is not used then the corresponding bits in the parameter returned from the display module are undefined.

Restrictions: -

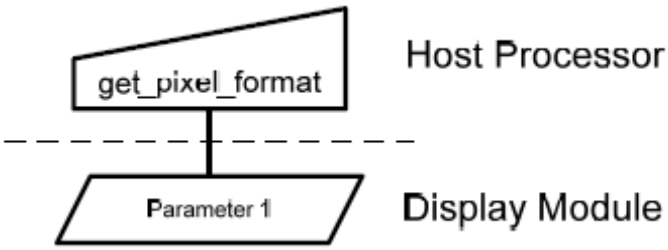
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power On Sequence	24-bit/pixel
S/W Reset	24-bit/pixel
H/W Reset	24-bit/pixel

Flow Chart



7.3.8 Get_power_mode (0Ah)

0A H	Get_power_mode (Read Display Power Mode)→RDDPM									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	1	0	1	0	0A
1st parameter	D→H	0	0	0	D4	0	D2	0	0	xx

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Comment
D7	Not Defined	Set to '0'
D6	Not Defined	Set to '0'
D5	Not Defined	Set to '0'
D4	Sleep In/Out	-
D3	Not Defined	Set to '0'
D2	Display On/Off	-
D1	Not Defined	Set to '0'
D0	Not Defined	Set to '0'

Bit D4 – Sleep In/Out
'0' = Sleep In Mode.
'1' = Sleep Out Mode.
Bit D2 – Display On/Off
'0' = Display is Off.
'1' = Display is On.
Bit D7,D6,D5,D3,D1,D0 – Not Defined
Set to '0'

Restrictions

-

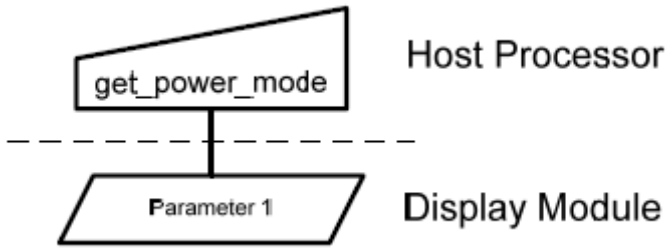
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



7.3.9 Get_signal_mode (0Eh)

0E H	Get_signal_mode (Read Display Signal Mode)→RDDSM									
	Direction	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**
Command	H→D	0	0	0	0	1	1	1	0	0E
1st parameter	D→H	D7	D6	0	0	0	0	0	D0	xx
Description	This command indicates the current status of the display as described in the table below: **Bit D7 – Tearing Effect Line On/Off** '0' = Tearing Effect Line Off. '1' = Tearing Effect On. **Bit D6 – Tearing Effect Line Output Mode** see section set_tear_on**(35h)** for mode definitions. '0' = Mode 0.**(M=0)** '1' = Mode 1.**(M=1)** **Bit [D5:D1]** –reserved and set to '0'. **Bit D0 – Error report bit** '0' = No Error happened . '1' = Error happened. **(after BTA ,Bit D0 will set to '0')**									
Restrictions	-									

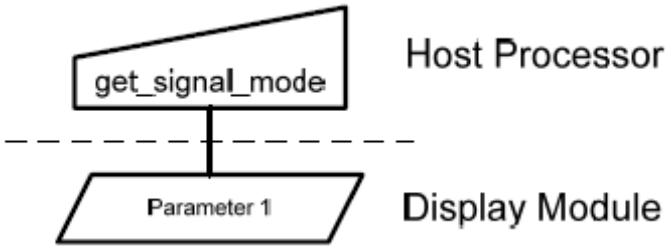
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



7.3.10 Nop (00h)

00 H	NOP (No Operation)									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	0	0	0	0	00
Parameter	NO PARAMETER									
Description	This command is an empty command; it does not have any effect on the display module. However it can be used to terminate Frame Memory Write as described in RAMWR **(Memory Write)** or RAMRD **(Memory Read)** command.									
Restriction	-									

Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A

Flow Chart: -

7.3.11 Read_DDB_continue (A8h)

A8h	Read_DDB_continue									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	1	0	1	0	1	0	0	0	A8
1st parameter	D→H	x	x	x	x	x	x	x	x	xx
2nd parameter	D→H	x	x	x	x	x	x	x	x	xx
:	D→H	x	x	x	x	x	x	x	x	xx
Nth parameter	D→H	x	x	x	x	x	x	x	x	xx
Description	A read_DDB_start command should be executed at least once before a read_DDB_continue command to define the read location. Otherwise, data read with a read_DDB_continue command is undefined.									
Restrictions	-									

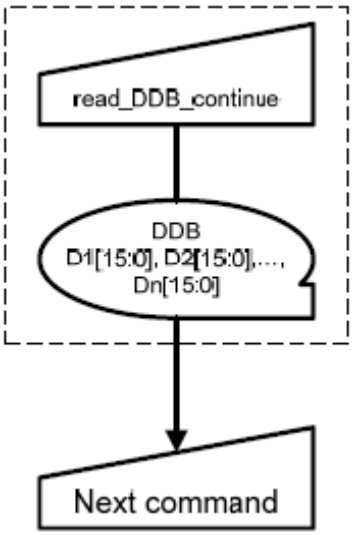
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power On Sequence	Read PA 1st~6th is the same as 00h , and the 7th read is FFh.
S/W Reset	Read PA 1st~6th is the same as 00h , and the 7th read is FFh.
H/W Reset	Read PA 1st~6th is the same as 00h , and the 7th read is FFh.

Flow Chart



7.3.12 Read_DDB_start (A1h)

A1h	Read_DDB_start									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H->D	1	0	1	0	0	0	0	1	A1
1st parameter	D->H	x	x	x	x	x	x	x	X	xx
2nd parameter	D->H	x	x	x	x	x	x	x	x	xx
3rd parameter	D->H	x	x	x	x	x	x	x	x	xx
4th parameter	D->H	x	x	x	x	x	x	x	x	xx
:	D->H	x	x	x	x	x	x	x	x	xx
7th parameter	D->H	1	1	1	1	1	1	1	1	FF

Description

The format of returned data is as follows:
Parameter 1: LS **(least significant)** byte of Supplier ID. Supplier ID is a unique value assigned to each peripheral supplier by the MIPI organization.
Parameter 2: MS **(most significant)** byte of Supplier ID.
Parameter 3: LS **(least significant)** byte of Supplier Elective Data. This is a byte of information that is determined by the supplier. It could include model number or revision information, for example.
Parameter 4: MS **(most significant)** byte of Supplier Elective Data
Parameter 7: single-byte *Escape or Exit Code* **(EEC)**. The code is interpreted as follows:
- FFh - Exit code – there is no more data in the Descriptor Block
- 00h - Escape code – there is supplier-proprietary data in the Descriptor Block **(does not conform to any MIPI standard)**

Restrictions

-

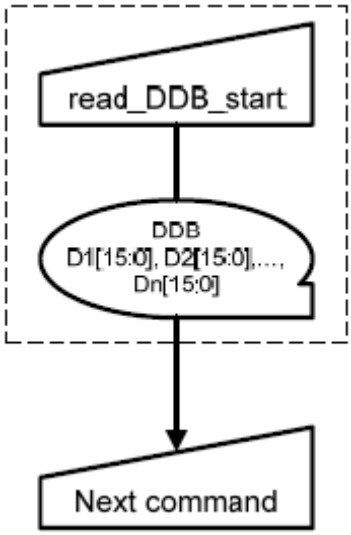
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power On Sequence	PA 1st~6th =00h, PA 7th =FFh
S/W Reset	PA 1st~6th =00h, PA 7th =FFh
H/W Reset	PA 1st~6th =00h, PA 7th =FFh

Flow Chart



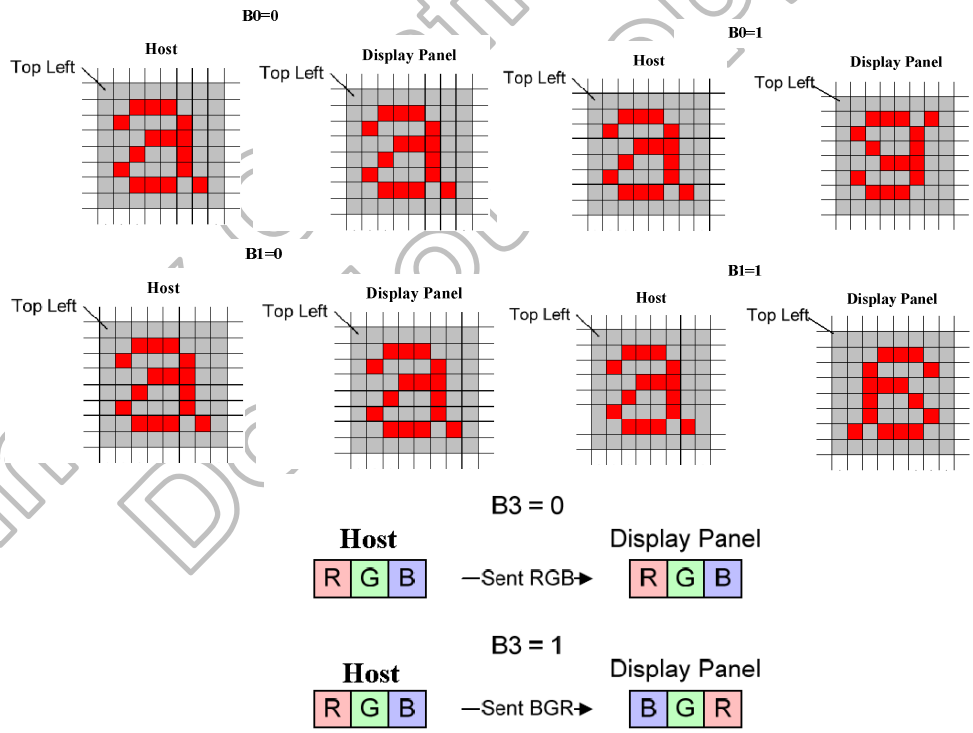
7.3.13 Set_address_mode (36h)

36 H	Set_address_mode (Memory Access Control)→MADCTL									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	0	1	1	0	36
1st parameter	H→D	0	0	0	0	BGR	0	Flip V	Flip H	-

Description

This command defines read/write scanning direction of frame memory.
This command makes no change on the other driver status.
Bit Assignment

Bit	Name	Description
B7	-	-
B6	-	-
B5	Not Defined	-
B4	Not Defined	-
B3	RGB-BGR ORDER **(BGR)**	Color selector switch control. 0=RGB color filter panel. 1=BGR color filter panel.
B2	Not Defined	-
B1	Flip Horizontal	Flip Horizontal. 0= Display from Left to Right. 1= Display from Right to Left.
B0	Flip Vertical	Flip Vertical 0= Display from Top to Bottom. 1= Display from Bottom to Top.



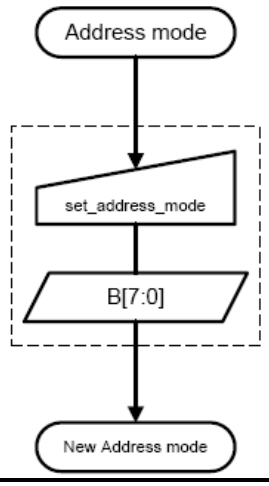
Restriction: -

Register Availability

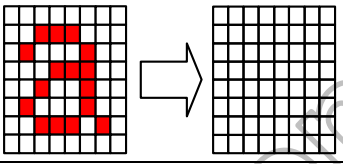
Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power On Sequence	00h
S/W Reset	No change
H/W Reset	00h

Flow Chart	

7.3.14 Set_display_off (28h)

28 H	Set_display_off (Display Off)→DISPOFF									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	0	1	0	0	0	28
Parameter	No parameter.									
Description	This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted. This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display. (Example) Host display 									
Restriction	This command has no effect when module is already in display off mode.									

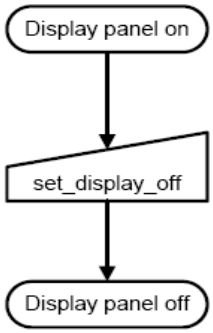
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

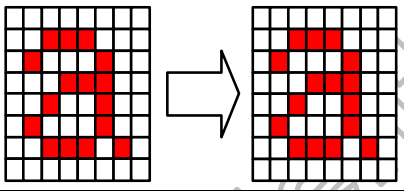
Default

Status	Default value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



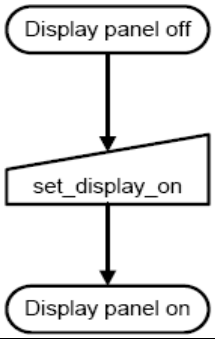
7.3.15 Set_display_on (29h)

29 H	Set_display_on (Display On)→DISPON									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	0	1	0	0	1	29
Parameter	No parameter.									
Description	This command is used to recover from DISPLAY OFF mode. Output from the Frame Memory is enabled. This command makes no change of contents of frame memory. This command does not change any other status. (Example) memory display 									
Restriction	This command has no effect when module is already in display on mode.									

Register Availability	Status	Availability
	Sleep Out	Yes
	Sleep In	Yes

Default	Status	Default value
	Power On Sequence	Display Off
	S/W Reset	Display Off
	H/W Reset	Display Off

Flow Chart



7.3.16 Set_pixel _format (3Ah)

3A H	Set_pixel_format (Interface Pixel Format)→COLMOD									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	1	0	1	0	3A
1st parameter	H→D	0	D6	D5	D4	0	0	0	0	-

Description

This command is used to define the format of RGB picture data, which is to be transfer via the system and RGB interface. The formats are shown in the table:

Bit D6,D5,D4 - DPI Pixel Format Definition

DPI interface :

Interface Format	D6	D5	D4
Not Defined	0	0	0
Not Defined	0	0	1
Not Defined	0	1	0
Not Defined	0	1	1
Not Defined	1	0	0
16 Bit/Pixel	1	0	1
18 Bit/Pixel	1	1	0
24 Bit/Pixel	1	1	1

Bit D7,D3,D2,D1,D0 – Not Defined

Set to '0'

Restriction

There is no visible effect until the Frame Memory is written to.

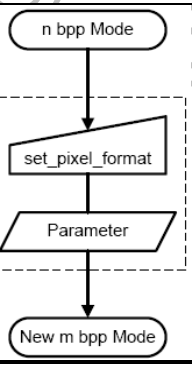
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power On Sequence	24-bit/pixel
S/W Reset	No Change
H/W Reset	24-bit/pixel

Flow Chart



7.3.17 Set_tear _off (34h)

34 H	Set_tear_off (Tearing Effect Line OFF)→TEOFF									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	0	1	0	0	34
Parameter	No parameter.									
Description	This command is used to turn OFF the Tearing Effect output signal from the TE signal line.									
Restriction	This command has no effect when Tearing Effect output is already OFF.									

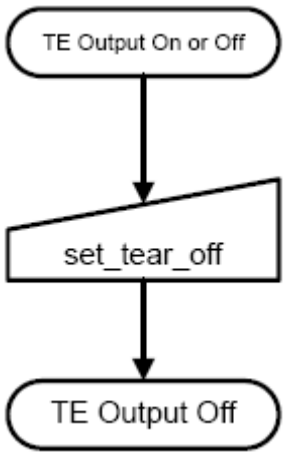
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

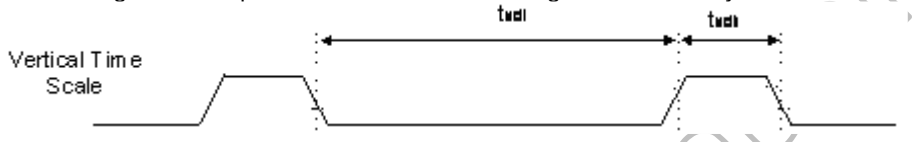
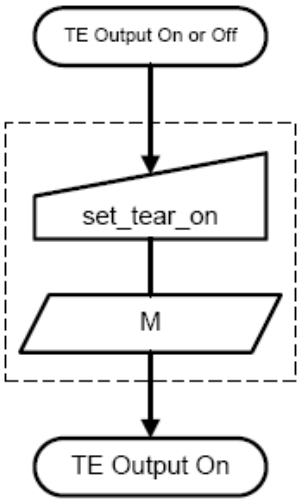
Default

Status	Default value
Power On Sequence	Tearing Effect Off
S/W Reset	Tearing Effect Off
H/W Reset	Tearing Effect Off

Flow Chart



7.3.18 Set_tear _on (35h)

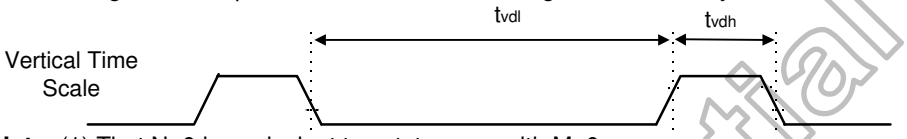
35 H	Set_tear_off (Tearing Effect Line ON)→TEON									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	0	1	0	1	35
1st parameter	H→D	-	-	-	-	-	-	-	M	-
Description	This command is used to turn ON the Tearing Effect output signal from the TE signal line. The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line. **(X=Don't Care)**. When **M=0 (mode0)** : The Tearing Effect Output line consists of V-Blanking information only:  When **M=1 (mode1)** : The Tearing Effect Output Line consists of both V-Blanking and H-Blanking information:  **Note:** (1) During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.									
Restriction	This command has no effect when Tearing Effect output is already ON.									
Register Availability	**Status** / **Availability** Sleep Out / Yes Sleep In / Yes									
Default	**Status** / **Default value** Power On Sequence / Tearing Effect Off S/W Reset / Tearing Effect Off H/W Reset / Tearing Effect Off									
Flow Chart										

7.3.19 Set_tear _scanline (44h)

44 H	Set_tear_scanline (Tear Effect Scan Lines)→TESL									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	1	0	0	0	1	0	0	44
1st parameter	H→D	N15	N14	N13	N12	N11	N10	N9	N8	00..FF
2nd parameter	H→D	N7	N6	N5	N4	N3	N2	N1	N0	00..FF

Description

This command is turns on the display module's Tearing Effect output signal on the TE signal Line when the display module reacfes line N.
The Tearing Effect Line On has one parameter which describes the mode of the Tearing Effect Output Line.
The Tearing Effect Output line consists of V-Blanking information only:



Note: (1) That N=0 is equivalent to set_tear_on with M=0.
The Tearing Effect Output Line shall be active low when the display module is in Sleep mode.

Restriction

The command has no effect when Tearing Effect output is already ON.

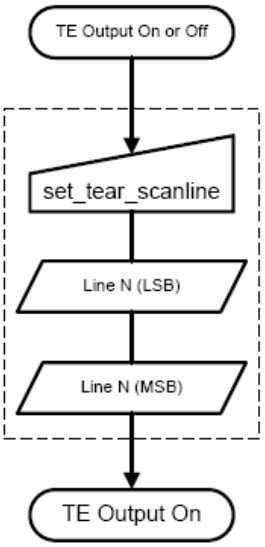
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

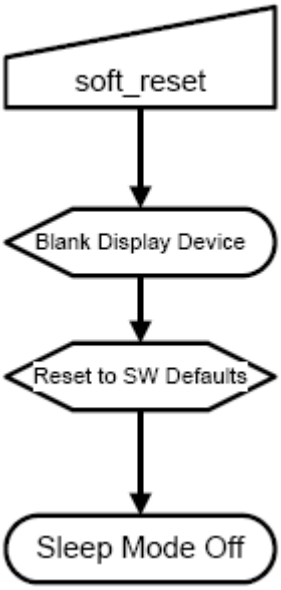
Default

Status	Default value
Power On Sequence	N[15:0]=0000h
S/W Reset	N[15:0]=0000h
H/W Reset	N[15:0]=0000h

Flow Chart



7.3.20 Soft_reset (01h)

01 H	Soft reset (Software Reset)→SWRESET									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	0	0	0	1	01
Parameter	No parameter.									
Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values. **(See default tables in each command description.)** The display is blank immediately. Note: The frame memory contents are unaffected by this command.									
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display supplier's factory default values to the registers during this 5m sec. If SW Reset is applied during Sleep Out mode, it will be necessary to wait 120m sec before sending Sleep Out command. SW Reset command cannot be sent during Sleep Out sequence.									
Register Availability	**Status** / **Availability** Sleep Out / Yes Sleep In / Yes									
Default	**Status** / **Default value** Power On Sequence / N/A S/W Reset / N/A H/W Reset / N/A									
Flow Chart										

7.3.21 Exit Idle mode (38h)

38 H	Exit idle mode (Idle Mode Off)									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	1	0	0	0	38
Parameter	No parameter.									
Description	This command causes the display module to exit Idle mode . In the idle off mode, LCD can display maximum 262,144 colors.									
Restriction	This command has no effect when module is already in idle off mode.									

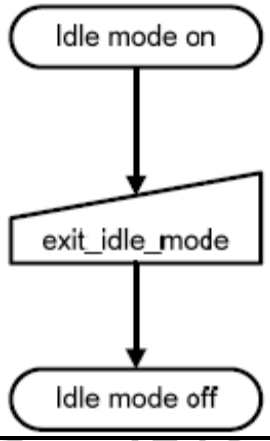
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart

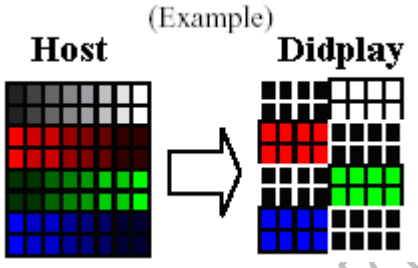


7.3.22 Enter Idle mode (39h)

39 H	Enter idle mode (Idle Mode ON)									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	1	1	1	0	0	1	39
Parameter	No parameter.									

Description

This command causes the display module to enter Idle Mode.
In the idle on mode, color expression is reduced. The primary and the secondary colors using MSB of each R, G and B in the Frame Memory, 8 color depth data is displayed.



Memory contents vs. Display Color			
	R5 R4 R3 R2 R1 R0	G5 G4 G3 G2 G1 G0	B5 B4 B3 B2 B1 B0
Black	0XXXXX	0XXXXX	0XXXXX
Blue	0XXXXX	0XXXXX	1XXXXX
Red	1XXXXX	0XXXXX	0XXXXX
Magenta	1XXXXX	0XXXXX	1XXXXX
Green	0XXXXX	1XXXXX	0XXXXX
Cyan	0XXXXX	1XXXXX	1XXXXX
Yellow	1XXXXX	1XXXXX	0XXXXX
White	1XXXXX	1XXXXX	1XXXXX

Restriction

This command has no effect when module is already in idle off mode.

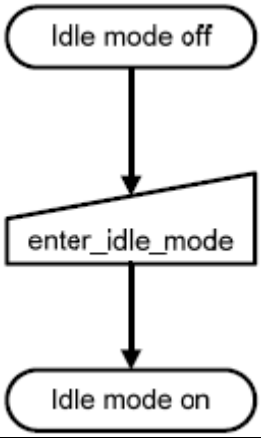
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power On Sequence	Idle Mode Off
S/W Reset	Idle Mode Off
H/W Reset	Idle Mode Off

Flow Chart



7.3.23 Get diagnostic result (0Fh)

0F H	Get diagnostic result (Read Display Self-Diagnostic Result)→RDDSDR									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	1	1	1	1	0F
1st parameter	H→D	D7	D6	0	0	0	0	0	0	-
Description	The display module returns the self-diagnostic results following a Sleep Out command. Bit D7 – Register Loading Detection Bit D6 – Functionality Detection Bits D[5:0] – Reserved, Set to '0'.									
Restriction	-									

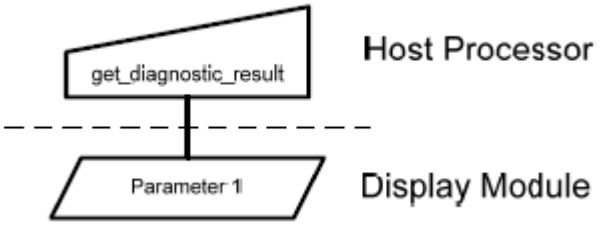
Register Availability

Status	Availability
Sleep Out	Yes
Sleep In	Yes

Default

Status	Default value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



7.3.24 RDNUMED (05h)

05 H	RDNUMED (Read Number of the errors on DSI)									
	Direction	D7	D6	D5	D4	D3	D2	D1	D0	HEX
Command	H→D	0	0	0	0	1	0	0	1	05
1st parameter	H→D	D7	D6	D5	D4	D3	D2	D1	D0	-
Description	The parameter is telling a number of the errors on DSI. D[6:0] bits are telling number of the errors. D[7] is set to '1' if there is overflow with D[6:0] bits. D[7:0] bits are set to '00h' **(as well as get_signal_mode (0Eh)'s D0 is setting to '0' at the same time).** Please also refer to get_signal_mode **(0Eh)**.									
Restriction	-									
Register Availability	**Status** / **Availability** Sleep Out / Yes Sleep In / Yes									
Default	**Status** / **Default value** Power On Sequence / 00h S/W Reset / 00h H/W Reset / 00h									
Flow Chart	-									

7.3.25 LVDS/MIPI video input timing

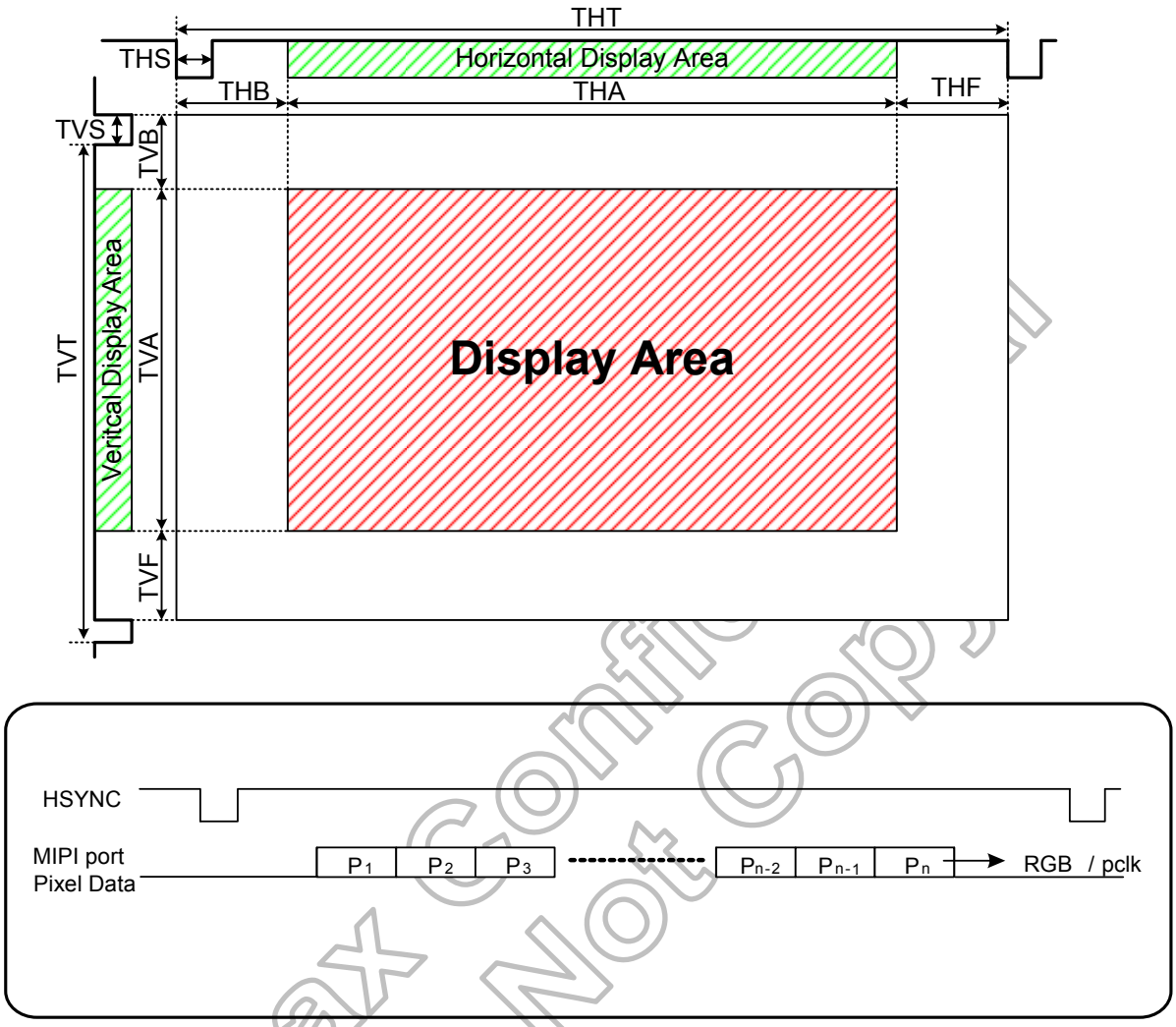


Figure 7.7: MIPI video input timing

Video input timing

Resolution		800RGBx1280			768RGBx1024			Unit
Input Timing	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	
PCLK frequency	-	-	71.9	80	-	55.8	80	MHz
Horizontal total	THT	880	920	1600	848	888	1536	DCLK
Horizontal synchronization	THS	10	24	-	10	24	-	DCLK
Horizontal back porch	THB	10	24	-	10	24	-	DCLK
Horizontal address	THA	-	800	-	-	768	-	DCLK
Horizontal front porch	THF	20	72	-	20	72	-	DCLK
Vertical frequency	-	-	60	-	-	60	-	Hz
Vertical total	TVT	1300	1304	2047	1044	1048	2047	THT
Vertical synchronization	TVS	1	2	-	1	2	-	THT
Vertical back porch	TVB	8	10	-	8	10	-	THT
Vertical address	TVA	-	1280	-	-	1024	-	THT
Vertical front porch	TVF	8	12	-	8	12	-	THT

Resolution		720RGBx1280			600RGBx1024			Unit
Input Timing	Symbol	Min.	Typ.	Max.	Min.	Typ.	Max.	
PCLK frequency	-	-	65.7	80	-	45.2	80	MHz
Horizontal total	THT	800	840	1440	680	720	1200	DCLK
Horizontal synchronization	THS	10	24	-	10	24	-	DCLK
Horizontal back porch	THB	10	24	-	10	24	-	DCLK
Horizontal address	THA	-	720	-	-	600	-	DCLK
Horizontal front porch	THF	20	72	-	20	72	-	DCLK
Vertical frequency	-	-	60	-	-	60	-	Hz
Vertical total	TVT	1300	1304	2047	1044	1048	2047	THT
Vertical synchronization	TVS	1	2	-	1	2	-	THT
Vertical back porch	TVB	8	10	-	8	10	-	THT
Vertical address	TVA	-	1280	-	-	1024	-	THT
Vertical front porch	TVF	8	12	-	8	12	-	THT

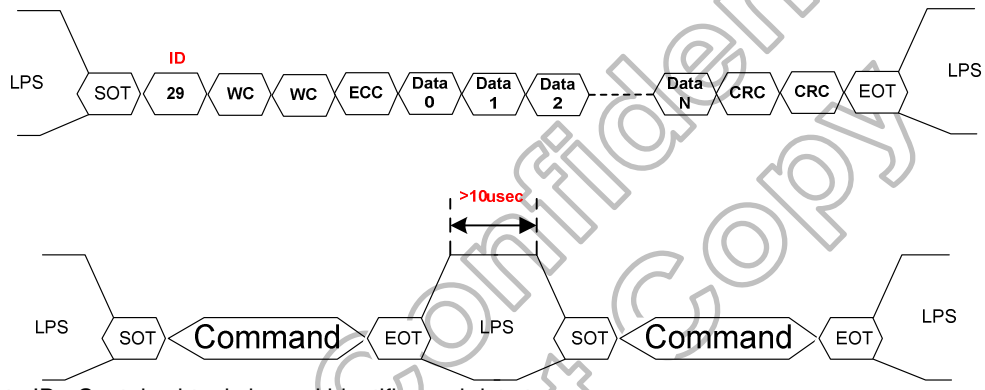
Table 7.5: MIPI input video timing

8. Register table

The HX8260-A supports set internal register by MIPI interface and SPI interface. MIPI and SPI interface use different register address.The MSB bit [7] of address is only for MIPI interface. The SPI must be ignored its. “MIPI address” and “SPI address” showed in register table.

8.1 MIPI command mode control register

The HX8260-A supports the generic long write command to set internal register. User could use HS or LP mode to write internal register. Figure 8.1 showed the reference long package structure. There is a LP timing request between HS command to next HS command. This time needs more than 10usec as figure 8.1. Detial MIPI commands describation showed in Section 8.4.



Note: (1) Data ID : Contain virtual channel identifier and data type.
(2) ECC **(Error Correction Code)** : The error correction code allows single-bit errors to be corrected and 2-bit errors to be detected in the short packet..

Figure 8.1: Support the DSI data short write

8.2 SPI format

The HX8260-A supports the 3-pin serial peripheral interface **(SPI)** to set internal register. The data is written to the register of assigned address when “End of transfer” is detected after the 16th SCL rising cycles.

Data is not accepted if there are less or more than 16 cycles for one transaction. Only when SCL is input 16 times and CSB is in the "Low" period simultaneously, SDA is accepted.

The first 7 bits **(A6 ~ A0)** specify the address of the register. The 8th bit means Read/Write command. “0” is WRITE. “1” is READ. The last 8 bits are for Data setting **(D7 ~D0)**. The address and data are transferred from the MSB to LSB sequentially. And next cycle is turn-round cycle.

For the MIPI mode 3-wire SPI pin are “MIPI_CSB, MIPI_SCK and MIPI_SD”
For the LVDS mode 3-wire SPI pin are “”LNSW_CSB, PNSW_SCL, MIPITE_SDA”

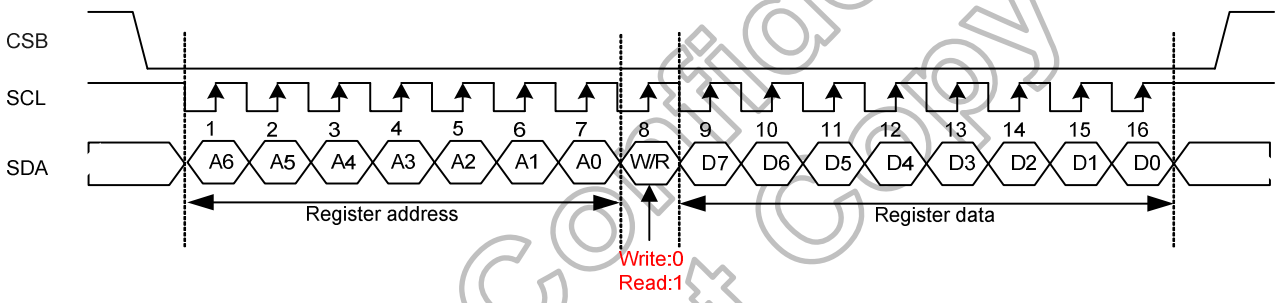


Figure 8.2: SPI format

8.3 Page change

The HX8260-A supports multi-page for register write. TCON have two path control register—SPI and MIPI. MIPI command has high priority than SPI.

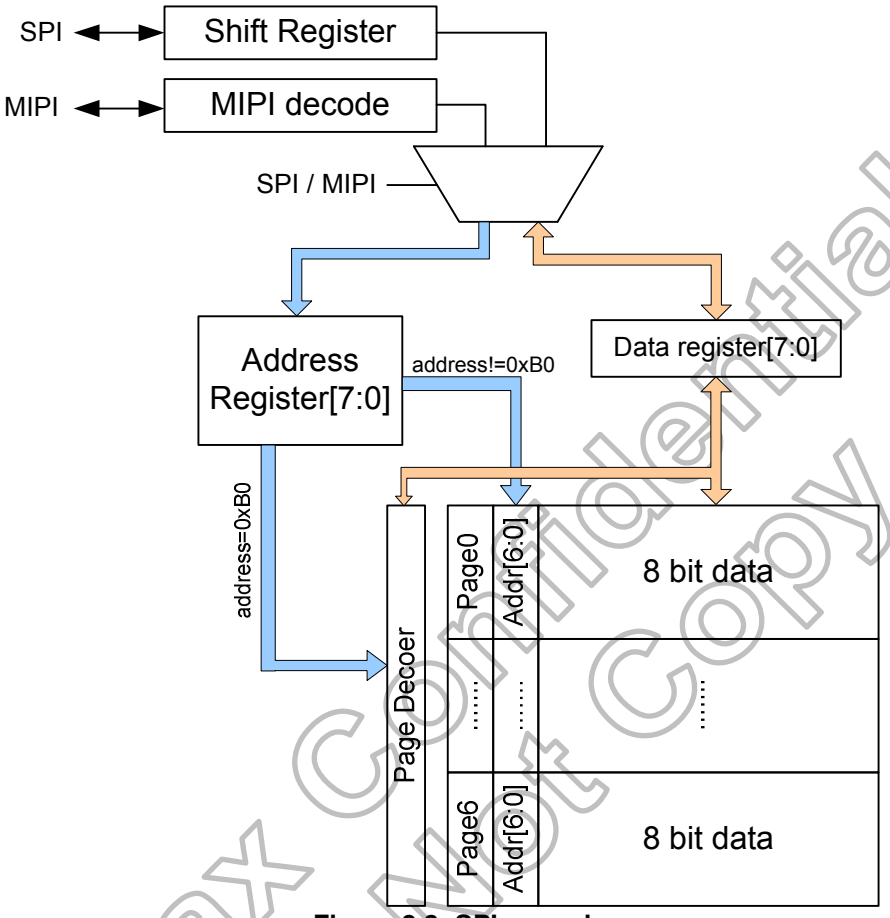


Figure 8.3: SPI page decoer

8.4 User define command list and description (For MIPI command mode)

8.4.1 User define command list table

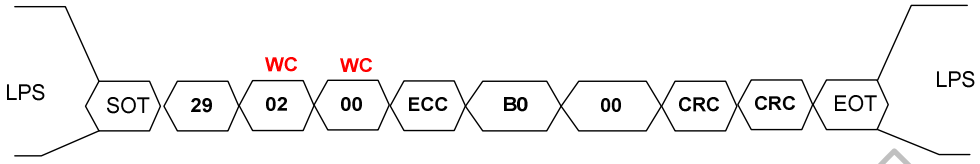
Page	Hex	operation	parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default
				1	0	1	1	0	0	0	1	Hex
0	B1	function control	1	VCOMS								80
			2	-	STB	UPDNB	LR	ZIGZAG_SEL	DISP_ON	NBW_SEL	BIST	4B
			3	ZTYPE_SEL		PWRMD		VRES_FIX	-	RES		28
			4	VRES								C0
			5	ZDATA								00
			6	LNSW		PNSW	HFRC_INV	CABC_CTRL		DITHER_EN	HFRC_EN	03
			7	PCLK_SEL	RX_DINT	RX_VB		-	LVDS_VB		LVDS_FMT	53
			8	-	LVDS_TD			-	LVDS_TC			00
			9	-	-	LVDS_BW		-	LVDS_CPB			12
			10	BLREV		BLREVONOFF	SD_ISSEL		INV_SEL			A9
			11	BC_CTRL	GOA_EN	RB_SWAP	DPFM_OSC_SEL		LNSEL		-	68
			12	GAS_GOA_EN	VRES_BLACK	GCHL_Blanking	-	-	-	-	-	E0
0	BD	Power	parameter index	1	0	1	1	1	1	0	1	
			1	VSPS				VSNS				AA
			2	-	-	VGHS						23
			3	-	-	VGLS						14
			4	reserve								00
			5	VSPON				VSPOFF				66
			6	VSNON				VSNOFF				66
			7		VGLXSP	VGHXSP		PFMFREN	T_OFFSET			70
			8	VPHS								04
			9	CGPP_INV		SOFT_EN	CLK_SEL			CMD_SEL		AD
			10	VNHS								04
			11	-	-	VCL_CPCTL		VGL_CPCTL		VGH_CPCTL		15
			12	POCSD_CTL		EQ0W						06
			13	-	-	-	EQ1W					00
			14	-	-	-	EQ2W					18
0	CB	Gamma	parameter index	1	1	0	0	1	0	1	1	
			1	PVP1								3F
			2	PVP2								34
			3	PVP3								2D
			4	PVP4								2D
			5	PVP5								21
			6	PVP6								1B
			7	PVP7								1E
			8	PVP8								25
			9	PVP9								20
			10	PVP10								20
			11	PVP11								16
			12	PVN1								3F
			13	PVN2								33
			14	PVN3								2C
			15	PVN4								2E
			16	PVN5								21
			17	PVN6								1B
			18	PVN7								1D
			19	PVN8								24
			20	PVN9								21
			21	PVN10								1F
			22	PVN11								16
			23					VBP		VBN		B5
1	B1	OTP	parameter index	1	1	0	0	1	0	1	1	
			1	OTP_Group								00
			2	OTP_pwd								5A
			3		OTP_PTM			OTP_prog_sel	OTP_re_Load	OTP_RD	OTP_WR	00
			4	OTP_ADDR								00
			5	OTP_PDOB								00
			6	OTP_PDIN								00
			7	OTP_MANUAL								5A
			8					POR	PPROG	VPS	PWE	00
2	B1	MUXL	parameter	1	0	1	1	0	0	0	1	

Page	Hex	operation	parameter index	D7	D6	D5	D4	D3	D2	D1	D0	Default
				1	0	1	1	0	0	0	1	Hex
			index									
			1	GOUTL1_STBYB_MOD		GOUTL_1_SEL						08
			2	GOUTL2_STBYB_MOD		GOUTL_2_SEL						08
			3	GOUTL3_STBYB_MOD		GOUTL_3_SEL						06
			4	GOUTL4_STBYB_MOD		GOUTL_4_SEL						06
			5	GOUTL5_STBYB_MOD		GOUTL_5_SEL						0C
			6	GOUTL6_STBYB_MOD		GOUTL_6_SEL						0C
			7	GOUTL7_STBYB_MOD		GOUTL_7_SEL						0A
			8	GOUTL8_STBYB_MOD		GOUTL_8_SEL						0A
			9	GOUTL9_STBYB_MOD		GOUTL_9_SEL						02
			10	GOUTL10_STBYB_MOD		GOUTL_10_SEL						00
			11	GOUTL11_STBYB_MOD		GOUTL_11_SEL						00
			12	GOUTL12_STBYB_MOD		GOUTL_12_SEL						00
			13	GOUTL13_STBYB_MOD		GOUTL_13_SEL						00
			14	GOUTL14_STBYB_MOD		GOUTL_14_SEL						00
			15	GOUTL15_STBYB_MOD		GOUTL_15_SEL						00
			16	GOUTL16_STBYB_MOD		GOUTL_16_SEL						04
			17	GOUTL17_STBYB_MOD		GOUTL_17_SEL						00
			18	GOUTL18_STBYB_MOD		GOUTL_18_SEL						00
			19	GOUTL19_STBYB_MOD		GOUTL_19_SEL						00
			20	GOUTL20_STBYB_MOD		GOUTL_20_SEL						00
			21	GOUTL21_STBYB_MOD		GOUTL_21_SEL						00
			22	GOUTL22_STBYB_MOD		GOUTL_22_SEL						00
2	C7	MUXR	parameter index	1	1	0	0	0	1	1	1	
			1	GOUTR1_STBYB_MOD		GOUTR_1_SEL						07
			2	GOUTR2_STBYB_MOD		GOUTR_2_SEL						07
			3	GOUTR3_STBYB_MOD		GOUTR_3_SEL						05
			4	GOUTR4_STBYB_MOD		GOUTR_4_SEL						05
			5	GOUTR5_STBYB_MOD		GOUTR_5_SEL						0B
			6	GOUTR6_STBYB_MOD		GOUTR_6_SEL						0B
			7	GOUTR7_STBYB_MOD		GOUTR_7_SEL						09
			8	GOUTR8_STBYB_MOD		GOUTR_8_SEL						09
			9	GOUTR9_STBYB_MOD		GOUTR_9_SEL						01
			10	GOUTR10_STBYB_MOD		GOUTR_10_SEL						00
			11	GOUTR11_STBYB_MOD		GOUTR_11_SEL						00
			12	GOUTR12_STBYB_MOD		GOUTR_12_SEL						00
			13	GOUTR13_STBYB_MOD		GOUTR_13_SEL						00
			14	GOUTR14_STBYB_MOD		GOUTR_14_SEL						00
			15	GOUTR15_STBYB_MOD		GOUTR_15_SEL						00
			16	GOUTR16_STBYB_MOD		GOUTR_16_SEL						03
			17	GOUTR17_STBYB_MOD		GOUTR_17_SEL						00
			18	GOUTR18_STBYB_MOD		GOUTR_18_SEL						00
			19	GOUTR19_STBYB_MOD		GOUTR_19_SEL						00
			20	GOUTR20_STBYB_MOD		GOUTR_20_SEL						00
			21	GOUTR21_STBYB_MOD		GOUTR_21_SEL						00
			22	GOUTR22_STBYB_MOD		GOUTR_22_SEL						00
			23	VGL_GAS	GOA_VGOFF_EN	GOA_PWROFF	GOA_HZ_EN					40
4	B1	CABC	parameter index	1	1	0	0	0	1	1	1	
			1			DIM_EN	BL_EN	CABC_AGAIN		CABC_AGAIN		3B
			2					DIM_STEP		DIM_FRME		09
			3	DUTY_UD								FF
			4	CABC_MB								10
			5	PWM_PRD								00
			6						PWM_DIV			02
			7	Reserve								00
			8	MAX_DUTY								FF
6	B1	MIPI	parameter index	1	0	1	1	0	0	0	1	
			1	EoTp_EN	CRCEN	CRCErr_FilterOut	VC4FRAME	VC_S		VC_m		E0
			2	reserve								80
			3	reserve								80
			4	reserve								00
			5		RT3				RT2			55
			6		RT1				RT0			53
			7	TurnDisable					RTC			05

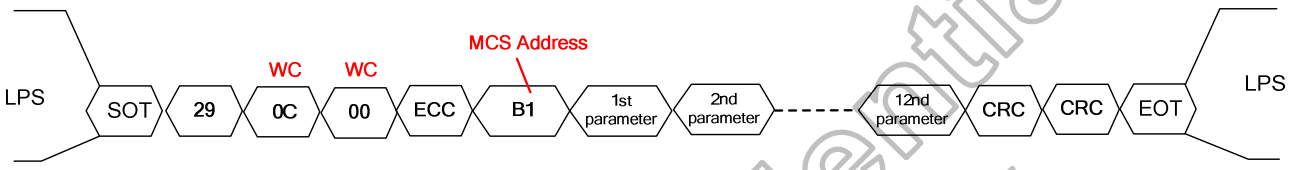
8.4.2 Function Control register (page0 B1h)

User could use HS or LP command send data.

Step 1 set to page0



Step 2 set function control register



Page	B1H	Function control register								
0	Command	D7	D6	D5	D4	D3	D2	D1	D0	Hex
		1	0	1	1	0	0	0	1	B1
	1st parameter	VCOMS								-
	2nd parameter	-	STB	UPDNB	LR	ZIGZAG_SEL	DISP_ON	NBW_SEL	BIST	-
	3rd parameter	ZTYPE_SEL		PWRMD		VRES_FIX	-	RES		-
	4th parameter	VRES								-
	5th parameter	ZDATA								-
	6th parameter	LNSW		PNSW	HFRC_INV	CABC_CTRL		DITHER_EN	HFRC_EN	-
	7th parameter	PCLK_SEL	RX_DINT	RX_VB		-	LVDS_VB		LVDS_FMT	-
	8th parameter	-	LVDS_TD			-	LVDS_TC			-
	9th parameter	-	-	LVDS_BW		-	LVDS_CPB			-
	10th parameter	BLREV		BLREVONOFF	SD_ISSEL		INV_SEL			-
	11th parameter	BC_CTRL	GOA_EN	RB_SWAP	DPFM_OSC_SEL		LNSEL		-	-
	12th parameter	GAS_GOA_EN	VRES_BLACK	GCHL_Blanking	-	-	-	-	-	-

Description

This command is used for function control.

VCOMS[7:0]: Adjust the VCOM output voltage **(default VCOM voltage -1.48V)**.

VCOMS[7:0]	VCOM voltage
00000000	-0.2V
00000001	-0.21V
00000010	-0.22V
:	:
:	:
10000000	-1.48V**(default)**
:	:
:	:
11111111	-2.75V

BIST: BIST mode selection.
1: Normal display mode.
0: BIST mode.

NBW_SEL: Normal Black and Normal white panel selection.
1: Normally black.
0: Normally White.

DISP_ON: MIPI DCS: 0x28 display on, 0x29 display off.
1: Reverse MIPI_DCS command **(to MIPI_DCS command do "XOR" operation)**.
0: Follow MIPI_DCS command.

ZIGZAG_SEL: Panel driving method selection.
1: Zigzag type panel.
0: Strip panel.

LR: Horizontal direction select.
MIPI DCS 0x36 set_address_mode[6] command and SPI register do XOR operation.

UPDNB: Vertical direction select.
MIPI DCS 0x36 set_address_mode[7] command and SPI register do XOR operation.

STB: TCON sleep mode selection.
MIPI DCS 0x10 **(Enter sleep mode)**, and 0x11 **(exit sleep mode)**. MIPI DCS command do XOR with SPI register.

RES[1:0]: Resolution selection **(to pin HW RES do XOR operation)**.
Resolution setting please refer section 6.1

VRES_FIX: Display vertical Line decide by
1: RES[2:0].
0: VRES **(4th parameter)**.

PWRMD[1:0]: POWR ON mode **(to pin PWRMD do XOR operation)**.

PWRMD[1]	PWRMD[0]	Driving mode
0	0	Support HX5186-C power mode
0	1	Suppot PFM circuit power mode
1	0	External VSP,VSN, VGH,VGL power mode
1	1	External VSP,VSN power mode

ZTYPE_SEL[1:0]: Zigzag type slection **(panel type please refer section 6.3)**.

VRES [7:0]: Vertical Resolution select, HX8260-A support user define vertical resolution.
User could enable the set **VRES_FIX=1** and set VRES [7:0]. Range=80~ 253, step= 8H

ZDATA [5:0]: Setting ZigZag dummy data select.range 0~63

HFRC_EN: Hi-FRC function enable.
1: HFRC enable.
0: HFRC disable.

DITHER_EN: Dithering function enable.
1: Dithering enable.
0: Dithering disable.

CABC_CTRL[1:0]: CABC-Mode selection:

CABC_CTRL[1]	CABC_CTRL[0]	CABC Mode
0	0	Bypass Mode<default>
0	1	Still-Mode
1	0	UI-Mode
1	1	Movingl-Mode

HFRC_INV: HI-FRC function inversion.
1: HFRC code 4, 9, 14 **(Default=1)**.
0: HFRC code=241, 246, 251

PNSW: MIPI/LVDS pin change polarity **(to pin PNSW do XOR operation)**.
1: P/N swap.
0: P/N follow pin name.

LNSW[1:0]: MIPI lane swap **(to pin LNSW do XOR operation)**.

		D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N
LNSW[1]	LNSW[0]	MIPI lanes mapping table									
0	0	D3P	D3N	D2P	D2N	CLKP	CLKN	D1P	D1N	D0P	D0N
0	1	D3P	D3N	D0P	D0N	CLKP	CLKN	D1P	D1N	D2P	D2N
1	0	D0P	D0N	D1P	D1N	CLKP	CLKN	D2P	D2N	D3P	D3N
1	1	D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N

LVDS_FMT: LVDS data format selection.
1: Thine or VESA format.
0: NS or JEIDA format.

LVDS_VB[1:0]: LVDS DLL bias current selection.

LVDS_VB[1]	LVDS_VB[0]	LVDS DLL bias current
0	0	82%
0	1	100% **(default)**
1	0	137%
1	1	160%

LVDS_RX[1:0]: LVDS bias current selection.

LVDS_RX[1]	LVDS_RX[0]	LVDS bias current
0	0	75%
0	1	100% **(default)**
1	0	125%
1	1	150%

RX_DINT: LVDS 8/6 bit mode.
1: 8bit mode.
0: 6 bit mode.

PCLK_SEL:TCON PCLK source selection.
1: From EXT_CLK.
0: Fome internal OSC25M.

LVDS_TC[2:0]: LVDS_TC skew tuning for LVDS Clock lanes 1setp delay 0.18 nsec.
LVDS_TD[2:0]: LVDS_TC skew tuning for LVDS Data lanes 1setp delay 0.18 nsec.

LVDS_CPB[2:0]: LVDS DLL pump current selection.
I=20u*CPB[2]+10u*CPB[1]+5u*CPB[0]

LVDS_BW[1:0]: LVDS DLL bandwidth selection.

LVDS_BW[1]	LVDS_BW[0]	LVDS bias current
0	0	100%
0	1	91% **(default)**
1	0	83%
1	1	77%

INV_SEL[2:0]: Normal mode POL inversion type selection **(for strip panel only)**.

INV_SEL[2]	INV_SEL[1]	INV_SEL[0]	Inversion tpye
0	0	0	line inversion
0	0	1	2-line inversion
0	1	0	4-line inversion
0	1	1	column inversion
1	0	0	8-line inversion

SD_ISSEL[1:0]: Source output bias current selection.

BLREV[1:0]: Source output status at V-blanking.
00:SD keep output the last line.
01: Hi-Z.
1X: GND.

LNSEL[1:0]: MIPI lane number control. The register do XOR with LANE1_STBYB & LANE0_BISTB pin.

DPFM_OSC_SEL[1:0]: DPFM clock selection **(for BIST mode use)**.

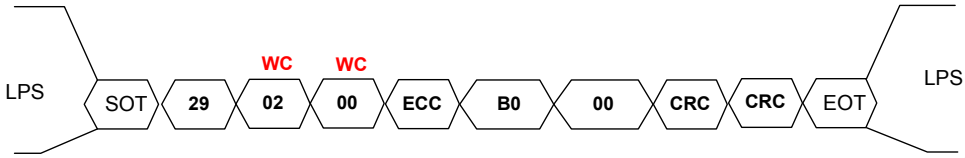
DPFM_OSC_SEL[1]	DPFM_OSC_SEL[0]	DPFM frequency
0	0	6.25MHz
0	1	12.5MHz
1	0	25MHz
1	1	25MHz

	RB_SWAP: Red and Blue color swap. 1: R/B swap. 0: Non-swap. **GOA_EN:** GOA signals enable. 1: Enable. 0: Disable. **BC_CTRL:** H/W pin BC_CTRL control. **GCHL_Blanking:**CLR power on status selection. 1: CLR1 =GND, CLR2=High level ,when power on status. 0: CLR1/2 =GND, when power on status. **VRES_BLACK**: when user change VRES register, TCON will send two black pattern. 1: Enable. 0: Disable. **GAS_GOA_EN:** when enable gas function, GOA CKV/STV pulled to high level. 1: Enable. 0: Disable.

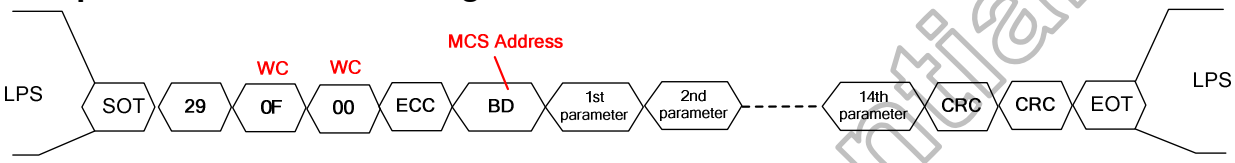
8.4.3 Power Control register(page0 BDh)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set Gamma control register



Page	BDH	Function control register								
0	Command	D7	D6	D5	D4	D3	D2	D1	D0	Hex
		1	0	1	1	1	1	0	1	BD
	1st parameter	VSPS				VSNS				-
	2nd parameter	-	-	VGHS						-
	3rd parameter	-	-	VGLS						-
	4th parameter	Reserved								-
	5th parameter	VSPON				VSPOFF				-
	6th parameter	VSNON				VSNOFF				-
	7th parameter		VGLXSP	VGHXSP		PFMFREN	T_OFFSET			-
	8th parameter	VPHS								-
	9th parameter	CGPP_INV		SOFT_EN	CLK_SEL			CMD_SEL		-
	10th parameter	VNHS								-
	11th parameter	-	-	VCL_CPCTL		VGL_CPCTL		VGH_CPCTL		-
	12th parameter	POCSD_CTL		EQ0W						-
	13th parameter	-	-	-	EQ1W					-
	14th parameter	-	-	-	EQ2W					-

Description

VSNS[3:0]: VDDN voltage selection **(step=0.1V)**.

VSNS [3:0]	Voltage
0000	-4.5V
0001	-4.6V
0010	-4.7V
:	:
1010	-5.5V **(default)**
:	:
1111	-6V

VSPS[3:0]: VDDP voltage selection **(step=0.1V)**.

VSPS [3:0]	Voltage
0000	4.5V
0001	4.6V
0010	4.7V
:	:
1010	5.5V **(default)**
:	:
1111	6V

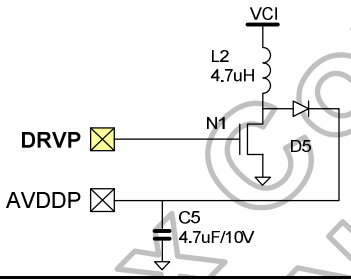
VGHS [5:0]: VGH voltage selection.

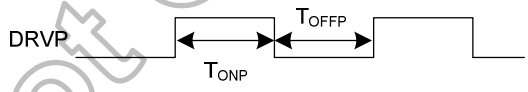
VGHS [5:0]	Voltage
000000	8V
000001	8.2V
000010	8.4V
:	:
:	:
100011	15V **(default)**
:	:
:	:
111111	20.6V

VGLS [5:0]: VGL voltage selection.

VGLS [5:0]	Voltage
000000	-6V
000001	-6.2V
000010	-6.4V
:	:
:	:
010100	-10V **(default)**
:	:
:	:
111111	-18.6V

VSPON [3:0]: Set VSP voltage PFM TON time.
VSPOFF [3:0]: Set VSP voltage PFM TOFF time.

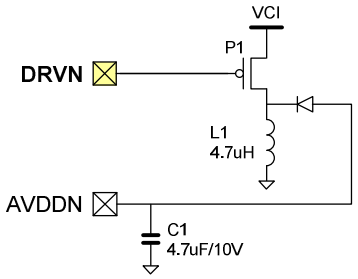


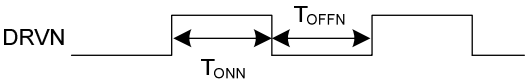


VSPON_T[3:0]	T_{ONP}(µs)
0	1.0
1	1.2
2	1.4
3	1.6
∫	
13	3.6
14	3.8
15	4.0

VSPOFF_T[3:0]	T_{OFFP}(µs)
0	1.0
1	1.2
2	1.4
3	1.6
∫	
13	3.6
14	3.8
15	4.0

VSNON [3:0]: Set VSN voltage PFM TON time.
VSNOFF [3:0]: Set VSN voltage PFM TOFF time.





VSNON_T[3:0]	T_{ONN}(µs)
0	1.0
1	1.2
2	1.4
3	1.6
∫	
13	3.6
14	3.8
15	4.0

VSNOFF_T[3:0]	T_{OFFN}(µs)
0	1.0
1	1.2
2	1.4
3	1.6
∫	
13	3.6
14	3.8
15	4.0

T_OFFSET: PFM ton / toff time offset.
1: Enable.
0: Disable.

PFMFREN: enablefrequency randomizer of both VDDP and VDDN PFM
1: Enable.
0: Disable.

VGHXSP[1:0]: VGL boost function selection.
00: 2VSP.
01: 2VSP+(-VSN).
1x: 2VSP+2(-VSN).

VGLXSP: VGL boost function selection.
1: 2VSN-VSP.
0: VSN-VSP.

VPHS [4:0]: Positive gamma_H selection.

VPHS [4:0]	Voltage
00000	4
00001	4.05V
00010	4.1V
:	:
00100	4.2V **(default)**
:	:
11111	5.5V

CMD_SEL[1:0]: Power mode 00: charge Pump command selection.

CMD_SEL[1]	CMD_SEL[0]	Pump command
0	0	x1.5
0	1	x2 **(default)**
1	0	x3
1	1	x3

CLK_SEL[2:0]: Power mode 00: charge Pump frequency selection.

CLK_SEL[2:0]	Frequency
000	403kHz
001	595kHz
010	781 kHz
011	963kHz **(default)**
100	1136 kHz
101	1389kHz
110	1786kHz
111	2083kHz

SOFT_EN: Power mode 00: Charge Pump soft start enable.
1: Enable.
0: Disable.

CGPP_INV[1:0]: Power mode 00 charge pump output signal invert.
CGPP_INV [1] set the DRVN signal, CGPP_INV [0] set the DRVP signal.
1: Invert.
0: Non-invert.

VNHS[4:0]: Negative gamma high selection.

VNHS [4:0]	Voltage
00000	-4
00001	-4.05V
00010	-4.1V
:	:
:	:
00100	-4.2V **(default)**
:	:
:	:
11111	-5.5V

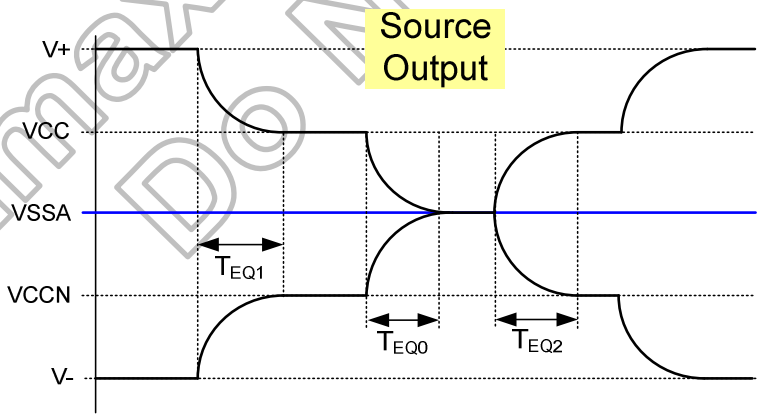
VGH_CPCTL[1:0]: VGH charge pump clock frequency selection.
VGL_CPCTL[1:0]: VGH charge pump clock frequency selection.
VCL_CPCTL[1:0]: VGH charge pump clock frequency selection.

CPCTL[1]	CPCTL[0]	Pump frequency (unit:line frequency)
0	0	x1
0	1	x2 **(default)**
1	0	x4
1	1	x8

EQ0W[5:0]: Source EQ0 time setting.
TEQ0=EQ0W[4:0]x4 DCLK **(Min is 12DCLK)**.

EQ1W[4:0]: Source EQ1 time setting.
TEQ1=EQ1W[4:0]x4 DCLK.

EQ2W[4:0]: Source EQ1 time setting.
TEQ2=EQ2W[4:0]x4 DCLK **(TEQ2≤TOEV-22DCLK satisfies gate driver settle time)**.



POCSD_CTL[1:0]: Source output offset cancel method selection.

POCSD_CTL=00b

	L1	L2	L3	L4	L5	L6	L7	L8
Frame1	0	1	1	0	0	1	1	0
Frame2	0	0	1	1	0	0	1	1
Frame3	1	0	0	1	1	0	0	1
Frame4	1	1	0	0	1	1	0	0
Frame5	0	1	1	0	0	1	1	0
Frame6	0	0	1	1	0	0	1	1

POCSD_CTL=01b

	L1	L2	L3	L4	L5	L6	L7	L8
Frame1	1	1	0	0	1	1	0	0
Frame2	1	1	0	0	1	1	0	0
Frame3	0	0	1	1	0	0	1	1
Frame4	0	0	1	1	0	0	1	1
Frame5	1	1	0	0	1	1	0	0
Frame6	1	1	0	0	1	1	0	0

POCSD_CTL=10b

	L1	L2	L3	L4	L5	L6	L7	L8
Frame1	1	0	1	0	1	0	1	0
Frame2	1	0	1	0	1	0	1	0
Frame3	0	1	0	1	0	1	0	1
Frame4	0	1	0	1	0	1	0	1
Frame5	1	0	1	0	1	0	1	0
Frame6	1	0	1	0	1	0	1	0

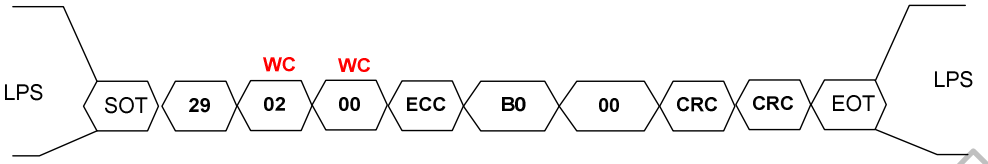
POCSD_CTL=11b

	L1	L2	L3	L4	L5	L6	L7	L8
Frame1	0	0	0	0	0	0	0	0
Frame2	0	0	0	0	0	0	0	0
Frame3	0	0	0	0	0	0	0	0
Frame4	0	0	0	0	0	0	0	0
Frame5	0	0	0	0	0	0	0	0
Frame6	0	0	0	0	0	0	0	0

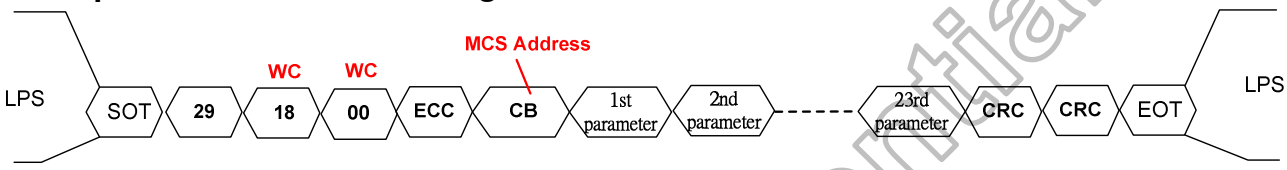
8.4.4 Gamma Control register(page0 CBh)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set Gamma control register



Page	CBH	Gamma control register								
0	Command	D7	D6	D5	D4	D3	D2	D1	D0	Hex
		1	1	0	0	1	0	1	1	CB
	1st parameter	PVP1								-
	2nd parameter	PVP2								-
	3rd parameter	PVP3								-
	4th parameter	PVP4								-
	5th parameter	PVP5								-
	6th parameter	PVP6								-
	7th parameter	PVP7								-
	8th parameter	PVP8								-
	9th parameter	PVP9								-
	10th parameter	PVP10								-
	11th parameter	PVP11								-
	12th parameter	PVN1								-
	13th parameter	PVN2								-
	14th parameter	PVN3								-
	15th parameter	PVN4								-
	16th parameter	PVN5								-
	17th parameter	PVN6								-
	18th parameter	PVN7								-
	19th parameter	PVN8								-
	20th parameter	PVN9								-
	21st parameter	PVN10								-
	22nd parameter	PVN11								-
	23rd parameter	-	-	-	-	VBP		VBN		-

Description

Name	Description
PVP1	Control 1st Positive gamma op's input voltage. default:3.462V~4.250V step=12.5mV
PVP2	Control 2nd Positive gamma op's input voltage. default:3.312V~4.100V step=12.5mV
PVP3	Control 3dr Positive gamma op's input voltage. default:3.212V~4.000V step=12.5mV
PVP4	Control 4th Positive gamma op's input voltage. default:2.750V~3.537V step=12.5mV
PVP5	Control 5th Positive gamma op's input voltage. default:2.350V~3.137V step=12.5mV
PVP6	Control 6th Positive gamma op's input voltage. default:1.862V~2.650V step=12.5mV
PVP7	Control 7th Positive gamma op's input voltage. default:1.337V~2.125V step=12.5mV
PVP8	Control 8th Positive gamma op's input voltage.default:1.175V~1.962V step=12.5mV
PVP9	Control 9th Positive gamma op's input voltage.default:0.500V~1.287V step=12.5mV
PVP10	Control 10th Positive gamma op's input voltage. default:0.237V~1.025V step=12.5mV
PVP11	Control 11th Positive gamma op's input voltage. default:0.012V~0.800V step=12.5mV
PVN1	Control 1st Negative gamma op's input voltage.default:-3.462V~-4.250V step=-12.5mV
PVN2	Control 2nd Negative gamma op's input voltage. default:-3.312V~-4.100V step=-12.5mV
PVN3	Control 3dr Negative gamma op's input voltage. default:-3.212V~-4.000V step=-12.5mV
PVN4	Control 4th Negative gamma op's input voltage.default:-2.750V~-3.537V step=-12.5mV

PVN5	Control 5th Negative gamma op's input voltage.default:-2.350V~-3.137V step=-12.5mV
PVN6	Control 6th Negative gamma op's input voltage.default:-1.862V~-2.650V step=-12.5mV
PVN7	Control 7th Negative gamma op's input voltage. default:-1.337V~-2.125V step=-12.5mV
PVN8	Control 8th Negative gamma op's input voltage.default:-1.175V~-1.962V step=-12.5mV
PVN9	Control 9th Negative gamma op's input voltage.default:-0.500V~-1.287V step=-12.5mV
PVN10	Control 10th Negative gamma op's input voltage.default:-0.237V~-1.025V step=-12.5mV
PVN11	Control 11th Negative gamma op's input voltage.default:0.012V~0.800V step=-12.5mV

PVP1~ PVP11 gamma voltage mapping.

Register setting	PVP1	PVP2	PVP3	PVP4	PVP5	PVP6	PVP7	PVP8	PVP9	PVP10	PVP11
3F	4.25	4.1	4	3.5375	3.1375	2.65	2.125	1.9625	1.2875	1.025	0.8
3E	4.2375	4.0875	3.9875	3.525	3.125	2.6375	2.1125	1.95	1.275	1.0125	0.7875
3D	4.225	4.075	3.975	3.5125	3.1125	2.625	2.1	1.9375	1.2625	1	0.775
3C	4.2125	4.0625	3.9625	3.5	3.1	2.6125	2.0875	1.925	1.25	0.9875	0.7625
3B	4.2	4.05	3.95	3.4875	3.0875	2.6	2.075	1.9125	1.2375	0.975	0.75
3A	4.1875	4.0375	3.9375	3.475	3.075	2.5875	2.0625	1.9	1.225	0.9625	0.7375
39	4.175	4.025	3.925	3.4625	3.0625	2.575	2.05	1.8875	1.2125	0.95	0.725
38	4.1625	4.0125	3.9125	3.45	3.05	2.5625	2.0375	1.875	1.2	0.9375	0.7125
37	4.15	4	3.9	3.4375	3.0375	2.55	2.025	1.8625	1.1875	0.925	0.7
36	4.1375	3.9875	3.8875	3.425	3.025	2.5375	2.0125	1.85	1.175	0.9125	0.6875
35	4.125	3.975	3.875	3.4125	3.0125	2.525	2	1.8375	1.1625	0.9	0.675
34	4.1125	3.9625	3.8625	3.4	3	2.5125	1.9875	1.825	1.15	0.8875	0.6625
33	4.1	3.95	3.85	3.3875	2.9875	2.5	1.975	1.8125	1.1375	0.875	0.65
32	4.0875	3.9375	3.8375	3.375	2.975	2.4875	1.9625	1.8	1.125	0.8625	0.6375
31	4.075	3.925	3.825	3.3625	2.9625	2.475	1.95	1.7875	1.1125	0.85	0.625
30	4.0625	3.9125	3.8125	3.35	2.95	2.4625	1.9375	1.775	1.1	0.8375	0.6125
2F	4.05	3.9	3.8	3.3375	2.9375	2.45	1.925	1.7625	1.0875	0.825	0.6
2E	4.0375	3.8875	3.7875	3.325	2.925	2.4375	1.9125	1.75	1.075	0.8125	0.5875
2D	4.025	3.875	3.775	3.3125	2.9125	2.425	1.9	1.7375	1.0625	0.8	0.575
2C	4.0125	3.8625	3.7625	3.3	2.9	2.4125	1.8875	1.725	1.05	0.7875	0.5625
2B	4	3.85	3.75	3.2875	2.8875	2.4	1.875	1.7125	1.0375	0.775	0.55
2A	3.9875	3.8375	3.7375	3.275	2.875	2.3875	1.8625	1.7	1.025	0.7625	0.5375
29	3.975	3.825	3.725	3.2625	2.8625	2.375	1.85	1.6875	1.0125	0.75	0.525
28	3.9625	3.8125	3.7125	3.25	2.85	2.3625	1.8375	1.675	1	0.7375	0.5125
27	3.95	3.8	3.7	3.2375	2.8375	2.35	1.825	1.6625	0.9875	0.725	0.5
26	3.9375	3.7875	3.6875	3.225	2.825	2.3375	1.8125	1.65	0.975	0.7125	0.4875
25	3.925	3.775	3.675	3.2125	2.8125	2.325	1.8	1.6375	0.9625	0.7	0.475
24	3.9125	3.7625	3.6625	3.2	2.8	2.3125	1.7875	1.625	0.95	0.6875	0.4625
23	3.9	3.75	3.65	3.1875	2.7875	2.3	1.775	1.6125	0.9375	0.675	0.45
22	3.8875	3.7375	3.6375	3.175	2.775	2.2875	1.7625	1.6	0.925	0.6625	0.4375
21	3.875	3.725	3.625	3.1625	2.7625	2.275	1.75	1.5875	0.9125	0.65	0.425
20	3.8625	3.7125	3.6125	3.15	2.75	2.2625	1.7375	1.575	0.9	0.6375	0.4125
1F	3.85	3.7	3.6	3.1375	2.7375	2.25	1.725	1.5625	0.8875	0.625	0.4
1E	3.8375	3.6875	3.5875	3.125	2.725	2.2375	1.7125	1.55	0.875	0.6125	0.3875
1D	3.825	3.675	3.575	3.1125	2.7125	2.225	1.7	1.5375	0.8625	0.6	0.375
1C	3.8125	3.6625	3.5625	3.1	2.7	2.2125	1.6875	1.525	0.85	0.5875	0.3625
1B	3.8	3.65	3.55	3.0875	2.6875	2.2	1.675	1.5125	0.8375	0.575	0.35
1A	3.7875	3.6375	3.5375	3.075	2.675	2.1875	1.6625	1.5	0.825	0.5625	0.3375
19	3.775	3.625	3.525	3.0625	2.6625	2.175	1.65	1.4875	0.8125	0.55	0.325
18	3.7625	3.6125	3.5125	3.05	2.65	2.1625	1.6375	1.475	0.8	0.5375	0.3125
17	3.75	3.6	3.5	3.0375	2.6375	2.15	1.625	1.4625	0.7875	0.525	0.3
16	3.7375	3.5875	3.4875	3.025	2.625	2.1375	1.6125	1.45	0.775	0.5125	0.2875
15	3.725	3.575	3.475	3.0125	2.6125	2.125	1.6	1.4375	0.7625	0.5	0.275
14	3.7125	3.5625	3.4625	3	2.6	2.1125	1.5875	1.425	0.75	0.4875	0.2625
13	3.7	3.55	3.45	2.9875	2.5875	2.1	1.575	1.4125	0.7375	0.475	0.25
12	3.6875	3.5375	3.4375	2.975	2.575	2.0875	1.5625	1.4	0.725	0.4625	0.2375
11	3.675	3.525	3.425	2.9625	2.5625	2.075	1.55	1.3875	0.7125	0.45	0.225
10	3.6625	3.5125	3.4125	2.95	2.55	2.0625	1.5375	1.375	0.7	0.4375	0.2125
F	3.65	3.5	3.4	2.9375	2.5375	2.05	1.525	1.3625	0.6875	0.425	0.2
E	3.6375	3.4875	3.3875	2.925	2.525	2.0375	1.5125	1.35	0.675	0.4125	0.1875
D	3.625	3.475	3.375	2.9125	2.5125	2.025	1.5	1.3375	0.6625	0.4	0.175
C	3.6125	3.4625	3.3625	2.9	2.5	2.0125	1.4875	1.325	0.65	0.3875	0.1625
B	3.6	3.45	3.35	2.8875	2.4875	2	1.475	1.3125	0.6375	0.375	0.15
A	3.5875	3.4375	3.3375	2.875	2.475	1.9875	1.4625	1.3	0.625	0.3625	0.1375
9	3.575	3.425	3.325	2.8625	2.4625	1.975	1.45	1.2875	0.6125	0.35	0.125
8	3.5625	3.4125	3.3125	2.85	2.45	1.9625	1.4375	1.275	0.6	0.3375	0.1125
7	3.55	3.4	3.3	2.8375	2.4375	1.95	1.425	1.2625	0.5875	0.325	0.1
6	3.5375	3.3875	3.2875	2.825	2.425	1.9375	1.4125	1.25	0.575	0.3125	0.0875
5	3.525	3.375	3.275	2.8125	2.4125	1.925	1.4	1.2375	0.5625	0.3	0.075
4	3.5125	3.3625	3.2625	2.8	2.4	1.9125	1.3875	1.225	0.55	0.2875	0.0625
3	3.5	3.35	3.25	2.7875	2.3875	1.9	1.375	1.2125	0.5375	0.275	0.05

2	3.4875	3.3375	3.2375	2.775	2.375	1.8875	1.3625	1.2	0.525	0.2625	0.0375
1	3.475	3.325	3.225	2.7625	2.3625	1.875	1.35	1.1875	0.5125	0.25	0.025
0	3.4625	3.3125	3.2125	2.75	2.35	1.8625	1.3375	1.175	0.5	0.2375	0.0125

PVN1~ PVN11 gamma voltage mapping.

Register setting	PVN1	PVN2	PVN3	PVN4	PVN5	PVN6	PVN7	PVN8	PVN9	PVN10	PVN11
3F	-4.25	-4.1	-4	-3.5375	-3.1375	-2.65	-2.125	-1.9625	-1.2875	-1.025	-0.8
3E	-4.2375	-4.0875	-3.9875	-3.525	-3.125	-2.6375	-2.1125	-1.95	-1.275	-1.0125	-0.7875
3D	-4.225	-4.375	-3.975	-3.5125	-3.1125	-2.625	-2.1	-1.9375	-1.2625	-1	-0.775
3C	-4.2125	-4.0625	-3.9625	-3.5	-3.1	-2.6125	-2.0875	-1.925	-1.25	-0.9875	-0.7625
3B	-4.2	-4.35	-3.95	-3.4875	-3.0875	-2.6	-2.075	-1.9125	-1.2375	-0.975	-0.75
3A	-4.1875	-4.0375	-3.9375	-3.475	-3.075	-2.5875	-2.0625	-1.9	-1.225	-0.9625	-0.7375
39	-4.175	-4.325	-3.925	-3.4625	-3.0625	-2.575	-2.05	-1.8875	-1.2125	-0.95	-0.725
38	-4.1625	-4.0125	-3.9125	-3.45	-3.05	-2.5625	-2.0375	-1.875	-1.2	-0.9375	-0.7125
37	-4.15	-4.3	-3.9	-3.4375	-3.0375	-2.55	-2.025	-1.8625	-1.1875	-0.925	-0.7
36	-4.1375	-3.9875	-3.8875	-3.425	-3.025	-2.5375	-2.0125	-1.85	-1.175	-0.9125	-0.6875
35	-4.125	-4.275	-3.875	-3.4125	-3.0125	-2.525	-2	-1.8375	-1.1625	-0.9	-0.675
34	-4.1125	-3.9625	-3.8625	-3.4	-3	-2.5125	-1.9875	-1.825	-1.15	-0.8875	-0.6625
33	-4.1	-4.25	-3.85	-3.3875	-2.9875	-2.5	-1.975	-1.8125	-1.1375	-0.875	-0.65
32	-4.0875	-3.9375	-3.8375	-3.375	-2.975	-2.4875	-1.9625	-1.8	-1.125	-0.8625	-0.6375
31	-4.075	-4.225	-3.825	-3.3625	-2.9625	-2.475	-1.95	-1.7875	-1.1125	-0.85	-0.625
30	-4.0625	-3.9125	-3.8125	-3.35	-2.95	-2.4625	-1.9375	-1.775	-1.1	-0.8375	-0.6125
2F	-4.05	-4.2	-3.8	-3.3375	-2.9375	-2.45	-1.925	-1.7625	-1.0875	-0.825	-0.6
2E	-4.0375	-3.8875	-3.7875	-3.325	-2.925	-2.4375	-1.9125	-1.75	-1.075	-0.8125	-0.5875
2D	-4.025	-4.175	-3.775	-3.3125	-2.9125	-2.425	-1.9	-1.7375	-1.0625	-0.8	-0.575
2C	-4.0125	-3.8625	-3.7625	-3.3	-2.9	-2.4125	-1.8875	-1.725	-1.05	-0.7875	-0.5625
2B	-4	-4.15	-3.75	-3.2875	-2.8875	-2.4	-1.875	-1.7125	-1.0375	-0.775	-0.55
2A	-3.9875	-3.8375	-3.7375	-3.275	-2.875	-2.3875	-1.8625	-1.7	-1.025	-0.7625	-0.5375
29	-3.975	-4.125	-3.725	-3.2625	-2.8625	-2.375	-1.85	-1.6875	-1.0125	-0.75	-0.525
28	-3.9625	-3.8125	-3.7125	-3.25	-2.85	-2.3625	-1.8375	-1.675	-1	-0.7375	-0.5125
27	-3.95	-4.1	-3.7	-3.2375	-2.8375	-2.35	-1.825	-1.6625	-0.9875	-0.725	-0.5
26	-3.9375	-3.7875	-3.6875	-3.225	-2.825	-2.3375	-1.8125	-1.65	-0.975	-0.7125	-0.4875
25	-3.925	-4.075	-3.675	-3.2125	-2.8125	-2.325	-1.8	-1.6375	-0.9625	-0.7	-0.475
24	-3.9125	-3.7625	-3.6625	-3.2	-2.8	-2.3125	-1.7875	-1.625	-0.95	-0.6875	-0.4625
23	-3.9	-4.05	-3.65	-3.1875	-2.7875	-2.3	-1.775	-1.6125	-0.9375	-0.675	-0.45
22	-3.8875	-3.7375	-3.6375	-3.175	-2.775	-2.2875	-1.7625	-1.6	-0.925	-0.6625	-0.4375
21	-3.875	-4.025	-3.625	-3.1625	-2.7625	-2.275	-1.75	-1.5875	-0.9125	-0.65	-0.425
20	-3.8625	-3.7125	-3.6125	-3.15	-2.75	-2.2625	-1.7375	-1.575	-0.9	-0.6375	-0.4125
1F	-3.85	-4	-3.6	-3.1375	-2.7375	-2.25	-1.725	-1.5625	-0.8875	-0.625	-0.4
1E	-3.8375	-3.6875	-3.5875	-3.125	-2.725	-2.2375	-1.7125	-1.55	-0.875	-0.6125	-0.3875
1D	-3.825	-3.975	-3.575	-3.1125	-2.7125	-2.225	-1.7	-1.5375	-0.8625	-0.6	-0.375
1C	-3.8125	-3.6625	-3.5625	-3.1	-2.7	-2.2125	-1.6875	-1.525	-0.85	-0.5875	-0.3625
1B	-3.8	-3.95	-3.55	-3.0875	-2.6875	-2.2	-1.675	-1.5125	-0.8375	-0.575	-0.35
1A	-3.7875	-3.6375	-3.5375	-3.075	-2.675	-2.1875	-1.6625	-1.5	-0.825	-0.5625	-0.3375
19	-3.775	-3.925	-3.525	-3.0625	-2.6625	-2.175	-1.65	-1.4875	-0.8125	-0.55	-0.325
18	-3.7625	-3.6125	-3.5125	-3.05	-2.65	-2.1625	-1.6375	-1.475	-0.8	-0.5375	-0.3125
17	-3.75	-3.9	-3.5	-3.0375	-2.6375	-2.15	-1.625	-1.4625	-0.7875	-0.525	-0.3
16	-3.7375	-3.5875	-3.4875	-3.025	-2.625	-2.1375	-1.6125	-1.45	-0.775	-0.5125	-0.2875
15	-3.725	-3.875	-3.475	-3.0125	-2.6125	-2.125	-1.6	-1.4375	-0.7625	-0.5	-0.275
14	-3.7125	-3.5625	-3.4625	-3	-2.6	-2.1125	-1.5875	-1.425	-0.75	-0.4875	-0.2625
13	-3.7	-3.85	-3.45	-2.9875	-2.5875	-2.1	-1.575	-1.4125	-0.7375	-0.475	-0.25
12	-3.6875	-3.5375	-3.4375	-2.975	-2.575	-2.0875	-1.5625	-1.4	-0.725	-0.4625	-0.2375
11	-3.675	-3.825	-3.425	-2.9625	-2.5625	-2.075	-1.55	-1.3875	-0.7125	-0.45	-0.225
10	-3.6625	-3.5125	-3.4125	-2.95	-2.55	-2.0625	-1.5375	-1.375	-0.7	-0.4375	-0.2125
F	-3.65	-3.8	-3.4	-2.9375	-2.5375	-2.05	-1.525	-1.3625	-0.6875	-0.425	-0.2
E	-3.6375	-3.4875	-3.3875	-2.925	-2.525	-2.0375	-1.5125	-1.35	-0.675	-0.4125	-0.1875
D	-3.625	-3.775	-3.375	-2.9125	-2.5125	-2.025	-1.5	-1.3375	-0.6625	-0.4	-0.175
C	-3.6125	-3.4625	-3.3625	-2.9	-2.5	-2.0125	-1.4875	-1.325	-0.65	-0.3875	-0.1625
B	-3.6	-3.75	-3.35	-2.8875	-2.4875	-2	-1.475	-1.3125	-0.6375	-0.375	-0.15
A	-3.5875	-3.4375	-3.3375	-2.875	-2.475	-1.9875	-1.4625	-1.3	-0.625	-0.3625	-0.1375
9	-3.575	-3.725	-3.325	-2.8625	-2.4625	-1.975	-1.45	-1.2875	-0.6125	-0.35	-0.125
8	-3.5625	-3.4125	-3.3125	-2.85	-2.45	-1.9625	-1.4375	-1.275	-0.6	-0.3375	-0.1125
7	-3.55	-3.7	-3.3	-2.8375	-2.4375	-1.95	-1.425	-1.2625	-0.5875	-0.325	-0.1
6	-3.5375	-3.3875	-3.2875	-2.825	-2.425	-1.9375	-1.4125	-1.25	-0.575	-0.3125	-0.0875
5	-3.525	-3.675	-3.275	-2.8125	-2.4125	-1.925	-1.4	-1.2375	-0.5625	-0.3	-0.075
4	-3.5125	-3.3625	-3.2625	-2.8	-2.4	-1.9125	-1.3875	-1.225	-0.55	-0.2875	-0.0625
3	-3.5	-3.65	-3.25	-2.7875	-2.3875	-1.9	-1.375	-1.2125	-0.5375	-0.275	-0.05
2	-3.4875	-3.3375	-3.2375	-2.775	-2.375	-1.8875	-1.3625	-1.2	-0.525	-0.2625	-0.0375
1	-3.475	-3.625	-3.225	-2.7625	-2.3625	-1.875	-1.35	-1.1875	-0.5125	-0.25	-0.025
0	-3.4625	-3.3125	-3.2125	-2.75	-2.35	-1.8625	-1.3375	-1.175	-0.5	-0.2375	-0.0125

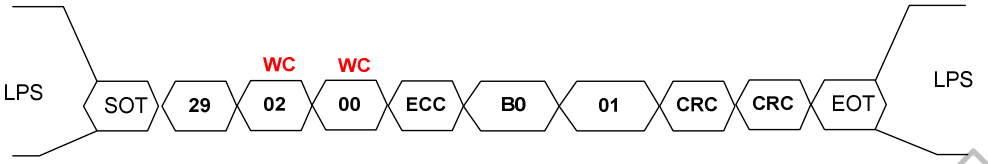
VBP[1:0]: Positive GAMMAN bias current selection.
VBN[1:0]: Negative GAMMAN bias current selection..

VBP/N[1]	VBP/N[0]	Gamma bias current
0	0	80%
0	1	100% **(default)**
1	0	120%
1	1	140%

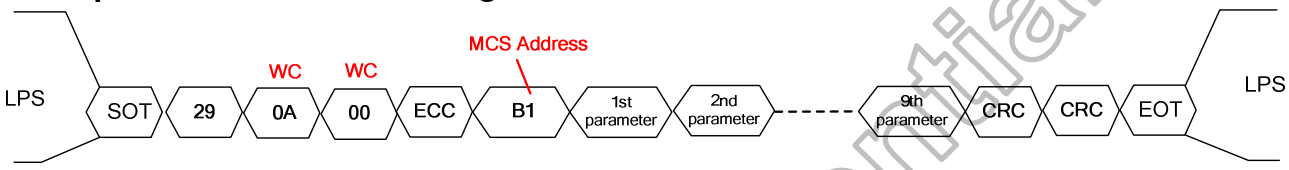
8.4.5 OTP Control register(page1 B1h)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set Gamma control register



Page	B1H	OTP control register								
1	Command	D7	D6	D5	D4	D3	D2	D1	D0	Hex
		1	0	1	1	0	0	0	1	B1
	1st parameter	OTP_Group								-
	2nd parameter	OTP_pwd								-
	3rd parameter		OTP_PTM			OTP_prog_sel	OTP_re_Load	OTP_RD	OTP_WR	-
	4th parameter	NC								-
	5th parameter	OTP_ADDR								-
	6th parameter	OTP_PDOB								-
	7th parameter	OTP_PDIN								-
	8th parameter	OTP_MANUAL								-
	9th parameter	-	-	-	-	POR	PPROG	VPS	PWE	-

Description

Detial OTP program flow please refer section 10.3

OTP_GROUP[4:0]: OTP trimming group selection. The group range is from group1 to group27
OTP_PWD[7:0]: The OTP password enter auto program mode.
OTP_WR: OTP write control.
OTP_RD: OTP read control.
OTP_RE_LOAD: OTP auto re-load control.
OTP_PTM[1:0]: OTP test mode.
OTP_ADDR[7:0]: OTP address set.
OTP_PDOB[7:0]: Read data from OTP.
OTP_PDIN[7:0]: Write data to OTP.**(for manual mode)**
OTP_MANUAL[7:0]: OTP password enter manual program mode.
DISABLE_OTP[1:0]: OTP function disables. **(for manual mode)**

DISABLE_OTP	Master OTP function	Slave OTP function
00b	Enable	Enable
01b	Enable	Disable
10b	Disable	Enable
11b	Disable	Disable

POR: OTP POR control signal. **(for manual mode)**
PPROG: OTP PPROG control signal. **(for manual mode)**

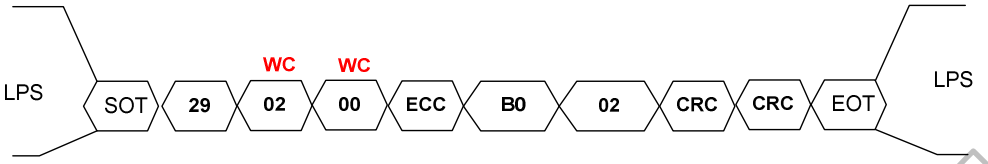
VPS: OTP VPS control signal. **(for manual mode)**

PWE: OTP PWE control signal. **(for manual mode)**

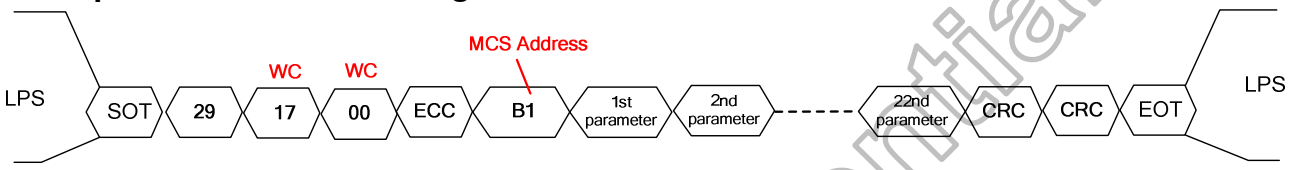
8.4.6 MUXL Control register(page2 B1h)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set MUXL control register

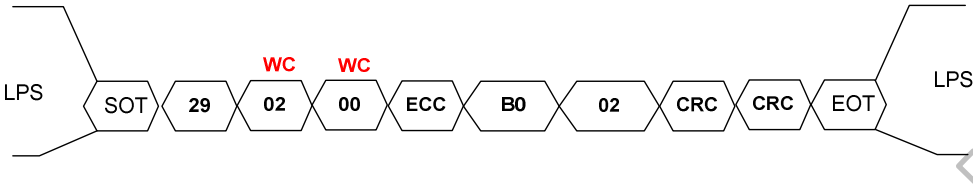


Page	B1H	MUXL Control register								
2	Command	D7	D6	D5	D4	D3	D2	D1	D0	Hex
		1	0	1	1	0	0	0	1	B1
	1st parameter	GOUTL1_STBYB_MOD		GOUTL_1_SEL						-
	2nd parameter	GOUTL2_STBYB_MOD		GOUTL_2_SEL						-
	3rd parameter	GOUTL3_STBYB_MOD		GOUTL_3_SEL						-
	4th parameter	GOUTL4_STBYB_MOD		GOUTL_4_SEL						-
	5th parameter	GOUTL5_STBYB_MOD		GOUTL_5_SEL						-
	6th parameter	GOUTL6_STBYB_MOD		GOUTL_6_SEL						-
	7th parameter	GOUTL7_STBYB_MOD		GOUTL_7_SEL						-
	8th parameter	GOUTL8_STBYB_MOD		GOUTL_8_SEL						-
	9th parameter	GOUTL9_STBYB_MOD		GOUTL_9_SEL						-
	10th parameter	GOUTL10_STBYB_MOD		GOUTL_10_SEL						-
	11th parameter	GOUTL11_STBYB_MOD		GOUTL_11_SEL						-
	12th parameter	GOUTL12_STBYB_MOD		GOUTL_12_SEL						-
	13th parameter	GOUTL13_STBYB_MOD		GOUTL_13_SEL						-
	14th parameter	GOUTL14_STBYB_MOD		GOUTL_14_SEL						-
	15th parameter	GOUTL15_STBYB_MOD		GOUTL_15_SEL						-
	16th parameter	GOUTL16_STBYB_MOD		GOUTL_16_SEL						-
	17th parameter	GOUTL17_STBYB_MOD		GOUTL_17_SEL						-
	18th parameter	GOUTL18_STBYB_MOD		GOUTL_18_SEL						-
	19th parameter	GOUTL19_STBYB_MOD		GOUTL_19_SEL						-
	20th parameter	GOUTL20_STBYB_MOD		GOUTL_20_SEL						-
	21st parameter	GOUTL21_STBYB_MOD		GOUTL_21_SEL						-
	22nd parameter	GOUTL22_STBYB_MOD		GOUTL_22_SEL						-
Description		**GOUTL_1_SEL ~ GOUTL_22_SEL:** Mux GOA signal to GOUTL1~ GOUTL22 **GOUTL1_STBYB_MOD~ GOUTL22_STBYB_MOD:** GOUTL1~ GOUTL22 standby staus selection 00:VGL 01:VGH 1X:GND								

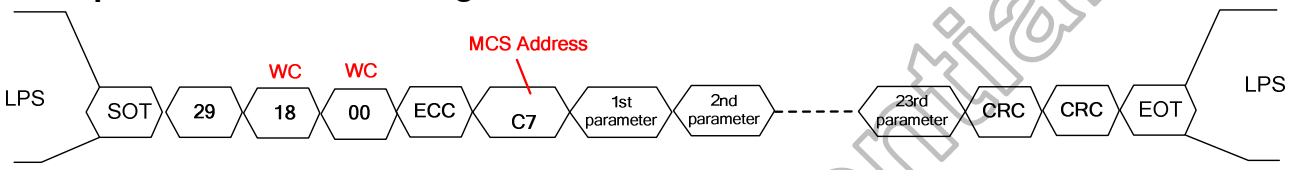
8.4.7 MUXR Control register(page2 C7h)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set MUXR control register



Page	C7H	MUXR control register								
2	Command	D7	D6	D5	D4	D3	D2	D1	D0	Hex
		1	1	0	0	0	1	1	1	C7
	1st parameter	GOUTR1_STBYB_MOD		GOUTR_1_SEL						-
	2nd parameter	GOUTR2_STBYB_MOD		GOUTR_2_SEL						-
	3rd parameter	GOUTR3_STBYB_MOD		GOUTR_3_SEL						-
	4th parameter	GOUTR4_STBYB_MOD		GOUTR_4_SEL						-
	5th parameter	GOUTR5_STBYB_MOD		GOUTR_5_SEL						-
	6th parameter	GOUTR6_STBYB_MOD		GOUTR_6_SEL						-
	7th parameter	GOUTR7_STBYB_MOD		GOUTR_7_SEL						-
	8th parameter	GOUTR8_STBYB_MOD		GOUTR_8_SEL						-
	9th parameter	GOUTR9_STBYB_MOD		GOUTR_9_SEL						-
	10th parameter	GOUTR10_STBYB_MOD		GOUTR_10_SEL						-
	11th parameter	GOUTR11_STBYB_MOD		GOUTR_11_SEL						-
	12th parameter	GOUTR12_STBYB_MOD		GOUTR_12_SEL						-
	13th parameter	GOUTR13_STBYB_MOD		GOUTR_13_SEL						-
	14th parameter	GOUTR14_STBYB_MOD		GOUTR_14_SEL						-
	15th parameter	GOUTR15_STBYB_MOD		GOUTR_15_SEL						-
	16th parameter	GOUTR16_STBYB_MOD		GOUTR_16_SEL						-
	17th parameter	GOUTR17_STBYB_MOD		GOUTR_17_SEL						-
	18th parameter	GOUTR18_STBYB_MOD		GOUTR_18_SEL						-
	19th parameter	GOUTR19_STBYB_MOD		GOUTR_19_SEL						-
	20th parameter	GOUTR20_STBYB_MOD		GOUTR_20_SEL						-
	21st parameter	GOUTR21_STBYB_MOD		GOUTR_21_SEL						-
	22nd parameter	GOUTR22_STBYB_MOD		GOUTR_22_SEL						-
	23rd parameter	VGL_GAS	GOA_VGOFF_EN	GOA_PWROFF	GOA_HZ_EN					-
	Description	**GOUTR_1_SEL ~ GOUTR_22_SEL:** Mux GOA signal to GOUTR1~ GOUTR22 **GOUTR1_STBYB_MOD~ GOUTR22_STBYB_MOD:** GOUTR1~ GOUTR22 standby staus selection. 00:VGL 01:VGH 1X:GND. **GOA_HZ_EN:** GOA HI Z enable. 1: Enable GOA single is HIZ. 0: Disable. **goa_poweroff:** goa all on and source pull to GND when power off phase. 1: Enable. 0: Disable. **GOA_VGOFF_EN:**GOA VGOFF mode enable. 1: Enable. 0: Disable. **VGL_GAS:**GOA output VGL level control 1:vgl tie to hi when GAS is eable 0:only VGL output									

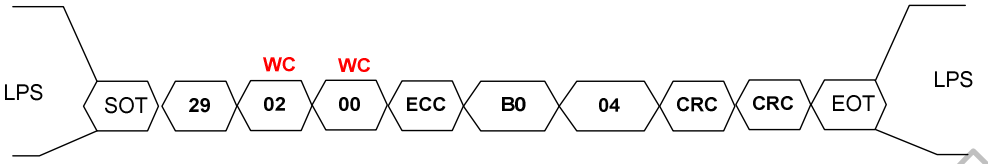
8.4.8 GOA Control register(page3 B1h)

GOA control register setting please refers Application Note.

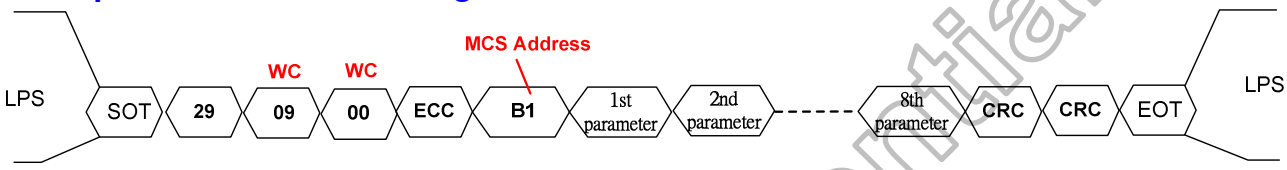
8.4.9 CABC Control register(page4 B1h)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set CABC control register



Page	B1H	CABC control register								
2	Command	D7	D6	D5	D4	D3	D2	D1	D0	Hex
		1	0	1	1	0	0	0	1	B1
	1st parameter	-	-	DIM_EN	BL_EN	CABC_AGAIN		-	CABC_AGAIN	-	-
	2nd parameter	-	-	-	-	DIM_STEP			DIM_FM		-
	3rd parameter	DUTY_UD									-
	4th parameter	CABC_MB									-
	5th parameter	PWM_PRD									-
	6th parameter						PWM_DIV				-
	7th parameter	Reserve									-
	8th parameter	MAX_DUTY									-

Description

CABC_AGING_EN: CABC aging enables.
1: Enable.
0: Disable.

PWM_POL: Poliarty of PWM control signal setting.
1: PWM output is inversion.
0: PWM output is non-inversion.

BL_EN: CABC back light control enables.
1: Enable.
0: Disable.

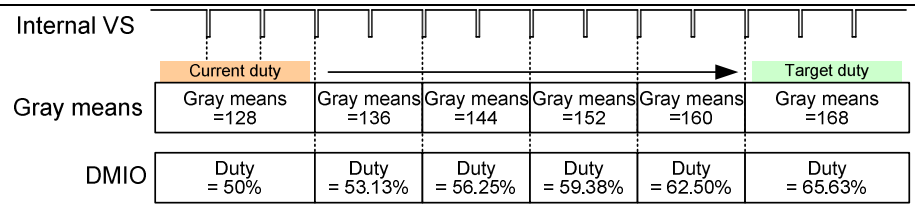
DIM_EN: CABC dimming enables.
1: Enable.
0: Disable.

DIM_FM[1:0]: CABC dimimng cycle settling.

DIM_FM[1]	DIM_FM[0]	CABC dimimng cycle
0	0	1 frame per step
0	1	2 frame per step **(default)**
1	0	3 frame per step
1	1	4 frame per step

DIM_STEP[1:0]:CABC dimming step setting

DIM_FM[1]	DIM_FM[0]	CABC dimimng cycle
0	0	2 steps
0	1	4 steps
1	0	8 steps **(default)**
1	1	16 steps



Note: (1) DIM_FRME[1:0]=01, DIM_STEP[1:0]=10, Max duty is 100%, Min duty is 0%.

DUTY_UD[7:0]: Set user-defined PWM duty on CABC bypass mode.
The CABC bypass mode is setting at 0xB6[3:2] of page0.

CABC_MB[7:0]: Set PWM minimum duty.

PWM_PRD[7:0]: CABC PWM period setting.

PWM_DIV[2:0]: CABC PWM period divider

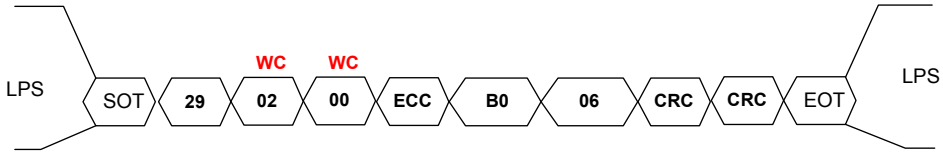
PWM_DIV[2]	PWM_DIV[1]	PWM_DIV[0]	CABC PWM period divider
0	0	0	DIV 1
0	0	1	DIV 2
0	1	0	DIV 4 **(default)**
0	1	1	DIV 8
1	0	0	DIV 16
1	0	1	DIV 32
1	1	0	DIV 64
1	1	1	DIV 128

MAX_DUTY[7:0]: Set PWM maximum duty.8'hff=100%,8'h00=0%.

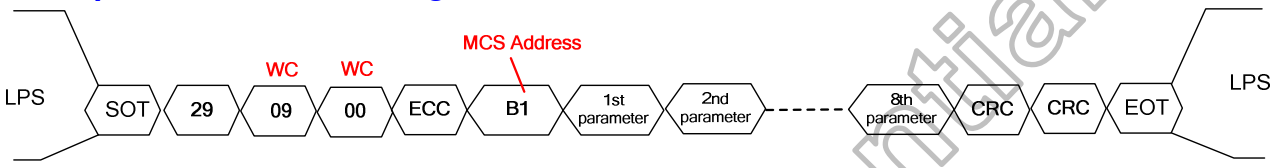
8.4.10 MIPI Control register(page6 B1h)

User could use HS or LP command send data

Step 1 set to page0



Step 2 set MIPI control register



Page	B1H	MIPI control register								
5	Command	D7	D6	D5	D4	D3	D2	D1	D0	Hex
		1	0	1	1	0	0	0	1	B1
	1st parameter	EoTp_EN	CRCEN	CRCErr_FilterOut	VC4FRAME	VC_S		VC_m		-
	2nd parameter	Reserved								-
	3rd parameter	Reserved								-
	4th parameter	Reserved								
	6th parameter	-	RT3			-	RT2			-
	7th parameter	-	RT1			-	RT0			-
	8th parameter	TurnDisable	-	-	-	-	RTC			-

Description

VC_m[1:0]: virtual channel ID setting of master **(for LP tx)**.
VC_S[1:0]: virtual channel ID setting of slave **(for LP/HS rx)**.
VC4FRAME: RX virtual channel filtering mode.
1: Enable.
0: Disable.

C**RCErr_FilterOut:** Filter-out by CRC check result enable.
1: Enable.
0: Disable.

CRCEN: CRC check enable.
1: Enable.
0: Disable.

EoTp_EN: Process of EoT packet enable.
1: Enable.
0: Disable.

RT0[2:0]: Lane0 termination resistance control.
RT1[2:0]: Lane1 termination resistance control.
RT2[2:0]: Lane2 termination resistance control.
RT3[2:0]: Lane3 termination resistance control.

RTC[2:0]: Clock lane termination resistance control.

RTx[2:0]	Ohm Ω
111	81
110	90
101	102 **(default)**
100	118
011	128
010	153
001	192
000	255

TurnDisable: BTA→TX procedure function enable.
1: Enable.
0: Disable.

8.5 Register Table (For LVDS input SPI mode)

8.5.1 Register of Page0

MIPI address	SPI address	Default	Bit name	Data[7:0]								Description	Group
0xB0	0x30	0Fh	PAGE									Page setting.	
0xB1	0x31	80h	VCOMS	1	0	0	0	0	0	0	0	VCOM voltage select.	0
0xB2	0x32	4bh	STB		1							Standby mode select.	1
			UPDNB			0						Veritical direction selection.	
			LR				0					Horizontal direction selection.	
			ZIGZAG_SEL					1				Panel type of selection.	
			DISP_ON						0			Disply on/off command.	
			NBW_SEL							1		Normal black/white panel selection.	
			BIST								1	TCON bist mode.	
0xB3	0x33	28h	ZTYPE_SEL	0	0							Type of zigzag selection.	
			PWRMD			1	0					Power mode selection.	
			VRES_FIX					1				Vertical Line changeable selection.	
			RES							0	0	Vertical Line selection.	
0xB4	0x34	C0h	VRES	1	1	0	0	0	0	0	0	Vertical Resolution select.	
0xB5	0x35	00h	ZDATA			0	0	0	0	0	0	ZigZag dummy data select.	
0xB6	0x36	03h	LNSW	0	0							MIPI data lane swap.	
			PNSW			0						MIPI lane P/N swap.	
			HFRC_INV				0					HI-FRC function inversion.	
			CABC_CTRL					0	0			CABC-Mode selection.	
			DITHER_EN							1		Dithering enable.	
			HFRC_EN								1	Hi-FRC enable.	
0xB7	0x37	53h	PCLK_SEL	0								PCLK source seclect.	
			RX_DINT		1							LVDS 6bit/8bit input select.	
			RX_VB			0	1					LVDS bias currect selection.	
			LVDS_VB						0	1		LVDS DLL bias currect selection.	
			LVDS_FMT								1	LVDS JEIDA / VESA format select.	
0xB8	0x38	00h	LVDS_TD		0	0	0					LVDS datalanes skew tuning.	
			LVDS_TC						0	0	0	LVDS clock lanesskew tuning.	
0xB9	0x39	12h	LVDS_BW			0	1					LVDS DLL bandwidth select.	
			LVDS_CPB						0	1	0	LVDS DLL pump current select .	
0xBA	0x3A	a9h	BLREV	1	0							Source output defines at Vblanking.	
			BLREVONOFF			1						Source output defines at Power on/off.	
			SD_ISSEL				0	1				Source Bias current.	
			INV_SEL						0	0	1	Inversion type select.	
0xBB	0x3B	68h	BC_CTRL	0								BC_CTRL output contrl.	
			GOA_EN		1							GOA enable.	
			RB_SWAP			1						R/B color swap.	
			DPFM_OSC_SEL				0	1				DPFM clcok selection.	
			LNSEL						0	0		MIPI lane nunmber select.	
0xBC	0x3C	E0h	GAS_GOA_EN	1								CKV/STV status select when GAS enable.	
			VRES_BLACK		1							Send black pattern when change VRES.	
			GCHL_Blanking			1						GCH/GCL output define at power on.	
0xBD	0x3D	aah	VSPS	1	0	1	0					VDDP voltage select.	
			VSNS					1	0	1	0	VDDN voltage select.	
0xBE	0x3E	23h	VGHS			1	0	0	0	1	1	VGH voltage select.	
0xBF	0x3F	14h	VGLS			0	1	0	1	0	0	VGL voltage select.	
0xC1	0x41	66h	VSPON	0	1	1	0					VSP PFM TON setting.	
			VSPOFF					0	1	1	0	VSP PFM TOFF setting.	

MIPI address	SPI address	Default	Bit name	Data[7:0]								Description	Group
0xC2	0x42	66h	VSNON	0	1	1	0					VSN PFM TON setting.	1
			VSNOFF					0	1	1	0	VSN PFM TOFFsetting.	
0xC3	0x43	70h	VGLXSP		1							VGH boost function.	
			VGHXSP			1	1					VGH boost function.	
			PFMFREN					0				PFM frequency randomizer enable.	
			T_OFFSET						0			PFM Ton Toff offset.	
0xC4	0x44	04h	VPHS				0	0	1	0	0	Positive gamma_H select.	
0xC5	0x45	adh	CGPP_INV	1								CGPP output invert enable.	
			SOFT_EN			1						Charge Pump soft start enable.	
			CLK_SEL				0	1	1			Charge Pump clock select.	
			CMD_SEL							0	1	Charge Pump command select.	
0xC6	0x46	04h	VNHS				0	0	1	0	0	Negative gamma_H select.	
0xC7	0x47		VCL_CPCTL			0	1					VCL charge pump frequency select.	
			VGL_CPCTL					0	1			VGL charge pump frequency select.	
			VGH_CPCTL							0	1	VGH charge pump frequency select.	
0xC8	0x48	06h	POCSD_CTL	0	0							SD offset cancel method select.	
			EQ0W			0	0	0	1	1	0	EQ0 precharge pluse width select.	
0xC9	0x49	00h	EQ1W				0	0	0	0	0	EQ1 precharge pluse width select.	
0xCA	0x4A	18h	EQ2W				1	1	0	0	0	EQ2 precharge pluse width select.	
0xCB	0x4B	3fh	PVP1			1	1	1	1	1	1	2nd Positive gamma op's input voltage.	2
0xCC	0x4C	34h	PVP2			1	1	0	1	0	0	3nd Positive gamma op's input voltage.	
0xCD	0x4D	2dh	PVP3			1	0	1	1	0	1	4dr Positive gamma op's input voltage.	
0xCE	0x4E	2dh	PVP4			1	0	1	1	0	1	5th Positive gamma op's input voltage.	
0XCF	0X4F	21h	PVP5			1	0	0	0	0	1	6th Positive gamma op's input voltage.	
0XD0	0X50	1bh	PVP6			0	1	1	0	1	1	7th Positive gamma op's input voltage.	
0XD1	0X51	1eh	PVP7			0	1	1	1	1	0	8th Positive gamma op's input voltage.	
0XD2	0X52	25h	PVP8			1	0	0	1	0	1	9th Positive gamma op's input voltage.	
0XD3	0X53	20h	PVP9			1	0	0	0	0	0	10th Positive gamma op's input voltage.	
0XD4	0X54	20h	PVP10			1	0	0	0	0	0	11th Positive gamma op's input voltage.	
0XD5	0X55	16h	PVP11			0	1	0	1	1	0	12th Positive gamma op's input voltage.	
0XD6	0X56	3fh	PVN1			1	1	1	1	1	1	2nd Negative gamma op's input voltage.	3
0XD7	0X57	33h	PVN2			1	1	0	0	1	1	3nd Negative gamma op's input voltage.	
0XD8	0X58	2ch	PVN3			1	0	1	1	0	0	4dr Negative gamma op's input voltage.	
0XD9	0X59	2eh	PVN4			1	0	1	1	1	0	5th Negative gamma op's input voltage.	
0XDA	0X5A	21h	PVN5			1	0	0	0	0	1	6th Negative gamma op's input voltage.	
0XDB	0X5B	1bh	PVN6			0	1	1	0	1	1	7th Negative gamma op's input voltage.	
0XDC	0X5C	1dh	PVN7			0	1	1	1	0	1	8th Negative gamma op's input voltage.	
0xDD	0x5D	24h	PVN8			1	0	0	1	0	0	9th Negative gamma op's input voltage.	
0XDE	0X5E	21h	PVN9			1	0	0	0	0	1	10th Negative gamma op's input voltage.	
0XDF	0X5F	1fh	PVN10			0	1	1	1	1	1	11th Negative gamma op's input voltage.	
0xE0	0x60	16h	PVN11			0	1	0	1	1	0	12th Negative gamma op's input voltage.	
0xE1	0x61	B5h	VBP					0	1			GAMMAP bias current select.	
			VBN							0	1	GAMMAN bias current select.	
0xFA	0x7A	70h	VENDER_ID	0	1	1	1	0	0	0	0	Driver ID and module ID.	X
0XFB	0X7B	01h	GRB								1	Global reset.	X
0XFC	0X7C	82h	PRODUCT ID1	1	0	0	0	0	0	1	0	PRODUCT ID 1.	X
0XFD	0X7D	60h	PRODUCT ID2	0	1	1	0	0	0	0	0	PRODUCT ID 2.	X
0XFE	0X7E	0Ah	PRODUCT ID3					1	0	1	0	PRODUCT ID 3.	X
0xFF	0x7F	03h	VERSIONID	0	0	0	0	0	0	1	1	IC version ID.	X

8.5.2 Register of Page(OTP)

MIPI Address	SPI Address	Default	Bit name	Data[7:0]								Description
0xB1	0x31	00h	OTP_Group				0	0	0	0	0	OTP trimming group select.
0xB2	0x32	5Ah	OTP_pwd	0	1	0	1	1	0	1	0	OTP program password.
0xB3	0x33	00h	OTP_PTM		0	0	0					Urer /margin read select.
			OTP_prog_sel					0				OTP program select.
			OTP_re_Load						0			OTP auto load.
			OTP_RD							0		OTP read command.
			OTP_WR								0	OTP write command.
0xB5	0x35	00h	OTP_ADDR	0	0	0	0	0	0	0	0	OTP address.
0xB6	0x36	00h	OTP_PDOB	0	0	0	0	0	0	0	0	OTP read out data.
0xB7	0x37	00h	OTP_PDIN	0	0	0	0	0	0	0	0	OTP program data.
0xB8	0x38	5Ah	OTP_MANUAL	0	1	0	1	1	0	1	0	OTP manual program.
0xB9	0x39	00h	POR					0				OTP POR control.
			PPROG						0			OTP PPROG control.
			VPS							0		OTP VPS control.
			PWE								0	OTP PWE control.

8.5.3 Registers of Page2 (GOA MUX)

MIPI address	SPI address	Default	Bit name	Data								Description	Group
0xB1	0x31	08h	GOUTL1_STBYB_MOD	0	0							GOUTL_1 standby staus select.	4
			GOUTL_1_SEL			0	0	1	0	0	0	Mux GOA signal to GINL1.	
0xB2	0x32	08h	GOUTL2_STBYB_MOD	0	0							GOUTL_2 standby staus select.	
			GOUTL_2_SEL			0	0	1	0	0	0	Mux GOA signal to GINL2.	
0xB3	0x33	06h	GOUTL3_STBYB_MOD	0	0							GOUTL_3 standby staus select.	
			GOUTL_3_SEL			0	0	0	1	1	0	Mux GOA signal to GINL3.	
0xB4	0x34	06h	GOUTL4_STBYB_MOD	0	0							GOUTL_4 standby staus select.	
			GOUTL_4_SEL			0	0	0	1	1	0	Mux GOA signal to GINL4.	
0xB5	0x35	0Ch	GOUTL5_STBYB_MOD	0	0							GOUTL_5 standby staus select.	
			GOUTL_5_SEL			0	0	1	1	0	0	Mux GOA signal to GINL5.	
0xB6	0x36	0Ch	GOUTL6_STBYB_MOD	0	0							GOUTL_6 standby staus select.	
			GOUTL_6_SEL			0	0	1	1	0	0	Mux GOA signal to GINL6.	
0xB7	0x37	0Ah	GOUTL7_STBYB_MOD	0	0							GOUTL_7 standby staus select.	
			GOUTL_7_SEL			0	0	1	0	1	0	Mux GOA signal to GINL7.	
0xB8	0x38	0Ah	GOUTL8_STBYB_MOD	0	0							GOUTL_8 standby staus select.	
			GOUTL_8_SEL			0	0	1	0	1	0	Mux GOA signal to GINL8.	
0xB9	0x39	02h	GOUTL9_STBYB_MOD	0	0							GOUTL_9 standby staus select.	
			GOUTL_9_SEL			0	0	0	0	1	0	Mux GOA signal to GINL9.	
0xBA	0x3A	00h	GOUTL10_STBYB_MOD	0	0							GOUTL_10 standby staus select.	
			GOUTL_10_SEL			0	0	0	0	0	0	Mux GOA signal to GINL10.	
0xBB	0x3B	00h	GOUTL11_STBYB_MOD	0	0							GOUTL_11 standby staus select.	
			GOUTL_11_SEL			0	0	0	0	0	0	Mux GOA signal to GINL11.	
0xBC	0x3C	00h	GOUTL12_STBYB_MOD	0	0							GOUTL_12 standby staus select.	
			GOUTL_12_SEL			0	0	0	0	0	0	Mux GOA signal to GINL12.	
0xBD	0x3D	00h	GOUTL13_STBYB_MOD	0	0							GOUTL_13 standby staus select.	
			GOUTL_13_SEL			0	0	0	0	0	0	Mux GOA signal to GINL13.	
0xBE	0x3E	00h	GOUTL14_STBYB_MOD	0	0							GOUTL_14 standby staus select.	
			GOUTL_14_SEL			0	0	0	0	0	0	Mux GOA signal to GINL14.	
0xBF	0x3F	00h	GOUTL15_STBYB_MOD	0	0							GOUTL_15 standby staus select.	
			GOUTL_15_SEL			0	0	0	0	0	0	Mux GOA signal to GINL15.	
0xC0	0x40	04h	GOUTL16_STBYB_MOD	0	0							GOUTL_16 standby staus select.	
			GOUTL_16_SEL			0	0	0	1	0	0	Mux GOA signal to GINL16.	
0xC1	0x41	00h	GOUTL17_STBYB_MOD	0	0							GOUTL_17 standby staus select.	
			GOUTL_17_SEL			0	0	0	0	0	0	Mux GOA signal to GINL17.	
0xC2	0x42	00h	GOUTL18_STBYB_MOD	0	0							GOUTL_18 standby staus select.	
			GOUTL_18_SEL			0	0	0	0	0	0	Mux GOA signal to GINL18.	
0xC3	0x43	00h	GOUTL19_STBYB_MOD	0	0							GOUTL_19 standby staus select.	
			GOUTL_19_SEL			0	0	0	0	0	0	Mux GOA signal to GINL19.	
0xC4	0x44	00h	GOUTL20_STBYB_MOD	0	0							GOUTL_20 standby staus select.	
			GOUTL_20_SEL			0	0	0	0	0	0	Mux GOA signal to GINL20.	
0xC5	0x45	00h	GOUTL21_STBYB_MOD	0	0							GOUTL_21 standby staus select.	
			GOUTL_21_SEL			0	0	0	0	0	0	Mux GOA signal to GINL21.	
0xC6	0x46	00h	GOUTL22_STBYB_MOD	0	0							GOUTL_22 standby staus select.	
			GOUTL_22_SEL			0	0	0	0	0	0	Mux GOA signal to GINL22.	

MIPI address	SPI address	Default	Bit name	Data								Description	Group
0xC7	0x47	07h	GOUTR1_STBYB_MOD	0	0							GOUTR_1 standby staus select.	4
			GOUTR_1_SEL			0	0	0	1	1	1	Mux GOA signal to GINR_1.	
0xC8	0x48	07h	GOUTR2_STBYB_MOD	0	0							GOUTR_2 standby staus select.	
			GOUTR_2_SEL			0	0	0	1	1	1	Mux GOA signal to GINR_2.	
0xC9	0x49	05h	GOUTR3_STBYB_MOD	0	0							GOUTR_3 standby staus select.	
			GOUTR_3_SEL			0	0	0	1	0	1	Mux GOA signal to GINR_3.	
0xCA	0x4A	05h	GOUTR4_STBYB_MOD	0	0							GOUTR_4 standby staus select.	
			GOUTR_4_SEL			0	0	0	1	0	1	Mux GOA signal to GINR_4.	
0xCB	0x4B	0Bh	GOUTR5_STBYB_MOD	0	0							GOUTR_5 standby staus select.	
			GOUTR_5_SEL			0	0	1	0	1	1	Mux GOA signal to GINR_5.	
0xCC	0x4C	0Bh	GOUTR6_STBYB_MOD	0	0							GOUTR_6 standby staus select.	
			GOUTR_6_SEL			0	0	1	0	1	1	Mux GOA signal to GINR_6.	
0xCD	0x4D	09h	GOUTR7_STBYB_MOD	0	0							GOUTR_7 standby staus select.	
			GOUTR_7_SEL			0	0	1	0	0	1	Mux GOA signal to GINR_7.	
0xCE	0x4E	09h	GOUTR8_STBYB_MOD	0	0							GOUTR_8 standby staus select.	
			GOUTR_8_SEL			0	0	1	0	0	1	Mux GOA signal to GINR_8.	
0xCF	0x4F	01h	GOUTR9_STBYB_MOD	0	0							GOUTR_9 standby staus select.	
			GOUTR_9_SEL			0	0	0	0	0	1	Mux GOA signal to GINR_9.	
0xD0	0x40	00h	GOUTR10_STBYB_MOD	0	0							GOUTR_10 standby staus select.	
			GOUTR_10_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_10.	
0xD1	0x41	00h	GOUTR11_STBYB_MOD	0	0							GOUTR_11 standby staus select.	
			GOUTR_11_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_11.	
0xD2	0x42	00h	GOUTR12_STBYB_MOD	0	0							GOUTR_12 standby staus select.	
			GOUTR_12_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_12.	
0xD3	0x43	00h	GOUTR13_STBYB_MOD	0	0							GOUTR_13 standby staus select.	
			GOUTR_13_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_13.	
0xD4	0x44	00h	GOUTR14_STBYB_MOD	0	0							GOUTR_14 standby staus select.	
			GOUTR_14_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_14.	
0xD5	0x45	00h	GOUTR15_STBYB_MOD	0	0							GOUTR_15 standby staus select.	
			GOUTR_15_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_15.	
0xD6	0x46	03h	GOUTR16_STBYB_MOD	0	0							GOUTR_16 standby staus select.	
			GOUTR_16_SEL			0	0	0	0	1	1	Mux GOA signal to GINR_16.	
0xD7	0x47	00h	GOUTR17_STBYB_MOD	0	0							GOUTR_17 standby staus select.	
			GOUTR_17_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_17.	
0xD8	0x48	00h	GOUTR18_STBYB_MOD	0	0							GOUTR_18 standby staus select.	
			GOUTR_18_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_18.	
0xD9	0x49	00h	GOUTR19_STBYB_MOD	0	0							GOUTR_19 standby staus select.	
			GOUTR_19_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_19.	
0xDA	0x4A	00h	GOUTR20_STBYB_MOD	0	0							GOUTR_20 standby staus select.	
			GOUTR_20_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_20.	
0xDB	0x4B	00h	GOUTR21_STBYB_MOD	0	0							GOUTR_21 standby staus select.	
			GOUTR_21_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_21.	
0xDC	0x4C	00h	GOUTR22_STBYB_MOD	0	0							GOUTR_22 standby staus select.	
			GOUTR_22_SEL			0	0	0	0	0	0	Mux GOA signal to GINR_22.	
0xDD	0x4D	40h	VGL_GAS	0								GOAOUT status when GAS enable.	
			GOA_VGOFF_EN		1							GOA VGOFF mode enable.	
			GOA_PWROFF			0						GOAOUT status when power off.	
			GOA_HZ_EN				0					GOA HI Z enable.	

8.5.4 Registers of Page3 (GOA)

GOA register setting please refers Application Note.

8.5.5 Registers of Page4 (CABC)

MIPI address	SPI address	Default	Bit name	Data								Description	Group
0xB1	0x31	3Bh	DIM_EN			1						Dimming function enable.	5
			BL_EN				1					Blacklight enable.	
			PWM_POL					1				PWM output polarity select.	
			CABC_AGAIN							1		CABC block aging enable.	
0xB2	0x32	09h	DIM_STEP					1	0			Dimming step setting.	
			DIM_FRME							0	1	Dimming cycle setting.	
0xB3	0x33	FFh	DUTY_UD	1	1	1	1	1	1	1	1	Bypass mode duty setting.	
0xB4	0x34	10h	CABC_MB	0	0	0	1	0	0	0	0	Minimun duty constraint.	
0xB5	0x35	00h	PWM_PRD	0	0	0	0	0	0	0	0	PWM period setting.	
0xB6	0x36	02h	PWM_DIV						0	1	0	PWM period divider setting.	
0xB8	0x38	FFh	MAX_DUTY	1	1	1	1	1	1	1	1	CABC max duty.	

8.5.6 Registers of Page6 (MIPI)

MIPI address	SPI address	Default	Bit name	Data								Description	Group
0xB1	0x31	E0h	EoTp_EN	1								Process of EoT packet enable.	6
			CRCEN		1							CRC check enable.	
			CRCErr_FilterOut			1						Filter-out by CRC check result enable.	
			VC4FRAME				0					RX virtual channel filtering mode.	
			VC_S					0	0			virtual channel ID setting of slave **(for LP/HS rx)**.	
			VC_m							0	0	virtual channel ID setting of master **(for LP tx)**.	
0xB5	0x35	55h	RT3		1	0	1					Lane3 termination resistance control.	8
			RT2						1	0	1	Lane2 termination resistance control.	
0xB6	0x36	55h	RT1		1	0	1					Lane1 termination resistance control.	
			RT0						1	0	1	Lane0 termination resistance control.	
0xB7	0x37	05h	TurnDisable	0								BTA->TX procedure function enable.	
			RTC						1	0	1	Clock lane termination resistance control.	

9. Register Description (for LVDS input SPI mode)

9.1 Registers of Page0

- Address is 0xB1

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	VCOMS								V
Description	VCOM voltage select **(step=10mV) (OTP 3 times)**								
Default	1	0	0	0	0	0	0	0	

VCOMS[7:0]	VCOM Voltage
00000000	-0.2V
00000001	-0.21V
00000010	-0.22V
:	:
:	:
10000000	-1.48V **(default)**
:	:
:	:
11111111	-2.75V

- Address is 0xB2

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NA	STB	UPDNB	LR	ZIGZAG_SEL	DISP_ON	NBW_SEL	BIST	V
Default	0	1	0	0	1	0	1	1	

Bit	Item	Description
6	STB	TCON sleep mode selection. MIPI DCS 0x10 **(Enter sleep mode)**, and 0x11 **(exit sleep mode)**. MIPI DCS command do XOR with SPI register.
5	UPDNB	Vertical direction selection. MIPI DCS 0x36 set_address_mode[7] command and SPI register do XOR operation.
4	LR	Horizontal direction selection. MIPI DCS 0x36 set_address_mode[6] command and SPI register do XOR operation.
3	ZIGZAG_SEL	Panel driving method selection.0:Strip panel ,1:Zigzag type panel
2	DISP_ON	MIPI DCS: 0x28 display on, 0x29 display off 0: Follow MIPI_DCS command. 1: Reverse MIPI_DCS command. **(to MIPI_DCS command do "XOR" operation)**
1	NBW_SEL	Normal Black and Normal white panel selection. 0:Normally white ,1:Normally black
0	BIST	TCON bist mode selection. 0:BIST mode ,1:Normal mode

- Address is 0xB3

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	ZTYPE_SEL[1]	ZTYPE_SEL[0]	PWRMD[1]	PWRMD[0]	VRES_FIX	NC	RES[1]	RES[0]	V
Default	0	0	1	0	1	0	0	0	

Bit	Item	Description
7	ZTYPE_SEL[1]	Zigzag type slection **(panel type please refer section 6.3)**.
6	ZTYPE_SEL[0]	0: Zigzag type 0 , 1: Zigzag type 1 2:Zigzag type 2 3:Zigzag type3
5	PWRMD[1]	POWR ON mode **(to pin PWRMD do XOR operation)**.
4	PWRMD[0]	**PWRMD[1]** / **PWRMD[0]** / **Driving mode** 0 / 0 / Support HX5186-C power mode 0 / 1 / Suppot PFM circuit power mode 1 / 0 / External VSP,VSN, VGH,VGL power mode**(default)**. 1 / 1 / External VSP,VSN power mode
3	VRES_FIX	Display vertical Line decide by(1):RES[2:0] or (0) VRES **(Register 0xB4)**
1	RES[1]	Resolution selection **(to pin HW RES do XOR operation)**.
0	RES[0]	Resolution setting please refer section 6.1

- Address is 0xB4

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	VRES								V
Description	Vertical Resolution selection , VRES[7:0], range=80~ 253, step= 8H								
Default	1	1	0	0	0	0	0	0	

- Address is 0xB5

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	ZDATA						V
Description	ZigZag dummy data selection								
Default	0	0	0	0	0	0	0	0	

- Address is 0xB6

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	LNSW[1]	LNSW[0]	PNSW	HFRC_INV	CABC_CTRL[1]	CABC_CTRL[0]	DITHER_EN	HFRC_EN	V
Default	0	0	0	0	0	0	1	1	

Bit	Item	Description
7	LNSW[1]	MIPI lane swap **(to pin LNSW do XOR operation)**.
6	LNSW[0]	

		D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N
LNSW[1]	LNSW[0]	MIPI lanes mapping table									
0	0	D3P	D3N	D2P	D2N	CLKP	CLKN	D1P	D1N	D0P	D0N
0	1	D3P	D3N	D0P	D0N	CLKP	CLKN	D1P	D1N	D2P	D2N
1	0	D0P	D0N	D1P	D1N	CLKP	CLKN	D2P	D2N	D3P	D3N
1	1	D2P	D2N	D1P	D1N	CLKP	CLKN	D0P	D0N	D3P	D3N

5	PNSW	MIPI/LVDS pin change polarity **(to pin PNSW do XOR operation)** 1:P/N swap.
4	HFRC_INV	HI-FRC function inversion.1: HFRC code=4, 9, 14, 0: HFRC code=241, 246, 251 **(Default=0)**
3	CABC_CTRL[1]	CABC-Mode selection:
2	CABC_CTRL[0]	

CABC_CTRL[1]	CABC_CTRL[0]	CABC Mode
0	0	Bypass mode **(default)**
0	1	Still-mode
1	0	UI-mode
1	1	MovingI-mode

1	DITHER_EN	Dithering enable.1: dithering enable, 0: dithering disable.
0	HFRC_EN	Hi-FRC enable.1:HFRC enable 0:HFRC disable.

- Address is 0xB7

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	PCLK_SEL	RX_DINT	RX_VB[1]	RX_VB[0]	NC	LVDS_VB[1]	LVDS_VB[0]	LVDS_FMT	V
Default	0	1	0	1	0	0	1	1	

Bit	Item	Description
7	PCLK_SEL	TCON PCLK source 0:frome internal OSC25M 1:from EXT_CLK.
6	RX_DINT	LVDS 8 bit mode 1:8bit mode 0:6 bit mode.
5	RX_VB[1]	LVDS bias current selection.
4	RX_VB[0]	

LVDS_RX[1]	LVDS_RX[0]	LVDS bias current
0	0	75%
0	1	100%
1	0	125%
1	1	150%

2	LVDS_VB[1]	LVDS DLL bias current selection.
1	LVDS_VB[0]	

LVDS_VB[1]	LVDS_VB[0]	LVDS DLL bias current
0	0	82%
0	1	100%
1	0	137%
1	1	160%

0	LVDS_FMT	LVDS data format select 0:NS or JEIDA forma 1:Thine or VESA format

- Address is 0xB8

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	LVDS_TD[2]	LVDS_TD[1]	LVDS_TD[0]	NC	LVDS_TC[2]	LVDS_TC[1]	LVDS_TC[0]	V
Default	0	0	0	0	0	0	0	0	

Bit	Item	Description
6	LVDS_TD[2]	LVDS_TC skew tuning for LVDS Data lanes 1setp delay 0.18 nsec.
5	LVDS_TD[1]	
4	LVDS_TD[0]	
2	LVDS_TC[2]	LVDS_TC skew tuning for LVDS Clock lanes 1setp delay 0.18 nsec.
1	LVDS_TC[1]	
0	LVDS_TC[0]	

- Address is 0xB9

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	LVDS_BW[1]	LVDS_BW[0]	NC	LVDS_CPB[2]	LVDS_CPB[1]	LVDS_CPB[0]	V
Default	0	0	0	1	0	0	1	0	

Bit	Item	Description
5	LVDS_BW[1]	LVDS DLL bandwidth selection
4	LVDS_BW[0]	
2	LVDS_CPB[2]	LVDS DLL pump current selection. I=20u*CPB[2]+10u*CPB[1]+5u*CPB[0]
1	LVDS_CPB[1]	
0	LVDS_CPB[0]	

LVDS_BW[1]	LVDS_BW[0]	LVDS bias current
0	0	100%
0	1	91%
1	0	83%
1	1	77%

- Address is 0xBA

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	BLREV[1]	BLREV[0]	BLREVONOFF	SD_ISSEL[1]	SD_ISSEL[0]	INV_SEL[2]	INV_SEL[1]	INV_SEL[0]	V
Default	1	0	1	0	1	0	0	1	

Bit	Item	Description
7	BLREV[1]	Source output at V-blanking. 00:SD keep output the last line. 01: Hi-Z. 1X: GND.
6	BLREV[0]	
5	BLREVONOFF	Source output at power on off. 1: GND. 0: Hi-Z.
4	SD_ISSEL[1]	Source output bias current selection.
3	SD_ISSEL[0]	
2	INV_SEL[2]	Normal mode POL inversion type selection **(for strip panel only)**.
1	INV_SEL[1]	
0	INV_SEL[0]	

INV_SEL[2]	INV_SEL[1]	INV_SEL[0]	Inversion tpye
0	0	0	line inversion
0	0	1	2-line inversion
0	1	0	4-line inversion
0	1	1	column inversion
1	0	0	8-line inversion

- Address is 0xBB

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	BC_CTRL	GOA_EN	RB_SWAP	DPFM_OSC_SEL[1]	DPFM_OSC_SEL[0]	LNSEL[1]	LNSEL[0]	NC	V
Default	0	1	1	0	1	0	0	0	

Bit	Item	Description
7	BC_CTRL	H/W pin BC_CTRL control.
6	GOA_EN	GOA function enables.1:enable ,0:disable.
5	RB_SWAP	Red and Blue color swap.1:R/B swap,0:non-swap.
4	DPFM_OSC_SEL[1]	DPFM clock selection **(for BIST mode use clock)**.
3	DPFM_OSC_SEL[0]	
2	LNSEL[1]	MIPI lane number control. The register do XOR with LANE1_STBYB & LANE0_BISTB pin.
1	LNSEL[0]	

DPFM_OSC_SEL[1]	DPFM_OSC_SEL[0]	DPFM frequency
0	0	6.25MHz
0	1	12.5MHz
1	0	25MHz
1	1	25MHz

- Address is 0xBC

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	GAS_GOA_EN	VRES_BLACK	GCHL_Blanking	NC	NC	NC	NC	NC	V
Default	1	1	1	0	0	0	0	0	

Bit	Item	Description
7	GAS_GOA_EN	1: When enable gas function, GOA CKV/STV pulled to high level.
6	VRES_BLACK	1: When user change VRES register, TCON will send two black pattern.
5	GCHL_Blanking	1: CLR1 =GND, CLR2=High level ,when power on status. 0: CLR1/2 =GND, when power on status.

- Address is 0xBD

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	VSPS[3]	VSPS[2]	VSPS[1]	VSPS[0]	VSNS[3]	VSNS[2]	VSNS[1]	VSNS[0]	V
Description	VDDP voltage selection **(step=0.1V)**				VDDN voltage selection **(step=0.1V)**				
Default	1	0	1	0	1	0	1	0	

VSPS [3:0]	Voltage
0000	4.5V
0001	4.6V
0010	4.7V
:	:
1010	5.5V
:	:
1111	6V

VSNS [3:0]	Voltage
0000	-4.5V
0001	-4.6V
0010	-4.7V
:	:
1010	-5.5V
:	:
1111	-6V

- Address is 0xBE

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	VGHS[5]	VGHS[4]	VGHS[3]	VGHS[2]	VGHS[1]	VGHS[0]	V
Description			VGH voltage selection						
Default	0	0	1	0	0	0	1	1	

VGHS [5:0]	Voltage
000000	8V
000001	8.2V
000010	8.4V
:	:
:	:
100011	15V
:	:
:	:
111111	20.6V

- Address is 0xBF

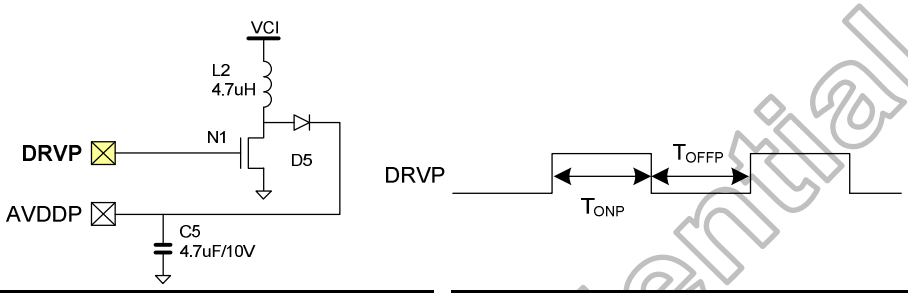
Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	VGLS[5]	VGLS[4]	VGLS[3]	VGLS[2]	VGLS[1]	VGLS[0]	V
Description			VGL voltage selection						
Default	0	0	0	1	0	1	0	0	

VGLS [5:0]	Voltage
000000	-6V
000001	-6.2V
000010	-6.4V
:	:
:	:
010100	-10V
:	:
:	:
111111	-18.6V

- Address is 0xC1

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	VSPON[3]	VSPON[2]	VSPON[1]	VSPON[0]	VSPOFF[3]	VSPOFF[2]	VSPOFF[1]	VSPOFF[0]	V
Default	0	1	1	0	0	1	1	0	

Bit	Item	Description
[7:4]	VSPON [3:0]	Select VSP PFM TON tonp = tpfmclk * (TONP[3:0]+ 4 + N) if PRMFREN=0 N=1.
[3:0]	VSPOFF[3:0]	Select VSP PFM TOFF toffp = tpfmclk * (TOFFP[3:0]+ 5).



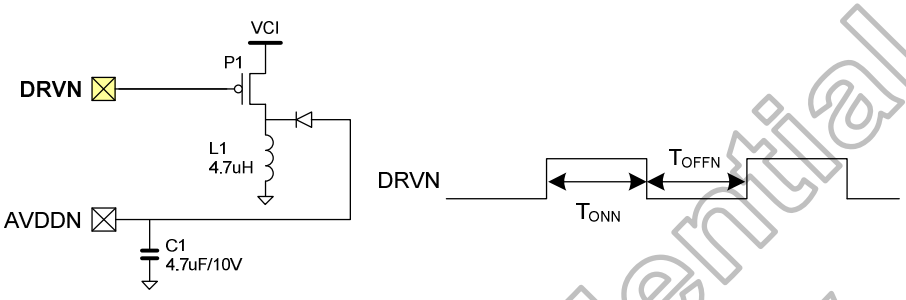
VSPON_T[3:0]	T_{ONP}(µs)
0	1.0
1	1.2
2	1.4
3	1.6
∫	
13	3.6
14	3.8
15	4.0

VSPOFF_T[3:0]	T_{OFFP}(µs)
0	1.0
1	1.2
2	1.4
3	1.6
∫	
13	3.6
14	3.8
15	4.0

- Address is 0xC2

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	VSNON[3]	VSNON[2]	VSNON[1]	VSNON[0]	VSNOFF[3]	VSNOFF[2]	VSNOFF[1]	VSNOFF[0]	V
Default	0	1	1	0	0	1	1	0	

Bit	Item	Description
[7:4]	VSNON [3:0]	Select VSN PFM TON tonp = tpfmclk * (TONP[3:0]+ 4 + N) if PRMFREN=0 N=1.
[3:0]	VSNPOFF[3:0]	Select VSN PFM TOFF toffp = tpfmclk * (TOFFP[3:0]+ 5).



VSNON_T[3:0]	T_{ONN}(µs)
0	1.0
1	1.2
2	1.4
3	1.6
∫	
13	3.6
14	3.8
15	4.0

VSNOFF_T[3:0]	T_{OFFN}(µs)
0	1.0
1	1.2
2	1.4
3	1.6
∫	
13	3.6
14	3.8
15	4.0

- Address is 0xC3

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	VGLXSP	VGHXSP[1]	VGHXSP[0]	PFMFREN	T_OFFSET	NC	NC	NC	V
Default	1	1	1	0	0	0	0	0	

Bit	Item	Description
7	VGLXSP	VGL boost function selection. 0:VSN-VSP. 1:2VSN-VSP.
[6:5]	VGHXSP[1:0]	VGH boost function selection. 00: 2VSP. 01: 2VSP+(-VSN). 1x: 2VSP+2(-VSN).
4	PFMFREN	Enable frequency randomizer of both VDDP and VDDN PFM.
3	T_OFFSET	PFM ton / toff offset.

- Address is 0xC4

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	NC	VPHS[4]	VPHS[3]	VPHS[2]	VPHS[1]	VPHS[0]	V
Description	Positive gamma high selection								
Default	0	0	0	0	0	1	0	1	

VPHS [4:0]	Voltage
00000	4
00001	4.05V
00010	4.1V
:	:
:	:
00100	4.2V **(default)**
:	:
:	:
11111	5.5V

- Address is 0xC5

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	CGPP_INV[1]	CGPP_INV[0]	SOFT_EN	CLK_SEL[2]	CLK_SEL[1]	CLK_SEL[0]	CMD_SEL[1]	CMD_SEL[0]	V
Default	1	0	1	0	1	1	0	1	

Bit	Item	Description
[7:6]	CGPP_INV	CGPP_INV [1] set the DRVN signal, CGPP_INV [0] set the DRVP signal. 1: Invert. 0: Non-invert.
5	SOFT_EN	Power mode 00 Charge Pump soft start. 0: Disable. 1: Enable.
[4:2]	CLK_SEL	CLK_SEL[2:0] / Frequency 000 / 403kHz 001 / 595kHz 010 / 781 kHz 011 / 963kHz **(default)** 100 / 1136 kHz 101 / 1389kHz 110 / 1786kHz 111 / 2083kHz
[1:0]	CMD_SEL	Power mode 00: charge Pump command select CMD_SEL[1] / CMD_SEL[0] / Pump command 0 / 0 / x1.5 0 / 1 / x2 **(default)** 1 / 0 / x3 1 / 1 / x3

- Address is 0xC6

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	NC	VNHS[4]	VNHS[3]	VNHS[2]	VNHS[1]	VNHS[0]	V
Description	Negative gamma high selection								
Default	0	0	0	0	0	1	0	0	

VNHS [4:0]	Voltage
00000	-4
00001	-4.05V
00010	-4.1V
:	:
:	:
00100 **(default)**	-4.2V
:	:
:	:
11111	-5.5V

- Address is 0xC7

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	VCL_CPCTL[1]	VCL_CPCTL[0]	VGL_CPCTL[1]	VGL_CPCTL[0]	VGH_CPCTL[1]	VGH_CPCTL[0]	V
Default	0	0	0	1	0	1	0	1	

Bit	Item	Description
[5:4]	VCL_CPCTL	VCL charge pump clock frequency. 00: X1. 01: X2. 10: X4. 11: X8. **(unit=line frequency)**
[3:2]	VGL_CPCTL	VGL charge pump clock frequency. 00: X1. 01: X2. 10: X4. 11: X8. **(unit=line frequency)**
[1:0]	VGH_CPCTL	VGH charge pump clock frequency. 00: X1. 01: X2. 10: X4. 11: X8. **(unit=line frequency)**

- Address is 0xC8

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	POCSD_CTL[1]	POCSD_CTL[0]	EQ0W[5]	EQ0W[4]	EQ0W[3]	EQ0W[2]	EQ0W[1]	EQ0W[0]	V
Default	0	0	0	0	0	1	1	0	

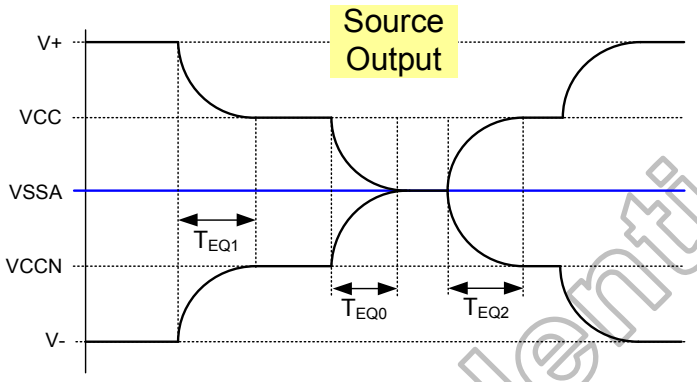
Bit	Item	Description
[7:6]	POCSD_CTL	Source output offset cancel method selection. POCSD_CTL=00b L1 L2 L3 L4 L5 L6 L7 L8 Frame1 0 1 1 0 0 1 1 0 Frame2 0 0 1 1 0 0 1 1 Frame3 1 0 0 1 1 0 0 1 Frame4 1 1 0 0 1 1 0 0 Frame5 0 1 1 0 0 1 1 0 Frame6 0 0 1 1 0 0 1 1 POCSD_CTL=01b L1 L2 L3 L4 L5 L6 L7 L8 Frame1 1 1 0 0 1 1 0 0 Frame2 1 1 0 0 1 1 0 0 Frame3 0 0 1 1 0 0 1 1 Frame4 0 0 1 1 0 0 1 1 Frame5 1 1 0 0 1 1 0 0 Frame6 1 1 0 0 1 1 0 0 POCSD_CTL=10b L1 L2 L3 L4 L5 L6 L7 L8 Frame1 1 0 1 0 1 0 1 0 Frame2 1 0 1 0 1 0 1 0 Frame3 0 1 0 1 0 1 0 1 Frame4 0 1 0 1 0 1 0 1 Frame5 1 0 1 0 1 0 1 0 Frame6 1 0 1 0 1 0 1 0 POCSD_CTL=11b L1 L2 L3 L4 L5 L6 L7 L8 Frame1 0 0 0 0 0 0 0 0 Frame2 0 0 0 0 0 0 0 0 Frame3 0 0 0 0 0 0 0 0 Frame4 0 0 0 0 0 0 0 0 Frame5 0 0 0 0 0 0 0 0 Frame6 0 0 0 0 0 0 0 0
[5:0]	EQ0W	Source EQ0 time setting. TEQ0=EQ0W[4:0]x4 DCLK **(Min is 12DCLK)**.

- Address is 0xC9

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	NC	EQ1W[4]	EQ1W[3]	EQ1W[2]	EQ1W[1]	EQ1W[0]	V
Description	Source EQ1 time setting. TEQ1=EQ1W[4:0]x4 DCLK.								
Default	0	0	0	0	0	0	0	0	

- Address is 0xCA

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	NC	EQ2W[4]	EQ2W[3]	EQ2W[2]	EQ2W[1]	EQ2W[0]	V
Description	Source EQ2 time setting. TEQ2=EQ2W[4:0]x4 DCLK **(TEQ2≤TOEV-22DCLK satisfies gate driver settle time)**.								
Default	0	0	0	1	1	0	0	0	



- Address are 0xCB~E0

MIPI address	Default	Name	Description	OTP
0xCB	3fh	PVP1	Control 1st Positive gamma op's input voltage. Default: 3.462V~4.250V. Step=12.5mV.	V
0xCC	34h	PVP2	Control 2nd Positive gamma op's input voltage. Default:3.312V~4.100V. Step=12.5mV.	
0xCD	2dh	PVP3	Control 3dr Positive gamma op's input voltage. Default:3.212V~4.000V. Step=12.5mV.	
0xCE	2dh	PVP4	Control 4th Positive gamma op's input voltage. Default:2.750V~3.537V. Step=12.5mV.	
0XCF	21h	PVP5	Control 5th Positive gamma op's input voltage. Default:2.350V~3.137V. Step=12.5mV.	
0XD0	1bh	PVP6	Control 6th Positive gamma op's input voltage. Default:1.862V~2.650V. Step=12.5mV.	
0XD1	1eh	PVP7	Control 7th Positive gamma op's input voltage. Default:1.337V~2.125V. Step=12.5mV.	
0XD2	25h	PVP8	Control 8th Positive gamma op's input voltage.Default:1.175V~1.962V. Step=12.5mV.	
0XD3	20h	PVP9	Control 9th Positive gamma op's input voltage. Default:0.500V~1.287V. Step=12.5mV.	
0XD4	20h	PVP10	Control 10th Positive gamma op's input voltage. Default:0.237V~1.025V. Step=12.5mV.	
0XD5	16h	PVP11	Control 11th Positive gamma op's input voltage. Default:0.012V~0.800V. Step=12.5mV.	
0XD6	3fh	PVN1	Control 1st Negative gamma op's input voltage.Default:-3.462V~-4.250V. Step=-12.5mV.	
0XD7	33h	PVN2	Control 2nd Negative gamma op's input voltage. Default:-3.312V~-4.100V. Step=-12.5mV.	
0XD8	2ch	PVN3	Control 3dr Negative gamma op's input voltage. Default:-3.212V~-4.000V. Step=-12.5mV.	
0XD9	2eh	PVN4	Control 4th Negative gamma op's input voltage. Default:-2.750V~-3.537V. Step=-12.5mV.	
0XDA	21h	PVN5	Control 5th Negative gamma op's input voltage. Default:-2.350V~-3.137V. Step=-12.5mV.	
0XDB	1bh	PVN6	Control 6th Negative gamma op's input voltage. Default:-1.862V~-2.650V. Step=-12.5mV.	
0XDC	1dh	PVN7	Control 7th Negative gamma op's input voltage. Default:-1.337V~-2.125V. Step=-12.5mV.	
0xDD	24h	PVN8	Control 8th Negative gamma op's input voltage. Default:-1.175V~-1.962V. Step=-12.5mV.	
0XDE	21h	PVN9	Control 9th Negative gamma op's input voltage. Default:-0.500V~-1.287V. Step=-12.5mV.	
0XDF	1fh	PVN10	Control 10th Negative gamma op's input voltage. Default:-0.237V~-1.025V. Step=-12.5mV.	
0xE0	16h	PVN11	Control 11th Negative gamma op's input voltage. Default:0.012V~0.800V. Step=-12.5mV.	

PVP1~ PVP11 gamma voltage mapping

Register setting	PVP1	PVP2	PVP3	PVP4	PVP5	PVP6	PVP7	PVP8	PVP9	PVP10	PVP11
3F	4.25	4.1	4	3.5375	3.1375	2.65	2.125	1.9625	1.2875	1.025	0.8
3E	4.2375	4.0875	3.9875	3.525	3.125	2.6375	2.1125	1.95	1.275	1.0125	0.7875
3D	4.225	4.075	3.975	3.5125	3.1125	2.625	2.1	1.9375	1.2625	1	0.775
3C	4.2125	4.0625	3.9625	3.5	3.1	2.6125	2.0875	1.925	1.25	0.9875	0.7625
3B	4.2	4.05	3.95	3.4875	3.0875	2.6	2.075	1.9125	1.2375	0.975	0.75
3A	4.1875	4.0375	3.9375	3.475	3.075	2.5875	2.0625	1.9	1.225	0.9625	0.7375
39	4.175	4.025	3.925	3.4625	3.0625	2.575	2.05	1.8875	1.2125	0.95	0.725
38	4.1625	4.0125	3.9125	3.45	3.05	2.5625	2.0375	1.875	1.2	0.9375	0.7125
37	4.15	4	3.9	3.4375	3.0375	2.55	2.025	1.8625	1.1875	0.925	0.7
36	4.1375	3.9875	3.8875	3.425	3.025	2.5375	2.0125	1.85	1.175	0.9125	0.6875
35	4.125	3.975	3.875	3.4125	3.0125	2.525	2	1.8375	1.1625	0.9	0.675
34	4.1125	3.9625	3.8625	3.4	3	2.5125	1.9875	1.825	1.15	0.8875	0.6625
33	4.1	3.95	3.85	3.3875	2.9875	2.5	1.975	1.8125	1.1375	0.875	0.65
32	4.0875	3.9375	3.8375	3.375	2.975	2.4875	1.9625	1.8	1.125	0.8625	0.6375
31	4.075	3.925	3.825	3.3625	2.9625	2.475	1.95	1.7875	1.1125	0.85	0.625
30	4.0625	3.9125	3.8125	3.35	2.95	2.4625	1.9375	1.775	1.1	0.8375	0.6125
2F	4.05	3.9	3.8	3.3375	2.9375	2.45	1.925	1.7625	1.0875	0.825	0.6
2E	4.0375	3.8875	3.7875	3.325	2.925	2.4375	1.9125	1.75	1.075	0.8125	0.5875
2D	4.025	3.875	3.775	3.3125	2.9125	2.425	1.9	1.7375	1.0625	0.8	0.575
2C	4.0125	3.8625	3.7625	3.3	2.9	2.4125	1.8875	1.725	1.05	0.7875	0.5625
2B	4	3.85	3.75	3.2875	2.8875	2.4	1.875	1.7125	1.0375	0.775	0.55
2A	3.9875	3.8375	3.7375	3.275	2.875	2.3875	1.8625	1.7	1.025	0.7625	0.5375
29	3.975	3.825	3.725	3.2625	2.8625	2.375	1.85	1.6875	1.0125	0.75	0.525
28	3.9625	3.8125	3.7125	3.25	2.85	2.3625	1.8375	1.675	1	0.7375	0.5125
27	3.95	3.8	3.7	3.2375	2.8375	2.35	1.825	1.6625	0.9875	0.725	0.5
26	3.9375	3.7875	3.6875	3.225	2.825	2.3375	1.8125	1.65	0.975	0.7125	0.4875
25	3.925	3.775	3.675	3.2125	2.8125	2.325	1.8	1.6375	0.9625	0.7	0.475
24	3.9125	3.7625	3.6625	3.2	2.8	2.3125	1.7875	1.625	0.95	0.6875	0.4625
23	3.9	3.75	3.65	3.1875	2.7875	2.3	1.775	1.6125	0.9375	0.675	0.45
22	3.8875	3.7375	3.6375	3.175	2.775	2.2875	1.7625	1.6	0.925	0.6625	0.4375
21	3.875	3.725	3.625	3.1625	2.7625	2.275	1.75	1.5875	0.9125	0.65	0.425
20	3.8625	3.7125	3.6125	3.15	2.75	2.2625	1.7375	1.575	0.9	0.6375	0.4125
1F	3.85	3.7	3.6	3.1375	2.7375	2.25	1.725	1.5625	0.8875	0.625	0.4
1E	3.8375	3.6875	3.5875	3.125	2.725	2.2375	1.7125	1.55	0.875	0.6125	0.3875
1D	3.825	3.675	3.575	3.1125	2.7125	2.225	1.7	1.5375	0.8625	0.6	0.375
1C	3.8125	3.6625	3.5625	3.1	2.7	2.2125	1.6875	1.525	0.85	0.5875	0.3625
1B	3.8	3.65	3.55	3.0875	2.6875	2.2	1.675	1.5125	0.8375	0.575	0.35
1A	3.7875	3.6375	3.5375	3.075	2.675	2.1875	1.6625	1.5	0.825	0.5625	0.3375
19	3.775	3.625	3.525	3.0625	2.6625	2.175	1.65	1.4875	0.8125	0.55	0.325
18	3.7625	3.6125	3.5125	3.05	2.65	2.1625	1.6375	1.475	0.8	0.5375	0.3125
17	3.75	3.6	3.5	3.0375	2.6375	2.15	1.625	1.4625	0.7875	0.525	0.3
16	3.7375	3.5875	3.4875	3.025	2.625	2.1375	1.6125	1.45	0.775	0.5125	0.2875
15	3.725	3.575	3.475	3.0125	2.6125	2.125	1.6	1.4375	0.7625	0.5	0.275
14	3.7125	3.5625	3.4625	3	2.6	2.1125	1.5875	1.425	0.75	0.4875	0.2625
13	3.7	3.55	3.45	2.9875	2.5875	2.1	1.575	1.4125	0.7375	0.475	0.25
12	3.6875	3.5375	3.4375	2.975	2.575	2.0875	1.5625	1.4	0.725	0.4625	0.2375
11	3.675	3.525	3.425	2.9625	2.5625	2.075	1.55	1.3875	0.7125	0.45	0.225
10	3.6625	3.5125	3.4125	2.95	2.55	2.0625	1.5375	1.375	0.7	0.4375	0.2125
F	3.65	3.5	3.4	2.9375	2.5375	2.05	1.525	1.3625	0.6875	0.425	0.2
E	3.6375	3.4875	3.3875	2.925	2.525	2.0375	1.5125	1.35	0.675	0.4125	0.1875
D	3.625	3.475	3.375	2.9125	2.5125	2.025	1.5	1.3375	0.6625	0.4	0.175
C	3.6125	3.4625	3.3625	2.9	2.5	2.0125	1.4875	1.325	0.65	0.3875	0.1625
B	3.6	3.45	3.35	2.8875	2.4875	2	1.475	1.3125	0.6375	0.375	0.15
A	3.5875	3.4375	3.3375	2.875	2.475	1.9875	1.4625	1.3	0.625	0.3625	0.1375
9	3.575	3.425	3.325	2.8625	2.4625	1.975	1.45	1.2875	0.6125	0.35	0.125
8	3.5625	3.4125	3.3125	2.85	2.45	1.9625	1.4375	1.275	0.6	0.3375	0.1125
7	3.55	3.4	3.3	2.8375	2.4375	1.95	1.425	1.2625	0.5875	0.325	0.1
6	3.5375	3.3875	3.2875	2.825	2.425	1.9375	1.4125	1.25	0.575	0.3125	0.0875
5	3.525	3.375	3.275	2.8125	2.4125	1.925	1.4	1.2375	0.5625	0.3	0.075
4	3.5125	3.3625	3.2625	2.8	2.4	1.9125	1.3875	1.225	0.55	0.2875	0.0625
3	3.5	3.35	3.25	2.7875	2.3875	1.9	1.375	1.2125	0.5375	0.275	0.05
2	3.4875	3.3375	3.2375	2.775	2.375	1.8875	1.3625	1.2	0.525	0.2625	0.0375
1	3.475	3.325	3.225	2.7625	2.3625	1.875	1.35	1.1875	0.5125	0.25	0.025
0	3.4625	3.3125	3.2125	2.75	2.35	1.8625	1.3375	1.175	0.5	0.2375	0.0125

Note: (1) Blue marks are the default value. Unit : V.

PVN1~ PVN11 gamma voltage mapping

Register setting	PVN1	PVN2	PVN3	PVN4	PVN5	PVN6	PVN7	PVN8	PVN9	PVN10	PVN11
3F	-4.25	-4.1	-4	-3.5375	-3.1375	-2.65	-2.125	-1.9625	-1.2875	-1.025	-0.8
3E	-4.2375	-4.0875	-3.9875	-3.525	-3.125	-2.6375	-2.1125	-1.95	-1.275	-1.0125	-0.7875
3D	-4.225	-4.375	-3.975	-3.5125	-3.1125	-2.625	-2.1	-1.9375	-1.2625	-1	-0.775
3C	-4.2125	-4.0625	-3.9625	-3.5	-3.1	-2.6125	-2.0875	-1.925	-1.25	-0.9875	-0.7625
3B	-4.2	-4.35	-3.95	-3.4875	-3.0875	-2.6	-2.075	-1.9125	-1.2375	-0.975	-0.75
3A	-4.1875	-4.0375	-3.9375	-3.475	-3.075	-2.5875	-2.0625	-1.9	-1.225	-0.9625	-0.7375
39	-4.175	-4.325	-3.925	-3.4625	-3.0625	-2.575	-2.05	-1.8875	-1.2125	-0.95	-0.725
38	-4.1625	-4.0125	-3.9125	-3.45	-3.05	-2.5625	-2.0375	-1.875	-1.2	-0.9375	-0.7125
37	-4.15	-4.3	-3.9	-3.4375	-3.0375	-2.55	-2.025	-1.8625	-1.1875	-0.925	-0.7
36	-4.1375	-3.9875	-3.8875	-3.425	-3.025	-2.5375	-2.0125	-1.85	-1.175	-0.9125	-0.6875
35	-4.125	-4.275	-3.875	-3.4125	-3.0125	-2.525	-2	-1.8375	-1.1625	-0.9	-0.675
34	-4.1125	-3.9625	-3.8625	-3.4	-3	-2.5125	-1.9875	-1.825	-1.15	-0.8875	-0.6625
33	-4.1	-4.25	-3.85	-3.3875	-2.9875	-2.5	-1.975	-1.8125	-1.1375	-0.875	-0.65
32	-4.0875	-3.9375	-3.8375	-3.375	-2.975	-2.4875	-1.9625	-1.8	-1.125	-0.8625	-0.6375
31	-4.075	-4.225	-3.825	-3.3625	-2.9625	-2.475	-1.95	-1.7875	-1.1125	-0.85	-0.625
30	-4.0625	-3.9125	-3.8125	-3.35	-2.95	-2.4625	-1.9375	-1.775	-1.1	-0.8375	-0.6125
2F	-4.05	-4.2	-3.8	-3.3375	-2.9375	-2.45	-1.925	-1.7625	-1.0875	-0.825	-0.6
2E	-4.0375	-3.8875	-3.7875	-3.325	-2.925	-2.4375	-1.9125	-1.75	-1.075	-0.8125	-0.5875
2D	-4.025	-4.175	-3.775	-3.3125	-2.9125	-2.425	-1.9	-1.7375	-1.0625	-0.8	-0.575
2C	-4.0125	-3.8625	-3.7625	-3.3	-2.9	-2.4125	-1.8875	-1.725	-1.05	-0.7875	-0.5625
2B	-4	-4.15	-3.75	-3.2875	-2.8875	-2.4	-1.875	-1.7125	-1.0375	-0.775	-0.55
2A	-3.9875	-3.8375	-3.7375	-3.275	-2.875	-2.3875	-1.8625	-1.7	-1.025	-0.7625	-0.5375
29	-3.975	-4.125	-3.725	-3.2625	-2.8625	-2.375	-1.85	-1.6875	-1.0125	-0.75	-0.525
28	-3.9625	-3.8125	-3.7125	-3.25	-2.85	-2.3625	-1.8375	-1.675	-1	-0.7375	-0.5125
27	-3.95	-4.1	-3.7	-3.2375	-2.8375	-2.35	-1.825	-1.6625	-0.9875	-0.725	-0.5
26	-3.9375	-3.7875	-3.6875	-3.225	-2.825	-2.3375	-1.8125	-1.65	-0.975	-0.7125	-0.4875
25	-3.925	-4.075	-3.675	-3.2125	-2.8125	-2.325	-1.8	-1.6375	-0.9625	-0.7	-0.475
24	-3.9125	-3.7625	-3.6625	-3.2	-2.8	-2.3125	-1.7875	-1.625	-0.95	-0.6875	-0.4625
23	-3.9	-4.05	-3.65	-3.1875	-2.7875	-2.3	-1.775	-1.6125	-0.9375	-0.675	-0.45
22	-3.8875	-3.7375	-3.6375	-3.175	-2.775	-2.2875	-1.7625	-1.6	-0.925	-0.6625	-0.4375
21	-3.875	-4.025	-3.625	-3.1625	-2.7625	-2.275	-1.75	-1.5875	-0.9125	-0.65	-0.425
20	-3.8625	-3.7125	-3.6125	-3.15	-2.75	-2.2625	-1.7375	-1.575	-0.9	-0.6375	-0.4125
1F	-3.85	-4	-3.6	-3.1375	-2.7375	-2.25	-1.725	-1.5625	-0.8875	-0.625	-0.4
1E	-3.8375	-3.6875	-3.5875	-3.125	-2.725	-2.2375	-1.7125	-1.55	-0.875	-0.6125	-0.3875
1D	-3.825	-3.975	-3.575	-3.1125	-2.7125	-2.225	-1.7	-1.5375	-0.8625	-0.6	-0.375
1C	-3.8125	-3.6625	-3.5625	-3.1	-2.7	-2.2125	-1.6875	-1.525	-0.85	-0.5875	-0.3625
1B	-3.8	-3.95	-3.55	-3.0875	-2.6875	-2.2	-1.675	-1.5125	-0.8375	-0.575	-0.35
1A	-3.7875	-3.6375	-3.5375	-3.075	-2.675	-2.1875	-1.6625	-1.5	-0.825	-0.5625	-0.3375
19	-3.775	-3.925	-3.525	-3.0625	-2.6625	-2.175	-1.65	-1.4875	-0.8125	-0.55	-0.325
18	-3.7625	-3.6125	-3.5125	-3.05	-2.65	-2.1625	-1.6375	-1.475	-0.8	-0.5375	-0.3125
17	-3.75	-3.9	-3.5	-3.0375	-2.6375	-2.15	-1.625	-1.4625	-0.7875	-0.525	-0.3
16	-3.7375	-3.5875	-3.4875	-3.025	-2.625	-2.1375	-1.6125	-1.45	-0.775	-0.5125	-0.2875
15	-3.725	-3.875	-3.475	-3.0125	-2.6125	-2.125	-1.6	-1.4375	-0.7625	-0.5	-0.275
14	-3.7125	-3.5625	-3.4625	-3	-2.6	-2.1125	-1.5875	-1.425	-0.75	-0.4875	-0.2625
13	-3.7	-3.85	-3.45	-2.9875	-2.5875	-2.1	-1.575	-1.4125	-0.7375	-0.475	-0.25
12	-3.6875	-3.5375	-3.4375	-2.975	-2.575	-2.0875	-1.5625	-1.4	-0.725	-0.4625	-0.2375
11	-3.675	-3.825	-3.425	-2.9625	-2.5625	-2.075	-1.55	-1.3875	-0.7125	-0.45	-0.225
10	-3.6625	-3.5125	-3.4125	-2.95	-2.55	-2.0625	-1.5375	-1.375	-0.7	-0.4375	-0.2125
F	-3.65	-3.8	-3.4	-2.9375	-2.5375	-2.05	-1.525	-1.3625	-0.6875	-0.425	-0.2
E	-3.6375	-3.4875	-3.3875	-2.925	-2.525	-2.0375	-1.5125	-1.35	-0.675	-0.4125	-0.1875
D	-3.625	-3.775	-3.375	-2.9125	-2.5125	-2.025	-1.5	-1.3375	-0.6625	-0.4	-0.175
C	-3.6125	-3.4625	-3.3625	-2.9	-2.5	-2.0125	-1.4875	-1.325	-0.65	-0.3875	-0.1625
B	-3.6	-3.75	-3.35	-2.8875	-2.4875	-2	-1.475	-1.3125	-0.6375	-0.375	-0.15
A	-3.5875	-3.4375	-3.3375	-2.875	-2.475	-1.9875	-1.4625	-1.3	-0.625	-0.3625	-0.1375
9	-3.575	-3.725	-3.325	-2.8625	-2.4625	-1.975	-1.45	-1.2875	-0.6125	-0.35	-0.125
8	-3.5625	-3.4125	-3.3125	-2.85	-2.45	-1.9625	-1.4375	-1.275	-0.6	-0.3375	-0.1125
7	-3.55	-3.7	-3.3	-2.8375	-2.4375	-1.95	-1.425	-1.2625	-0.5875	-0.325	-0.1
6	-3.5375	-3.3875	-3.2875	-2.825	-2.425	-1.9375	-1.4125	-1.25	-0.575	-0.3125	-0.0875
5	-3.525	-3.675	-3.275	-2.8125	-2.4125	-1.925	-1.4	-1.2375	-0.5625	-0.3	-0.075
4	-3.5125	-3.3625	-3.2625	-2.8	-2.4	-1.9125	-1.3875	-1.225	-0.55	-0.2875	-0.0625
3	-3.5	-3.65	-3.25	-2.7875	-2.3875	-1.9	-1.375	-1.2125	-0.5375	-0.275	-0.05
2	-3.4875	-3.3375	-3.2375	-2.775	-2.375	-1.8875	-1.3625	-1.2	-0.525	-0.2625	-0.0375
1	-3.475	-3.625	-3.225	-2.7625	-2.3625	-1.875	-1.35	-1.1875	-0.5125	-0.25	-0.025
0	-3.4625	-3.3125	-3.2125	-2.75	-2.35	-1.8625	-1.3375	-1.175	-0.5	-0.2375	-0.0125

Note: (1) Blue marks are the default value. Unit : V.

- Address is 0xE1

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	NC	NC	VBP[1]	VBP[0]	VBN[1]	VBN[0]	V
Default	0	0	0	0	0	1	0	1	

Bit	Item	Description
[3:2]	VBP	GAMMAP bias current select. 00=80% 01=100% 10=120% 11=140%.
[1:0]	VBN	GAMMAN bias current select. 00=80% 01=100% 10=120% 11=140%.

- Address is 0xFA

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	X
Description	VENDER_ID								
Default	0	1	1	1	0	0	0	0	

- Address is 0xFB

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	NC	NC	NC	NC	NC	GRB	X
Description	GRB								
Default	0	0	0	0	0	0	0	1	

- Address is 0xFC

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	X
Description	PRODUCT ID1								
Default	1	0	0	0	0	0	1	0	

- Address is 0xFD

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	X
Description	PRODUCT ID2								
Default	0	1	1	0	0	0	0	0	

- Address is 0xFE

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	NC	NC	ID[3]	ID[2]	ID[1]	ID[0]	X
Description	PRODUCT ID3								
Default	0	0	0	0	1	0	0	1	

- Address is 0xFF

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	ID[7]	ID[6]	ID[5]	ID[4]	ID[3]	ID[2]	ID[1]	ID[0]	X
Description	VERSIONID								
Default	0	0	0	0	0	0	1	1	

9.2 Registers of Page1

- Address is 0xB1

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NA			OTP_GROUP[4:0]					X
Default	0	0	0	0	0	0	0	0	

Bit	Item	Description
[4:0]	OTP_GROUP[4:0]	OTP trimming group select. The group range is from group1 to group27.

- Address is 0xB2

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	OTP_PWD[7:0]								X
Default	0	1	0	1	1	0	1	0	

Bit	Item	Description
[7:0]	OTP_PWD[7:0]	OTP enter auto program mode.

- Address is 0xB3

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC		OTP_PTM[1:0]		NA	OTP_RE_LOAD	OTP_RD	OTP_WR	X
Default	0	0	0	0	0	0	0	0	

Bit	Item	Description
[5:4]	OTP_PTM[1:0]	OTP test mode.
2	OTP_RE_LOAD	OTP auto re-load control.
1	OTP_RD	OTP read control.
0	OTP_WR	OTP write control.

- Address is 0xB4

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NA							OTP_ADDR[8]	X
Default	0	0	0	0	0	0	0	0	

- Address is 0xB5

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	OTP_ADDR[7:0]								X
Default	0	0	0	0	0	0	0	0	

Bit	Item	Description
0	OTP_ADDR[8]	OTP address set.
[7:0]	OTP_ADDR[7:0]	

- Address is 0xB6

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	OTP_PDOB[7:0]								X
Default	0	0	0	0	0	0	0	0	

Bit	Item	Description
[7:0]	OTP_PDOB[7:0]	Read data from OTP.

- Address is 0xB7

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	OTP_PDIN[7:0]								X
Default	0	0	0	0	0	0	0	0	

Bit	Item	Description
[7:0]	OTP_PDIN[7:0]	Write data to OTP.

- Address is 0xB8

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	OTP_MANUAL[7:0]								X
Default	0	1	0	1	1	0	1	0	

Bit	Item	Description
[7:0]	OTP_MANUAL[7:0]	OTP enter manual program mode.

- Address is 0xB9

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NA		DISABLE_OTP[1:0]		POR	PPROG	VPS	PWE	X
Default	0	0	0	0	0	0	0	0	

Bit	Item	Description
0	PWE	OTP PWE control signal.
1	VPS	OTP VPS control signal.
2	PPROG	OTP PPROG control signal.
3	POR	OTP POR control signal.
5:4	DISABLE_OTP[1:0]	OTP function disables.

DISABLE_OTP	Master OTP function	Slave OTP function
00b	Enable	Enable
01b	Enable	Disable
10b	Disable	Enable
11b	Disable	Disable

9.3 Registers of Page2

Please refer application note

9.4 Registers of Page3

Please refer application note

9.5 Registers of Page4

- Address is 0xB1

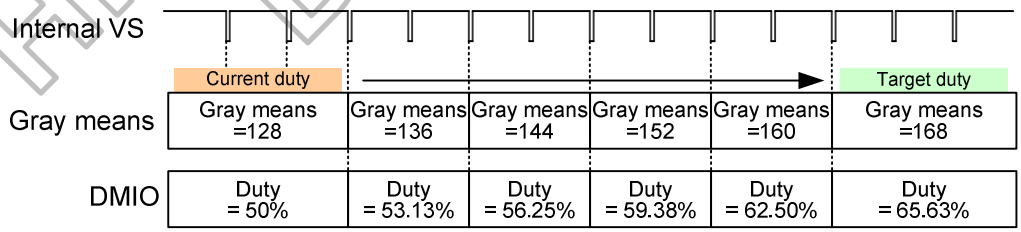
Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	DIM_EN	BL_EN	PWM_POL	NC	CABC_ AGING_EN	NC	V
Default	0	0	1	1	1	0	1	0	

Bit	Item	Description
1	CABC_AGING_EN	CABC aging enables. 0: Disable. 1: Enable.
3	PWM_POL	Poliarty of PWM control signal setting. 0: PWM output is non-inversion. 1: PWM output is inversion.
4	BL_EN	CABC back light control enables. 0: Disable. 1: Enable.
5	DIM_EN	CABC dimming enables. 0: Disable. 1: Enable.

- Address is 0xB2

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	NC	NC	DIM_STEP		DIM_FRME		V
Default	0	0	0	0	1	0	1	0	

Bit	Item	Description
[1:0]	DIM_FRME[1:0]	CABC dimimng cycle settling. 00b: 1 frame per step 01b: 2 frame per step. 10b: 3 frame per step. 11b: 4 frame per step.
[3:2]	DIM_STEP[1:0]	CABC dimming step setting. 00b: 2 steps. 01b: 4 steps. 10b: 8 steps. 11b: 16 steps.



Note: (1) DIM_FRME[1:0]=01, DIM_STEP[1:0]=10, Max duty is 100%, Min duty is 0%.

Figure 9.1: CABC dimming control

- Address is 0xB3

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	DUTY_UD								V
Default	1	1	1	1	1	1	1	1	

Bit	Item	Description
[7:0]	DUTY_UD[7:0]	Set user-defined PWM duty on CABC bypass mode. The CABC bypass mode is setting at 0xB6[3:2] of page0.

- Address is 0xB4

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	CABC_MB								V
Default	0	0	0	1	0	0	0	0	

Bit	Item	Description
[7:0]	CABC_MB[7:0]	Set PWM minimum duty.

- Address is 0xB5

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	PWM_PRD								V
Default	0	0	0	1	0	0	0	0	

Bit	Item	Description
[7:0]	PWM_PRD[7:0]	CABC PWM period setting.

- Address is 0xB6

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	NC	NC	NC	NC	PWM_DIV			V
Default	0	0	0	0	0	0	1	0	

Bit	Item	Description
[2:0]	PWM_DIV[2:0]	CABC PWM period divider.

PWM_DIV[2]	PWM_DIV[1]	PWM_DIV[0]	CABC PWM period divider
0	0	0	DIV 1
0	0	1	DIV 2
0	1	0	DIV 4
0	1	1	DIV 8
1	0	0	DIV 16
1	0	1	DIV 32
1	1	0	DIV 64
1	1	1	DIV 128

- Address is 0xB8

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	MAX_DUTY[7:0]								V
Default	1	1	1	1	1	1	1	1	

Bit	Item	Description
[7:0]	MAX_DUTY	Set PWM maximum duty.

9.6 Registers of Page6

- Address is 0xB0

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	EoTp_EN	CRCEN	CRCErr_FilterOut	VC4FRAME	VC_S[1]	VC_S[0]	VC_m[1]	VC_m[0]	V
Default	1	1	1	0	0	0	0	0	

Bit	Item	Description
[7]	EoTp_EN	Process of EoT packet enable. 1: Enable. 0: Disable.
[6]	CRCEN	CRC check enable. 1: Enable. 0: Disable.
[5]	CRCErr_FilterOut	Filter-out by CRC check result enable. 1: Enable. 0: Disable.
[4]	VC4FRAME	RX virtual channel filtering mode. 1: Enable. 0: Disable.
[3:2]	VC_S	virtual channel ID setting of slave **(for LP/HS rx)**.
[1:0]	VC_m	virtual channel ID setting of master **(for LP tx)**.

- Address is 0xB3

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	RT3[2]	RT3[1]	RT3[0]	NC	RT2[2]	RT2[1]	RT2[0]	V
Default	0	1	0	1	0	1	0	1	

Bit	Item	Description
[6:4]	RT3	Lane3 termination resistance control.
[2:0]	RT2	Lane2 termination resistance control.

RT3[2:0]	Ohm Ω
111	81
110	90
101	102
100	118
011	128
010	153
001	192
000	255

RT2[2:0]	Ohm Ω
111	81
110	90
101	102
100	118
011	128
010	153
001	192
000	255

- Address is 0xB4

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	NC	RT1[2]	RT1[1]	RT1[0]	NC	RT0[2]	RT0[1]	RT0[0]	V
Default	0	1	0	1	0	1	0	1	

Bit	Item	Description
[6:4]	RT1	Lane1 termination resistance control.
[2:0]	RT0	Lane0 termination resistance control.

RT3[2:0] / RT2[2:0]	Ohm Ω
111	81
110	90
101	102
100	118
011	128
010	153
001	192
000	255

- Address is 0xB5

Bit #	B7	B6	B5	B4	B3	B2	B1	B0	OTP
Name	TurnDisable	NC	NC	NC	NC	RTC[2]	RTC[1]	RTC[0]	V
Default	0	0	0	0	0	1	0	1	

Bit	Item	Description
7	TurnDisable	BTA→TX procedure function enable. 1: Enable. 0: Disable.
[2:0]	RT0	Clock Lane termination resistance control.

RTC[2:0]	Ohm Ω
111	81
110	90
101	102
100	118
011	128
010	153
001	192
000	255

10. Function Description

10.1 BIST pattern

When register BIST_EN is trigger to high, then HX8260-A will leave normal operation mode and starts to generate the BIST pattern to LCD panel without MIPI input signals.

The BIST pattern is illustrated as below figure.

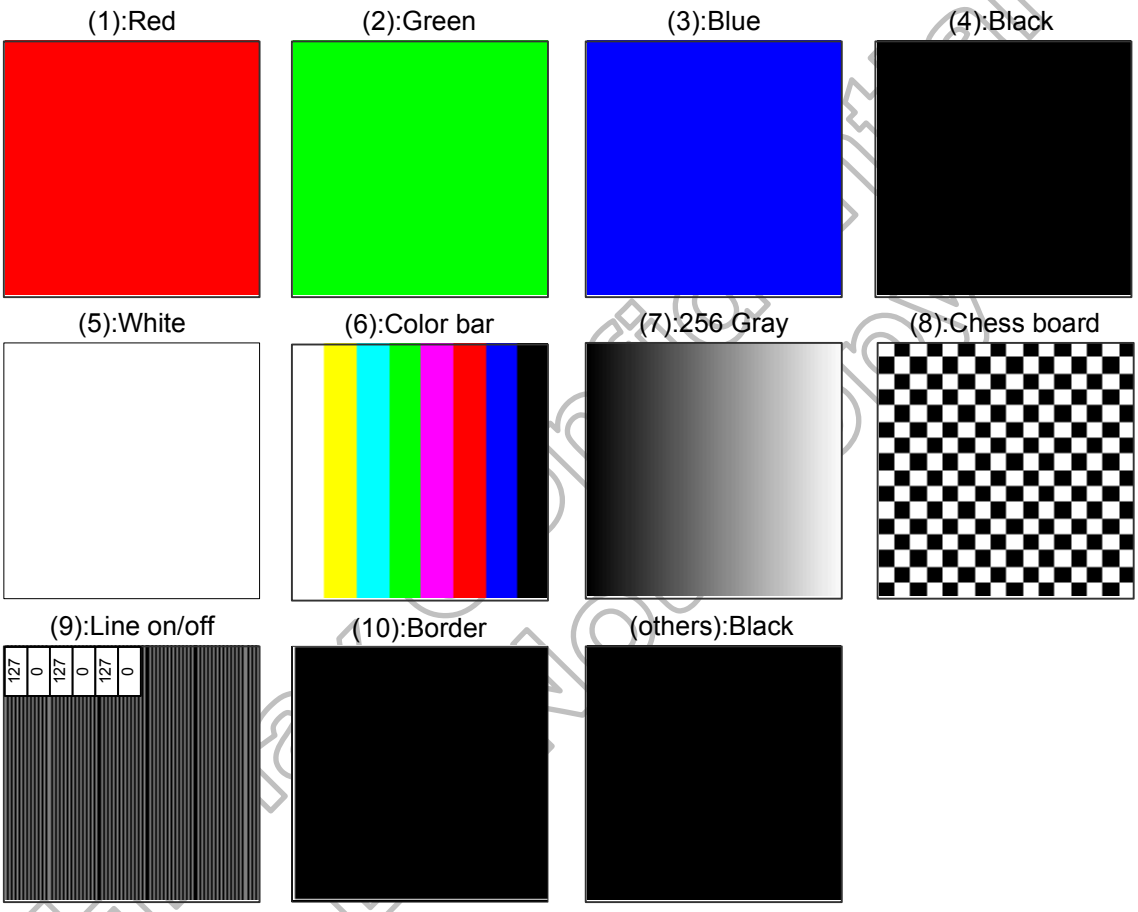


Figure 10.1: Bist pattern loop

10.2 CABC Function

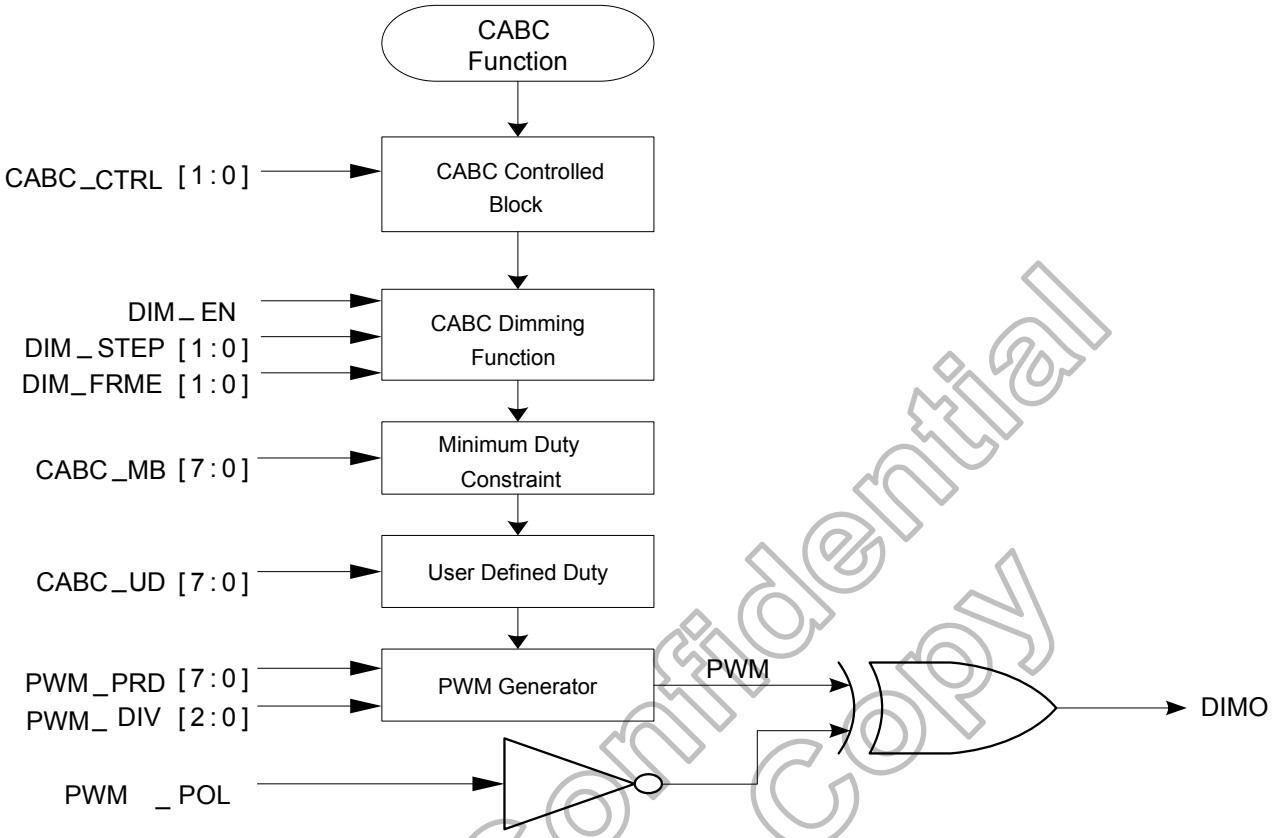


Figure 10.2: CABC flow chart

CABC controlled register:

- CABC_EN: CABC enable/ disable switch
- CABC_CTRL[1:0]: UI / Still / Moving / Bypass mode selection
- CABC_MB[7:0]: Minimum PWM duty constraint
- DUTY_UD[7:0]: Fixed PWM duty by user-defined when operating on Bypass mode
- PWM_POL: PWM duty polarity selection
- BL_EN: back-light On/ Off switch
- DIM_EN: Dimming function enable/ disable switch
- Dimming time selection : DIM_STEP[1:0] / DIM_FRME[1:0]
  - Total dimming time = DIM_STEP[1:0] × DIM_FRME[1:0]
- PWM duty frequency selection : PWM_PRD[7:0] / PWM_DIV[2:0]
  - PWM output period = CLK period × 256 × (PWM_PRD[7:0]) / (PWM_DIV[2:0] + 1)

10.3 OTP function

10.3.1 OTP flow of programming and read

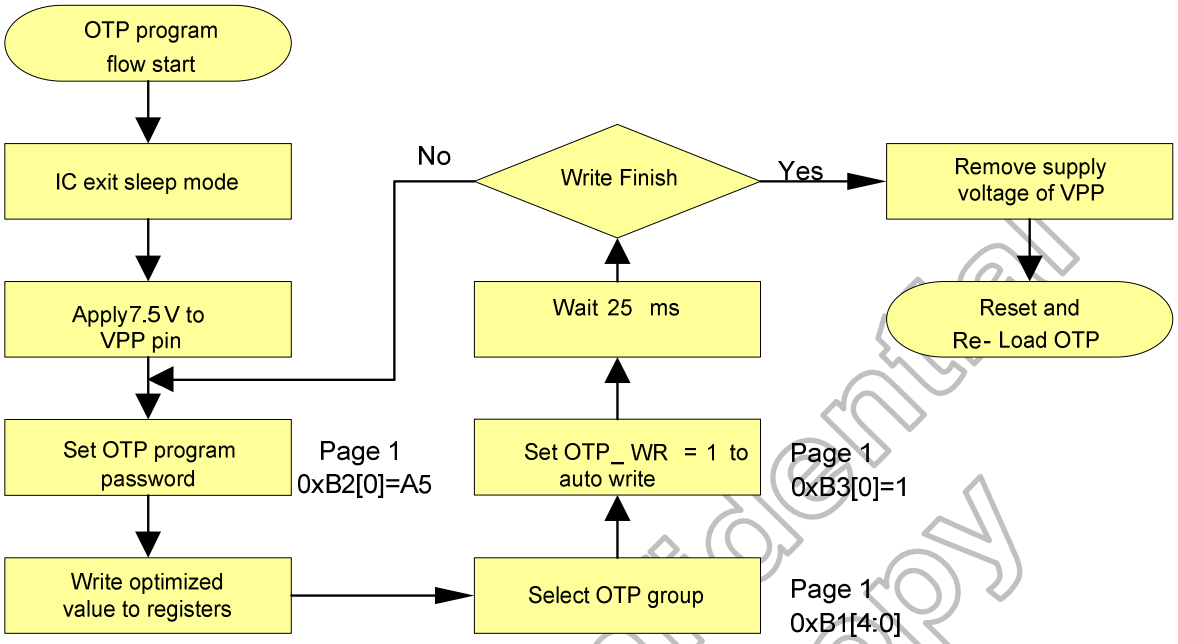


Figure 10.3: OTP program flow

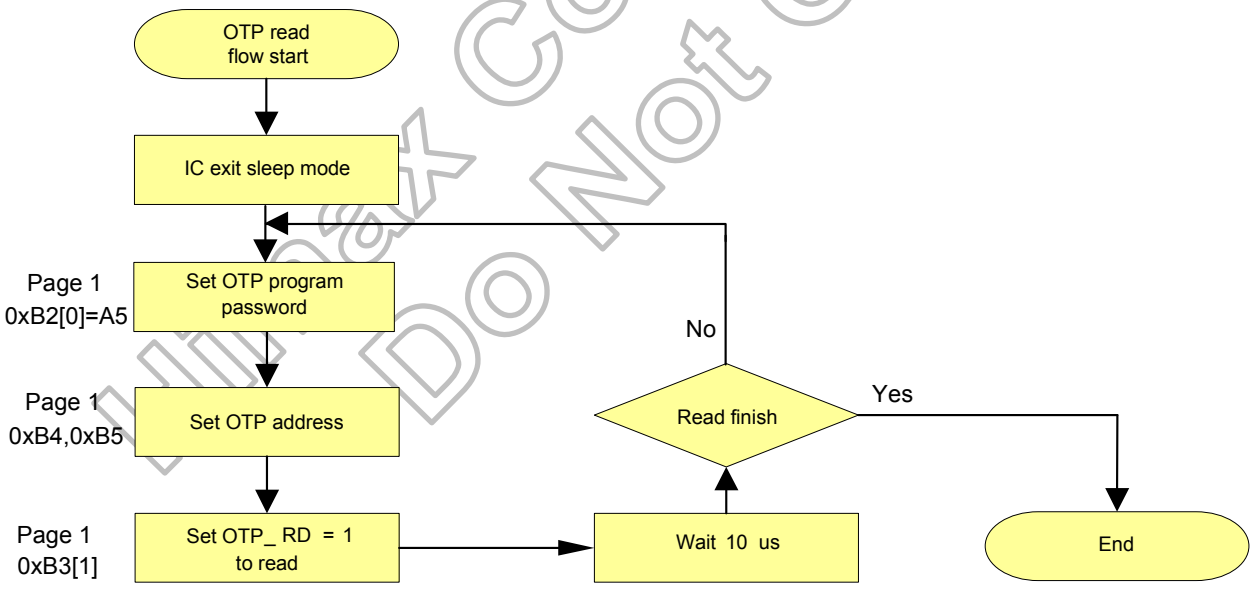


Figure 10.4: OTP read flow

10.3.2 OTP table

OTP address[7:0]	B7	B6	B5	B4	B3	B2	B1	B0	Group
2	W1								GROUP0
3	T_VCOMS[7:0]								
4	W2								
5	T_VCOMS[7:0]								
6	W3								
7	T_VCOMS[7:0]								

OTP address[7:0]	B7	B6	B5	B4	B3	B2	B1	B0	Group
8	W1	STB	UPDNB	LR	ZIGZAG_SEL	DISP_ON	NBW_SEL	BIST	Group 1
9	ZTYPE_SEL		PWRMD		VRES_FIX	RES			
10	VRES								
11	ZDATA								
12	LNSW		PNSW	HFRC_INV	CABC_CTRL		DITHER_EN	HFRC_EN	
13	PCLK_SEL	RX_DINT	RX_VB			LVDS_VB		LVDS_FMT	
14		LVDS_TD				LVDS_TC			
15			LVDS_BW			LVDS_CPB			
16	BLREV		BLREVONOFF		SD_ISSEL		INV_SEL		
17	BC_CTRL	GOA_EN	RB_SWAP	DPFM_OSC_SEL		LNSEL			
18	GAS_GOA_EN	VRES_BLACK	GCHL_Blanking	spi_tmp03c[4:0]					
19	VSPS				VSNS				
20			VGHS						
21			VGLS						
22									
23	VSPON				VSPOFF				
24	VSNON				VSNOFF				
25		VGLXSP	VGHXSP		PFMFREN	T_OFFSET			
26				VPHS					
27	CGPP_INV		SOFT_EN	CLK_SEL			CMD_SEL		
28				VNHS					
29			VCL_CPCTL		VGL_CPCTL		VGH_CPCTL		
30	POCSD_CTL			EQ0W					
31				EQ1W					
32				EQ2W					

OTP address[7:0]	B7	B6	B5	B4	B3	B2	B1	B0	Group
33	W1		PVP1						Group 2
34			PVP2						
35			PVP3						
36			PVP4						
37			PVP5						
38			PVP6						
39			PVP7						
40			PVP8						
41			PVP9						
42			PVP10						
43			PVP11						
44	W1		PVN1						Group 3
45			PVN2						
46			PVN3						
47			PVN4						
48			PVN5						
49			PVN6						
50			PVN7						
51			PVN8						
52			PVN9						
53			PVN10						
54			PVN11						
55					VBP			VBN	
56				T_OSCT[4:0]					
57									
58									
59			BIST_VFP			BIST_VBP			
60								MENU_EN	

OTP address[7:0]	B7	B6	B5	B4	B3	B2	B1	B0	Group
61	W1								Group 4
62	GOUTL1_STBYB_MOD		GOUTL_1_SEL[5:0]						
63	GOUTL2_STBYB_MOD		GOUTL_2_SEL[5:0]						
64	GOUTL3_STBYB_MOD		GOUTL_3_SEL[5:0]						
65	GOUTL4_STBYB_MOD		GOUTL_4_SEL[5:0]						
66	GOUTL5_STBYB_MOD		GOUTL_5_SEL[5:0]						
67	GOUTL6_STBYB_MOD		GOUTL_6_SEL[5:0]						
68	GOUTL7_STBYB_MOD		GOUTL_7_SEL[5:0]						
69	GOUTL8_STBYB_MOD		GOUTL_8_SEL[5:0]						
70	GOUTL9_STBYB_MOD		GOUTL_9_SEL[5:0]						
71	GOUTL10_STBYB_MOD		GOUTL_10_SEL[5:0]						
72	GOUTL11_STBYB_MOD		GOUTL_11_SEL[5:0]						
73	GOUTL12_STBYB_MOD		GOUTL_12_SEL[5:0]						
74	GOUTL13_STBYB_MOD		GOUTL_13_SEL[5:0]						
75	GOUTL14_STBYB_MOD		GOUTL_14_SEL[5:0]						
76	GOUTL15_STBYB_MOD		GOUTL_15_SEL[5:0]						
77	GOUTL16_STBYB_MOD		GOUTL_16_SEL[5:0]						
78	GOUTL17_STBYB_MOD		GOUTL_17_SEL[5:0]						
79	GOUTL18_STBYB_MOD		GOUTL_18_SEL[5:0]						
80	GOUTL19_STBYB_MOD		GOUTL_19_SEL[5:0]						
81	GOUTL20_STBYB_MOD		GOUTL_20_SEL[5:0]						
82	GOUTL21_STBYB_MOD		GOUTL_21_SEL[5:0]						
83	GOUTL22_STBYB_MOD		GOUTL_22_SEL[5:0]						
84	GOUTR1_STBYB_MOD		GOUTR_1_SEL[5:0]						
85	GOUTR2_STBYB_MOD		GOUTR_2_SEL[5:0]						
86	GOUTR3_STBYB_MOD		GOUTR_3_SEL[5:0]						
87	GOUTR4_STBYB_MOD		GOUTR_4_SEL[5:0]						
88	GOUTR5_STBYB_MOD		GOUTR_5_SEL[5:0]						
89	GOUTR6_STBYB_MOD		GOUTR_6_SEL[5:0]						
90	GOUTR7_STBYB_MOD		GOUTR_7_SEL[5:0]						
91	GOUTR8_STBYB_MOD		GOUTR_8_SEL[5:0]						
92	GOUTR9_STBYB_MOD		GOUTR_9_SEL[5:0]						
93	GOUTR10_STBYB_MOD		GOUTR_10_SEL[5:0]						
94	GOUTR11_STBYB_MOD		GOUTR_11_SEL[5:0]						
95	GOUTR12_STBYB_MOD		GOUTR_12_SEL[5:0]						
96	GOUTR13_STBYB_MOD		GOUTR_13_SEL[5:0]						
97	GOUTR14_STBYB_MOD		GOUTR_14_SEL[5:0]						
98	GOUTR15_STBYB_MOD		GOUTR_15_SEL[5:0]						
99	GOUTR16_STBYB_MOD		GOUTR_16_SEL[5:0]						
100	GOUTR17_STBYB_MOD		GOUTR_17_SEL[5:0]						
101	GOUTR18_STBYB_MOD		GOUTR_18_SEL[5:0]						
102	GOUTR19_STBYB_MOD		GOUTR_19_SEL[5:0]						
103	GOUTR20_STBYB_MOD		GOUTR_20_SEL[5:0]						
104	GOUTR21_STBYB_MOD		GOUTR_21_SEL[5:0]						
105	GOUTR22_STBYB_MOD		GOUTR_22_SEL[5:0]						
106	VGL_GAS	GOA_VGOFF_EN	GOA_PWROFF	GOA_HZ_EN					

OTP address[7:0]	B7	B6	B5	B4	B3	B2	B1	B0	Group
107	W1		DAC_EN	SLC_DMY_CLK_EN	CPV_EN	CPV_4P_EN	AUO_EN	AUO_DC_4P_EN	Group 5
108		SYNC_POL	UD_POL	CLKV_BLANKON		CKV_PHASE			
109									
110	STV_DELAY		FACTOR		HS_NUM				
111	CLR_PREC_CNT		FLC_PREC_CNT		STV_PREC_CNT				
112	DL								
113	T0								
114	T1								
115	T2								
116	T3								
117	T4								
118	T5								
119	T2B								
120	T3B								
121	T6								
122	T7								
123	T6B								
124	T7B								
125					STV_WD				
126				STV_LEAD					
127					CKV_WD				
128				CKV_LEAD					
129			CKV_DUMY						
130	CKV_PRC_CNT								
131	GNO								
132	FLC								
133		FLCA_LEAD							
134						FLC_BLANKON_SEL	FLC_NON-OVERLAP		
135	BLANK_START								
136	BLANK_WD								
137			CLR_DL		CLR1_LEAD	CLR2_LEAD	CLR3_LEAD	CLR4_LEAD	
138	spi_goa_reserve50				CLR1234_FP_SEL	CLR1234_WD[10:8]			
139	CLR1_WD								
140	CLR234_WD								
141	CLR1_POL	CLR1_START							
142	CLR2_POL	CLR2_START							
143	CLR3_POL	CLR3_START							
144	CLR4_POL	CLR4_START							
145	CLR234_START_MSB				CLR1_START_MSB				
146		MASKSTART[6:0]							
147	MARK_LEAD			DL_FACTOR	MARK_CKV5	MARK_CKV7	MARK_CKV9	MARK_CKVA	
148									
149									
150	CKV_PREC_CNT2								
151	CLR1_SEL				CLR2_SEL				
152									

OTP address[7:0]	B7	B6	B5	B4	B3	B2	B1	B0	Group
153	W1		DIM_EN	BL_EN	PWM_POL		CABC_AGAIN		Group 6
154					DIM_STEP		DIM_FM		
155	DUTY_UD[7:0]								
156	CABC_MB[7:0]								
157	PWM_PRD								
158						PWM_DIV[2:0]			
159									
160	MAX_DUTY[7:0]								
176	W1								Group 8
177	EoTp_EN	CRCEN	CRCErr_FilterOut	VC4FRAME	VC_S		VC_m		
178	PCLK_Refine_Auto	PCLK_Manual_On		PCLK_Manual_Freq					
179									
180									
181		RT3[2:0]				RT2[2:0]			
182		RT1[2:0]				RT0[2:0]			
183	TurnDisable					RTC[2:0]			

10.4 No signal detect function

HX8260-A keeps detect input signals **(HS, VS)** for MIPI mode input and DCLK for LVDS mode input. If deticting of signals is missing, HX8260-A will enter no signal mode.

No signal mode:
A. All GOA signals will keep running.
B. Keep PFM and charge pump running.
C. Panel display will show black pattern.

10.5 GAS function

When power is removed from an electronic device during display, the image still keeps on the LCD panel for a long time. GAS function can speed the process that image disappears.

The GAS function is a voltage detector. By GAS circuit, HX8260 can detect low voltage of power and send control signal to discharge residual potential in LCD panel and remove image.

In any one of the following case, the chip will entry GAS function.
A. VCI is lower than 2V **(Case 1)**
B. VSP is lower than 3V **(Case 2)**

GAS function:
A. Source output pull to VSSA.
B. All GOA signals will be set to gas mode **(setting by register)**.
C. Stop PFM and charge pump function.
D. VCOM output pull to VSSA.

The GAS function has debounce protection circuit. EX: If the duration of voltage drop on VCI is less than 20us **(Ex: induced by ESD pulse)**, the GAS function will not be active even the VCI voltage level is less than 2V.

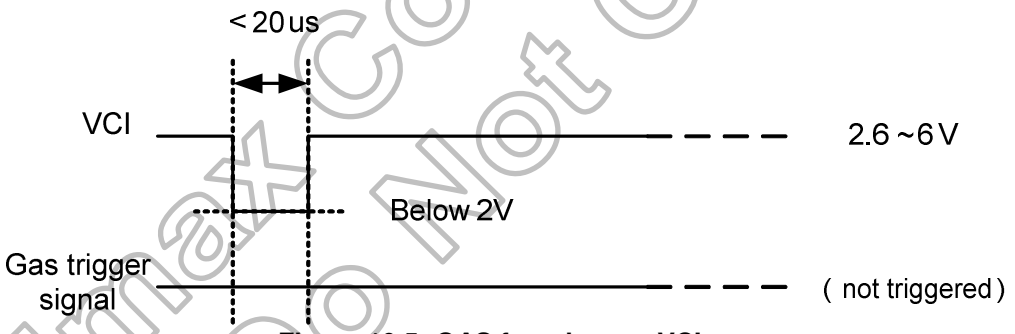


Figure 10.5: GAS function vs. VCI

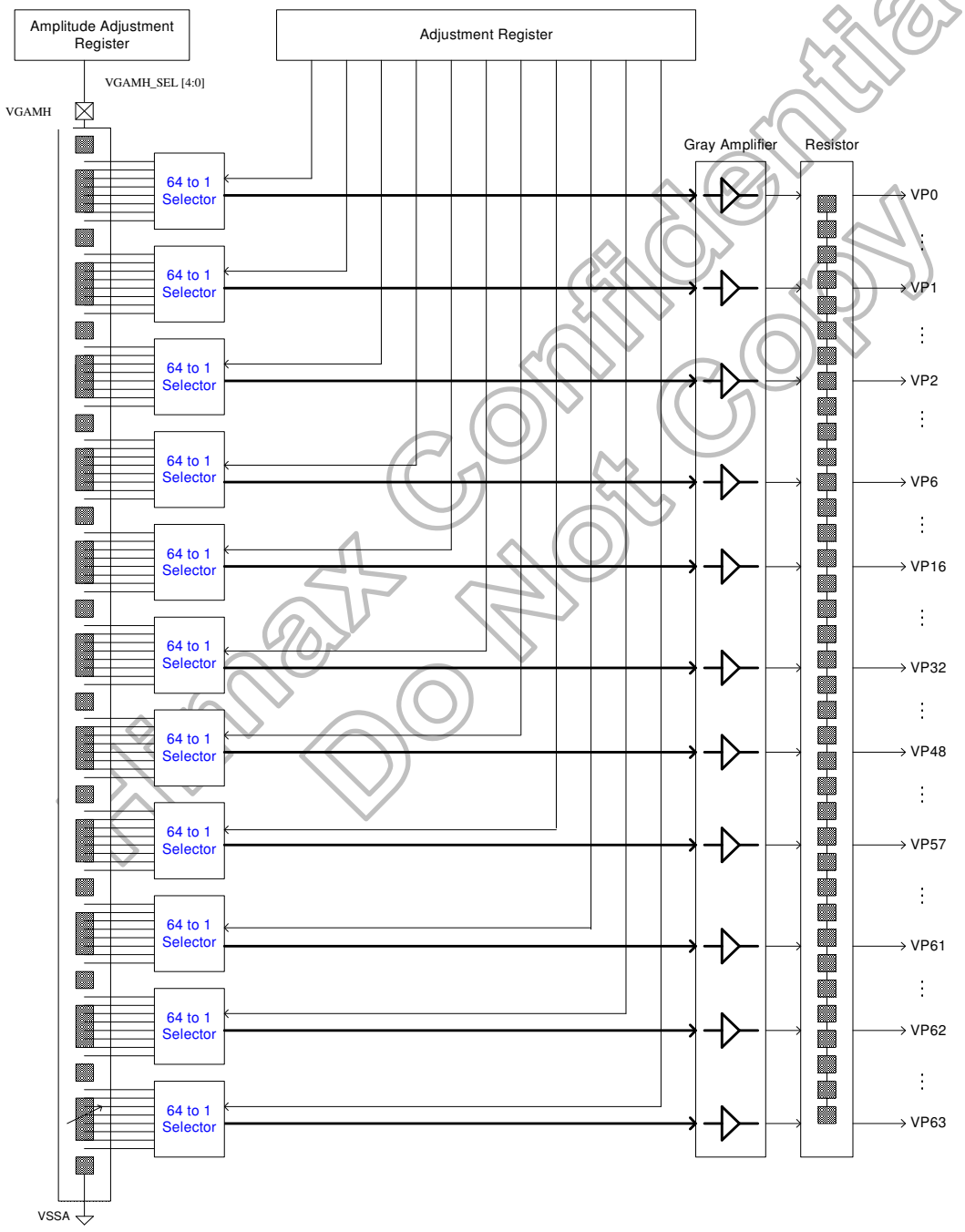
11. Gamma Adjustment Function

HX8260-A supports 11gamma correction reference point:

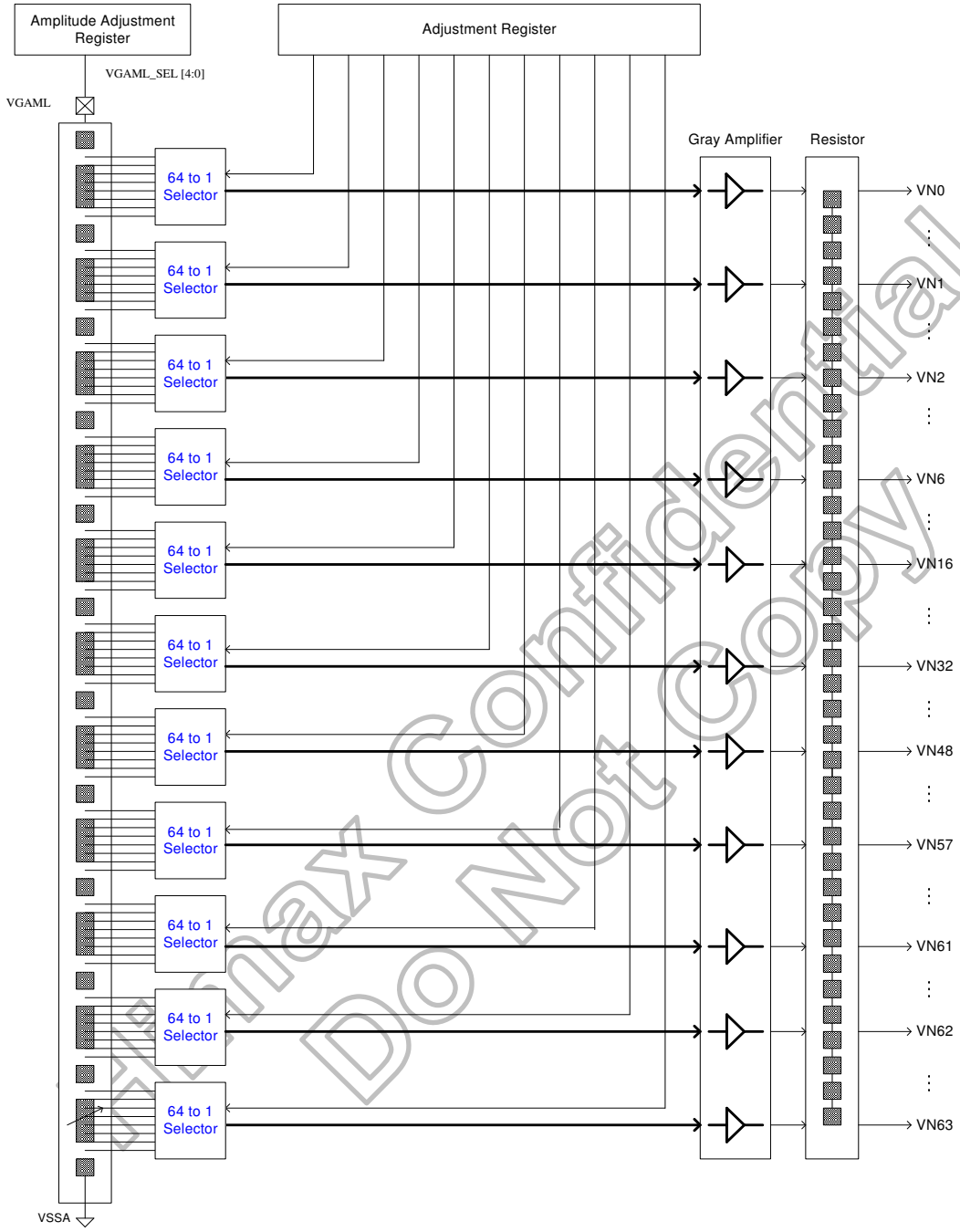
VP0/VP2/VP6/VP16/VP32/VP48/VP57/VP61/VP62/VP63 are generated within driver IC and adjustable by register setting.

11.1 Gamma architecture

11.1.1 Positive gamma



11.1.2 Negative gamma



11.2 Gamma resistor table

Positive gamma resistor (Ω)	
RV0	1050
RV1	826
RV2	525
RV3	217
RV4	126
RV5	378
RV6	462
RV7	315
RV8	266
RV9	336
RV10	161
RV11	161
RV12	161
RV13	140
RV14	140
RV15	140
RV16	140
RV17	140
RV18	140
RV19	133
RV20	105
RV21	105
RV22	105
RV23	105
RV24	105
RV25	98
RV26	98
RV27	98
RV28	98
RV29	126
RV30	105
RV31	112
RV32	91
RV33	91
RV34	91
RV35	105
RV36	77
RV37	84
RV38	91
RV39	112
RV40	91
RV41	91
RV42	91
RV43	91
RV44	105
RV45	105
RV46	105
RV47	105
RV48	105
RV49	154
RV50	189
RV51	189
RV52	196
RV53	210
RV54	210
RV55	224
RV56	280
RV57	294
RV58	343
RV59	539
RV60	525
RV61	406
RV62	476

Negative gamma resistor (Ω)	
RV0	1050
RV1	826
RV2	525
RV3	217
RV4	126
RV5	378
RV6	462
RV7	315
RV8	266
RV9	336
RV10	161
RV11	161
RV12	161
RV13	140
RV14	140
RV15	140
RV16	140
RV17	140
RV18	140
RV19	133
RV20	105
RV21	105
RV22	105
RV23	105
RV24	105
RV25	98
RV26	98
RV27	98
RV28	98
RV29	126
RV30	105
RV31	112
RV32	91
RV33	91
RV34	91
RV35	105
RV36	77
RV37	84
RV38	91
RV39	112
RV40	91
RV41	91
RV42	91
RV43	91
RV44	105
RV45	105
RV46	105
RV47	105
RV48	105
RV49	154
RV50	189
RV51	189
RV52	196
RV53	210
RV54	210
RV55	224
RV56	280
RV57	294
RV58	343
RV59	539
RV60	525
RV61	406
RV62	476

Table 11.1: Gamma resistor table

12. DC Characteristics

12.1 Absolute maximum ratings

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
I/O voltage	VDDI_RX VDDI_D	-0.3	-	3.96	V
Power input	VCI	-0.3	-	6.5	V
VSP voltage	VSP	-0.3	-	6.5	V
VSN voltage	VSN	-6.5	-	0.3	V
VPP **(OTP power)**	VPP	-0.3	-	8.64	V
Operating temperature(1)	Topr	-20	-	+85	℃
Storage temperature(1)	Tstg	-55	-	125	℃

Note: (1) Do not let condensation for low temperature.

12.2 Typical operating condition

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
IOVCC voltage	VDDI_RX VDDI_D	1.7	1.8	1.9	V
Power input	VCI	2.6	3.3	6	V
VSP voltage	VSP	4.5	-	6	V
VSN voltage	VSN	-6	-	-4.5	V
VPP **(OTP power)**	VPP	7.4	7.6	7.8	V

12.3 DC electrical characteristics

(Test condition: VCI=1.6~3.6V, T_A=-20℃~+85℃,VSS=VSSA=0V)

Parameter		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
VDDI_D Input high level voltage1		VIH1	0.8 x VDDI_D	-	VDDI_D	V
VDDI_D input low level voltage1		VIL1	VSS	-	0.2 x VDDI_D	V
Input Leakage Current		IL1	(-1)	-	(+1)	μA
VGLO2 output voltage		VGLO2	-15	-	-5	V
VGMAH output voltage		VGMAH	4	-	5.5	V
VGMAL output voltage		VGMAL	-5.5	-	-4	V
VCI_REG output voltage		VCI_REG	2.1	-	3.0	V
VGL output voltage		VGL	-16	-	-6	V
VGH output voltage		VGH	8	-	19	V
VCL output voltage		VCL	-2.1	-2.4	-3.0	V
VOM output voltage		VOM	-2.75	-1.48	-0.2	V
Input terminal pull-high resistance		RPU	-	300	-	KΩ
Input terminal pull-low resistance		RPD	-	300	-	KΩ
Source output level deviation	Graycode= 0 ~ 14 Graycode= 241 ~ 255	Sdev1	40	-	-	mV
	Graycode= 15 ~ 31 Graycode= 208 ~ 240	Sdev2	30	-	-	mV
	Graycode= 32 ~ 207	Sdev3	25	-	-	mV
Source output offset deviation	Graycode= 0 ~ 14 Graycode= 241 ~ 255	Sdev4	40	-	-	mV
	Graycode= 15 ~ 31 Graycode= 208 ~ 240	Sdev5	30	-	-	mV
	Graycode= 32 ~ 207	Sdev6	25	-	-	mV
Current consumption	Normal mode(2)	Ivdd	-	17.6	-	mA
	Standby mode	Ivdd	-	1.1	-	mA
Rush current(1)		Ivddpeak	-	60	-	mA
VPP operation current		I_{VPP}	-	-	8	mA

Note: (1) IC internal only, excluded PFM circuit's peak current of VCI
(2) Condition: 800RGBx1280 white pattern

12.4 MIPI DC electrical characteristics

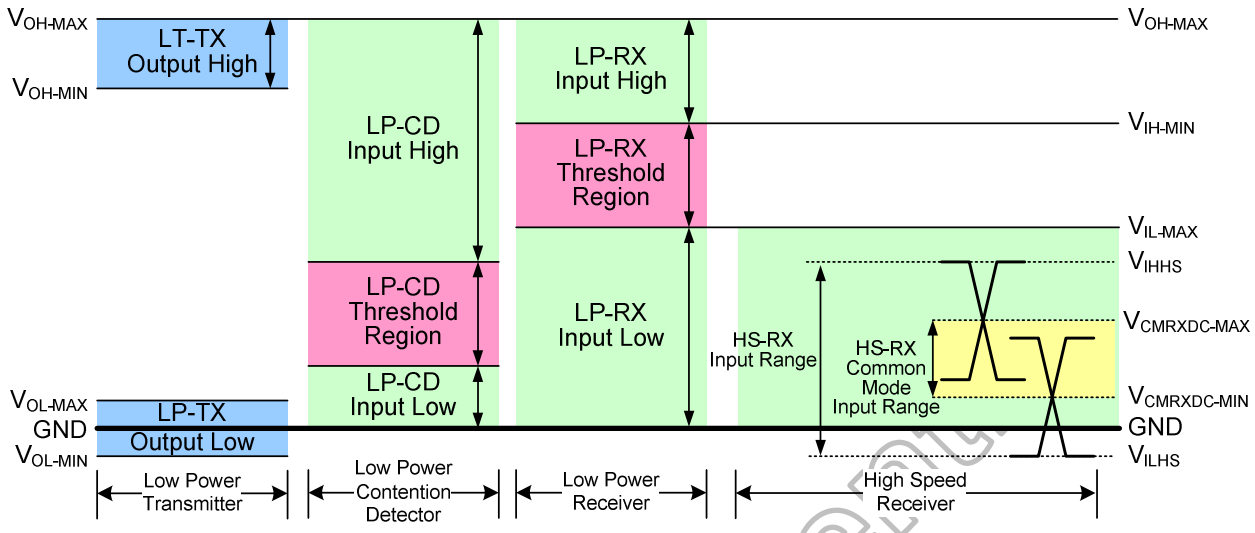


Figure 12.1: MIPI signaling and contention voltage levels

DC characteristics for MIPI LP mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Logic 1 input voltage	V_{IH}	880	-	-	mV
Logic 0 input voltage	V_{IL}	0	-	550	mV
Logic 1 output voltage	V_{OH}	1.1	1.2	1.3	V
Logic 0 output voltage	V_{OL}	-50	-	50	mV

DC characteristics for MIPI HS mode

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Common-mode voltage HS Receive mode	V_{CMRXDC}	70	-	330	mV
Differential input high threshold	V_{IDTH}	-	-	70	mV
Differential input low threshold	V_{IDTL}	70	-	-	mV
Single-ended input high voltage	V_{IHHS}	-	-	460	mV
Single-ended input low voltage	V_{ILHS}	-40	-	-	mV
Differential input impedance	Z_{ID}	80	100	125	Ω
HS transmit differential voltage **(VDP-VDN)**	|VOD|	140	200	270	mV

Note: (1) V_{IDTH} and V_{IDTL} only for reference, related to power and ground noise, this spec need to check on panel performance to fine tune

12.5 LVDS mode DC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Differential input high threshold voltage	R_{XVTH}	+0.1	-	-	V	R_{XVCM}=1.2V
Differential input low threshold voltage	R_{XVTL}	-	-	-0.1	V	
Input voltage range (**singled-end)**	R_{XVIN}	0	-	VDD-1.2+ $\|V_{ID}\|/2$	V	-
Differential input common Mode voltage	R_{XVCM}	$\|V_{ID}\|/2$	-	VDD-1.2	V	-
Differential input voltage	$\| V_{ID} \|$	0.2	-	0.6	V	-
Differential input leakage Current	RV_{Xliz}	-10	-	+10	µA	-
LVDS digital operating current	lddlvds	-	15	30	mA	Fclk=65MHz, VDD=3.3V
LVDS digital stand-by current	lstlvds	-	10	50	µA	Clock & all Functions are stopped

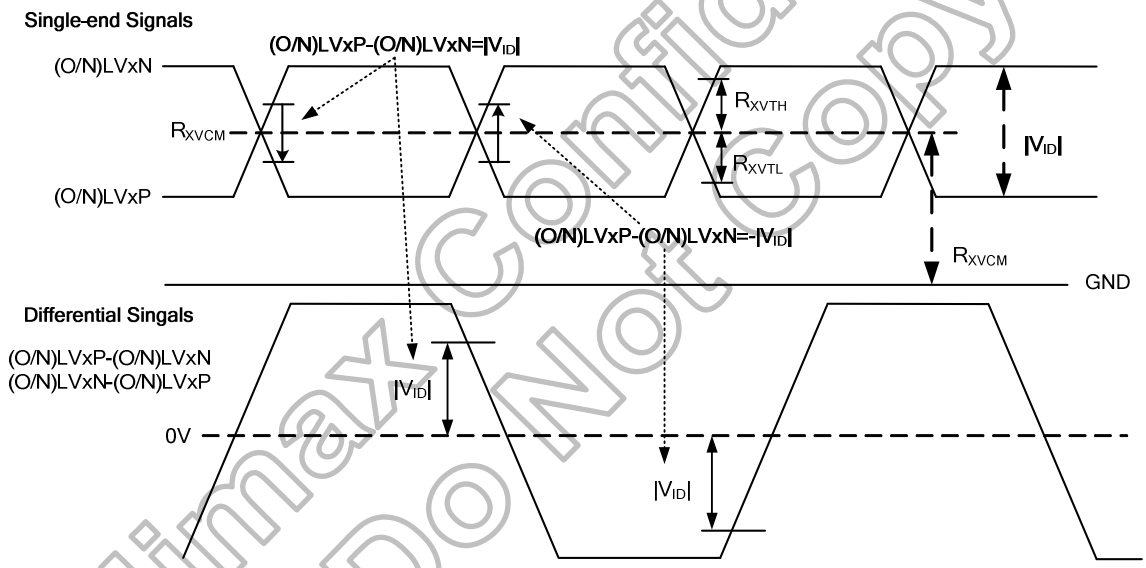


Figure 12.2: Single-end signals

13. AC Characteristics

13.1 MIPI AC characteristics

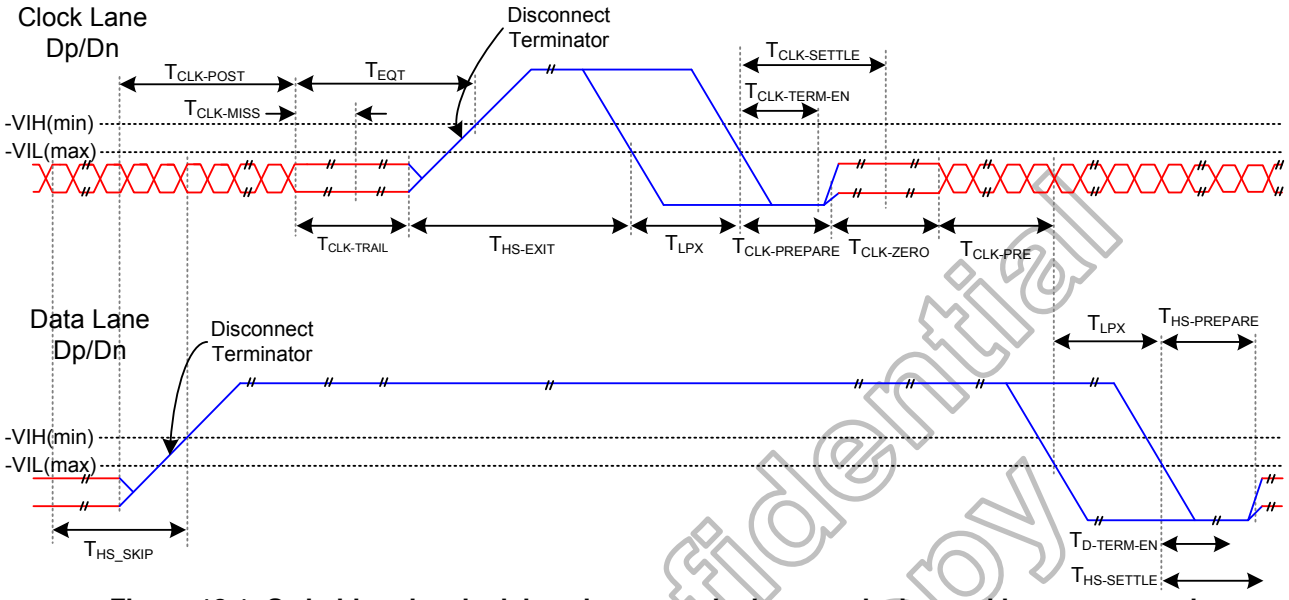


Figure 13.1: Switching the clock lane between clock transmission and low-power mode

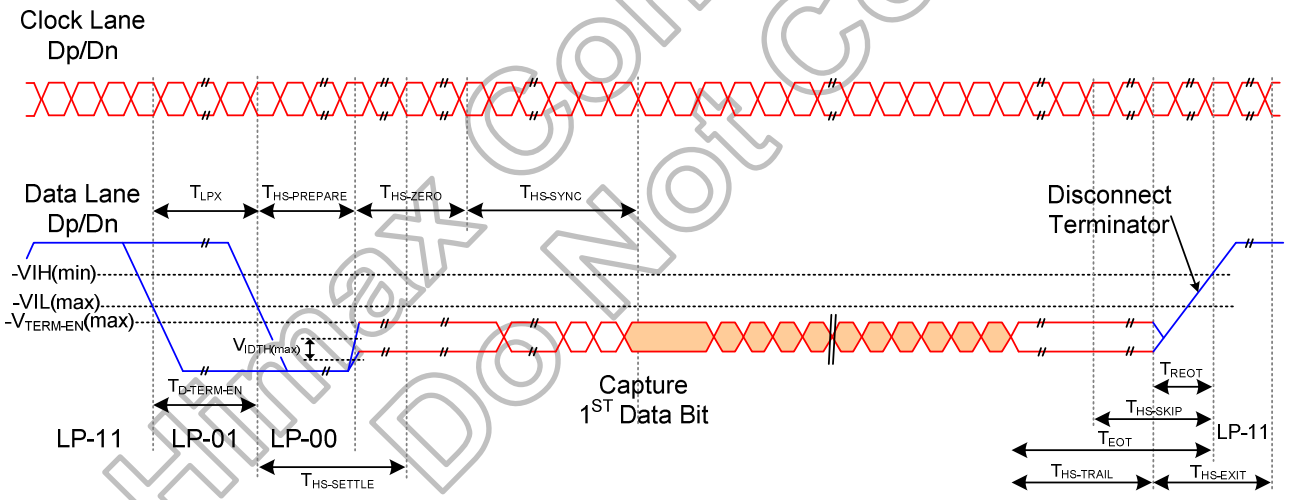


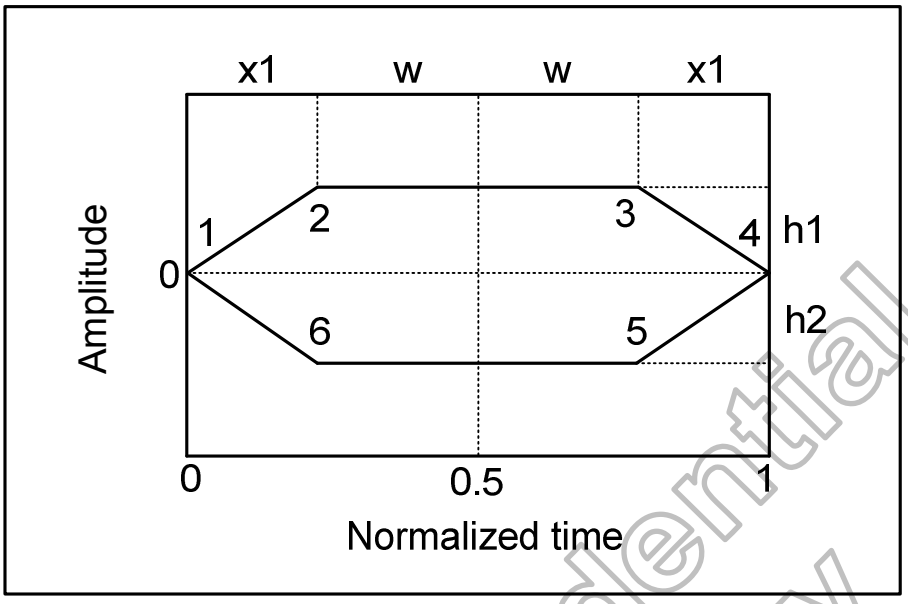
Figure 13.2: Timing of high-speed data transmission in bursts

MIPI AC Characteristics

Parameter	Description	Spec.			Unit
		Min	Typ	Max	
T_{REOT}	30%-85% rise time and fall time	-	-	35	ns
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.	-	-	60	ns
$T_{CLK-POST}$*1	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60 ns + 52*UI **(For DCS)**	-	-	ns
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8	-	-	ns
$T_{CLK-SETTLE}$	Time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of $T_{CLK-PRE}$.	95	-	300	ns
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HSPREPARE}$.	85 ns + 6*UI		145 ns + 10*UI	ns
T_{EOT}	Time from start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns+48*UI	-
$T_{HS-EXIT}$ (1)	time to drive LP-11 after HS burst	100	-	-	ns
$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40ns + 4*UI	-	85ns+6*UI	ns
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + Time to drive HS-0 before the Sync sequence	145ns + 10*UI	-	-	ns
$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns+4*UI	ns
$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60 + 4*UI	-	-	ns
T_{LPX}	Length of any Low-Power state period	50	-	-	ns
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPS(SLAVE)}$ between Master and Slave side	2/3	-	3/2	-
T_{TA-GET}	Time to drive LP-00 by new TX	$5*T_{LPX}$			ns
T_{TA-GO}	Time to drive LP-00 after Turnaround Request	$4*T_{LPX}$			ns
$T_{TA-SURE}$	Time-out before new TX side starts driving	T_{LPX}	-	$2*T_{LPX}$	ns

Note: (1) For image transmission:
$T_{CLK-POST}$ min value =164 when MIPI max frequency per lane = 0.53Gbps.
$T_{CLK-POST}$ min value =112 when MIPI max frequency per lane = 1Gbps

13.2 MIPI data-clock timing specification



Symbol	Time (UI)	Voltage
1	0	0
2	0.2	+70mV **(Min.)**
3	0.8	+70mV **(Min.)**
4	1	0
5	0.8	-70mV **(Min.)**
6	0.2	-70mV **(Min.)**
x1	0.2	-
w	0.3	-
h1	-	+70mV **(Min.)**
h2	-	-70mV **(Min.)**

13.3 LVDS mode AC electrical characteristics

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Clock frequency	R_{XFCLK}	20	-	85	MHz	-
Input data skew margin	T_{RSKM}	500	-	-	pS	| V_{ID} |=400mV R_{XVCM} =1.2V R_{XFCLK} =71MHz
Clock high time	T_{LVCH}	-	4/(7* R_{XFCLK})	-	ns	-
Clock low time	T_{LVCL}	-	3/(7* R_{XFCLK})	-	ns	-
PLL wake-up time	T_{emPLL}	-	-	150	µs	-

Table 13.1: LVDS mode AC electrical characteristics

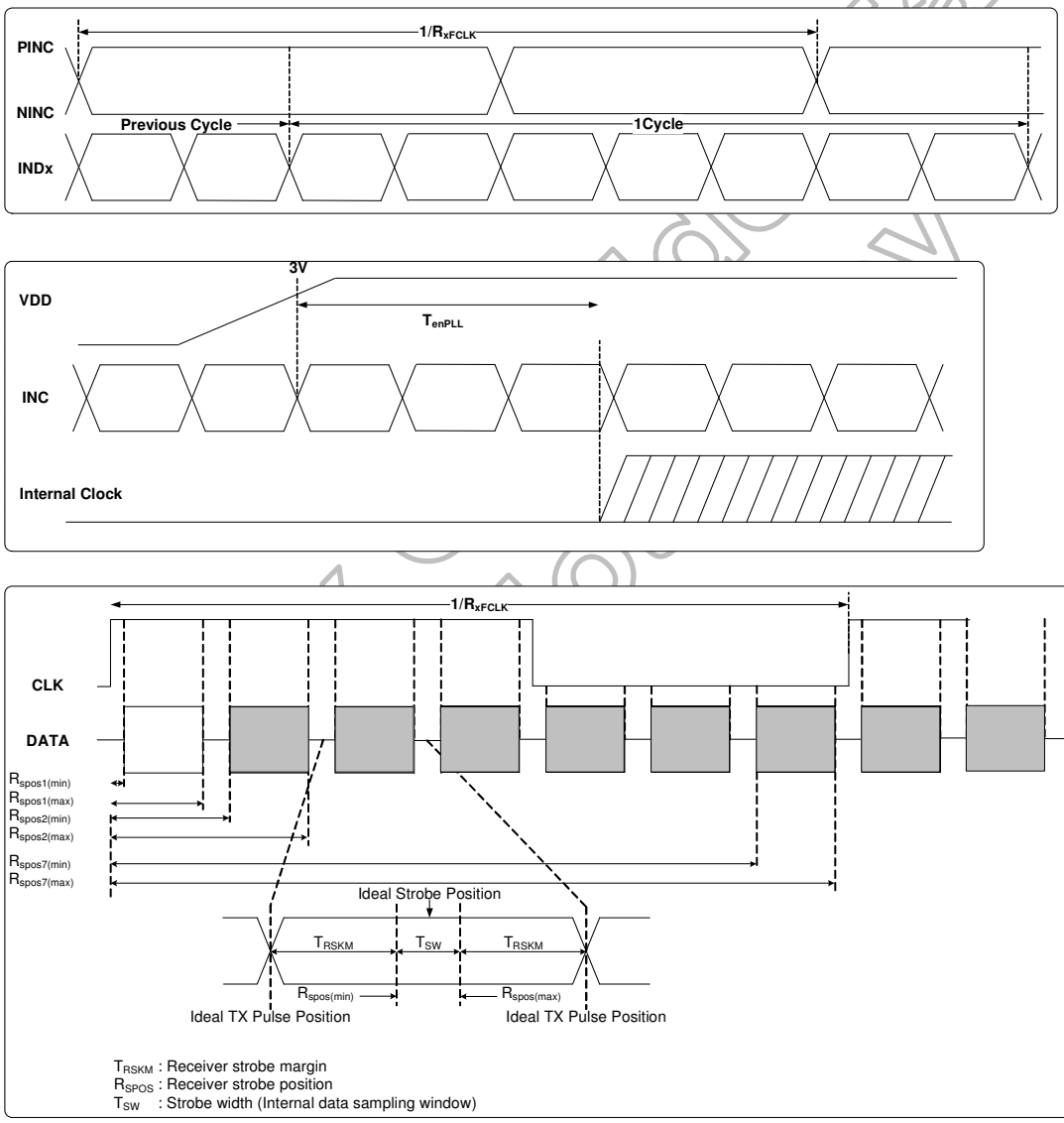
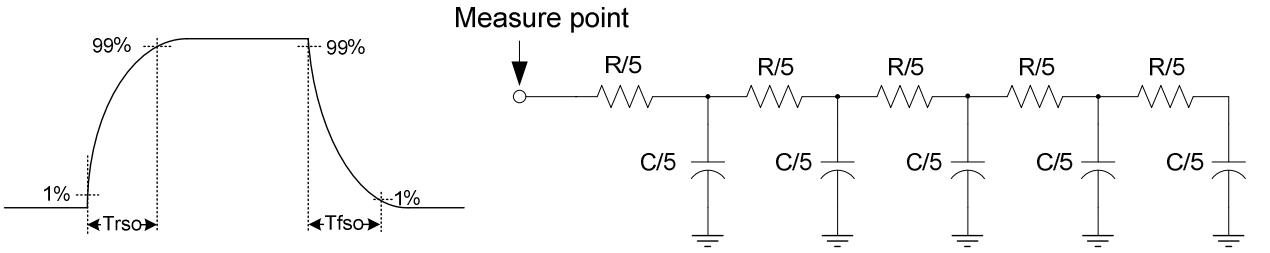


Figure 13.3: LVDS figure

Parameter	Symbol	Spec.			Unit	Condition
		Min.	Typ.	Max.		
Modulation frequency	SSC_{MF}	23	-	93	KHz	-
Modulation rate	SSC_{MR}	-	-	±3	%	LVDS clock =71MHz center spread

Table 13.2: SSC table

13.4 Source output timing (SOUT1 ~ SOUT2400, SL1, SR1)

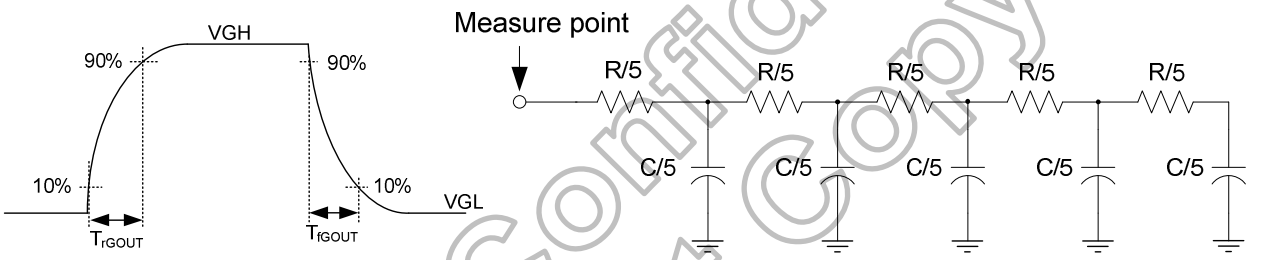


Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Source driver rising time	trSO	R=6.3kohm, C=105.2pF	-	-	3.01	µs
Source driver falling time	tfSO		-	-	4.2	µs

Note: (1) Himax can support simulation for customer design.

Table 13.3: Source output timing

Panel control signal output 1(GOUT1_L~GOUT16_L, GOUT1_R~GOUT16_R)



Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Panel control signal rising time	T_{rGOUT}	R=4.42kohm, C=156pF	-	-	1.74	µs
Panel control signal falling time	T_{fGOUT}		-	-	1.3	µs

Note: (1) Himax can support simulation for customer design.

Table 13.4: GOA output timing

13.5 Serial interface characteristics

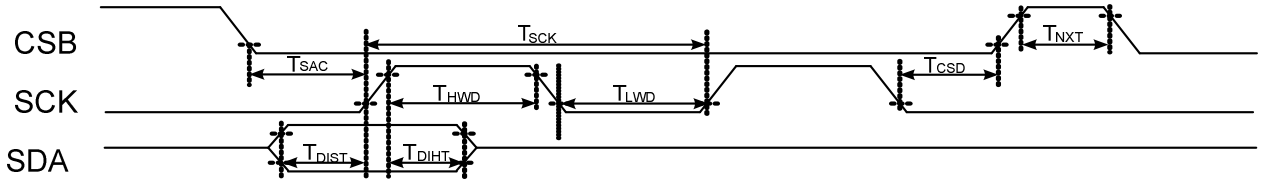


Figure 13.4: Serial interface characteristics

(VDDIO=1.65V~3.6V, VSS=0V, T_A=-20℃~+85℃)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
CSB assertion to first clock edge	T_{SAC}	-	120	-	-	ns
CSB deassertion frome last clock edge	T_{CSD}	-	120	-	-	ns
CSB next control enable	T_E	-	200	-	-	ns
SCK period time	T_{SCK}	-	200	-	-	ns
SCK high period time	T_{HWD}	-	100	-	-	ns
SCK low period time	T_{LWD}	-	100	-	-	ns
SDA input data setup time	T_{DIST}	-	50	-	-	ns
SDA input data hold time	T_{DIHT}	-	50	-	-	ns

Table 13.5: AC characteristic of SPI interface

13.6 Timing requirements for RESETB

When RESETB of the reset pin equals to Low, it will be in the condition of reset. When it is in the condition of reset, it will make the device recover the initial set.

However, in order to avoid the reset noise cause reset, there is a mechanism to judge about whether the reset is needed or not.

The closed interval of Low can be shown as the following.

(VDDIO=1.65V~3.6V, VSS=0V, T_A=-20℃~+85℃)

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Reset low pulse width	Trst	-	20	-	-	μs

Table 13.6: Reset timing

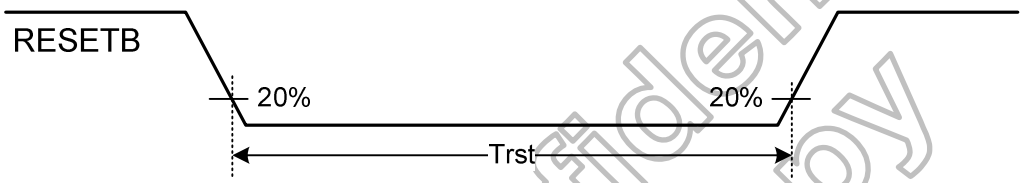


Figure 13.5: Reset timing

14. Pin Assignment (IC Face View)

14.1 PAD sequence

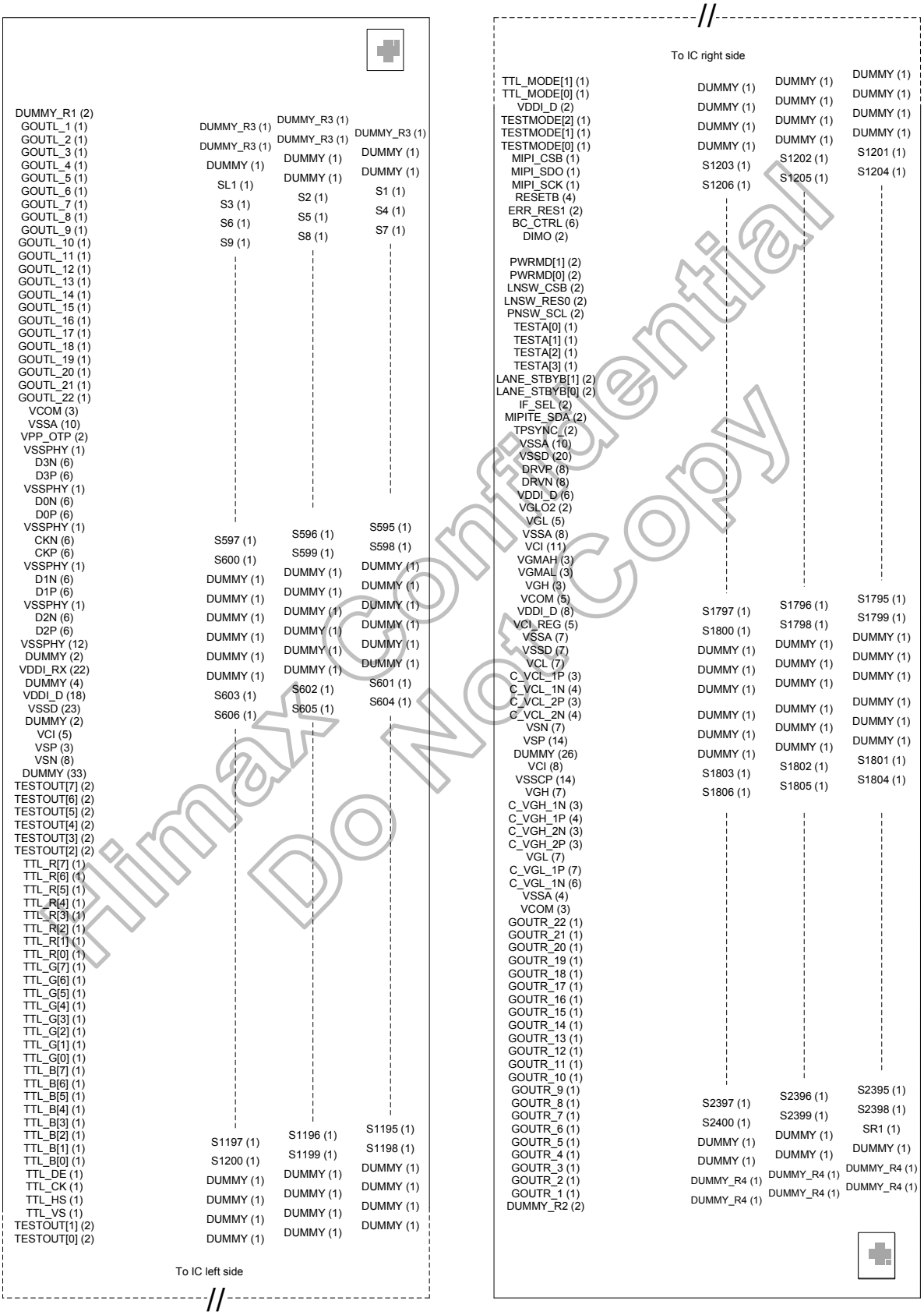
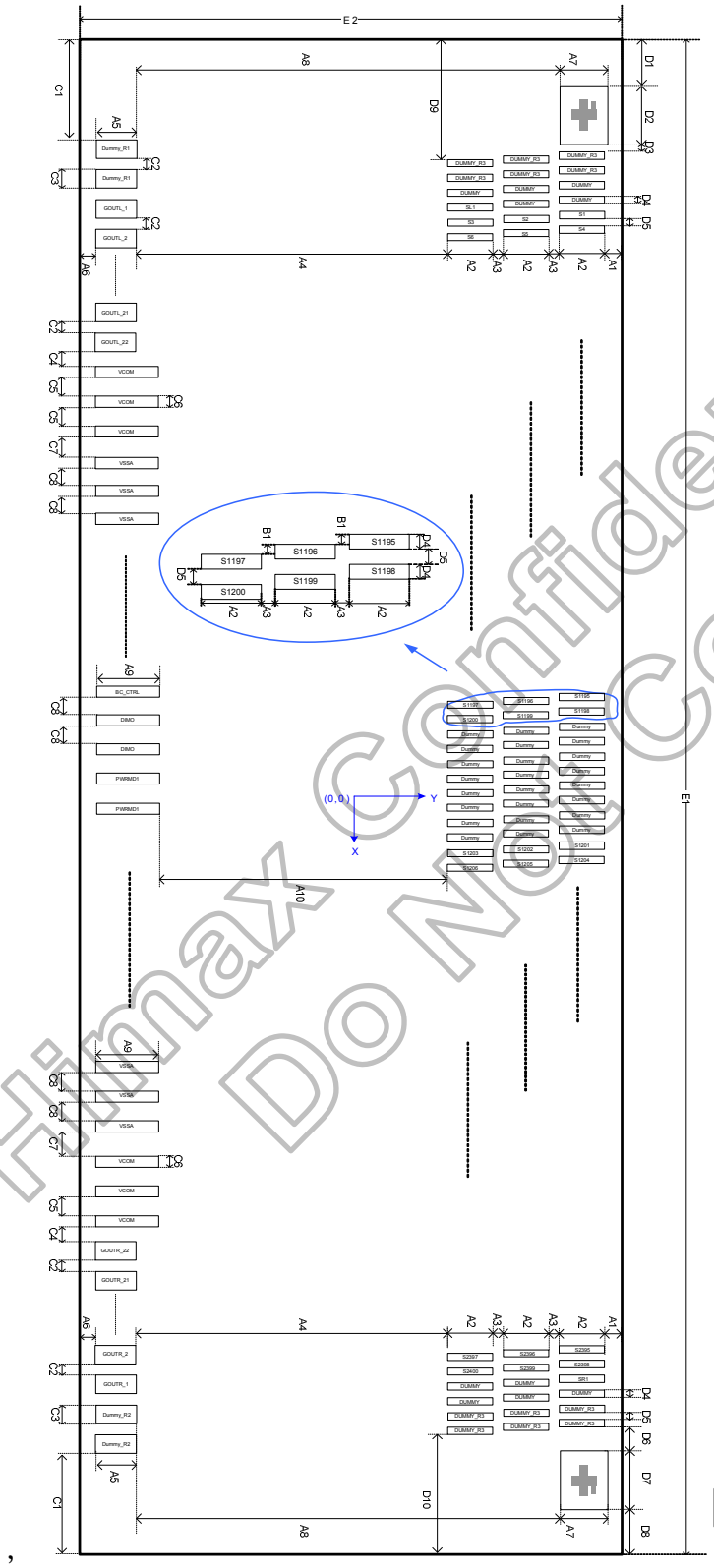


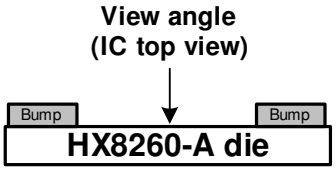
Figure 14.1: Pad sequence

14.2 Bump information

14.2.1 Chip outline dimension



Chip size (w/o scribe line): 27720um x 840um
Chip size (w/i scribe line): 27790um x 910um
Bump height: 12um (+/-3um)
Bump hardness: 80HV (+/-15HV) CP
IC thickness: 300um (+/-10um)
Total bump area: 4068576 um^2



14.2.2 Pad information

Symbol	Dimension (μm)	Symbol	Dimension (μm)	Symbol	Dimension (μm)	Symbol	Dimension (μm)	Symbol	Dimension (μm)
A1	9	B1	11	C1	177.5	D1	104	E1	27720
A2	73	-	-	C2	15	D2	89.5	E2	840
A3	17	-	-	C3	30	D3	6.1	-	-
A4	519	-	-	C4	20	D4	16	-	-
A5	50	-	-	C5	25	D5	17	-	-
A6	9	-	-	C6	20	D6	17.6	-	-
A7	78	-	-	C7	35	D7	100	-	-
A8	697	-	-	C8	25	D8	104	-	-
A9	100	-	-	-	-	D9	221.6	-	-
A10	469	-	-	-	-	D10	199.6	-	-

Table 14.1: Pad information

14.2.3 Alignment mark

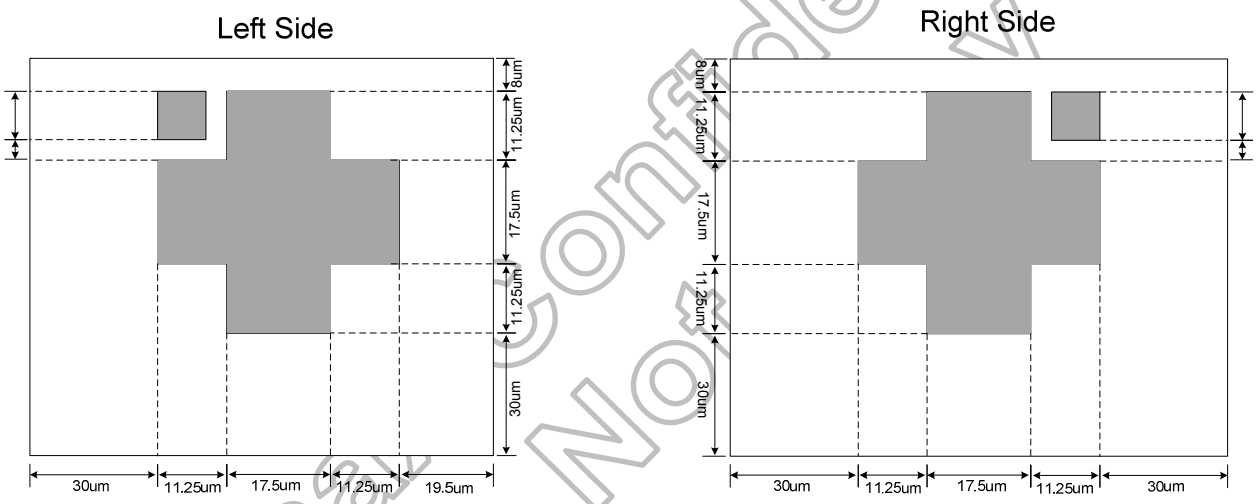


Figure 14.2: Alignment mark

14.3 Pad coordinates

No.	Name	X	Y	Bump size(μm)
1	DUMMY_R1	-13667.5	-386	30X50
2	DUMMY_R1	-13622.5	-386	30X50
3	GOUTL_1	-13577.5	-386	30X50
4	GOUTL_2	-13532.5	-386	30X50
5	GOUTL_3	-13487.5	-386	30X50
6	GOUTL_4	-13442.5	-386	30X50
7	GOUTL_5	-13397.5	-386	30X50
8	GOUTL_6	-13352.5	-386	30X50
9	GOUTL_7	-13307.5	-386	30X50
10	GOUTL_8	-13262.5	-386	30X50
11	GOUTL_9	-13217.5	-386	30X50
12	GOUTL_10	-13172.5	-386	30X50
13	GOUTL_11	-13127.5	-386	30X50
14	GOUTL_12	-13082.5	-386	30X50
15	GOUTL_13	-13037.5	-386	30X50
16	GOUTL_14	-12992.5	-386	30X50
17	GOUTL_15	-12947.5	-386	30X50
18	GOUTL_16	-12902.5	-386	30X50
19	GOUTL_17	-12857.5	-386	30X50
20	GOUTL_18	-12812.5	-386	30X50
21	GOUTL_19	-12767.5	-386	30X50
22	GOUTL_20	-12722.5	-386	30X50
23	GOUTL_21	-12677.5	-386	30X50
24	GOUTL_22	-12632.5	-386	30X50
25	VCOM	-12587.5	-361	20X100
26	VCOM	-12542.5	-361	20X100
27	VCOM	-12497.5	-361	20X100
28	VSSA	-12442.5	-361	20X100
29	VSSA	-12397.5	-361	20X100
30	VSSA	-12352.5	-361	20X100
31	VSSA	-12307.5	-361	20X100
32	VSSA	-12262.5	-361	20X100
33	VSSA	-12217.5	-361	20X100
34	VSSA	-12172.5	-361	20X100
35	VSSA	-12127.5	-361	20X100
36	VSSA	-12082.5	-361	20X100
37	VSSA	-12037.5	-361	20X100
38	VPP_OTP	-11992.5	-361	20X100
39	VPP_OTP	-11947.5	-361	20X100
40	VSSPHY	-11902.5	-361	20X100
41	D3N	-11857.5	-361	20X100
42	D3N	-11812.5	-361	20X100
43	D3N	-11767.5	-361	20X100
44	D3N	-11722.5	-361	20X100
45	D3N	-11677.5	-361	20X100
46	D3N	-11632.5	-361	20X100
47	D3P	-11587.5	-361	20X100
48	D3P	-11542.5	-361	20X100
49	D3P	-11497.5	-361	20X100
50	D3P	-11452.5	-361	20X100
51	D3P	-11407.5	-361	20X100
52	D3P	-11362.5	-361	20X100
53	VSSPHY	-11317.5	-361	20X100
54	D0N	-11272.5	-361	20X100
55	D0N	-11227.5	-361	20X100
56	D0N	-11182.5	-361	20X100
57	D0N	-11137.5	-361	20X100
58	D0N	-11092.5	-361	20X100
59	D0N	-11047.5	-361	20X100
60	D0P	-11002.5	-361	20X100
61	D0P	-10957.5	-361	20X100
62	D0P	-10912.5	-361	20X100
63	D0P	-10867.5	-361	20X100
64	D0P	-10822.5	-361	20X100
65	D0P	-10777.5	-361	20X100
66	VSSPHY	-10732.5	-361	20X100
67	CKN	-10687.5	-361	20X100
68	CKN	-10642.5	-361	20X100
69	CKN	-10597.5	-361	20X100
70	CKN	-10552.5	-361	20X100
71	CKN	-10507.5	-361	20X100
72	CKN	-10462.5	-361	20X100
73	CKP	-10417.5	-361	20X100
74	CKP	-10372.5	-361	20X100
75	CKP	-10327.5	-361	20X100
76	CKP	-10282.5	-361	20X100
77	CKP	-10237.5	-361	20X100
78	CKP	-10192.5	-361	20X100
79	VSSPHY	-10147.5	-361	20X100
80	D1N	-10102.5	-361	20X100
81	D1N	-10057.5	-361	20X100
82	D1N	-10012.5	-361	20X100
83	D1N	-9967.5	-361	20X100
84	D1N	-9922.5	-361	20X100
85	D1N	-9877.5	-361	20X100
86	D1P	-9832.5	-361	20X100
87	D1P	-9787.5	-361	20X100
88	D1P	-9742.5	-361	20X100
89	D1P	-9697.5	-361	20X100
90	D1P	-9652.5	-361	20X100
91	D1P	-9607.5	-361	20X100
92	VSSPHY	-9562.5	-361	20X100
93	D2N	-9517.5	-361	20X100
94	D2N	-9472.5	-361	20X100
95	D2N	-9427.5	-361	20X100
96	D2N	-9382.5	-361	20X100
97	D2N	-9337.5	-361	20X100
98	D2N	-9292.5	-361	20X100
99	D2P	-9247.5	-361	20X100
100	D2P	-9202.5	-361	20X100
101	D2P	-9157.5	-361	20X100
102	D2P	-9112.5	-361	20X100
103	D2P	-9067.5	-361	20X100
104	D2P	-9022.5	-361	20X100
105	VSSPHY	-8977.5	-361	20X100
106	VSSPHY	-8932.5	-361	20X100
107	VSSPHY	-8887.5	-361	20X100
108	VSSPHY	-8842.5	-361	20X100
109	VSSPHY	-8797.5	-361	20X100
110	VSSPHY	-8752.5	-361	20X100
111	VSSPHY	-8707.5	-361	20X100
112	VSSPHY	-8662.5	-361	20X100
113	VSSPHY	-8617.5	-361	20X100
114	VSSPHY	-8572.5	-361	20X100
115	VSSPHY	-8527.5	-361	20X100
116	VSSPHY	-8482.5	-361	20X100
117	DUMMY	-8437.5	-361	20X100
118	DUMMY	-8392.5	-361	20X100
119	VDDI_RX	-8347.5	-361	20X100
120	VDDI_RX	-8302.5	-361	20X100
121	VDDI_RX	-8257.5	-361	20X100
122	VDDI_RX	-8212.5	-361	20X100
123	VDDI_RX	-8167.5	-361	20X100
124	VDDI_RX	-8122.5	-361	20X100
125	VDDI_RX	-8077.5	-361	20X100
126	VDDI_RX	-8032.5	-361	20X100
127	VDDI_RX	-7987.5	-361	20X100
128	VDDI_RX	-7942.5	-361	20X100
129	VDDI_RX	-7897.5	-361	20X100
130	VDDI_RX	-7852.5	-361	20X100
131	VDDI_RX	-7807.5	-361	20X100
132	VDDI_RX	-7762.5	-361	20X100
133	VDDI_RX	-7717.5	-361	20X100
134	VDDI_RX	-7672.5	-361	20X100
135	VDDI_RX	-7627.5	-361	20X100
136	VDDI_RX	-7582.5	-361	20X100
137	VDDI_RX	-7537.5	-361	20X100
138	VDDI_RX	-7492.5	-361	20X100
139	VDDI_RX	-7447.5	-361	20X100
140	VDDI_RX	-7402.5	-361	20X100
141	DUMMY	-7357.5	-361	20X100
142	DUMMY	-7312.5	-361	20X100
143	DUMMY	-7267.5	-361	20X100
144	DUMMY	-7222.5	-361	20X100
145	VDDI_D	-7177.5	-361	20X100
146	VDDI_D	-7132.5	-361	20X100
147	VDDI_D	-7087.5	-361	20X100
148	VDDI_D	-7042.5	-361	20X100
149	VDDI_D	-6997.5	-361	20X100
150	VDDI_D	-6952.5	-361	20X100
151	VDDI_D	-6907.5	-361	20X100
152	VDDI_D	-6862.5	-361	20X100
153	VDDI_D	-6817.5	-361	20X100
154	VDDI_D	-6772.5	-361	20X100
155	VDDI_D	-6727.5	-361	20X100
156	VDDI_D	-6682.5	-361	20X100
157	VDDI_D	-6637.5	-361	20X100
158	VDDI_D	-6592.5	-361	20X100
159	VDDI_D	-6547.5	-361	20X100
160	VDDI_D	-6502.5	-361	20X100
161	VDDI_D	-6457.5	-361	20X100
162	VDDI_D	-6412.5	-361	20X100
163	VSSD	-6367.5	-361	20X100
164	VSSD	-6322.5	-361	20X100
165	VSSD	-6277.5	-361	20X100
166	VSSD	-6232.5	-361	20X100
167	VSSD	-6187.5	-361	20X100
168	VSSD	-6142.5	-361	20X100
169	VSSD	-6097.5	-361	20X100
170	VSSD	-6052.5	-361	20X100
171	VSSD	-6007.5	-361	20X100
172	VSSD	-5962.5	-361	20X100
173	VSSD	-5917.5	-361	20X100
174	VSSD	-5872.5	-361	20X100
175	VSSD	-5827.5	-361	20X100
176	VSSD	-5782.5	-361	20X100
177	VSSD	-5737.5	-361	20X100
178	VSSD	-5692.5	-361	20X100
179	VSSD	-5647.5	-361	20X100
180	VSSD	-5602.5	-361	20X100
181	VSSD	-5557.5	-361	20X100
182	VSSD	-5512.5	-361	20X100
183	VSSD	-5467.5	-361	20X100
184	VSSD	-5422.5	-361	20X100
185	VSSD	-5377.5	-361	20X100
186	DUMMY	-5332.5	-361	20X100
187	DUMMY	-5287.5	-361	20X100
188	VCI	-5242.5	-361	20X100
189	VCI	-5197.5	-361	20X100
190	VCI	-5152.5	-361	20X100
191	VCI	-5107.5	-361	20X100
192	VCI	-5062.5	-361	20X100
193	VSP	-5017.5	-361	20X100
194	VSP	-4972.5	-361	20X100
195	VSP	-4927.5	-361	20X100
196	VSN	-4882.5	-361	20X100
197	VSN	-4837.5	-361	20X100
198	VSN	-4792.5	-361	20X100
199	VSN	-4747.5	-361	20X100
200	VSN	-4702.5	-361	20X100
201	VSN	-4657.5	-361	20X100
202	VSN	-4612.5	-361	20X100
203	VSN	-4567.5	-361	20X100
204	DUMMY	-4522.5	-361	20X100
205	DUMMY	-4477.5	-361	20X100
206	DUMMY	-4432.5	-361	20X100
207	DUMMY	-4387.5	-361	20X100
208	DUMMY	-4342.5	-361	20X100
209	DUMMY	-4297.5	-361	20X100
210	DUMMY	-4252.5	-361	20X100
211	DUMMY	-4207.5	-361	20X100
212	DUMMY	-4162.5	-361	20X100
213	DUMMY	-4117.5	-361	20X100
214	DUMMY	-4072.5	-361	20X100
215	DUMMY	-4027.5	-361	20X100
216	DUMMY	-3982.5	-361	20X100
217	DUMMY	-3937.5	-361	20X100
218	DUMMY	-3892.5	-361	20X100
219	DUMMY	-3847.5	-361	20X100
220	DUMMY	-3802.5	-361	20X100
221	DUMMY	-3757.5	-361	20X100
222	DUMMY	-3712.5	-361	20X100
223	DUMMY	-3667.5	-361	20X100
224	DUMMY	-3622.5	-361	20X100
225	DUMMY	-3577.5	-361	20X100
226	DUMMY	-3532.5	-361	20X100
227	DUMMY	-3487.5	-361	20X100
228	DUMMY	-3442.5	-361	20X100
229	DUMMY	-3397.5	-361	20X100
230	DUMMY	-3352.5	-361	20X100
231	DUMMY	-3307.5	-361	20X100
232	DUMMY	-3262.5	-361	20X100
233	DUMMY	-3217.5	-361	20X100
234	DUMMY	-3172.5	-361	20X100
235	TESTOUT7	-3127.5	-361	20X100
236	TESTOUT7	-3082.5	-361	20X100
237	TESTOUT6	-3037.5	-361	20X100
238	TESTOUT6	-2992.5	-361	20X100
239	TESTOUT5	-2947.5	-361	20X100
240	TESTOUT5	-2902.5	-361	20X100

No.	Name	X	Y	Bump size(μm)
241	TESTOUT4	-2857.5	-361	20X100
242	TESTOUT4	-2812.5	-361	20X100
243	TESTOUT3	-2767.5	-361	20X100
244	TESTOUT3	-2722.5	-361	20X100
245	TESTOUT2	-2677.5	-361	20X100
246	TESTOUT2	-2632.5	-361	20X100
247	TTL_R7	-2587.5	-361	20X100
248	TTL_R6	-2542.5	-361	20X100
249	TTL_R5	-2497.5	-361	20X100
250	TTL_R4	-2452.5	-361	20X100
251	TTL_R3	-2407.5	-361	20X100
252	TTL_R2	-2362.5	-361	20X100
253	TTL_R1	-2317.5	-361	20X100
254	TTL_R0	-2272.5	-361	20X100
255	DUMMY	-2227.5	-361	20X100
256	DUMMY	-2182.5	-361	20X100
257	TTL_G7	-2137.5	-361	20X100
258	TTL_G6	-2092.5	-361	20X100
259	TTL_G5	-2047.5	-361	20X100
260	TTL_G4	-2002.5	-361	20X100
261	TTL_G3	-1957.5	-361	20X100
262	TTL_G2	-1912.5	-361	20X100
263	TTL_G1	-1867.5	-361	20X100
264	TTL_G0	-1822.5	-361	20X100
265	TTL_B7	-1777.5	-361	20X100
266	TTL_B6	-1732.5	-361	20X100
267	TTL_B5	-1687.5	-361	20X100
268	TTL_B4	-1642.5	-361	20X100
269	TTL_B3	-1597.5	-361	20X100
270	TTL_B2	-1552.5	-361	20X100
271	TTL_B1	-1507.5	-361	20X100
272	TTL_B0	-1462.5	-361	20X100
273	TTL_DE	-1417.5	-361	20X100
274	TTL_CK	-1372.5	-361	20X100
275	TTL_HS	-1327.5	-361	20X100
276	TTL_VS	-1282.5	-361	20X100
277	TESTOUT1	-1237.5	-361	20X100
278	TESTOUT1	-1192.5	-361	20X100
279	TESTOUT0	-1147.5	-361	20X100
280	TESTOUT0	-1102.5	-361	20X100
281	TTL_MODE1	-1057.5	-361	20X100
282	TTL_MODE0	-1012.5	-361	20X100
283	VDDI_D	-967.5	-361	20X100
284	VDDI_D	-922.5	-361	20X100
285	TESTMODE2	-877.5	-361	20X100
286	TESTMODE1	-832.5	-361	20X100
287	TESTMODE0	-787.5	-361	20X100
288	MIPI_CSB	-742.5	-361	20X100
289	MIPI_SCK	-697.5	-361	20X100
290	MIPI_SD	-652.5	-361	20X100
291	RESETB	-607.5	-361	20X100
292	RESETB	-562.5	-361	20X100
293	RESETB	-517.5	-361	20X100
294	RESETB	-472.5	-361	20X100
295	ERR_RES1	-427.5	-361	20X100
296	ERR_RES1	-382.5	-361	20X100
297	BC_CTRL	-337.5	-361	20X100
298	BC_CTRL	-292.5	-361	20X100
299	BC_CTRL	-247.5	-361	20X100
300	BC_CTRL	-202.5	-361	20X100
301	BC_CTRL	-157.5	-361	20X100
302	BC_CTRL	-112.5	-361	20X100
303	DIMO	-67.5	-361	20X100
304	DIMO	-22.5	-361	20X100
305	PWRMD1	22.5	-361	20X100
306	PWRMD1	67.5	-361	20X100
307	PWRMD0	112.5	-361	20X100
308	PWRMD0	157.5	-361	20X100
309	LNSW_CSB	202.5	-361	20X100
310	LNSW_CSB	247.5	-361	20X100
311	LNSW_RES0	292.5	-361	20X100
312	LNSW_RES0	337.5	-361	20X100
313	PNSW_SCL	382.5	-361	20X100
314	PNSW_SCL	427.5	-361	20X100
315	TESTA0	472.5	-361	20X100
316	TESTA1	517.5	-361	20X100
317	TESTA2	562.5	-361	20X100
318	TESTA3	607.5	-361	20X100
319	LANE1_STBYB	652.5	-361	20X100
320	LANE1_STBYB	697.5	-361	20X100
321	LANE0_BISTB	742.5	-361	20X100
322	LANE0_BISTB	787.5	-361	20X100
323	IF_SEL	832.5	-361	20X100
324	IF_SEL	877.5	-361	20X100
325	MIPITE_SDA	922.5	-361	20X100
326	MIPITE_SDA	967.5	-361	20X100
327	TPSYNC	1012.5	-361	20X100
328	TPSYNC	1057.5	-361	20X100
329	VSSA	1102.5	-361	20X100
330	VSSA	1147.5	-361	20X100
331	VSSA	1192.5	-361	20X100
332	VSSA	1237.5	-361	20X100
333	VSSA	1282.5	-361	20X100
334	VSSA	1327.5	-361	20X100
335	VSSA	1372.5	-361	20X100
336	VSSA	1417.5	-361	20X100
337	VSSA	1462.5	-361	20X100
338	VSSA	1507.5	-361	20X100
339	VSSD	1552.5	-361	20X100
340	VSSD	1597.5	-361	20X100
341	VSSD	1642.5	-361	20X100
342	VSSD	1687.5	-361	20X100
343	VSSD	1732.5	-361	20X100
344	VSSD	1777.5	-361	20X100
345	VSSD	1822.5	-361	20X100
346	VSSD	1867.5	-361	20X100
347	VSSD	1912.5	-361	20X100
348	VSSD	1957.5	-361	20X100
349	VSSD	2002.5	-361	20X100
350	VSSD	2047.5	-361	20X100
351	VSSD	2092.5	-361	20X100
352	VSSD	2137.5	-361	20X100
353	VSSD	2182.5	-361	20X100
354	VSSD	2227.5	-361	20X100
355	VSSD	2272.5	-361	20X100
356	VSSD	2317.5	-361	20X100
357	VSSD	2362.5	-361	20X100
358	VSSD	2407.5	-361	20X100
359	DRVP	2452.5	-361	20X100
360	DRVP	2497.5	-361	20X100
361	DRVP	2542.5	-361	20X100
362	DRVP	2587.5	-361	20X100
363	DRVP	2632.5	-361	20X100
364	DRVP	2677.5	-361	20X100
365	DRVP	2722.5	-361	20X100
366	DRVP	2767.5	-361	20X100
367	DRVN	2812.5	-361	20X100
368	DRVN	2857.5	-361	20X100
369	DRVN	2902.5	-361	20X100
370	DRVN	2947.5	-361	20X100
371	DRVN	2992.5	-361	20X100
372	DRVN	3037.5	-361	20X100
373	DRVN	3082.5	-361	20X100
374	DRVN	3127.5	-361	20X100
375	VDDI_D	3172.5	-361	20X100
376	VDDI_D	3217.5	-361	20X100
377	VDDI_D	3262.5	-361	20X100
378	VDDI_D	3307.5	-361	20X100
379	VDDI_D	3352.5	-361	20X100
380	VDDI_D	3397.5	-361	20X100
381	VGLO2	3442.5	-361	20X100
382	VGLO2	3487.5	-361	20X100
383	VGL	3532.5	-361	20X100
384	VGL	3577.5	-361	20X100
385	VGL	3622.5	-361	20X100
386	VGL	3667.5	-361	20X100
387	VGL	3712.5	-361	20X100
388	VSSA	3757.5	-361	20X100
389	VSSA	3802.5	-361	20X100
390	VSSA	3847.5	-361	20X100
391	VSSA	3892.5	-361	20X100
392	VSSA	3937.5	-361	20X100
393	VSSRC	3982.5	-361	20X100
394	VSSRC	4027.5	-361	20X100
395	VSSRC	4072.5	-361	20X100
396	VCI	4117.5	-361	20X100
397	VCI	4162.5	-361	20X100
398	VCI	4207.5	-361	20X100
399	VCI	4252.5	-361	20X100
400	VCI	4297.5	-361	20X100
401	VCI	4342.5	-361	20X100
402	VCI	4387.5	-361	20X100
403	VCI	4432.5	-361	20X100
404	VCI	4477.5	-361	20X100
405	VCI	4522.5	-361	20X100
406	VCI	4567.5	-361	20X100
407	VGMAH	4612.5	-361	20X100
408	VGMAH	4657.5	-361	20X100
409	VGMAH	4702.5	-361	20X100
410	VGMAL	4747.5	-361	20X100
411	VGMAL	4792.5	-361	20X100
412	VGMAL	4837.5	-361	20X100
413	VGH	4882.5	-361	20X100
414	VGH	4927.5	-361	20X100
415	VGH	4972.5	-361	20X100
416	VCOM	5017.5	-361	20X100
417	VCOM	5062.5	-361	20X100
418	VCOM	5107.5	-361	20X100
419	VCOM	5152.5	-361	20X100
420	VCOM	5197.5	-361	20X100
421	VDDI_D	5242.5	-361	20X100
422	VDDI_D	5287.5	-361	20X100
423	VDDI_D	5332.5	-361	20X100
424	VDDI_D	5377.5	-361	20X100
425	VDDI_D	5422.5	-361	20X100
426	VDDI_D	5467.5	-361	20X100
427	VDDI_D	5512.5	-361	20X100
428	VDDI_D	5557.5	-361	20X100
429	VCI_REG	5602.5	-361	20X100
430	VCI_REG	5647.5	-361	20X100
431	VCI_REG	5692.5	-361	20X100
432	VCI_REG	5737.5	-361	20X100
433	VCI_REG	5782.5	-361	20X100
434	VSSA	5827.5	-361	20X100
435	VSSA	5872.5	-361	20X100
436	VSSA	5917.5	-361	20X100
437	VSSA	5962.5	-361	20X100
438	VSSA	6007.5	-361	20X100
439	VSSA	6052.5	-361	20X100
440	VSSA	6097.5	-361	20X100
441	VSSD	6142.5	-361	20X100
442	VSSD	6187.5	-361	20X100
443	VSSD	6232.5	-361	20X100
444	VSSD	6277.5	-361	20X100
445	VSSD	6322.5	-361	20X100
446	VSSD	6367.5	-361	20X100
447	VSSD	6412.5	-361	20X100
448	VCL	6457.5	-361	20X100
449	VCL	6502.5	-361	20X100
450	VCL	6547.5	-361	20X100
451	VCL	6592.5	-361	20X100
452	VCL	6637.5	-361	20X100
453	VCL	6682.5	-361	20X100
454	VCL	6727.5	-361	20X100
455	C_VCL_1P	6772.5	-361	20X100
456	C_VCL_1P	6817.5	-361	20X100
457	C_VCL_1P	6862.5	-361	20X100
458	C_VCL_1N	6907.5	-361	20X100
459	C_VCL_1N	6952.5	-361	20X100
460	C_VCL_1N	6997.5	-361	20X100
461	C_VCL_1N	7042.5	-361	20X100
462	C_VCL_2P	7087.5	-361	20X100
463	C_VCL_2P	7132.5	-361	20X100
464	C_VCL_2P	7177.5	-361	20X100
465	C_VCL_2N	7222.5	-361	20X100
466	C_VCL_2N	7267.5	-361	20X100
467	C_VCL_2N	7312.5	-361	20X100
468	C_VCL_2N	7357.5	-361	20X100
469	VSN	7402.5	-361	20X100
470	VSN	7447.5	-361	20X100
471	VSN	7492.5	-361	20X100
472	VSN	7537.5	-361	20X100
473	VSN	7582.5	-361	20X100
474	VSN	7627.5	-361	20X100
475	VSN	7672.5	-361	20X100
476	VSP	7717.5	-361	20X100
477	VSP	7762.5	-361	20X100
478	VSP	7807.5	-361	20X100
479	VSP	7852.5	-361	20X100
480	VSP	7897.5	-361	20X100

No.	Name	X	Y	Bump size(μm)
481	VSP	7942.5	-361	20X100
482	VSP	7987.5	-361	20X100
483	VSP	8032.5	-361	20X100
484	VSP	8077.5	-361	20X100
485	VSP	8122.5	-361	20X100
486	VSP	8167.5	-361	20X100
487	VSP	8212.5	-361	20X100
488	VSP	8257.5	-361	20X100
489	VSP	8302.5	-361	20X100
490	DUMMY	8347.5	-361	20X100
491	DUMMY	8392.5	-361	20X100
492	DUMMY	8437.5	-361	20X100
493	DUMMY	8482.5	-361	20X100
494	DUMMY	8527.5	-361	20X100
495	DUMMY	8572.5	-361	20X100
496	DUMMY	8617.5	-361	20X100
497	DUMMY	8662.5	-361	20X100
498	DUMMY	8707.5	-361	20X100
499	DUMMY	8752.5	-361	20X100
500	DUMMY	8797.5	-361	20X100
501	DUMMY	8842.5	-361	20X100
502	DUMMY	8887.5	-361	20X100
503	DUMMY	8932.5	-361	20X100
504	DUMMY	8977.5	-361	20X100
505	DUMMY	9022.5	-361	20X100
506	DUMMY	9067.5	-361	20X100
507	DUMMY	9112.5	-361	20X100
508	DUMMY	9157.5	-361	20X100
509	DUMMY	9202.5	-361	20X100
510	DUMMY	9247.5	-361	20X100
511	DUMMY	9292.5	-361	20X100
512	DUMMY	9337.5	-361	20X100
513	DUMMY	9382.5	-361	20X100
514	DUMMY	9427.5	-361	20X100
515	DUMMY	9472.5	-361	20X100
516	VCI	9517.5	-361	20X100
517	VCI	9562.5	-361	20X100
518	VCI	9607.5	-361	20X100
519	VCI	9652.5	-361	20X100
520	VCI	9697.5	-361	20X100
521	VCI	9742.5	-361	20X100
522	VCI	9787.5	-361	20X100
523	VCI	9832.5	-361	20X100
524	VSSCP	9877.5	-361	20X100
525	VSSCP	9922.5	-361	20X100
526	VSSCP	9967.5	-361	20X100
527	VSSCP	10012.5	-361	20X100
528	VSSCP	10057.5	-361	20X100
529	VSSCP	10102.5	-361	20X100
530	VSSCP	10147.5	-361	20X100
531	VSSCP	10192.5	-361	20X100
532	VSSCP	10237.5	-361	20X100
533	VSSCP	10282.5	-361	20X100
534	VSSCP	10327.5	-361	20X100
535	VSSCP	10372.5	-361	20X100
536	VSSCP	10417.5	-361	20X100
537	VSSCP	10462.5	-361	20X100
538	VGH	10507.5	-361	20X100
539	VGH	10552.5	-361	20X100
540	VGH	10597.5	-361	20X100
541	VGH	10642.5	-361	20X100
542	VGH	10687.5	-361	20X100
543	VGH	10732.5	-361	20X100
544	VGH	10777.5	-361	20X100
545	C_VGH_1N	10822.5	-361	20X100
546	C_VGH_1N	10867.5	-361	20X100
547	C_VGH_1N	10912.5	-361	20X100
548	C_VGH_1P	10957.5	-361	20X100
549	C_VGH_1P	11002.5	-361	20X100
550	C_VGH_1P	11047.5	-361	20X100
551	C_VGH_1P	11092.5	-361	20X100
552	C_VGH_2N	11137.5	-361	20X100
553	C_VGH_2N	11182.5	-361	20X100
554	C_VGH_2N	11227.5	-361	20X100
555	C_VGH_2P	11272.5	-361	20X100
556	C_VGH_2P	11317.5	-361	20X100
557	C_VGH_2P	11362.5	-361	20X100
558	VGL	11407.5	-361	20X100
559	VGL	11452.5	-361	20X100
560	VGL	11497.5	-361	20X100
561	VGL	11542.5	-361	20X100
562	VGL	11587.5	-361	20X100
563	VGL	11632.5	-361	20X100
564	VGL	11677.5	-361	20X100
565	C_VGL_1P	11722.5	-361	20X100
566	C_VGL_1P	11767.5	-361	20X100
567	C_VGL_1P	11812.5	-361	20X100
568	C_VGL_1P	11857.5	-361	20X100
569	C_VGL_1P	11902.5	-361	20X100
570	C_VGL_1P	11947.5	-361	20X100
571	C_VGL_1P	11992.5	-361	20X100
572	C_VGL_1N	12037.5	-361	20X100
573	C_VGL_1N	12082.5	-361	20X100
574	C_VGL_1N	12127.5	-361	20X100
575	C_VGL_1N	12172.5	-361	20X100
576	C_VGL_1N	12217.5	-361	20X100
577	C_VGL_1N	12262.5	-361	20X100
578	VSSA	12307.5	-361	20X100
579	VSSA	12352.5	-361	20X100
580	VSSA	12397.5	-361	20X100
581	VSSA	12442.5	-361	20X100
582	VCOM	12497.5	-361	20X100
583	VCOM	12542.5	-361	20X100
584	VCOM	12587.5	-361	20X100
585	GOUTR_22	12632.5	-386	30X50
586	GOUTR_21	12677.5	-386	30X50
587	GOUTR_20	12722.5	-386	30X50
588	GOUTR_19	12767.5	-386	30X50
589	GOUTR_18	12812.5	-386	30X50
590	GOUTR_17	12857.5	-386	30X50
591	GOUTR_16	12902.5	-386	30X50
592	GOUTR_15	12947.5	-386	30X50
593	GOUTR_14	12992.5	-386	30X50
594	GOUTR_13	13037.5	-386	30X50
595	GOUTR_12	13082.5	-386	30X50
596	GOUTR_11	13127.5	-386	30X50
597	GOUTR_10	13172.5	-386	30X50
598	GOUTR_9	13217.5	-386	30X50
599	GOUTR_8	13262.5	-386	30X50
600	GOUTR_7	13307.5	-386	30X50
601	GOUTR_6	13352.5	-386	30X50
602	GOUTR_5	13397.5	-386	30X50
603	GOUTR_4	13442.5	-386	30X50
604	GOUTR_3	13487.5	-386	30X50
605	GOUTR_2	13532.5	-386	30X50
606	GOUTR_1	13577.5	-386	30X50
607	DUMMY_R2	13622.5	-386	30X50
608	DUMMY_R2	13667.5	-386	30X50
609	DUMMY_R4	13656.5	194.5	16X73
610	DUMMY_R4	13645.5	284.5	16X73
611	DUMMY_R4	13634.5	374.5	16X73
612	DUMMY_R4	13623.5	194.5	16X73
613	DUMMY_R4	13612.5	284.5	16X73
614	DUMMY_R4	13601.5	374.5	16X73
615	DUMMY	13590.5	194.5	16X73
616	DUMMY	13579.5	284.5	16X73
617	DUMMY	13568.5	374.5	16X73
618	DUMMY	13557.5	194.5	16X73
619	DUMMY	13546.5	284.5	16X73
620	SR1	13535.5	374.5	16X73
621	S2400	13524.5	194.5	16X73
622	S2399	13513.5	284.5	16X73
623	S2398	13502.5	374.5	16X73
624	S2397	13491.5	194.5	16X73
625	S2396	13480.5	284.5	16X73
626	S2395	13469.5	374.5	16X73
627	S2394	13458.5	194.5	16X73
628	S2393	13447.5	284.5	16X73
629	S2392	13436.5	374.5	16X73
630	S2391	13425.5	194.5	16X73
631	S2390	13414.5	284.5	16X73
632	S2389	13403.5	374.5	16X73
633	S2388	13392.5	194.5	16X73
634	S2387	13381.5	284.5	16X73
635	S2386	13370.5	374.5	16X73
636	S2385	13359.5	194.5	16X73
637	S2384	13348.5	284.5	16X73
638	S2383	13337.5	374.5	16X73
639	S2382	13326.5	194.5	16X73
640	S2381	13315.5	284.5	16X73
641	S2380	13304.5	374.5	16X73
642	S2379	13293.5	194.5	16X73
643	S2378	13282.5	284.5	16X73
644	S2377	13271.5	374.5	16X73
645	S2376	13260.5	194.5	16X73
646	S2375	13249.5	284.5	16X73
647	S2374	13238.5	374.5	16X73
648	S2373	13227.5	194.5	16X73
649	S2372	13216.5	284.5	16X73
650	S2371	13205.5	374.5	16X73
651	S2370	13194.5	194.5	16X73
652	S2369	13183.5	284.5	16X73
653	S2368	13172.5	374.5	16X73
654	S2367	13161.5	194.5	16X73
655	S2366	13150.5	284.5	16X73
656	S2365	13139.5	374.5	16X73
657	S2364	13128.5	194.5	16X73
658	S2363	13117.5	284.5	16X73
659	S2362	13106.5	374.5	16X73
660	S2361	13095.5	194.5	16X73
661	S2360	13084.5	284.5	16X73
662	S2359	13073.5	374.5	16X73
663	S2358	13062.5	194.5	16X73
664	S2357	13051.5	284.5	16X73
665	S2356	13040.5	374.5	16X73
666	S2355	13029.5	194.5	16X73
667	S2354	13018.5	284.5	16X73
668	S2353	13007.5	374.5	16X73
669	S2352	12996.5	194.5	16X73
670	S2351	12985.5	284.5	16X73
671	S2350	12974.5	374.5	16X73
672	S2349	12963.5	194.5	16X73
673	S2348	12952.5	284.5	16X73
674	S2347	12941.5	374.5	16X73
675	S2346	12930.5	194.5	16X73
676	S2345	12919.5	284.5	16X73
677	S2344	12908.5	374.5	16X73
678	S2343	12897.5	194.5	16X73
679	S2342	12886.5	284.5	16X73
680	S2341	12875.5	374.5	16X73
681	S2340	12864.5	194.5	16X73
682	S2339	12853.5	284.5	16X73
683	S2338	12842.5	374.5	16X73
684	S2337	12831.5	194.5	16X73
685	S2336	12820.5	284.5	16X73
686	S2335	12809.5	374.5	16X73
687	S2334	12798.5	194.5	16X73
688	S2333	12787.5	284.5	16X73
689	S2332	12776.5	374.5	16X73
690	S2331	12765.5	194.5	16X73
691	S2330	12754.5	284.5	16X73
692	S2329	12743.5	374.5	16X73
693	S2328	12732.5	194.5	16X73
694	S2327	12721.5	284.5	16X73
695	S2326	12710.5	374.5	16X73
696	S2325	12699.5	194.5	16X73
697	S2324	12688.5	284.5	16X73
698	S2323	12677.5	374.5	16X73
699	S2322	12666.5	194.5	16X73
700	S2321	12655.5	284.5	16X73
701	S2320	12644.5	374.5	16X73
702	S2319	12633.5	194.5	16X73
703	S2318	12622.5	284.5	16X73
704	S2317	12611.5	374.5	16X73
705	S2316	12600.5	194.5	16X73
706	S2315	12589.5	284.5	16X73
707	S2314	12578.5	374.5	16X73
708	S2313	12567.5	194.5	16X73
709	S2312	12556.5	284.5	16X73
710	S2311	12545.5	374.5	16X73
711	S2310	12534.5	194.5	16X73
712	S2309	12523.5	284.5	16X73
713	S2308	12512.5	374.5	16X73
714	S2307	12501.5	194.5	16X73
715	S2306	12490.5	284.5	16X73
716	S2305	12479.5	374.5	16X73
717	S2304	12468.5	194.5	16X73
718	S2303	12457.5	284.5	16X73
719	S2302	12446.5	374.5	16X73
720	S2301	12435.5	194.5	16X73

No.	Name	X	Y	Bump size(μm)
721	S2300	12424.5	284.5	16X73
722	S2299	12413.5	374.5	16X73
723	S2298	12402.5	194.5	16X73
724	S2297	12391.5	284.5	16X73
725	S2296	12380.5	374.5	16X73
726	S2295	12369.5	194.5	16X73
727	S2294	12358.5	284.5	16X73
728	S2293	12347.5	374.5	16X73
729	S2292	12336.5	194.5	16X73
730	S2291	12325.5	284.5	16X73
731	S2290	12314.5	374.5	16X73
732	S2289	12303.5	194.5	16X73
733	S2288	12292.5	284.5	16X73
734	S2287	12281.5	374.5	16X73
735	S2286	12270.5	194.5	16X73
736	S2285	12259.5	284.5	16X73
737	S2284	12248.5	374.5	16X73
738	S2283	12237.5	194.5	16X73
739	S2282	12226.5	284.5	16X73
740	S2281	12215.5	374.5	16X73
741	S2280	12204.5	194.5	16X73
742	S2279	12193.5	284.5	16X73
743	S2278	12182.5	374.5	16X73
744	S2277	12171.5	194.5	16X73
745	S2276	12160.5	284.5	16X73
746	S2275	12149.5	374.5	16X73
747	S2274	12138.5	194.5	16X73
748	S2273	12127.5	284.5	16X73
749	S2272	12116.5	374.5	16X73
750	S2271	12105.5	194.5	16X73
751	S2270	12094.5	284.5	16X73
752	S2269	12083.5	374.5	16X73
753	S2268	12072.5	194.5	16X73
754	S2267	12061.5	284.5	16X73
755	S2266	12050.5	374.5	16X73
756	S2265	12039.5	194.5	16X73
757	S2264	12028.5	284.5	16X73
758	S2263	12017.5	374.5	16X73
759	S2262	12006.5	194.5	16X73
760	S2261	11995.5	284.5	16X73
761	S2260	11984.5	374.5	16X73
762	S2259	11973.5	194.5	16X73
763	S2258	11962.5	284.5	16X73
764	S2257	11951.5	374.5	16X73
765	S2256	11940.5	194.5	16X73
766	S2255	11929.5	284.5	16X73
767	S2254	11918.5	374.5	16X73
768	S2253	11907.5	194.5	16X73
769	S2252	11896.5	284.5	16X73
770	S2251	11885.5	374.5	16X73
771	S2250	11874.5	194.5	16X73
772	S2249	11863.5	284.5	16X73
773	S2248	11852.5	374.5	16X73
774	S2247	11841.5	194.5	16X73
775	S2246	11830.5	284.5	16X73
776	S2245	11819.5	374.5	16X73
777	S2244	11808.5	194.5	16X73
778	S2243	11797.5	284.5	16X73
779	S2242	11786.5	374.5	16X73
780	S2241	11775.5	194.5	16X73
781	S2240	11764.5	284.5	16X73
782	S2239	11753.5	374.5	16X73
783	S2238	11742.5	194.5	16X73
784	S2237	11731.5	284.5	16X73
785	S2236	11720.5	374.5	16X73
786	S2235	11709.5	194.5	16X73
787	S2234	11698.5	284.5	16X73
788	S2233	11687.5	374.5	16X73
789	S2232	11676.5	194.5	16X73
790	S2231	11665.5	284.5	16X73
791	S2230	11654.5	374.5	16X73
792	S2229	11643.5	194.5	16X73
793	S2228	11632.5	284.5	16X73
794	S2227	11621.5	374.5	16X73
795	S2226	11610.5	194.5	16X73
796	S2225	11599.5	284.5	16X73
797	S2224	11588.5	374.5	16X73
798	S2223	11577.5	194.5	16X73
799	S2222	11566.5	284.5	16X73
800	S2221	11555.5	374.5	16X73
801	S2220	11544.5	194.5	16X73
802	S2219	11533.5	284.5	16X73
803	S2218	11522.5	374.5	16X73
804	S2217	11511.5	194.5	16X73
805	S2216	11500.5	284.5	16X73
806	S2215	11489.5	374.5	16X73
807	S2214	11478.5	194.5	16X73
808	S2213	11467.5	284.5	16X73
809	S2212	11456.5	374.5	16X73
810	S2211	11445.5	194.5	16X73
811	S2210	11434.5	284.5	16X73
812	S2209	11423.5	374.5	16X73
813	S2208	11412.5	194.5	16X73
814	S2207	11401.5	284.5	16X73
815	S2206	11390.5	374.5	16X73
816	S2205	11379.5	194.5	16X73
817	S2204	11368.5	284.5	16X73
818	S2203	11357.5	374.5	16X73
819	S2202	11346.5	194.5	16X73
820	S2201	11335.5	284.5	16X73
821	S2200	11324.5	374.5	16X73
822	S2199	11313.5	194.5	16X73
823	S2198	11302.5	284.5	16X73
824	S2197	11291.5	374.5	16X73
825	S2196	11280.5	194.5	16X73
826	S2195	11269.5	284.5	16X73
827	S2194	11258.5	374.5	16X73
828	S2193	11247.5	194.5	16X73
829	S2192	11236.5	284.5	16X73
830	S2191	11225.5	374.5	16X73
831	S2190	11214.5	194.5	16X73
832	S2189	11203.5	284.5	16X73
833	S2188	11192.5	374.5	16X73
834	S2187	11181.5	194.5	16X73
835	S2186	11170.5	284.5	16X73
836	S2185	11159.5	374.5	16X73
837	S2184	11148.5	194.5	16X73
838	S2183	11137.5	284.5	16X73
839	S2182	11126.5	374.5	16X73
840	S2181	11115.5	194.5	16X73
841	S2180	11104.5	284.5	16X73
842	S2179	11093.5	374.5	16X73
843	S2178	11082.5	194.5	16X73
844	S2177	11071.5	284.5	16X73
845	S2176	11060.5	374.5	16X73
846	S2175	11049.5	194.5	16X73
847	S2174	11038.5	284.5	16X73
848	S2173	11027.5	374.5	16X73
849	S2172	11016.5	194.5	16X73
850	S2171	11005.5	284.5	16X73
851	S2170	10994.5	374.5	16X73
852	S2169	10983.5	194.5	16X73
853	S2168	10972.5	284.5	16X73
854	S2167	10961.5	374.5	16X73
855	S2166	10950.5	194.5	16X73
856	S2165	10939.5	284.5	16X73
857	S2164	10928.5	374.5	16X73
858	S2163	10917.5	194.5	16X73
859	S2162	10906.5	284.5	16X73
860	S2161	10895.5	374.5	16X73
861	S2160	10884.5	194.5	16X73
862	S2159	10873.5	284.5	16X73
863	S2158	10862.5	374.5	16X73
864	S2157	10851.5	194.5	16X73
865	S2156	10840.5	284.5	16X73
866	S2155	10829.5	374.5	16X73
867	S2154	10818.5	194.5	16X73
868	S2153	10807.5	284.5	16X73
869	S2152	10796.5	374.5	16X73
870	S2151	10785.5	194.5	16X73
871	S2150	10774.5	284.5	16X73
872	S2149	10763.5	374.5	16X73
873	S2148	10752.5	194.5	16X73
874	S2147	10741.5	284.5	16X73
875	S2146	10730.5	374.5	16X73
876	S2145	10719.5	194.5	16X73
877	S2144	10708.5	284.5	16X73
878	S2143	10697.5	374.5	16X73
879	S2142	10686.5	194.5	16X73
880	S2141	10675.5	284.5	16X73
881	S2140	10664.5	374.5	16X73
882	S2139	10653.5	194.5	16X73
883	S2138	10642.5	284.5	16X73
884	S2137	10631.5	374.5	16X73
885	S2136	10620.5	194.5	16X73
886	S2135	10609.5	284.5	16X73
887	S2134	10598.5	374.5	16X73
888	S2133	10587.5	194.5	16X73
889	S2132	10576.5	284.5	16X73
890	S2131	10565.5	374.5	16X73
891	S2130	10554.5	194.5	16X73
892	S2129	10543.5	284.5	16X73
893	S2128	10532.5	374.5	16X73
894	S2127	10521.5	194.5	16X73
895	S2126	10510.5	284.5	16X73
896	S2125	10499.5	374.5	16X73
897	S2124	10488.5	194.5	16X73
898	S2123	10477.5	284.5	16X73
899	S2122	10466.5	374.5	16X73
900	S2121	10455.5	194.5	16X73
901	S2120	10444.5	284.5	16X73
902	S2119	10433.5	374.5	16X73
903	S2118	10422.5	194.5	16X73
904	S2117	10411.5	284.5	16X73
905	S2116	10400.5	374.5	16X73
906	S2115	10389.5	194.5	16X73
907	S2114	10378.5	284.5	16X73
908	S2113	10367.5	374.5	16X73
909	S2112	10356.5	194.5	16X73
910	S2111	10345.5	284.5	16X73
911	S2110	10334.5	374.5	16X73
912	S2109	10323.5	194.5	16X73
913	S2108	10312.5	284.5	16X73
914	S2107	10301.5	374.5	16X73
915	S2106	10290.5	194.5	16X73
916	S2105	10279.5	284.5	16X73
917	S2104	10268.5	374.5	16X73
918	S2103	10257.5	194.5	16X73
919	S2102	10246.5	284.5	16X73
920	S2101	10235.5	374.5	16X73
921	S2100	10224.5	194.5	16X73
922	S2099	10213.5	284.5	16X73
923	S2098	10202.5	374.5	16X73
924	S2097	10191.5	194.5	16X73
925	S2096	10180.5	284.5	16X73
926	S2095	10169.5	374.5	16X73
927	S2094	10158.5	194.5	16X73
928	S2093	10147.5	284.5	16X73
929	S2092	10136.5	374.5	16X73
930	S2091	10125.5	194.5	16X73
931	S2090	10114.5	284.5	16X73
932	S2089	10103.5	374.5	16X73
933	S2088	10092.5	194.5	16X73
934	S2087	10081.5	284.5	16X73
935	S2086	10070.5	374.5	16X73
936	S2085	10059.5	194.5	16X73
937	S2084	10048.5	284.5	16X73
938	S2083	10037.5	374.5	16X73
939	S2082	10026.5	194.5	16X73
940	S2081	10015.5	284.5	16X73
941	S2080	10004.5	374.5	16X73
942	S2079	9993.5	194.5	16X73
943	S2078	9982.5	284.5	16X73
944	S2077	9971.5	374.5	16X73
945	S2076	9960.5	194.5	16X73
946	S2075	9949.5	284.5	16X73
947	S2074	9938.5	374.5	16X73
948	S2073	9927.5	194.5	16X73
949	S2072	9916.5	284.5	16X73
950	S2071	9905.5	374.5	16X73
951	S2070	9894.5	194.5	16X73
952	S2069	9883.5	284.5	16X73
953	S2068	9872.5	374.5	16X73
954	S2067	9861.5	194.5	16X73
955	S2066	9850.5	284.5	16X73
956	S2065	9839.5	374.5	16X73
957	S2064	9828.5	194.5	16X73
958	S2063	9817.5	284.5	16X73
959	S2062	9806.5	374.5	16X73
960	S2061	9795.5	194.5	16X73

No.	Name	X	Y	Bump size(μm)
961	S2060	9784.5	284.5	16X73
962	S2059	9773.5	374.5	16X73
963	S2058	9762.5	194.5	16X73
964	S2057	9751.5	284.5	16X73
965	S2056	9740.5	374.5	16X73
966	S2055	9729.5	194.5	16X73
967	S2054	9718.5	284.5	16X73
968	S2053	9707.5	374.5	16X73
969	S2052	9696.5	194.5	16X73
970	S2051	9685.5	284.5	16X73
971	S2050	9674.5	374.5	16X73
972	S2049	9663.5	194.5	16X73
973	S2048	9652.5	284.5	16X73
974	S2047	9641.5	374.5	16X73
975	S2046	9630.5	194.5	16X73
976	S2045	9619.5	284.5	16X73
977	S2044	9608.5	374.5	16X73
978	S2043	9597.5	194.5	16X73
979	S2042	9586.5	284.5	16X73
980	S2041	9575.5	374.5	16X73
981	S2040	9564.5	194.5	16X73
982	S2039	9553.5	284.5	16X73
983	S2038	9542.5	374.5	16X73
984	S2037	9531.5	194.5	16X73
985	S2036	9520.5	284.5	16X73
986	S2035	9509.5	374.5	16X73
987	S2034	9498.5	194.5	16X73
988	S2033	9487.5	284.5	16X73
989	S2032	9476.5	374.5	16X73
990	S2031	9465.5	194.5	16X73
991	S2030	9454.5	284.5	16X73
992	S2029	9443.5	374.5	16X73
993	S2028	9432.5	194.5	16X73
994	S2027	9421.5	284.5	16X73
995	S2026	9410.5	374.5	16X73
996	S2025	9399.5	194.5	16X73
997	S2024	9388.5	284.5	16X73
998	S2023	9377.5	374.5	16X73
999	S2022	9366.5	194.5	16X73
1000	S2021	9355.5	284.5	16X73
1001	S2020	9344.5	374.5	16X73
1002	S2019	9333.5	194.5	16X73
1003	S2018	9322.5	284.5	16X73
1004	S2017	9311.5	374.5	16X73
1005	S2016	9300.5	194.5	16X73
1006	S2015	9289.5	284.5	16X73
1007	S2014	9278.5	374.5	16X73
1008	S2013	9267.5	194.5	16X73
1009	S2012	9256.5	284.5	16X73
1010	S2011	9245.5	374.5	16X73
1011	S2010	9234.5	194.5	16X73
1012	S2009	9223.5	284.5	16X73
1013	S2008	9212.5	374.5	16X73
1014	S2007	9201.5	194.5	16X73
1015	S2006	9190.5	284.5	16X73
1016	S2005	9179.5	374.5	16X73
1017	S2004	9168.5	194.5	16X73
1018	S2003	9157.5	284.5	16X73
1019	S2002	9146.5	374.5	16X73
1020	S2001	9135.5	194.5	16X73
1021	S2000	9124.5	284.5	16X73
1022	S1999	9113.5	374.5	16X73
1023	S1998	9102.5	194.5	16X73
1024	S1997	9091.5	284.5	16X73
1025	S1996	9080.5	374.5	16X73
1026	S1995	9069.5	194.5	16X73
1027	S1994	9058.5	284.5	16X73
1028	S1993	9047.5	374.5	16X73
1029	S1992	9036.5	194.5	16X73
1030	S1991	9025.5	284.5	16X73
1031	S1990	9014.5	374.5	16X73
1032	S1989	9003.5	194.5	16X73
1033	S1988	8992.5	284.5	16X73
1034	S1987	8981.5	374.5	16X73
1035	S1986	8970.5	194.5	16X73
1036	S1985	8959.5	284.5	16X73
1037	S1984	8948.5	374.5	16X73
1038	S1983	8937.5	194.5	16X73
1039	S1982	8926.5	284.5	16X73
1040	S1981	8915.5	374.5	16X73
1041	S1980	8904.5	194.5	16X73
1042	S1979	8893.5	284.5	16X73
1043	S1978	8882.5	374.5	16X73
1044	S1977	8871.5	194.5	16X73
1045	S1976	8860.5	284.5	16X73
1046	S1975	8849.5	374.5	16X73
1047	S1974	8838.5	194.5	16X73
1048	S1973	8827.5	284.5	16X73
1049	S1972	8816.5	374.5	16X73
1050	S1971	8805.5	194.5	16X73
1051	S1970	8794.5	284.5	16X73
1052	S1969	8783.5	374.5	16X73
1053	S1968	8772.5	194.5	16X73
1054	S1967	8761.5	284.5	16X73
1055	S1966	8750.5	374.5	16X73
1056	S1965	8739.5	194.5	16X73
1057	S1964	8728.5	284.5	16X73
1058	S1963	8717.5	374.5	16X73
1059	S1962	8706.5	194.5	16X73
1060	S1961	8695.5	284.5	16X73
1061	S1960	8684.5	374.5	16X73
1062	S1959	8673.5	194.5	16X73
1063	S1958	8662.5	284.5	16X73
1064	S1957	8651.5	374.5	16X73
1065	S1956	8640.5	194.5	16X73
1066	S1955	8629.5	284.5	16X73
1067	S1954	8618.5	374.5	16X73
1068	S1953	8607.5	194.5	16X73
1069	S1952	8596.5	284.5	16X73
1070	S1951	8585.5	374.5	16X73
1071	S1950	8574.5	194.5	16X73
1072	S1949	8563.5	284.5	16X73
1073	S1948	8552.5	374.5	16X73
1074	S1947	8541.5	194.5	16X73
1075	S1946	8530.5	284.5	16X73
1076	S1945	8519.5	374.5	16X73
1077	S1944	8508.5	194.5	16X73
1078	S1943	8497.5	284.5	16X73
1079	S1942	8486.5	374.5	16X73
1080	S1941	8475.5	194.5	16X73
1081	S1940	8464.5	284.5	16X73
1082	S1939	8453.5	374.5	16X73
1083	S1938	8442.5	194.5	16X73
1084	S1937	8431.5	284.5	16X73
1085	S1936	8420.5	374.5	16X73
1086	S1935	8409.5	194.5	16X73
1087	S1934	8398.5	284.5	16X73
1088	S1933	8387.5	374.5	16X73
1089	S1932	8376.5	194.5	16X73
1090	S1931	8365.5	284.5	16X73
1091	S1930	8354.5	374.5	16X73
1092	S1929	8343.5	194.5	16X73
1093	S1928	8332.5	284.5	16X73
1094	S1927	8321.5	374.5	16X73
1095	S1926	8310.5	194.5	16X73
1096	S1925	8299.5	284.5	16X73
1097	S1924	8288.5	374.5	16X73
1098	S1923	8277.5	194.5	16X73
1099	S1922	8266.5	284.5	16X73
1100	S1921	8255.5	374.5	16X73
1101	S1920	8244.5	194.5	16X73
1102	S1919	8233.5	284.5	16X73
1103	S1918	8222.5	374.5	16X73
1104	S1917	8211.5	194.5	16X73
1105	S1916	8200.5	284.5	16X73
1106	S1915	8189.5	374.5	16X73
1107	S1914	8178.5	194.5	16X73
1108	S1913	8167.5	284.5	16X73
1109	S1912	8156.5	374.5	16X73
1110	S1911	8145.5	194.5	16X73
1111	S1910	8134.5	284.5	16X73
1112	S1909	8123.5	374.5	16X73
1113	S1908	8112.5	194.5	16X73
1114	S1907	8101.5	284.5	16X73
1115	S1906	8090.5	374.5	16X73
1116	S1905	8079.5	194.5	16X73
1117	S1904	8068.5	284.5	16X73
1118	S1903	8057.5	374.5	16X73
1119	S1902	8046.5	194.5	16X73
1120	S1901	8035.5	284.5	16X73
1121	S1900	8024.5	374.5	16X73
1122	S1899	8013.5	194.5	16X73
1123	S1898	8002.5	284.5	16X73
1124	S1897	7991.5	374.5	16X73
1125	S1896	7980.5	194.5	16X73
1126	S1895	7969.5	284.5	16X73
1127	S1894	7958.5	374.5	16X73
1128	S1893	7947.5	194.5	16X73
1129	S1892	7936.5	284.5	16X73
1130	S1891	7925.5	374.5	16X73
1131	S1890	7914.5	194.5	16X73
1132	S1889	7903.5	284.5	16X73
1133	S1888	7892.5	374.5	16X73
1134	S1887	7881.5	194.5	16X73
1135	S1886	7870.5	284.5	16X73
1136	S1885	7859.5	374.5	16X73
1137	S1884	7848.5	194.5	16X73
1138	S1883	7837.5	284.5	16X73
1139	S1882	7826.5	374.5	16X73
1140	S1881	7815.5	194.5	16X73
1141	S1880	7804.5	284.5	16X73
1142	S1879	7793.5	374.5	16X73
1143	S1878	7782.5	194.5	16X73
1144	S1877	7771.5	284.5	16X73
1145	S1876	7760.5	374.5	16X73
1146	S1875	7749.5	194.5	16X73
1147	S1874	7738.5	284.5	16X73
1148	S1873	7727.5	374.5	16X73
1149	S1872	7716.5	194.5	16X73
1150	S1871	7705.5	284.5	16X73
1151	S1870	7694.5	374.5	16X73
1152	S1869	7683.5	194.5	16X73
1153	S1868	7672.5	284.5	16X73
1154	S1867	7661.5	374.5	16X73
1155	S1866	7650.5	194.5	16X73
1156	S1865	7639.5	284.5	16X73
1157	S1864	7628.5	374.5	16X73
1158	S1863	7617.5	194.5	16X73
1159	S1862	7606.5	284.5	16X73
1160	S1861	7595.5	374.5	16X73
1161	S1860	7584.5	194.5	16X73
1162	S1859	7573.5	284.5	16X73
1163	S1858	7562.5	374.5	16X73
1164	S1857	7551.5	194.5	16X73
1165	S1856	7540.5	284.5	16X73
1166	S1855	7529.5	374.5	16X73
1167	S1854	7518.5	194.5	16X73
1168	S1853	7507.5	284.5	16X73
1169	S1852	7496.5	374.5	16X73
1170	S1851	7485.5	194.5	16X73
1171	S1850	7474.5	284.5	16X73
1172	S1849	7463.5	374.5	16X73
1173	S1848	7452.5	194.5	16X73
1174	S1847	7441.5	284.5	16X73
1175	S1846	7430.5	374.5	16X73
1176	S1845	7419.5	194.5	16X73
1177	S1844	7408.5	284.5	16X73
1178	S1843	7397.5	374.5	16X73
1179	S1842	7386.5	194.5	16X73
1180	S1841	7375.5	284.5	16X73
1181	S1840	7364.5	374.5	16X73
1182	S1839	7353.5	194.5	16X73
1183	S1838	7342.5	284.5	16X73
1184	S1837	7331.5	374.5	16X73
1185	S1836	7320.5	194.5	16X73
1186	S1835	7309.5	284.5	16X73
1187	S1834	7298.5	374.5	16X73
1188	S1833	7287.5	194.5	16X73
1189	S1832	7276.5	284.5	16X73
1190	S1831	7265.5	374.5	16X73
1191	S1830	7254.5	194.5	16X73
1192	S1829	7243.5	284.5	16X73
1193	S1828	7232.5	374.5	16X73
1194	S1827	7221.5	194.5	16X73
1195	S1826	7210.5	284.5	16X73
1196	S1825	7199.5	374.5	16X73
1197	S1824	7188.5	194.5	16X73
1198	S1823	7177.5	284.5	16X73
1199	S1822	7166.5	374.5	16X73
1200	S1821	7155.5	194.5	16X73

No.	Name	X	Y	Bump size(μm)
1201	S1820	7144.5	284.5	16X73
1202	S1819	7133.5	374.5	16X73
1203	S1818	7122.5	194.5	16X73
1204	S1817	7111.5	284.5	16X73
1205	S1816	7100.5	374.5	16X73
1206	S1815	7089.5	194.5	16X73
1207	S1814	7078.5	284.5	16X73
1208	S1813	7067.5	374.5	16X73
1209	S1812	7056.5	194.5	16X73
1210	S1811	7045.5	284.5	16X73
1211	S1810	7034.5	374.5	16X73
1212	S1809	7023.5	194.5	16X73
1213	S1808	7012.5	284.5	16X73
1214	S1807	7001.5	374.5	16X73
1215	S1806	6990.5	194.5	16X73
1216	S1805	6979.5	284.5	16X73
1217	S1804	6968.5	374.5	16X73
1218	S1803	6957.5	194.5	16X73
1219	S1802	6946.5	284.5	16X73
1220	S1801	6935.5	374.5	16X73
1221	DUMMY	6924.5	194.5	16X73
1222	DUMMY	6913.5	284.5	16X73
1223	DUMMY	6902.5	374.5	16X73
1224	DUMMY	6891.5	194.5	16X73
1225	DUMMY	6880.5	284.5	16X73
1226	DUMMY	6869.5	374.5	16X73
1227	DUMMY	6858.5	194.5	16X73
1228	DUMMY	6847.5	284.5	16X73
1229	DUMMY	6836.5	374.5	16X73
1230	DUMMY	6825.5	194.5	16X73
1231	DUMMY	6814.5	284.5	16X73
1232	DUMMY	6803.5	374.5	16X73
1233	DUMMY	6792.5	194.5	16X73
1234	DUMMY	6781.5	284.5	16X73
1235	DUMMY	6770.5	374.5	16X73
1236	DUMMY	6759.5	194.5	16X73
1237	DUMMY	6748.5	284.5	16X73
1238	DUMMY	6737.5	374.5	16X73
1239	S1800	6726.5	194.5	16X73
1240	S1799	6715.5	284.5	16X73
1241	S1798	6704.5	374.5	16X73
1242	S1797	6693.5	194.5	16X73
1243	S1796	6682.5	284.5	16X73
1244	S1795	6671.5	374.5	16X73
1245	S1794	6660.5	194.5	16X73
1246	S1793	6649.5	284.5	16X73
1247	S1792	6638.5	374.5	16X73
1248	S1791	6627.5	194.5	16X73
1249	S1790	6616.5	284.5	16X73
1250	S1789	6605.5	374.5	16X73
1251	S1788	6594.5	194.5	16X73
1252	S1787	6583.5	284.5	16X73
1253	S1786	6572.5	374.5	16X73
1254	S1785	6561.5	194.5	16X73
1255	S1784	6550.5	284.5	16X73
1256	S1783	6539.5	374.5	16X73
1257	S1782	6528.5	194.5	16X73
1258	S1781	6517.5	284.5	16X73
1259	S1780	6506.5	374.5	16X73
1260	S1779	6495.5	194.5	16X73
1261	S1778	6484.5	284.5	16X73
1262	S1777	6473.5	374.5	16X73
1263	S1776	6462.5	194.5	16X73
1264	S1775	6451.5	284.5	16X73
1265	S1774	6440.5	374.5	16X73
1266	S1773	6429.5	194.5	16X73
1267	S1772	6418.5	284.5	16X73
1268	S1771	6407.5	374.5	16X73
1269	S1770	6396.5	194.5	16X73
1270	S1769	6385.5	284.5	16X73
1271	S1768	6374.5	374.5	16X73
1272	S1767	6363.5	194.5	16X73
1273	S1766	6352.5	284.5	16X73
1274	S1765	6341.5	374.5	16X73
1275	S1764	6330.5	194.5	16X73
1276	S1763	6319.5	284.5	16X73
1277	S1762	6308.5	374.5	16X73
1278	S1761	6297.5	194.5	16X73
1279	S1760	6286.5	284.5	16X73
1280	S1759	6275.5	374.5	16X73
1281	S1758	6264.5	194.5	16X73
1282	S1757	6253.5	284.5	16X73
1283	S1756	6242.5	374.5	16X73
1284	S1755	6231.5	194.5	16X73
1285	S1754	6220.5	284.5	16X73
1286	S1753	6209.5	374.5	16X73
1287	S1752	6198.5	194.5	16X73
1288	S1751	6187.5	284.5	16X73
1289	S1750	6176.5	374.5	16X73
1290	S1749	6165.5	194.5	16X73
1291	S1748	6154.5	284.5	16X73
1292	S1747	6143.5	374.5	16X73
1293	S1746	6132.5	194.5	16X73
1294	S1745	6121.5	284.5	16X73
1295	S1744	6110.5	374.5	16X73
1296	S1743	6099.5	194.5	16X73
1297	S1742	6088.5	284.5	16X73
1298	S1741	6077.5	374.5	16X73
1299	S1740	6066.5	194.5	16X73
1300	S1739	6055.5	284.5	16X73
1301	S1738	6044.5	374.5	16X73
1302	S1737	6033.5	194.5	16X73
1303	S1736	6022.5	284.5	16X73
1304	S1735	6011.5	374.5	16X73
1305	S1734	6000.5	194.5	16X73
1306	S1733	5989.5	284.5	16X73
1307	S1732	5978.5	374.5	16X73
1308	S1731	5967.5	194.5	16X73
1309	S1730	5956.5	284.5	16X73
1310	S1729	5945.5	374.5	16X73
1311	S1728	5934.5	194.5	16X73
1312	S1727	5923.5	284.5	16X73
1313	S1726	5912.5	374.5	16X73
1314	S1725	5901.5	194.5	16X73
1315	S1724	5890.5	284.5	16X73
1316	S1723	5879.5	374.5	16X73
1317	S1722	5868.5	194.5	16X73
1318	S1721	5857.5	284.5	16X73
1319	S1720	5846.5	374.5	16X73
1320	S1719	5835.5	194.5	16X73
1321	S1718	5824.5	284.5	16X73
1322	S1717	5813.5	374.5	16X73
1323	S1716	5802.5	194.5	16X73
1324	S1715	5791.5	284.5	16X73
1325	S1714	5780.5	374.5	16X73
1326	S1713	5769.5	194.5	16X73
1327	S1712	5758.5	284.5	16X73
1328	S1711	5747.5	374.5	16X73
1329	S1710	5736.5	194.5	16X73
1330	S1709	5725.5	284.5	16X73
1331	S1708	5714.5	374.5	16X73
1332	S1707	5703.5	194.5	16X73
1333	S1706	5692.5	284.5	16X73
1334	S1705	5681.5	374.5	16X73
1335	S1704	5670.5	194.5	16X73
1336	S1703	5659.5	284.5	16X73
1337	S1702	5648.5	374.5	16X73
1338	S1701	5637.5	194.5	16X73
1339	S1700	5626.5	284.5	16X73
1340	S1699	5615.5	374.5	16X73
1341	S1698	5604.5	194.5	16X73
1342	S1697	5593.5	284.5	16X73
1343	S1696	5582.5	374.5	16X73
1344	S1695	5571.5	194.5	16X73
1345	S1694	5560.5	284.5	16X73
1346	S1693	5549.5	374.5	16X73
1347	S1692	5538.5	194.5	16X73
1348	S1691	5527.5	284.5	16X73
1349	S1690	5516.5	374.5	16X73
1350	S1689	5505.5	194.5	16X73
1351	S1688	5494.5	284.5	16X73
1352	S1687	5483.5	374.5	16X73
1353	S1686	5472.5	194.5	16X73
1354	S1685	5461.5	284.5	16X73
1355	S1684	5450.5	374.5	16X73
1356	S1683	5439.5	194.5	16X73
1357	S1682	5428.5	284.5	16X73
1358	S1681	5417.5	374.5	16X73
1359	S1680	5406.5	194.5	16X73
1360	S1679	5395.5	284.5	16X73
1361	S1678	5384.5	374.5	16X73
1362	S1677	5373.5	194.5	16X73
1363	S1676	5362.5	284.5	16X73
1364	S1675	5351.5	374.5	16X73
1365	S1674	5340.5	194.5	16X73
1366	S1673	5329.5	284.5	16X73
1367	S1672	5318.5	374.5	16X73
1368	S1671	5307.5	194.5	16X73
1369	S1670	5296.5	284.5	16X73
1370	S1669	5285.5	374.5	16X73
1371	S1668	5274.5	194.5	16X73
1372	S1667	5263.5	284.5	16X73
1373	S1666	5252.5	374.5	16X73
1374	S1665	5241.5	194.5	16X73
1375	S1664	5230.5	284.5	16X73
1376	S1663	5219.5	374.5	16X73
1377	S1662	5208.5	194.5	16X73
1378	S1661	5197.5	284.5	16X73
1379	S1660	5186.5	374.5	16X73
1380	S1659	5175.5	194.5	16X73
1381	S1658	5164.5	284.5	16X73
1382	S1657	5153.5	374.5	16X73
1383	S1656	5142.5	194.5	16X73
1384	S1655	5131.5	284.5	16X73
1385	S1654	5120.5	374.5	16X73
1386	S1653	5109.5	194.5	16X73
1387	S1652	5098.5	284.5	16X73
1388	S1651	5087.5	374.5	16X73
1389	S1650	5076.5	194.5	16X73
1390	S1649	5065.5	284.5	16X73
1391	S1648	5054.5	374.5	16X73
1392	S1647	5043.5	194.5	16X73
1393	S1646	5032.5	284.5	16X73
1394	S1645	5021.5	374.5	16X73
1395	S1644	5010.5	194.5	16X73
1396	S1643	4999.5	284.5	16X73
1397	S1642	4988.5	374.5	16X73
1398	S1641	4977.5	194.5	16X73
1399	S1640	4966.5	284.5	16X73
1400	S1639	4955.5	374.5	16X73
1401	S1638	4944.5	194.5	16X73
1402	S1637	4933.5	284.5	16X73
1403	S1636	4922.5	374.5	16X73
1404	S1635	4911.5	194.5	16X73
1405	S1634	4900.5	284.5	16X73
1406	S1633	4889.5	374.5	16X73
1407	S1632	4878.5	194.5	16X73
1408	S1631	4867.5	284.5	16X73
1409	S1630	4856.5	374.5	16X73
1410	S1629	4845.5	194.5	16X73
1411	S1628	4834.5	284.5	16X73
1412	S1627	4823.5	374.5	16X73
1413	S1626	4812.5	194.5	16X73
1414	S1625	4801.5	284.5	16X73
1415	S1624	4790.5	374.5	16X73
1416	S1623	4779.5	194.5	16X73
1417	S1622	4768.5	284.5	16X73
1418	S1621	4757.5	374.5	16X73
1419	S1620	4746.5	194.5	16X73
1420	S1619	4735.5	284.5	16X73
1421	S1618	4724.5	374.5	16X73
1422	S1617	4713.5	194.5	16X73
1423	S1616	4702.5	284.5	16X73
1424	S1615	4691.5	374.5	16X73
1425	S1614	4680.5	194.5	16X73
1426	S1613	4669.5	284.5	16X73
1427	S1612	4658.5	374.5	16X73
1428	S1611	4647.5	194.5	16X73
1429	S1610	4636.5	284.5	16X73
1430	S1609	4625.5	374.5	16X73
1431	S1608	4614.5	194.5	16X73
1432	S1607	4603.5	284.5	16X73
1433	S1606	4592.5	374.5	16X73
1434	S1605	4581.5	194.5	16X73
1435	S1604	4570.5	284.5	16X73
1436	S1603	4559.5	374.5	16X73
1437	S1602	4548.5	194.5	16X73
1438	S1601	4537.5	284.5	16X73
1439	S1600	4526.5	374.5	16X73
1440	S1599	4515.5	194.5	16X73

No.	Name	X	Y	Bump size(μm)
1441	S1598	4504.5	284.5	16X73
1442	S1597	4493.5	374.5	16X73
1443	S1596	4482.5	194.5	16X73
1444	S1595	4471.5	284.5	16X73
1445	S1594	4460.5	374.5	16X73
1446	S1593	4449.5	194.5	16X73
1447	S1592	4438.5	284.5	16X73
1448	S1591	4427.5	374.5	16X73
1449	S1590	4416.5	194.5	16X73
1450	S1589	4405.5	284.5	16X73
1451	S1588	4394.5	374.5	16X73
1452	S1587	4383.5	194.5	16X73
1453	S1586	4372.5	284.5	16X73
1454	S1585	4361.5	374.5	16X73
1455	S1584	4350.5	194.5	16X73
1456	S1583	4339.5	284.5	16X73
1457	S1582	4328.5	374.5	16X73
1458	S1581	4317.5	194.5	16X73
1459	S1580	4306.5	284.5	16X73
1460	S1579	4295.5	374.5	16X73
1461	S1578	4284.5	194.5	16X73
1462	S1577	4273.5	284.5	16X73
1463	S1576	4262.5	374.5	16X73
1464	S1575	4251.5	194.5	16X73
1465	S1574	4240.5	284.5	16X73
1466	S1573	4229.5	374.5	16X73
1467	S1572	4218.5	194.5	16X73
1468	S1571	4207.5	284.5	16X73
1469	S1570	4196.5	374.5	16X73
1470	S1569	4185.5	194.5	16X73
1471	S1568	4174.5	284.5	16X73
1472	S1567	4163.5	374.5	16X73
1473	S1566	4152.5	194.5	16X73
1474	S1565	4141.5	284.5	16X73
1475	S1564	4130.5	374.5	16X73
1476	S1563	4119.5	194.5	16X73
1477	S1562	4108.5	284.5	16X73
1478	S1561	4097.5	374.5	16X73
1479	S1560	4086.5	194.5	16X73
1480	S1559	4075.5	284.5	16X73
1481	S1558	4064.5	374.5	16X73
1482	S1557	4053.5	194.5	16X73
1483	S1556	4042.5	284.5	16X73
1484	S1555	4031.5	374.5	16X73
1485	S1554	4020.5	194.5	16X73
1486	S1553	4009.5	284.5	16X73
1487	S1552	3998.5	374.5	16X73
1488	S1551	3987.5	194.5	16X73
1489	S1550	3976.5	284.5	16X73
1490	S1549	3965.5	374.5	16X73
1491	S1548	3954.5	194.5	16X73
1492	S1547	3943.5	284.5	16X73
1493	S1546	3932.5	374.5	16X73
1494	S1545	3921.5	194.5	16X73
1495	S1544	3910.5	284.5	16X73
1496	S1543	3899.5	374.5	16X73
1497	S1542	3888.5	194.5	16X73
1498	S1541	3877.5	284.5	16X73
1499	S1540	3866.5	374.5	16X73
1500	S1539	3855.5	194.5	16X73
1501	S1538	3844.5	284.5	16X73
1502	S1537	3833.5	374.5	16X73
1503	S1536	3822.5	194.5	16X73
1504	S1535	3811.5	284.5	16X73
1505	S1534	3800.5	374.5	16X73
1506	S1533	3789.5	194.5	16X73
1507	S1532	3778.5	284.5	16X73
1508	S1531	3767.5	374.5	16X73
1509	S1530	3756.5	194.5	16X73
1510	S1529	3745.5	284.5	16X73
1511	S1528	3734.5	374.5	16X73
1512	S1527	3723.5	194.5	16X73
1513	S1526	3712.5	284.5	16X73
1514	S1525	3701.5	374.5	16X73
1515	S1524	3690.5	194.5	16X73
1516	S1523	3679.5	284.5	16X73
1517	S1522	3668.5	374.5	16X73
1518	S1521	3657.5	194.5	16X73
1519	S1520	3646.5	284.5	16X73
1520	S1519	3635.5	374.5	16X73
1521	S1518	3624.5	194.5	16X73
1522	S1517	3613.5	284.5	16X73
1523	S1516	3602.5	374.5	16X73
1524	S1515	3591.5	194.5	16X73
1525	S1514	3580.5	284.5	16X73
1526	S1513	3569.5	374.5	16X73
1527	S1512	3558.5	194.5	16X73
1528	S1511	3547.5	284.5	16X73
1529	S1510	3536.5	374.5	16X73
1530	S1509	3525.5	194.5	16X73
1531	S1508	3514.5	284.5	16X73
1532	S1507	3503.5	374.5	16X73
1533	S1506	3492.5	194.5	16X73
1534	S1505	3481.5	284.5	16X73
1535	S1504	3470.5	374.5	16X73
1536	S1503	3459.5	194.5	16X73
1537	S1502	3448.5	284.5	16X73
1538	S1501	3437.5	374.5	16X73
1539	S1500	3426.5	194.5	16X73
1540	S1499	3415.5	284.5	16X73
1541	S1498	3404.5	374.5	16X73
1542	S1497	3393.5	194.5	16X73
1543	S1496	3382.5	284.5	16X73
1544	S1495	3371.5	374.5	16X73
1545	S1494	3360.5	194.5	16X73
1546	S1493	3349.5	284.5	16X73
1547	S1492	3338.5	374.5	16X73
1548	S1491	3327.5	194.5	16X73
1549	S1490	3316.5	284.5	16X73
1550	S1489	3305.5	374.5	16X73
1551	S1488	3294.5	194.5	16X73
1552	S1487	3283.5	284.5	16X73
1553	S1486	3272.5	374.5	16X73
1554	S1485	3261.5	194.5	16X73
1555	S1484	3250.5	284.5	16X73
1556	S1483	3239.5	374.5	16X73
1557	S1482	3228.5	194.5	16X73
1558	S1481	3217.5	284.5	16X73
1559	S1480	3206.5	374.5	16X73
1560	S1479	3195.5	194.5	16X73
1561	S1478	3184.5	284.5	16X73
1562	S1477	3173.5	374.5	16X73
1563	S1476	3162.5	194.5	16X73
1564	S1475	3151.5	284.5	16X73
1565	S1474	3140.5	374.5	16X73
1566	S1473	3129.5	194.5	16X73
1567	S1472	3118.5	284.5	16X73
1568	S1471	3107.5	374.5	16X73
1569	S1470	3096.5	194.5	16X73
1570	S1469	3085.5	284.5	16X73
1571	S1468	3074.5	374.5	16X73
1572	S1467	3063.5	194.5	16X73
1573	S1466	3052.5	284.5	16X73
1574	S1465	3041.5	374.5	16X73
1575	S1464	3030.5	194.5	16X73
1576	S1463	3019.5	284.5	16X73
1577	S1462	3008.5	374.5	16X73
1578	S1461	2997.5	194.5	16X73
1579	S1460	2986.5	284.5	16X73
1580	S1459	2975.5	374.5	16X73
1581	S1458	2964.5	194.5	16X73
1582	S1457	2953.5	284.5	16X73
1583	S1456	2942.5	374.5	16X73
1584	S1455	2931.5	194.5	16X73
1585	S1454	2920.5	284.5	16X73
1586	S1453	2909.5	374.5	16X73
1587	S1452	2898.5	194.5	16X73
1588	S1451	2887.5	284.5	16X73
1589	S1450	2876.5	374.5	16X73
1590	S1449	2865.5	194.5	16X73
1591	S1448	2854.5	284.5	16X73
1592	S1447	2843.5	374.5	16X73
1593	S1446	2832.5	194.5	16X73
1594	S1445	2821.5	284.5	16X73
1595	S1444	2810.5	374.5	16X73
1596	S1443	2799.5	194.5	16X73
1597	S1442	2788.5	284.5	16X73
1598	S1441	2777.5	374.5	16X73
1599	S1440	2766.5	194.5	16X73
1600	S1439	2755.5	284.5	16X73
1601	S1438	2744.5	374.5	16X73
1602	S1437	2733.5	194.5	16X73
1603	S1436	2722.5	284.5	16X73
1604	S1435	2711.5	374.5	16X73
1605	S1434	2700.5	194.5	16X73
1606	S1433	2689.5	284.5	16X73
1607	S1432	2678.5	374.5	16X73
1608	S1431	2667.5	194.5	16X73
1609	S1430	2656.5	284.5	16X73
1610	S1429	2645.5	374.5	16X73
1611	S1428	2634.5	194.5	16X73
1612	S1427	2623.5	284.5	16X73
1613	S1426	2612.5	374.5	16X73
1614	S1425	2601.5	194.5	16X73
1615	S1424	2590.5	284.5	16X73
1616	S1423	2579.5	374.5	16X73
1617	S1422	2568.5	194.5	16X73
1618	S1421	2557.5	284.5	16X73
1619	S1420	2546.5	374.5	16X73
1620	S1419	2535.5	194.5	16X73
1621	S1418	2524.5	284.5	16X73
1622	S1417	2513.5	374.5	16X73
1623	S1416	2502.5	194.5	16X73
1624	S1415	2491.5	284.5	16X73
1625	S1414	2480.5	374.5	16X73
1626	S1413	2469.5	194.5	16X73
1627	S1412	2458.5	284.5	16X73
1628	S1411	2447.5	374.5	16X73
1629	S1410	2436.5	194.5	16X73
1630	S1409	2425.5	284.5	16X73
1631	S1408	2414.5	374.5	16X73
1632	S1407	2403.5	194.5	16X73
1633	S1406	2392.5	284.5	16X73
1634	S1405	2381.5	374.5	16X73
1635	S1404	2370.5	194.5	16X73
1636	S1403	2359.5	284.5	16X73
1637	S1402	2348.5	374.5	16X73
1638	S1401	2337.5	194.5	16X73
1639	S1400	2326.5	284.5	16X73
1640	S1399	2315.5	374.5	16X73
1641	S1398	2304.5	194.5	16X73
1642	S1397	2293.5	284.5	16X73
1643	S1396	2282.5	374.5	16X73
1644	S1395	2271.5	194.5	16X73
1645	S1394	2260.5	284.5	16X73
1646	S1393	2249.5	374.5	16X73
1647	S1392	2238.5	194.5	16X73
1648	S1391	2227.5	284.5	16X73
1649	S1390	2216.5	374.5	16X73
1650	S1389	2205.5	194.5	16X73
1651	S1388	2194.5	284.5	16X73
1652	S1387	2183.5	374.5	16X73
1653	S1386	2172.5	194.5	16X73
1654	S1385	2161.5	284.5	16X73
1655	S1384	2150.5	374.5	16X73
1656	S1383	2139.5	194.5	16X73
1657	S1382	2128.5	284.5	16X73
1658	S1381	2117.5	374.5	16X73
1659	S1380	2106.5	194.5	16X73
1660	S1379	2095.5	284.5	16X73
1661	S1378	2084.5	374.5	16X73
1662	S1377	2073.5	194.5	16X73
1663	S1376	2062.5	284.5	16X73
1664	S1375	2051.5	374.5	16X73
1665	S1374	2040.5	194.5	16X73
1666	S1373	2029.5	284.5	16X73
1667	S1372	2018.5	374.5	16X73
1668	S1371	2007.5	194.5	16X73
1669	S1370	1996.5	284.5	16X73
1670	S1369	1985.5	374.5	16X73
1671	S1368	1974.5	194.5	16X73
1672	S1367	1963.5	284.5	16X73
1673	S1366	1952.5	374.5	16X73
1674	S1365	1941.5	194.5	16X73
1675	S1364	1930.5	284.5	16X73
1676	S1363	1919.5	374.5	16X73
1677	S1362	1908.5	194.5	16X73
1678	S1361	1897.5	284.5	16X73
1679	S1360	1886.5	374.5	16X73
1680	S1359	1875.5	194.5	16X73

No.	Name	X	Y	Bump size(μm)
1681	S1358	1864.5	284.5	16X73
1682	S1357	1853.5	374.5	16X73
1683	S1356	1842.5	194.5	16X73
1684	S1355	1831.5	284.5	16X73
1685	S1354	1820.5	374.5	16X73
1686	S1353	1809.5	194.5	16X73
1687	S1352	1798.5	284.5	16X73
1688	S1351	1787.5	374.5	16X73
1689	S1350	1776.5	194.5	16X73
1690	S1349	1765.5	284.5	16X73
1691	S1348	1754.5	374.5	16X73
1692	S1347	1743.5	194.5	16X73
1693	S1346	1732.5	284.5	16X73
1694	S1345	1721.5	374.5	16X73
1695	S1344	1710.5	194.5	16X73
1696	S1343	1699.5	284.5	16X73
1697	S1342	1688.5	374.5	16X73
1698	S1341	1677.5	194.5	16X73
1699	S1340	1666.5	284.5	16X73
1700	S1339	1655.5	374.5	16X73
1701	S1338	1644.5	194.5	16X73
1702	S1337	1633.5	284.5	16X73
1703	S1336	1622.5	374.5	16X73
1704	S1335	1611.5	194.5	16X73
1705	S1334	1600.5	284.5	16X73
1706	S1333	1589.5	374.5	16X73
1707	S1332	1578.5	194.5	16X73
1708	S1331	1567.5	284.5	16X73
1709	S1330	1556.5	374.5	16X73
1710	S1329	1545.5	194.5	16X73
1711	S1328	1534.5	284.5	16X73
1712	S1327	1523.5	374.5	16X73
1713	S1326	1512.5	194.5	16X73
1714	S1325	1501.5	284.5	16X73
1715	S1324	1490.5	374.5	16X73
1716	S1323	1479.5	194.5	16X73
1717	S1322	1468.5	284.5	16X73
1718	S1321	1457.5	374.5	16X73
1719	S1320	1446.5	194.5	16X73
1720	S1319	1435.5	284.5	16X73
1721	S1318	1424.5	374.5	16X73
1722	S1317	1413.5	194.5	16X73
1723	S1316	1402.5	284.5	16X73
1724	S1315	1391.5	374.5	16X73
1725	S1314	1380.5	194.5	16X73
1726	S1313	1369.5	284.5	16X73
1727	S1312	1358.5	374.5	16X73
1728	S1311	1347.5	194.5	16X73
1729	S1310	1336.5	284.5	16X73
1730	S1309	1325.5	374.5	16X73
1731	S1308	1314.5	194.5	16X73
1732	S1307	1303.5	284.5	16X73
1733	S1306	1292.5	374.5	16X73
1734	S1305	1281.5	194.5	16X73
1735	S1304	1270.5	284.5	16X73
1736	S1303	1259.5	374.5	16X73
1737	S1302	1248.5	194.5	16X73
1738	S1301	1237.5	284.5	16X73
1739	S1300	1226.5	374.5	16X73
1740	S1299	1215.5	194.5	16X73
1741	S1298	1204.5	284.5	16X73
1742	S1297	1193.5	374.5	16X73
1743	S1296	1182.5	194.5	16X73
1744	S1295	1171.5	284.5	16X73
1745	S1294	1160.5	374.5	16X73
1746	S1293	1149.5	194.5	16X73
1747	S1292	1138.5	284.5	16X73
1748	S1291	1127.5	374.5	16X73
1749	S1290	1116.5	194.5	16X73
1750	S1289	1105.5	284.5	16X73
1751	S1288	1094.5	374.5	16X73
1752	S1287	1083.5	194.5	16X73
1753	S1286	1072.5	284.5	16X73
1754	S1285	1061.5	374.5	16X73
1755	S1284	1050.5	194.5	16X73
1756	S1283	1039.5	284.5	16X73
1757	S1282	1028.5	374.5	16X73
1758	S1281	1017.5	194.5	16X73
1759	S1280	1006.5	284.5	16X73
1760	S1279	995.5	374.5	16X73
1761	S1278	984.5	194.5	16X73
1762	S1277	973.5	284.5	16X73
1763	S1276	962.5	374.5	16X73
1764	S1275	951.5	194.5	16X73
1765	S1274	940.5	284.5	16X73
1766	S1273	929.5	374.5	16X73
1767	S1272	918.5	194.5	16X73
1768	S1271	907.5	284.5	16X73
1769	S1270	896.5	374.5	16X73
1770	S1269	885.5	194.5	16X73
1771	S1268	874.5	284.5	16X73
1772	S1267	863.5	374.5	16X73
1773	S1266	852.5	194.5	16X73
1774	S1265	841.5	284.5	16X73
1775	S1264	830.5	374.5	16X73
1776	S1263	819.5	194.5	16X73
1777	S1262	808.5	284.5	16X73
1778	S1261	797.5	374.5	16X73
1779	S1260	786.5	194.5	16X73
1780	S1259	775.5	284.5	16X73
1781	S1258	764.5	374.5	16X73
1782	S1257	753.5	194.5	16X73
1783	S1256	742.5	284.5	16X73
1784	S1255	731.5	374.5	16X73
1785	S1254	720.5	194.5	16X73
1786	S1253	709.5	284.5	16X73
1787	S1252	698.5	374.5	16X73
1788	S1251	687.5	194.5	16X73
1789	S1250	676.5	284.5	16X73
1790	S1249	665.5	374.5	16X73
1791	S1248	654.5	194.5	16X73
1792	S1247	643.5	284.5	16X73
1793	S1246	632.5	374.5	16X73
1794	S1245	621.5	194.5	16X73
1795	S1244	610.5	284.5	16X73
1796	S1243	599.5	374.5	16X73
1797	S1242	588.5	194.5	16X73
1798	S1241	577.5	284.5	16X73
1799	S1240	566.5	374.5	16X73
1800	S1239	555.5	194.5	16X73
1801	S1238	544.5	284.5	16X73
1802	S1237	533.5	374.5	16X73
1803	S1236	522.5	194.5	16X73
1804	S1235	511.5	284.5	16X73
1805	S1234	500.5	374.5	16X73
1806	S1233	489.5	194.5	16X73
1807	S1232	478.5	284.5	16X73
1808	S1231	467.5	374.5	16X73
1809	S1230	456.5	194.5	16X73
1810	S1229	445.5	284.5	16X73
1811	S1228	434.5	374.5	16X73
1812	S1227	423.5	194.5	16X73
1813	S1226	412.5	284.5	16X73
1814	S1225	401.5	374.5	16X73
1815	S1224	390.5	194.5	16X73
1816	S1223	379.5	284.5	16X73
1817	S1222	368.5	374.5	16X73
1818	S1221	357.5	194.5	16X73
1819	S1220	346.5	284.5	16X73
1820	S1219	335.5	374.5	16X73
1821	S1218	324.5	194.5	16X73
1822	S1217	313.5	284.5	16X73
1823	S1216	302.5	374.5	16X73
1824	S1215	291.5	194.5	16X73
1825	S1214	280.5	284.5	16X73
1826	S1213	269.5	374.5	16X73
1827	S1212	258.5	194.5	16X73
1828	S1211	247.5	284.5	16X73
1829	S1210	236.5	374.5	16X73
1830	S1209	225.5	194.5	16X73
1831	S1208	214.5	284.5	16X73
1832	S1207	203.5	374.5	16X73
1833	S1206	192.5	194.5	16X73
1834	S1205	181.5	284.5	16X73
1835	S1204	170.5	374.5	16X73
1836	S1203	159.5	194.5	16X73
1837	S1202	148.5	284.5	16X73
1838	S1201	137.5	374.5	16X73
1839	DUMMY	126.5	194.5	16X73
1840	DUMMY	115.5	284.5	16X73
1841	DUMMY	104.5	374.5	16X73
1842	DUMMY	93.5	194.5	16X73
1843	DUMMY	82.5	284.5	16X73
1844	DUMMY	71.5	374.5	16X73
1845	DUMMY	60.5	194.5	16X73
1846	DUMMY	49.5	284.5	16X73
1847	DUMMY	38.5	374.5	16X73
1848	DUMMY	27.5	194.5	16X73
1849	DUMMY	16.5	284.5	16X73
1850	DUMMY	5.5	374.5	16X73
1851	DUMMY	-5.5	194.5	16X73
1852	DUMMY	-16.5	284.5	16X73
1853	DUMMY	-27.5	374.5	16X73
1854	DUMMY	-38.5	194.5	16X73
1855	DUMMY	-49.5	284.5	16X73
1856	DUMMY	-60.5	374.5	16X73
1857	DUMMY	-71.5	194.5	16X73
1858	DUMMY	-82.5	284.5	16X73
1859	DUMMY	-93.5	374.5	16X73
1860	DUMMY	-104.5	194.5	16X73
1861	DUMMY	-115.5	284.5	16X73
1862	DUMMY	-126.5	374.5	16X73
1863	S1200	-137.5	194.5	16X73
1864	S1199	-148.5	284.5	16X73
1865	S1198	-159.5	374.5	16X73
1866	S1197	-170.5	194.5	16X73
1867	S1196	-181.5	284.5	16X73
1868	S1195	-192.5	374.5	16X73
1869	S1194	-203.5	194.5	16X73
1870	S1193	-214.5	284.5	16X73
1871	S1192	-225.5	374.5	16X73
1872	S1191	-236.5	194.5	16X73
1873	S1190	-247.5	284.5	16X73
1874	S1189	-258.5	374.5	16X73
1875	S1188	-269.5	194.5	16X73
1876	S1187	-280.5	284.5	16X73
1877	S1186	-291.5	374.5	16X73
1878	S1185	-302.5	194.5	16X73
1879	S1184	-313.5	284.5	16X73
1880	S1183	-324.5	374.5	16X73
1881	S1182	-335.5	194.5	16X73
1882	S1181	-346.5	284.5	16X73
1883	S1180	-357.5	374.5	16X73
1884	S1179	-368.5	194.5	16X73
1885	S1178	-379.5	284.5	16X73
1886	S1177	-390.5	374.5	16X73
1887	S1176	-401.5	194.5	16X73
1888	S1175	-412.5	284.5	16X73
1889	S1174	-423.5	374.5	16X73
1890	S1173	-434.5	194.5	16X73
1891	S1172	-445.5	284.5	16X73
1892	S1171	-456.5	374.5	16X73
1893	S1170	-467.5	194.5	16X73
1894	S1169	-478.5	284.5	16X73
1895	S1168	-489.5	374.5	16X73
1896	S1167	-500.5	194.5	16X73
1897	S1166	-511.5	284.5	16X73
1898	S1165	-522.5	374.5	16X73
1899	S1164	-533.5	194.5	16X73
1900	S1163	-544.5	284.5	16X73
1901	S1162	-555.5	374.5	16X73
1902	S1161	-566.5	194.5	16X73
1903	S1160	-577.5	284.5	16X73
1904	S1159	-588.5	374.5	16X73
1905	S1158	-599.5	194.5	16X73
1906	S1157	-610.5	284.5	16X73
1907	S1156	-621.5	374.5	16X73
1908	S1155	-632.5	194.5	16X73
1909	S1154	-643.5	284.5	16X73
1910	S1153	-654.5	374.5	16X73
1911	S1152	-665.5	194.5	16X73
1912	S1151	-676.5	284.5	16X73
1913	S1150	-687.5	374.5	16X73
1914	S1149	-698.5	194.5	16X73
1915	S1148	-709.5	284.5	16X73
1916	S1147	-720.5	374.5	16X73
1917	S1146	-731.5	194.5	16X73
1918	S1145	-742.5	284.5	16X73
1919	S1144	-753.5	374.5	16X73
1920	S1143	-764.5	194.5	16X73

No.	Name	X	Y	Bump size(μm)
1921	S1142	-775.5	284.5	16X73
1922	S1141	-786.5	374.5	16X73
1923	S1140	-797.5	194.5	16X73
1924	S1139	-808.5	284.5	16X73
1925	S1138	-819.5	374.5	16X73
1926	S1137	-830.5	194.5	16X73
1927	S1136	-841.5	284.5	16X73
1928	S1135	-852.5	374.5	16X73
1929	S1134	-863.5	194.5	16X73
1930	S1133	-874.5	284.5	16X73
1931	S1132	-885.5	374.5	16X73
1932	S1131	-896.5	194.5	16X73
1933	S1130	-907.5	284.5	16X73
1934	S1129	-918.5	374.5	16X73
1935	S1128	-929.5	194.5	16X73
1936	S1127	-940.5	284.5	16X73
1937	S1126	-951.5	374.5	16X73
1938	S1125	-962.5	194.5	16X73
1939	S1124	-973.5	284.5	16X73
1940	S1123	-984.5	374.5	16X73
1941	S1122	-995.5	194.5	16X73
1942	S1121	-1006.5	284.5	16X73
1943	S1120	-1017.5	374.5	16X73
1944	S1119	-1028.5	194.5	16X73
1945	S1118	-1039.5	284.5	16X73
1946	S1117	-1050.5	374.5	16X73
1947	S1116	-1061.5	194.5	16X73
1948	S1115	-1072.5	284.5	16X73
1949	S1114	-1083.5	374.5	16X73
1950	S1113	-1094.5	194.5	16X73
1951	S1112	-1105.5	284.5	16X73
1952	S1111	-1116.5	374.5	16X73
1953	S1110	-1127.5	194.5	16X73
1954	S1109	-1138.5	284.5	16X73
1955	S1108	-1149.5	374.5	16X73
1956	S1107	-1160.5	194.5	16X73
1957	S1106	-1171.5	284.5	16X73
1958	S1105	-1182.5	374.5	16X73
1959	S1104	-1193.5	194.5	16X73
1960	S1103	-1204.5	284.5	16X73
1961	S1102	-1215.5	374.5	16X73
1962	S1101	-1226.5	194.5	16X73
1963	S1100	-1237.5	284.5	16X73
1964	S1099	-1248.5	374.5	16X73
1965	S1098	-1259.5	194.5	16X73
1966	S1097	-1270.5	284.5	16X73
1967	S1096	-1281.5	374.5	16X73
1968	S1095	-1292.5	194.5	16X73
1969	S1094	-1303.5	284.5	16X73
1970	S1093	-1314.5	374.5	16X73
1971	S1092	-1325.5	194.5	16X73
1972	S1091	-1336.5	284.5	16X73
1973	S1090	-1347.5	374.5	16X73
1974	S1089	-1358.5	194.5	16X73
1975	S1088	-1369.5	284.5	16X73
1976	S1087	-1380.5	374.5	16X73
1977	S1086	-1391.5	194.5	16X73
1978	S1085	-1402.5	284.5	16X73
1979	S1084	-1413.5	374.5	16X73
1980	S1083	-1424.5	194.5	16X73
1981	S1082	-1435.5	284.5	16X73
1982	S1081	-1446.5	374.5	16X73
1983	S1080	-1457.5	194.5	16X73
1984	S1079	-1468.5	284.5	16X73
1985	S1078	-1479.5	374.5	16X73
1986	S1077	-1490.5	194.5	16X73
1987	S1076	-1501.5	284.5	16X73
1988	S1075	-1512.5	374.5	16X73
1989	S1074	-1523.5	194.5	16X73
1990	S1073	-1534.5	284.5	16X73
1991	S1072	-1545.5	374.5	16X73
1992	S1071	-1556.5	194.5	16X73
1993	S1070	-1567.5	284.5	16X73
1994	S1069	-1578.5	374.5	16X73
1995	S1068	-1589.5	194.5	16X73
1996	S1067	-1600.5	284.5	16X73
1997	S1066	-1611.5	374.5	16X73
1998	S1065	-1622.5	194.5	16X73
1999	S1064	-1633.5	284.5	16X73
2000	S1063	-1644.5	374.5	16X73

No.	Name	X	Y	Bump size(μm)
2001	S1062	-1655.5	194.5	16X73
2002	S1061	-1666.5	284.5	16X73
2003	S1060	-1677.5	374.5	16X73
2004	S1059	-1688.5	194.5	16X73
2005	S1058	-1699.5	284.5	16X73
2006	S1057	-1710.5	374.5	16X73
2007	S1056	-1721.5	194.5	16X73
2008	S1055	-1732.5	284.5	16X73
2009	S1054	-1743.5	374.5	16X73
2010	S1053	-1754.5	194.5	16X73
2011	S1052	-1765.5	284.5	16X73
2012	S1051	-1776.5	374.5	16X73
2013	S1050	-1787.5	194.5	16X73
2014	S1049	-1798.5	284.5	16X73
2015	S1048	-1809.5	374.5	16X73
2016	S1047	-1820.5	194.5	16X73
2017	S1046	-1831.5	284.5	16X73
2018	S1045	-1842.5	374.5	16X73
2019	S1044	-1853.5	194.5	16X73
2020	S1043	-1864.5	284.5	16X73
2021	S1042	-1875.5	374.5	16X73
2022	S1041	-1886.5	194.5	16X73
2023	S1040	-1897.5	284.5	16X73
2024	S1039	-1908.5	374.5	16X73
2025	S1038	-1919.5	194.5	16X73
2026	S1037	-1930.5	284.5	16X73
2027	S1036	-1941.5	374.5	16X73
2028	S1035	-1952.5	194.5	16X73
2029	S1034	-1963.5	284.5	16X73
2030	S1033	-1974.5	374.5	16X73
2031	S1032	-1985.5	194.5	16X73
2032	S1031	-1996.5	284.5	16X73
2033	S1030	-2007.5	374.5	16X73
2034	S1029	-2018.5	194.5	16X73
2035	S1028	-2029.5	284.5	16X73
2036	S1027	-2040.5	374.5	16X73
2037	S1026	-2051.5	194.5	16X73
2038	S1025	-2062.5	284.5	16X73
2039	S1024	-2073.5	374.5	16X73
2040	S1023	-2084.5	194.5	16X73
2041	S1022	-2095.5	284.5	16X73
2042	S1021	-2106.5	374.5	16X73
2043	S1020	-2117.5	194.5	16X73
2044	S1019	-2128.5	284.5	16X73
2045	S1018	-2139.5	374.5	16X73
2046	S1017	-2150.5	194.5	16X73
2047	S1016	-2161.5	284.5	16X73
2048	S1015	-2172.5	374.5	16X73
2049	S1014	-2183.5	194.5	16X73
2050	S1013	-2194.5	284.5	16X73
2051	S1012	-2205.5	374.5	16X73
2052	S1011	-2216.5	194.5	16X73
2053	S1010	-2227.5	284.5	16X73
2054	S1009	-2238.5	374.5	16X73
2055	S1008	-2249.5	194.5	16X73
2056	S1007	-2260.5	284.5	16X73
2057	S1006	-2271.5	374.5	16X73
2058	S1005	-2282.5	194.5	16X73
2059	S1004	-2293.5	284.5	16X73
2060	S1003	-2304.5	374.5	16X73
2061	S1002	-2315.5	194.5	16X73
2062	S1001	-2326.5	284.5	16X73
2063	S1000	-2337.5	374.5	16X73
2064	S999	-2348.5	194.5	16X73
2065	S998	-2359.5	284.5	16X73
2066	S997	-2370.5	374.5	16X73
2067	S996	-2381.5	194.5	16X73
2068	S995	-2392.5	284.5	16X73
2069	S994	-2403.5	374.5	16X73
2070	S993	-2414.5	194.5	16X73
2071	S992	-2425.5	284.5	16X73
2072	S991	-2436.5	374.5	16X73
2073	S990	-2447.5	194.5	16X73
2074	S989	-2458.5	284.5	16X73
2075	S988	-2469.5	374.5	16X73
2076	S987	-2480.5	194.5	16X73
2077	S986	-2491.5	284.5	16X73
2078	S985	-2502.5	374.5	16X73
2079	S984	-2513.5	194.5	16X73
2080	S983	-2524.5	284.5	16X73

No.	Name	X	Y	Bump size(μm)
2081	S982	-2535.5	374.5	16X73
2082	S981	-2546.5	194.5	16X73
2083	S980	-2557.5	284.5	16X73
2084	S979	-2568.5	374.5	16X73
2085	S978	-2579.5	194.5	16X73
2086	S977	-2590.5	284.5	16X73
2087	S976	-2601.5	374.5	16X73
2088	S975	-2612.5	194.5	16X73
2089	S974	-2623.5	284.5	16X73
2090	S973	-2634.5	374.5	16X73
2091	S972	-2645.5	194.5	16X73
2092	S971	-2656.5	284.5	16X73
2093	S970	-2667.5	374.5	16X73
2094	S969	-2678.5	194.5	16X73
2095	S968	-2689.5	284.5	16X73
2096	S967	-2700.5	374.5	16X73
2097	S966	-2711.5	194.5	16X73
2098	S965	-2722.5	284.5	16X73
2099	S964	-2733.5	374.5	16X73
2100	S963	-2744.5	194.5	16X73
2101	S962	-2755.5	284.5	16X73
2102	S961	-2766.5	374.5	16X73
2103	S960	-2777.5	194.5	16X73
2104	S959	-2788.5	284.5	16X73
2105	S958	-2799.5	374.5	16X73
2106	S957	-2810.5	194.5	16X73
2107	S956	-2821.5	284.5	16X73
2108	S955	-2832.5	374.5	16X73
2109	S954	-2843.5	194.5	16X73
2110	S953	-2854.5	284.5	16X73
2111	S952	-2865.5	374.5	16X73
2112	S951	-2876.5	194.5	16X73
2113	S950	-2887.5	284.5	16X73
2114	S949	-2898.5	374.5	16X73
2115	S948	-2909.5	194.5	16X73
2116	S947	-2920.5	284.5	16X73
2117	S946	-2931.5	374.5	16X73
2118	S945	-2942.5	194.5	16X73
2119	S944	-2953.5	284.5	16X73
2120	S943	-2964.5	374.5	16X73
2121	S942	-2975.5	194.5	16X73
2122	S941	-2986.5	284.5	16X73
2123	S940	-2997.5	374.5	16X73
2124	S939	-3008.5	194.5	16X73
2125	S938	-3019.5	284.5	16X73
2126	S937	-3030.5	374.5	16X73
2127	S936	-3041.5	194.5	16X73
2128	S935	-3052.5	284.5	16X73
2129	S934	-3063.5	374.5	16X73
2130	S933	-3074.5	194.5	16X73
2131	S932	-3085.5	284.5	16X73
2132	S931	-3096.5	374.5	16X73
2133	S930	-3107.5	194.5	16X73
2134	S929	-3118.5	284.5	16X73
2135	S928	-3129.5	374.5	16X73
2136	S927	-3140.5	194.5	16X73
2137	S926	-3151.5	284.5	16X73
2138	S925	-3162.5	374.5	16X73
2139	S924	-3173.5	194.5	16X73
2140	S923	-3184.5	284.5	16X73
2141	S922	-3195.5	374.5	16X73
2142	S921	-3206.5	194.5	16X73
2143	S920	-3217.5	284.5	16X73
2144	S919	-3228.5	374.5	16X73
2145	S918	-3239.5	194.5	16X73
2146	S917	-3250.5	284.5	16X73
2147	S916	-3261.5	374.5	16X73
2148	S915	-3272.5	194.5	16X73
2149	S914	-3283.5	284.5	16X73
2150	S913	-3294.5	374.5	16X73
2151	S912	-3305.5	194.5	16X73
2152	S911	-3316.5	284.5	16X73
2153	S910	-3327.5	374.5	16X73
2154	S909	-3338.5	194.5	16X73
2155	S908	-3349.5	284.5	16X73
2156	S907	-3360.5	374.5	16X73
2157	S906	-3371.5	194.5	16X73
2158	S905	-3382.5	284.5	16X73
2159	S904	-3393.5	374.5	16X73
2160	S903	-3404.5	194.5	16X73

No.	Name	X	Y	Bump size(μm)
2161	S902	-3415.5	284.5	16x73
2162	S901	-3426.5	374.5	16x73
2163	S900	-3437.5	194.5	16x73
2164	S899	-3448.5	284.5	16x73
2165	S898	-3459.5	374.5	16x73
2166	S897	-3470.5	194.5	16x73
2167	S896	-3481.5	284.5	16x73
2168	S895	-3492.5	374.5	16x73
2169	S894	-3503.5	194.5	16x73
2170	S893	-3514.5	284.5	16x73
2171	S892	-3525.5	374.5	16x73
2172	S891	-3536.5	194.5	16x73
2173	S890	-3547.5	284.5	16x73
2174	S889	-3558.5	374.5	16x73
2175	S888	-3569.5	194.5	16x73
2176	S887	-3580.5	284.5	16x73
2177	S886	-3591.5	374.5	16x73
2178	S885	-3602.5	194.5	16x73
2179	S884	-3613.5	284.5	16x73
2180	S883	-3624.5	374.5	16x73
2181	S882	-3635.5	194.5	16x73
2182	S881	-3646.5	284.5	16x73
2183	S880	-3657.5	374.5	16x73
2184	S879	-3668.5	194.5	16x73
2185	S878	-3679.5	284.5	16x73
2186	S877	-3690.5	374.5	16x73
2187	S876	-3701.5	194.5	16x73
2188	S875	-3712.5	284.5	16x73
2189	S874	-3723.5	374.5	16x73
2190	S873	-3734.5	194.5	16x73
2191	S872	-3745.5	284.5	16x73
2192	S871	-3756.5	374.5	16x73
2193	S870	-3767.5	194.5	16x73
2194	S869	-3778.5	284.5	16x73
2195	S868	-3789.5	374.5	16x73
2196	S867	-3800.5	194.5	16x73
2197	S866	-3811.5	284.5	16x73
2198	S865	-3822.5	374.5	16x73
2199	S864	-3833.5	194.5	16x73
2200	S863	-3844.5	284.5	16x73
2201	S862	-3855.5	374.5	16x73
2202	S861	-3866.5	194.5	16x73
2203	S860	-3877.5	284.5	16x73
2204	S859	-3888.5	374.5	16x73
2205	S858	-3899.5	194.5	16x73
2206	S857	-3910.5	284.5	16x73
2207	S856	-3921.5	374.5	16x73
2208	S855	-3932.5	194.5	16x73
2209	S854	-3943.5	284.5	16x73
2210	S853	-3954.5	374.5	16x73
2211	S852	-3965.5	194.5	16x73
2212	S851	-3976.5	284.5	16x73
2213	S850	-3987.5	374.5	16x73
2214	S849	-3998.5	194.5	16x73
2215	S848	-4009.5	284.5	16x73
2216	S847	-4020.5	374.5	16x73
2217	S846	-4031.5	194.5	16x73
2218	S845	-4042.5	284.5	16x73
2219	S844	-4053.5	374.5	16x73
2220	S843	-4064.5	194.5	16x73
2221	S842	-4075.5	284.5	16x73
2222	S841	-4086.5	374.5	16x73
2223	S840	-4097.5	194.5	16x73
2224	S839	-4108.5	284.5	16x73
2225	S838	-4119.5	374.5	16x73
2226	S837	-4130.5	194.5	16x73
2227	S836	-4141.5	284.5	16x73
2228	S835	-4152.5	374.5	16x73
2229	S834	-4163.5	194.5	16x73
2230	S833	-4174.5	284.5	16x73
2231	S832	-4185.5	374.5	16x73
2232	S831	-4196.5	194.5	16x73
2233	S830	-4207.5	284.5	16x73
2234	S829	-4218.5	374.5	16x73
2235	S828	-4229.5	194.5	16x73
2236	S827	-4240.5	284.5	16x73
2237	S826	-4251.5	374.5	16x73
2238	S825	-4262.5	194.5	16x73
2239	S824	-4273.5	284.5	16x73
2240	S823	-4284.5	374.5	16x73

No.	Name	X	Y	Bump size(μm)
2241	S822	-4295.5	194.5	16X73
2242	S821	-4306.5	284.5	16X73
2243	S820	-4317.5	374.5	16X73
2244	S819	-4328.5	194.5	16X73
2245	S818	-4339.5	284.5	16X73
2246	S817	-4350.5	374.5	16X73
2247	S816	-4361.5	194.5	16X73
2248	S815	-4372.5	284.5	16X73
2249	S814	-4383.5	374.5	16X73
2250	S813	-4394.5	194.5	16X73
2251	S812	-4405.5	284.5	16X73
2252	S811	-4416.5	374.5	16X73
2253	S810	-4427.5	194.5	16X73
2254	S809	-4438.5	284.5	16X73
2255	S808	-4449.5	374.5	16X73
2256	S807	-4460.5	194.5	16X73
2257	S806	-4471.5	284.5	16X73
2258	S805	-4482.5	374.5	16X73
2259	S804	-4493.5	194.5	16X73
2260	S803	-4504.5	284.5	16X73
2261	S802	-4515.5	374.5	16X73
2262	S801	-4526.5	194.5	16X73
2263	S800	-4537.5	284.5	16X73
2264	S799	-4548.5	374.5	16X73
2265	S798	-4559.5	194.5	16X73
2266	S797	-4570.5	284.5	16X73
2267	S796	-4581.5	374.5	16X73
2268	S795	-4592.5	194.5	16X73
2269	S794	-4603.5	284.5	16X73
2270	S793	-4614.5	374.5	16X73
2271	S792	-4625.5	194.5	16X73
2272	S791	-4636.5	284.5	16X73
2273	S790	-4647.5	374.5	16X73
2274	S789	-4658.5	194.5	16X73
2275	S788	-4669.5	284.5	16X73
2276	S787	-4680.5	374.5	16X73
2277	S786	-4691.5	194.5	16X73
2278	S785	-4702.5	284.5	16X73
2279	S784	-4713.5	374.5	16X73
2280	S783	-4724.5	194.5	16X73
2281	S782	-4735.5	284.5	16X73
2282	S781	-4746.5	374.5	16X73
2283	S780	-4757.5	194.5	16X73
2284	S779	-4768.5	284.5	16X73
2285	S778	-4779.5	374.5	16X73
2286	S777	-4790.5	194.5	16X73
2287	S776	-4801.5	284.5	16X73
2288	S775	-4812.5	374.5	16X73
2289	S774	-4823.5	194.5	16X73
2290	S773	-4834.5	284.5	16X73
2291	S772	-4845.5	374.5	16X73
2292	S771	-4856.5	194.5	16X73
2293	S770	-4867.5	284.5	16X73
2294	S769	-4878.5	374.5	16X73
2295	S768	-4889.5	194.5	16X73
2296	S767	-4900.5	284.5	16X73
2297	S766	-4911.5	374.5	16X73
2298	S765	-4922.5	194.5	16X73
2299	S764	-4933.5	284.5	16X73
2300	S763	-4944.5	374.5	16X73
2301	S762	-4955.5	194.5	16X73
2302	S761	-4966.5	284.5	16X73
2303	S760	-4977.5	374.5	16X73
2304	S759	-4988.5	194.5	16X73
2305	S758	-4999.5	284.5	16X73
2306	S757	-5010.5	374.5	16X73
2307	S756	-5021.5	194.5	16X73
2308	S755	-5032.5	284.5	16X73
2309	S754	-5043.5	374.5	16X73
2310	S753	-5054.5	194.5	16X73
2311	S752	-5065.5	284.5	16X73
2312	S751	-5076.5	374.5	16X73
2313	S750	-5087.5	194.5	16X73
2314	S749	-5098.5	284.5	16X73
2315	S748	-5109.5	374.5	16X73
2316	S747	-5120.5	194.5	16X73
2317	S746	-5131.5	284.5	16X73
2318	S745	-5142.5	374.5	16X73
2319	S744	-5153.5	194.5	16X73
2320	S743	-5164.5	284.5	16X73

No.	Name	X	Y	Bump size(μm)
2321	S742	-5175.5	374.5	16X73
2322	S741	-5186.5	194.5	16X73
2323	S740	-5197.5	284.5	16X73
2324	S739	-5208.5	374.5	16X73
2325	S738	-5219.5	194.5	16X73
2326	S737	-5230.5	284.5	16X73
2327	S736	-5241.5	374.5	16X73
2328	S735	-5252.5	194.5	16X73
2329	S734	-5263.5	284.5	16X73
2330	S733	-5274.5	374.5	16X73
2331	S732	-5285.5	194.5	16X73
2332	S731	-5296.5	284.5	16X73
2333	S730	-5307.5	374.5	16X73
2334	S729	-5318.5	194.5	16X73
2335	S728	-5329.5	284.5	16X73
2336	S727	-5340.5	374.5	16X73
2337	S726	-5351.5	194.5	16X73
2338	S725	-5362.5	284.5	16X73
2339	S724	-5373.5	374.5	16X73
2340	S723	-5384.5	194.5	16X73
2341	S722	-5395.5	284.5	16X73
2342	S721	-5406.5	374.5	16X73
2343	S720	-5417.5	194.5	16X73
2344	S719	-5428.5	284.5	16X73
2345	S718	-5439.5	374.5	16X73
2346	S717	-5450.5	194.5	16X73
2347	S716	-5461.5	284.5	16X73
2348	S715	-5472.5	374.5	16X73
2349	S714	-5483.5	194.5	16X73
2350	S713	-5494.5	284.5	16X73
2351	S712	-5505.5	374.5	16X73
2352	S711	-5516.5	194.5	16X73
2353	S710	-5527.5	284.5	16X73
2354	S709	-5538.5	374.5	16X73
2355	S708	-5549.5	194.5	16X73
2356	S707	-5560.5	284.5	16X73
2357	S706	-5571.5	374.5	16X73
2358	S705	-5582.5	194.5	16X73
2359	S704	-5593.5	284.5	16X73
2360	S703	-5604.5	374.5	16X73
2361	S702	-5615.5	194.5	16X73
2362	S701	-5626.5	284.5	16X73
2363	S700	-5637.5	374.5	16X73
2364	S699	-5648.5	194.5	16X73
2365	S698	-5659.5	284.5	16X73
2366	S697	-5670.5	374.5	16X73
2367	S696	-5681.5	194.5	16X73
2368	S695	-5692.5	284.5	16X73
2369	S694	-5703.5	374.5	16X73
2370	S693	-5714.5	194.5	16X73
2371	S692	-5725.5	284.5	16X73
2372	S691	-5736.5	374.5	16X73
2373	S690	-5747.5	194.5	16X73
2374	S689	-5758.5	284.5	16X73
2375	S688	-5769.5	374.5	16X73
2376	S687	-5780.5	194.5	16X73
2377	S686	-5791.5	284.5	16X73
2378	S685	-5802.5	374.5	16X73
2379	S684	-5813.5	194.5	16X73
2380	S683	-5824.5	284.5	16X73
2381	S682	-5835.5	374.5	16X73
2382	S681	-5846.5	194.5	16X73
2383	S680	-5857.5	284.5	16X73
2384	S679	-5868.5	374.5	16X73
2385	S678	-5879.5	194.5	16X73
2386	S677	-5890.5	284.5	16X73
2387	S676	-5901.5	374.5	16X73
2388	S675	-5912.5	194.5	16X73
2389	S674	-5923.5	284.5	16X73
2390	S673	-5934.5	374.5	16X73
2391	S672	-5945.5	194.5	16X73
2392	S671	-5956.5	284.5	16X73
2393	S670	-5967.5	374.5	16X73
2394	S669	-5978.5	194.5	16X73
2395	S668	-5989.5	284.5	16X73
2396	S667	-6000.5	374.5	16X73
2397	S666	-6011.5	194.5	16X73
2398	S665	-6022.5	284.5	16X73
2399	S664	-6033.5	374.5	16X73
2400	S663	-6044.5	194.5	16X73

No.	Name	X	Y	Bump size(μm)
2401	S662	-6055.5	284.5	16X73
2402	S661	-6066.5	374.5	16X73
2403	S660	-6077.5	194.5	16X73
2404	S659	-6088.5	284.5	16X73
2405	S658	-6099.5	374.5	16X73
2406	S657	-6110.5	194.5	16X73
2407	S656	-6121.5	284.5	16X73
2408	S655	-6132.5	374.5	16X73
2409	S654	-6143.5	194.5	16X73
2410	S653	-6154.5	284.5	16X73
2411	S652	-6165.5	374.5	16X73
2412	S651	-6176.5	194.5	16X73
2413	S650	-6187.5	284.5	16X73
2414	S649	-6198.5	374.5	16X73
2415	S648	-6209.5	194.5	16X73
2416	S647	-6220.5	284.5	16X73
2417	S646	-6231.5	374.5	16X73
2418	S645	-6242.5	194.5	16X73
2419	S644	-6253.5	284.5	16X73
2420	S643	-6264.5	374.5	16X73
2421	S642	-6275.5	194.5	16X73
2422	S641	-6286.5	284.5	16X73
2423	S640	-6297.5	374.5	16X73
2424	S639	-6308.5	194.5	16X73
2425	S638	-6319.5	284.5	16X73
2426	S637	-6330.5	374.5	16X73
2427	S636	-6341.5	194.5	16X73
2428	S635	-6352.5	284.5	16X73
2429	S634	-6363.5	374.5	16X73
2430	S633	-6374.5	194.5	16X73
2431	S632	-6385.5	284.5	16X73
2432	S631	-6396.5	374.5	16X73
2433	S630	-6407.5	194.5	16X73
2434	S629	-6418.5	284.5	16X73
2435	S628	-6429.5	374.5	16X73
2436	S627	-6440.5	194.5	16X73
2437	S626	-6451.5	284.5	16X73
2438	S625	-6462.5	374.5	16X73
2439	S624	-6473.5	194.5	16X73
2440	S623	-6484.5	284.5	16X73
2441	S622	-6495.5	374.5	16X73
2442	S621	-6506.5	194.5	16X73
2443	S620	-6517.5	284.5	16X73
2444	S619	-6528.5	374.5	16X73
2445	S618	-6539.5	194.5	16X73
2446	S617	-6550.5	284.5	16X73
2447	S616	-6561.5	374.5	16X73
2448	S615	-6572.5	194.5	16X73
2449	S614	-6583.5	284.5	16X73
2450	S613	-6594.5	374.5	16X73
2451	S612	-6605.5	194.5	16X73
2452	S611	-6616.5	284.5	16X73
2453	S610	-6627.5	374.5	16X73
2454	S609	-6638.5	194.5	16X73
2455	S608	-6649.5	284.5	16X73
2456	S607	-6660.5	374.5	16X73
2457	S606	-6671.5	194.5	16X73
2458	S605	-6682.5	284.5	16X73
2459	S604	-6693.5	374.5	16X73
2460	S603	-6704.5	194.5	16X73
2461	S602	-6715.5	284.5	16X73
2462	S601	-6726.5	374.5	16X73
2463	DUMMY	-6737.5	194.5	16X73
2464	DUMMY	-6748.5	284.5	16X73
2465	DUMMY	-6759.5	374.5	16X73
2466	DUMMY	-6770.5	194.5	16X73
2467	DUMMY	-6781.5	284.5	16X73
2468	DUMMY	-6792.5	374.5	16X73
2469	DUMMY	-6803.5	194.5	16X73
2470	DUMMY	-6814.5	284.5	16X73
2471	DUMMY	-6825.5	374.5	16X73
2472	DUMMY	-6836.5	194.5	16X73
2473	DUMMY	-6847.5	284.5	16X73
2474	DUMMY	-6858.5	374.5	16X73
2475	DUMMY	-6869.5	194.5	16X73
2476	DUMMY	-6880.5	284.5	16X73
2477	DUMMY	-6891.5	374.5	16X73
2478	DUMMY	-6902.5	194.5	16X73
2479	DUMMY	-6913.5	284.5	16X73
2480	DUMMY	-6924.5	374.5	16X73

No.	Name	X	Y	Bump size(μm)
2481	S600	-6935.5	194.5	16X73
2482	S599	-6946.5	284.5	16X73
2483	S598	-6957.5	374.5	16X73
2484	S597	-6968.5	194.5	16X73
2485	S596	-6979.5	284.5	16X73
2486	S595	-6990.5	374.5	16X73
2487	S594	-7001.5	194.5	16X73
2488	S593	-7012.5	284.5	16X73
2489	S592	-7023.5	374.5	16X73
2490	S591	-7034.5	194.5	16X73
2491	S590	-7045.5	284.5	16X73
2492	S589	-7056.5	374.5	16X73
2493	S588	-7067.5	194.5	16X73
2494	S587	-7078.5	284.5	16X73
2495	S586	-7089.5	374.5	16X73
2496	S585	-7100.5	194.5	16X73
2497	S584	-7111.5	284.5	16X73
2498	S583	-7122.5	374.5	16X73
2499	S582	-7133.5	194.5	16X73
2500	S581	-7144.5	284.5	16X73
2501	S580	-7155.5	374.5	16X73
2502	S579	-7166.5	194.5	16X73
2503	S578	-7177.5	284.5	16X73
2504	S577	-7188.5	374.5	16X73
2505	S576	-7199.5	194.5	16X73
2506	S575	-7210.5	284.5	16X73
2507	S574	-7221.5	374.5	16X73
2508	S573	-7232.5	194.5	16X73
2509	S572	-7243.5	284.5	16X73
2510	S571	-7254.5	374.5	16X73
2511	S570	-7265.5	194.5	16X73
2512	S569	-7276.5	284.5	16X73
2513	S568	-7287.5	374.5	16X73
2514	S567	-7298.5	194.5	16X73
2515	S566	-7309.5	284.5	16X73
2516	S565	-7320.5	374.5	16X73
2517	S564	-7331.5	194.5	16X73
2518	S563	-7342.5	284.5	16X73
2519	S562	-7353.5	374.5	16X73
2520	S561	-7364.5	194.5	16X73
2521	S560	-7375.5	284.5	16X73
2522	S559	-7386.5	374.5	16X73
2523	S558	-7397.5	194.5	16X73
2524	S557	-7408.5	284.5	16X73
2525	S556	-7419.5	374.5	16X73
2526	S555	-7430.5	194.5	16X73
2527	S554	-7441.5	284.5	16X73
2528	S553	-7452.5	374.5	16X73
2529	S552	-7463.5	194.5	16X73
2530	S551	-7474.5	284.5	16X73
2531	S550	-7485.5	374.5	16X73
2532	S549	-7496.5	194.5	16X73
2533	S548	-7507.5	284.5	16X73
2534	S547	-7518.5	374.5	16X73
2535	S546	-7529.5	194.5	16X73
2536	S545	-7540.5	284.5	16X73
2537	S544	-7551.5	374.5	16X73
2538	S543	-7562.5	194.5	16X73
2539	S542	-7573.5	284.5	16X73
2540	S541	-7584.5	374.5	16X73
2541	S540	-7595.5	194.5	16X73
2542	S539	-7606.5	284.5	16X73
2543	S538	-7617.5	374.5	16X73
2544	S537	-7628.5	194.5	16X73
2545	S536	-7639.5	284.5	16X73
2546	S535	-7650.5	374.5	16X73
2547	S534	-7661.5	194.5	16X73
2548	S533	-7672.5	284.5	16X73
2549	S532	-7683.5	374.5	16X73
2550	S531	-7694.5	194.5	16X73
2551	S530	-7705.5	284.5	16X73
2552	S529	-7716.5	374.5	16X73
2553	S528	-7727.5	194.5	16X73
2554	S527	-7738.5	284.5	16X73
2555	S526	-7749.5	374.5	16X73
2556	S525	-7760.5	194.5	16X73
2557	S524	-7771.5	284.5	16X73
2558	S523	-7782.5	374.5	16X73
2559	S522	-7793.5	194.5	16X73
2560	S521	-7804.5	284.5	16X73

No.	Name	X	Y	Bump size(μm)
2561	S520	-7815.5	374.5	16X73
2562	S519	-7826.5	194.5	16X73
2563	S518	-7837.5	284.5	16X73
2564	S517	-7848.5	374.5	16X73
2565	S516	-7859.5	194.5	16X73
2566	S515	-7870.5	284.5	16X73
2567	S514	-7881.5	374.5	16X73
2568	S513	-7892.5	194.5	16X73
2569	S512	-7903.5	284.5	16X73
2570	S511	-7914.5	374.5	16X73
2571	S510	-7925.5	194.5	16X73
2572	S509	-7936.5	284.5	16X73
2573	S508	-7947.5	374.5	16X73
2574	S507	-7958.5	194.5	16X73
2575	S506	-7969.5	284.5	16X73
2576	S505	-7980.5	374.5	16X73
2577	S504	-7991.5	194.5	16X73
2578	S503	-8002.5	284.5	16X73
2579	S502	-8013.5	374.5	16X73
2580	S501	-8024.5	194.5	16X73
2581	S500	-8035.5	284.5	16X73
2582	S499	-8046.5	374.5	16X73
2583	S498	-8057.5	194.5	16X73
2584	S497	-8068.5	284.5	16X73
2585	S496	-8079.5	374.5	16X73
2586	S495	-8090.5	194.5	16X73
2587	S494	-8101.5	284.5	16X73
2588	S493	-8112.5	374.5	16X73
2589	S492	-8123.5	194.5	16X73
2590	S491	-8134.5	284.5	16X73
2591	S490	-8145.5	374.5	16X73
2592	S489	-8156.5	194.5	16X73
2593	S488	-8167.5	284.5	16X73
2594	S487	-8178.5	374.5	16X73
2595	S486	-8189.5	194.5	16X73
2596	S485	-8200.5	284.5	16X73
2597	S484	-8211.5	374.5	16X73
2598	S483	-8222.5	194.5	16X73
2599	S482	-8233.5	284.5	16X73
2600	S481	-8244.5	374.5	16X73
2601	S480	-8255.5	194.5	16X73
2602	S479	-8266.5	284.5	16X73
2603	S478	-8277.5	374.5	16X73
2604	S477	-8288.5	194.5	16X73
2605	S476	-8299.5	284.5	16X73
2606	S475	-8310.5	374.5	16X73
2607	S474	-8321.5	194.5	16X73
2608	S473	-8332.5	284.5	16X73
2609	S472	-8343.5	374.5	16X73
2610	S471	-8354.5	194.5	16X73
2611	S470	-8365.5	284.5	16X73
2612	S469	-8376.5	374.5	16X73
2613	S468	-8387.5	194.5	16X73
2614	S467	-8398.5	284.5	16X73
2615	S466	-8409.5	374.5	16X73
2616	S465	-8420.5	194.5	16X73
2617	S464	-8431.5	284.5	16X73
2618	S463	-8442.5	374.5	16X73
2619	S462	-8453.5	194.5	16X73
2620	S461	-8464.5	284.5	16X73
2621	S460	-8475.5	374.5	16X73
2622	S459	-8486.5	194.5	16X73
2623	S458	-8497.5	284.5	16X73
2624	S457	-8508.5	374.5	16X73
2625	S456	-8519.5	194.5	16X73
2626	S455	-8530.5	284.5	16X73
2627	S454	-8541.5	374.5	16X73
2628	S453	-8552.5	194.5	16X73
2629	S452	-8563.5	284.5	16X73
2630	S451	-8574.5	374.5	16X73
2631	S450	-8585.5	194.5	16X73
2632	S449	-8596.5	284.5	16X73
2633	S448	-8607.5	374.5	16X73
2634	S447	-8618.5	194.5	16X73
2635	S446	-8629.5	284.5	16X73
2636	S445	-8640.5	374.5	16X73
2637	S444	-8651.5	194.5	16X73
2638	S443	-8662.5	284.5	16X73
2639	S442	-8673.5	374.5	16X73
2640	S441	-8684.5	194.5	16X73

No.	Name	X	Y	Bump size(μm)
2641	S440	-8695.5	284.5	16X73
2642	S439	-8706.5	374.5	16X73
2643	S438	-8717.5	194.5	16X73
2644	S437	-8728.5	284.5	16X73
2645	S436	-8739.5	374.5	16X73
2646	S435	-8750.5	194.5	16X73
2647	S434	-8761.5	284.5	16X73
2648	S433	-8772.5	374.5	16X73
2649	S432	-8783.5	194.5	16X73
2650	S431	-8794.5	284.5	16X73
2651	S430	-8805.5	374.5	16X73
2652	S429	-8816.5	194.5	16X73
2653	S428	-8827.5	284.5	16X73
2654	S427	-8838.5	374.5	16X73
2655	S426	-8849.5	194.5	16X73
2656	S425	-8860.5	284.5	16X73
2657	S424	-8871.5	374.5	16X73
2658	S423	-8882.5	194.5	16X73
2659	S422	-8893.5	284.5	16X73
2660	S421	-8904.5	374.5	16X73
2661	S420	-8915.5	194.5	16X73
2662	S419	-8926.5	284.5	16X73
2663	S418	-8937.5	374.5	16X73
2664	S417	-8948.5	194.5	16X73
2665	S416	-8959.5	284.5	16X73
2666	S415	-8970.5	374.5	16X73
2667	S414	-8981.5	194.5	16X73
2668	S413	-8992.5	284.5	16X73
2669	S412	-9003.5	374.5	16X73
2670	S411	-9014.5	194.5	16X73
2671	S410	-9025.5	284.5	16X73
2672	S409	-9036.5	374.5	16X73
2673	S408	-9047.5	194.5	16X73
2674	S407	-9058.5	284.5	16X73
2675	S406	-9069.5	374.5	16X73
2676	S405	-9080.5	194.5	16X73
2677	S404	-9091.5	284.5	16X73
2678	S403	-9102.5	374.5	16X73
2679	S402	-9113.5	194.5	16X73
2680	S401	-9124.5	284.5	16X73
2681	S400	-9135.5	374.5	16X73
2682	S399	-9146.5	194.5	16X73
2683	S398	-9157.5	284.5	16X73
2684	S397	-9168.5	374.5	16X73
2685	S396	-9179.5	194.5	16X73
2686	S395	-9190.5	284.5	16X73
2687	S394	-9201.5	374.5	16X73
2688	S393	-9212.5	194.5	16X73
2689	S392	-9223.5	284.5	16X73
2690	S391	-9234.5	374.5	16X73
2691	S390	-9245.5	194.5	16X73
2692	S389	-9256.5	284.5	16X73
2693	S388	-9267.5	374.5	16X73
2694	S387	-9278.5	194.5	16X73
2695	S386	-9289.5	284.5	16X73
2696	S385	-9300.5	374.5	16X73
2697	S384	-9311.5	194.5	16X73
2698	S383	-9322.5	284.5	16X73
2699	S382	-9333.5	374.5	16X73
2700	S381	-9344.5	194.5	16X73
2701	S380	-9355.5	284.5	16X73
2702	S379	-9366.5	374.5	16X73
2703	S378	-9377.5	194.5	16X73
2704	S377	-9388.5	284.5	16X73
2705	S376	-9399.5	374.5	16X73
2706	S375	-9410.5	194.5	16X73
2707	S374	-9421.5	284.5	16X73
2708	S373	-9432.5	374.5	16X73
2709	S372	-9443.5	194.5	16X73
2710	S371	-9454.5	284.5	16X73
2711	S370	-9465.5	374.5	16X73
2712	S369	-9476.5	194.5	16X73
2713	S368	-9487.5	284.5	16X73
2714	S367	-9498.5	374.5	16X73
2715	S366	-9509.5	194.5	16X73
2716	S365	-9520.5	284.5	16X73
2717	S364	-9531.5	374.5	16X73
2718	S363	-9542.5	194.5	16X73
2719	S362	-9553.5	284.5	16X73
2720	S361	-9564.5	374.5	16X73
2721	S360	-9575.5	194.5	16X73
2722	S359	-9586.5	284.5	16X73
2723	S358	-9597.5	374.5	16X73
2724	S357	-9608.5	194.5	16X73
2725	S356	-9619.5	284.5	16X73
2726	S355	-9630.5	374.5	16X73
2727	S354	-9641.5	194.5	16X73
2728	S353	-9652.5	284.5	16X73
2729	S352	-9663.5	374.5	16X73
2730	S351	-9674.5	194.5	16X73
2731	S350	-9685.5	284.5	16X73
2732	S349	-9696.5	374.5	16X73
2733	S348	-9707.5	194.5	16X73
2734	S347	-9718.5	284.5	16X73
2735	S346	-9729.5	374.5	16X73
2736	S345	-9740.5	194.5	16X73
2737	S344	-9751.5	284.5	16X73
2738	S343	-9762.5	374.5	16X73
2739	S342	-9773.5	194.5	16X73
2740	S341	-9784.5	284.5	16X73
2741	S340	-9795.5	374.5	16X73
2742	S339	-9806.5	194.5	16X73
2743	S338	-9817.5	284.5	16X73
2744	S337	-9828.5	374.5	16X73
2745	S336	-9839.5	194.5	16X73
2746	S335	-9850.5	284.5	16X73
2747	S334	-9861.5	374.5	16X73
2748	S333	-9872.5	194.5	16X73
2749	S332	-9883.5	284.5	16X73
2750	S331	-9894.5	374.5	16X73
2751	S330	-9905.5	194.5	16X73
2752	S329	-9916.5	284.5	16X73
2753	S328	-9927.5	374.5	16X73
2754	S327	-9938.5	194.5	16X73
2755	S326	-9949.5	284.5	16X73
2756	S325	-9960.5	374.5	16X73
2757	S324	-9971.5	194.5	16X73
2758	S323	-9982.5	284.5	16X73
2759	S322	-9993.5	374.5	16X73
2760	S321	-10004.5	194.5	16X73
2761	S320	-10015.5	284.5	16X73
2762	S319	-10026.5	374.5	16X73
2763	S318	-10037.5	194.5	16X73
2764	S317	-10048.5	284.5	16X73
2765	S316	-10059.5	374.5	16X73
2766	S315	-10070.5	194.5	16X73
2767	S314	-10081.5	284.5	16X73
2768	S313	-10092.5	374.5	16X73
2769	S312	-10103.5	194.5	16X73
2770	S311	-10114.5	284.5	16X73
2771	S310	-10125.5	374.5	16X73
2772	S309	-10136.5	194.5	16X73
2773	S308	-10147.5	284.5	16X73
2774	S307	-10158.5	374.5	16X73
2775	S306	-10169.5	194.5	16X73
2776	S305	-10180.5	284.5	16X73
2777	S304	-10191.5	374.5	16X73
2778	S303	-10202.5	194.5	16X73
2779	S302	-10213.5	284.5	16X73
2780	S301	-10224.5	374.5	16X73
2781	S300	-10235.5	194.5	16X73
2782	S299	-10246.5	284.5	16X73
2783	S298	-10257.5	374.5	16X73
2784	S297	-10268.5	194.5	16X73
2785	S296	-10279.5	284.5	16X73
2786	S295	-10290.5	374.5	16X73
2787	S294	-10301.5	194.5	16X73
2788	S293	-10312.5	284.5	16X73
2789	S292	-10323.5	374.5	16X73
2790	S291	-10334.5	194.5	16X73
2791	S290	-10345.5	284.5	16X73
2792	S289	-10356.5	374.5	16X73
2793	S288	-10367.5	194.5	16X73
2794	S287	-10378.5	284.5	16X73
2795	S286	-10389.5	374.5	16X73
2796	S285	-10400.5	194.5	16X73
2797	S284	-10411.5	284.5	16X73
2798	S283	-10422.5	374.5	16X73
2799	S282	-10433.5	194.5	16X73
2800	S281	-10444.5	284.5	16X73
2801	S280	-10455.5	374.5	16X73
2802	S279	-10466.5	194.5	16X73
2803	S278	-10477.5	284.5	16X73
2804	S277	-10488.5	374.5	16X73
2805	S276	-10499.5	194.5	16X73
2806	S275	-10510.5	284.5	16X73
2807	S274	-10521.5	374.5	16X73
2808	S273	-10532.5	194.5	16X73
2809	S272	-10543.5	284.5	16X73
2810	S271	-10554.5	374.5	16X73
2811	S270	-10565.5	194.5	16X73
2812	S269	-10576.5	284.5	16X73
2813	S268	-10587.5	374.5	16X73
2814	S267	-10598.5	194.5	16X73
2815	S266	-10609.5	284.5	16X73
2816	S265	-10620.5	374.5	16X73
2817	S264	-10631.5	194.5	16X73
2818	S263	-10642.5	284.5	16X73
2819	S262	-10653.5	374.5	16X73
2820	S261	-10664.5	194.5	16X73
2821	S260	-10675.5	284.5	16X73
2822	S259	-10686.5	374.5	16X73
2823	S258	-10697.5	194.5	16X73
2824	S257	-10708.5	284.5	16X73
2825	S256	-10719.5	374.5	16X73
2826	S255	-10730.5	194.5	16X73
2827	S254	-10741.5	284.5	16X73
2828	S253	-10752.5	374.5	16X73
2829	S252	-10763.5	194.5	16X73
2830	S251	-10774.5	284.5	16X73
2831	S250	-10785.5	374.5	16X73
2832	S249	-10796.5	194.5	16X73
2833	S248	-10807.5	284.5	16X73
2834	S247	-10818.5	374.5	16X73
2835	S246	-10829.5	194.5	16X73
2836	S245	-10840.5	284.5	16X73
2837	S244	-10851.5	374.5	16X73
2838	S243	-10862.5	194.5	16X73
2839	S242	-10873.5	284.5	16X73
2840	S241	-10884.5	374.5	16X73
2841	S240	-10895.5	194.5	16X73
2842	S239	-10906.5	284.5	16X73
2843	S238	-10917.5	374.5	16X73
2844	S237	-10928.5	194.5	16X73
2845	S236	-10939.5	284.5	16X73
2846	S235	-10950.5	374.5	16X73
2847	S234	-10961.5	194.5	16X73
2848	S233	-10972.5	284.5	16X73
2849	S232	-10983.5	374.5	16X73
2850	S231	-10994.5	194.5	16X73
2851	S230	-11005.5	284.5	16X73
2852	S229	-11016.5	374.5	16X73
2853	S228	-11027.5	194.5	16X73
2854	S227	-11038.5	284.5	16X73
2855	S226	-11049.5	374.5	16X73
2856	S225	-11060.5	194.5	16X73
2857	S224	-11071.5	284.5	16X73
2858	S223	-11082.5	374.5	16X73
2859	S222	-11093.5	194.5	16X73
2860	S221	-11104.5	284.5	16X73
2861	S220	-11115.5	374.5	16X73
2862	S219	-11126.5	194.5	16X73
2863	S218	-11137.5	284.5	16X73
2864	S217	-11148.5	374.5	16X73
2865	S216	-11159.5	194.5	16X73
2866	S215	-11170.5	284.5	16X73
2867	S214	-11181.5	374.5	16X73
2868	S213	-11192.5	194.5	16X73
2869	S212	-11203.5	284.5	16X73
2870	S211	-11214.5	374.5	16X73
2871	S210	-11225.5	194.5	16X73
2872	S209	-11236.5	284.5	16X73
2873	S208	-11247.5	374.5	16X73
2874	S207	-11258.5	194.5	16X73
2875	S206	-11269.5	284.5	16X73
2876	S205	-11280.5	374.5	16X73
2877	S204	-11291.5	194.5	16X73
2878	S203	-11302.5	284.5	16X73
2879	S202	-11313.5	374.5	16X73
2880	S201	-11324.5	194.5	16X73

No.	Name	X	Y	Bump size(μm)
2881	S200	-11335.5	284.5	16X73
2882	S199	-11346.5	374.5	16X73
2883	S198	-11357.5	194.5	16X73
2884	S197	-11368.5	284.5	16X73
2885	S196	-11379.5	374.5	16X73
2886	S195	-11390.5	194.5	16X73
2887	S194	-11401.5	284.5	16X73
2888	S193	-11412.5	374.5	16X73
2889	S192	-11423.5	194.5	16X73
2890	S191	-11434.5	284.5	16X73
2891	S190	-11445.5	374.5	16X73
2892	S189	-11456.5	194.5	16X73
2893	S188	-11467.5	284.5	16X73
2894	S187	-11478.5	374.5	16X73
2895	S186	-11489.5	194.5	16X73
2896	S185	-11500.5	284.5	16X73
2897	S184	-11511.5	374.5	16X73
2898	S183	-11522.5	194.5	16X73
2899	S182	-11533.5	284.5	16X73
2900	S181	-11544.5	374.5	16X73
2901	S180	-11555.5	194.5	16X73
2902	S179	-11566.5	284.5	16X73
2903	S178	-11577.5	374.5	16X73
2904	S177	-11588.5	194.5	16X73
2905	S176	-11599.5	284.5	16X73
2906	S175	-11610.5	374.5	16X73
2907	S174	-11621.5	194.5	16X73
2908	S173	-11632.5	284.5	16X73
2909	S172	-11643.5	374.5	16X73
2910	S171	-11654.5	194.5	16X73
2911	S170	-11665.5	284.5	16X73
2912	S169	-11676.5	374.5	16X73
2913	S168	-11687.5	194.5	16X73
2914	S167	-11698.5	284.5	16X73
2915	S166	-11709.5	374.5	16X73
2916	S165	-11720.5	194.5	16X73
2917	S164	-11731.5	284.5	16X73
2918	S163	-11742.5	374.5	16X73
2919	S162	-11753.5	194.5	16X73
2920	S161	-11764.5	284.5	16X73
2921	S160	-11775.5	374.5	16X73
2922	S159	-11786.5	194.5	16X73
2923	S158	-11797.5	284.5	16X73
2924	S157	-11808.5	374.5	16X73
2925	S156	-11819.5	194.5	16X73
2926	S155	-11830.5	284.5	16X73
2927	S154	-11841.5	374.5	16X73
2928	S153	-11852.5	194.5	16X73
2929	S152	-11863.5	284.5	16X73
2930	S151	-11874.5	374.5	16X73
2931	S150	-11885.5	194.5	16X73
2932	S149	-11896.5	284.5	16X73
2933	S148	-11907.5	374.5	16X73
2934	S147	-11918.5	194.5	16X73
2935	S146	-11929.5	284.5	16X73
2936	S145	-11940.5	374.5	16X73
2937	S144	-11951.5	194.5	16X73
2938	S143	-11962.5	284.5	16X73
2939	S142	-11973.5	374.5	16X73
2940	S141	-11984.5	194.5	16X73
2941	S140	-11995.5	284.5	16X73
2942	S139	-12006.5	374.5	16X73
2943	S138	-12017.5	194.5	16X73
2944	S137	-12028.5	284.5	16X73
2945	S136	-12039.5	374.5	16X73
2946	S135	-12050.5	194.5	16X73
2947	S134	-12061.5	284.5	16X73
2948	S133	-12072.5	374.5	16X73
2949	S132	-12083.5	194.5	16X73
2950	S131	-12094.5	284.5	16X73
2951	S130	-12105.5	374.5	16X73
2952	S129	-12116.5	194.5	16X73
2953	S128	-12127.5	284.5	16X73
2954	S127	-12138.5	374.5	16X73
2955	S126	-12149.5	194.5	16X73
2956	S125	-12160.5	284.5	16X73
2957	S124	-12171.5	374.5	16X73
2958	S123	-12182.5	194.5	16X73
2959	S122	-12193.5	284.5	16X73
2960	S121	-12204.5	374.5	16X73
2961	S120	-12215.5	194.5	16X73
2962	S119	-12226.5	284.5	16X73
2963	S118	-12237.5	374.5	16X73
2964	S117	-12248.5	194.5	16X73
2965	S116	-12259.5	284.5	16X73
2966	S115	-12270.5	374.5	16X73
2967	S114	-12281.5	194.5	16X73
2968	S113	-12292.5	284.5	16X73
2969	S112	-12303.5	374.5	16X73
2970	S111	-12314.5	194.5	16X73
2971	S110	-12325.5	284.5	16X73
2972	S109	-12336.5	374.5	16X73
2973	S108	-12347.5	194.5	16X73
2974	S107	-12358.5	284.5	16X73
2975	S106	-12369.5	374.5	16X73
2976	S105	-12380.5	194.5	16X73
2977	S104	-12391.5	284.5	16X73
2978	S103	-12402.5	374.5	16X73
2979	S102	-12413.5	194.5	16X73
2980	S101	-12424.5	284.5	16X73
2981	S100	-12435.5	374.5	16X73
2982	S99	-12446.5	194.5	16X73
2983	S98	-12457.5	284.5	16X73
2984	S97	-12468.5	374.5	16X73
2985	S96	-12479.5	194.5	16X73
2986	S95	-12490.5	284.5	16X73
2987	S94	-12501.5	374.5	16X73
2988	S93	-12512.5	194.5	16X73
2989	S92	-12523.5	284.5	16X73
2990	S91	-12534.5	374.5	16X73
2991	S90	-12545.5	194.5	16X73
2992	S89	-12556.5	284.5	16X73
2993	S88	-12567.5	374.5	16X73
2994	S87	-12578.5	194.5	16X73
2995	S86	-12589.5	284.5	16X73
2996	S85	-12600.5	374.5	16X73
2997	S84	-12611.5	194.5	16X73
2998	S83	-12622.5	284.5	16X73
2999	S82	-12633.5	374.5	16X73
3000	S81	-12644.5	194.5	16X73
3001	S80	-12655.5	284.5	16X73
3002	S79	-12666.5	374.5	16X73
3003	S78	-12677.5	194.5	16X73
3004	S77	-12688.5	284.5	16X73
3005	S76	-12699.5	374.5	16X73
3006	S75	-12710.5	194.5	16X73
3007	S74	-12721.5	284.5	16X73
3008	S73	-12732.5	374.5	16X73
3009	S72	-12743.5	194.5	16X73
3010	S71	-12754.5	284.5	16X73
3011	S70	-12765.5	374.5	16X73
3012	S69	-12776.5	194.5	16X73
3013	S68	-12787.5	284.5	16X73
3014	S67	-12798.5	374.5	16X73
3015	S66	-12809.5	194.5	16X73
3016	S65	-12820.5	284.5	16X73
3017	S64	-12831.5	374.5	16X73
3018	S63	-12842.5	194.5	16X73
3019	S62	-12853.5	284.5	16X73
3020	S61	-12864.5	374.5	16X73
3021	S60	-12875.5	194.5	16X73
3022	S59	-12886.5	284.5	16X73
3023	S58	-12897.5	374.5	16X73
3024	S57	-12908.5	194.5	16X73
3025	S56	-12919.5	284.5	16X73
3026	S55	-12930.5	374.5	16X73
3027	S54	-12941.5	194.5	16X73
3028	S53	-12952.5	284.5	16X73
3029	S52	-12963.5	374.5	16X73
3030	S51	-12974.5	194.5	16X73
3031	S50	-12985.5	284.5	16X73
3032	S49	-12996.5	374.5	16X73
3033	S48	-13007.5	194.5	16X73
3034	S47	-13018.5	284.5	16X73
3035	S46	-13029.5	374.5	16X73
3036	S45	-13040.5	194.5	16X73
3037	S44	-13051.5	284.5	16X73
3038	S43	-13062.5	374.5	16X73
3039	S42	-13073.5	194.5	16X73
3040	S41	-13084.5	284.5	16X73
3041	S40	-13095.5	374.5	16X73
3042	S39	-13106.5	194.5	16X73
3043	S38	-13117.5	284.5	16X73
3044	S37	-13128.5	374.5	16X73
3045	S36	-13139.5	194.5	16X73
3046	S35	-13150.5	284.5	16X73
3047	S34	-13161.5	374.5	16X73
3048	S33	-13172.5	194.5	16X73
3049	S32	-13183.5	284.5	16X73
3050	S31	-13194.5	374.5	16X73
3051	S30	-13205.5	194.5	16X73
3052	S29	-13216.5	284.5	16X73
3053	S28	-13227.5	374.5	16X73
3054	S27	-13238.5	194.5	16X73
3055	S26	-13249.5	284.5	16X73
3056	S25	-13260.5	374.5	16X73
3057	S24	-13271.5	194.5	16X73
3058	S23	-13282.5	284.5	16X73
3059	S22	-13293.5	374.5	16X73
3060	S21	-13304.5	194.5	16X73
3061	S20	-13315.5	284.5	16X73
3062	S19	-13326.5	374.5	16X73
3063	S18	-13337.5	194.5	16X73
3064	S17	-13348.5	284.5	16X73
3065	S16	-13359.5	374.5	16X73
3066	S15	-13370.5	194.5	16X73
3067	S14	-13381.5	284.5	16X73
3068	S13	-13392.5	374.5	16X73
3069	S12	-13403.5	194.5	16X73
3070	S11	-13414.5	284.5	16X73
3071	S10	-13425.5	374.5	16X73
3072	S9	-13436.5	194.5	16X73
3073	S8	-13447.5	284.5	16X73
3074	S7	-13458.5	374.5	16X73
3075	S6	-13469.5	194.5	16X73
3076	S5	-13480.5	284.5	16X73
3077	S4	-13491.5	374.5	16X73
3078	S3	-13502.5	194.5	16X73
3079	S2	-13513.5	284.5	16X73
3080	S1	-13524.5	374.5	16X73
3081	SL1	-13535.5	194.5	16X73
3082	DUMMY	-13546.5	284.5	16X73
3083	DUMMY	-13557.5	374.5	16X73
3084	DUMMY	-13568.5	194.5	16X73
3085	DUMMY	-13579.5	284.5	16X73
3086	DUMMY	-13590.5	374.5	16X73
3087	DUMMY_R3	-13601.5	194.5	16X73
3088	DUMMY_R3	-13612.5	284.5	16X73
3089	DUMMY_R3	-13623.5	374.5	16X73
3090	DUMMY_R3	-13634.5	194.5	16X73
3091	DUMMY_R3	-13645.5	284.5	16X73
3092	DUMMY_R3	-13656.5	374.5	16X73
*	Alignment (L)	-13706	386	
*	Alignment (R)	+13706	386	

Table 14.2: Pad coordinates

15. Ordering Information

Part no.	Package type
HX8260-AxPDxxx	X : meab fab code PD : mean COG xxx : mean chip thickness (μm)