

ANKAA_BASE BOARD

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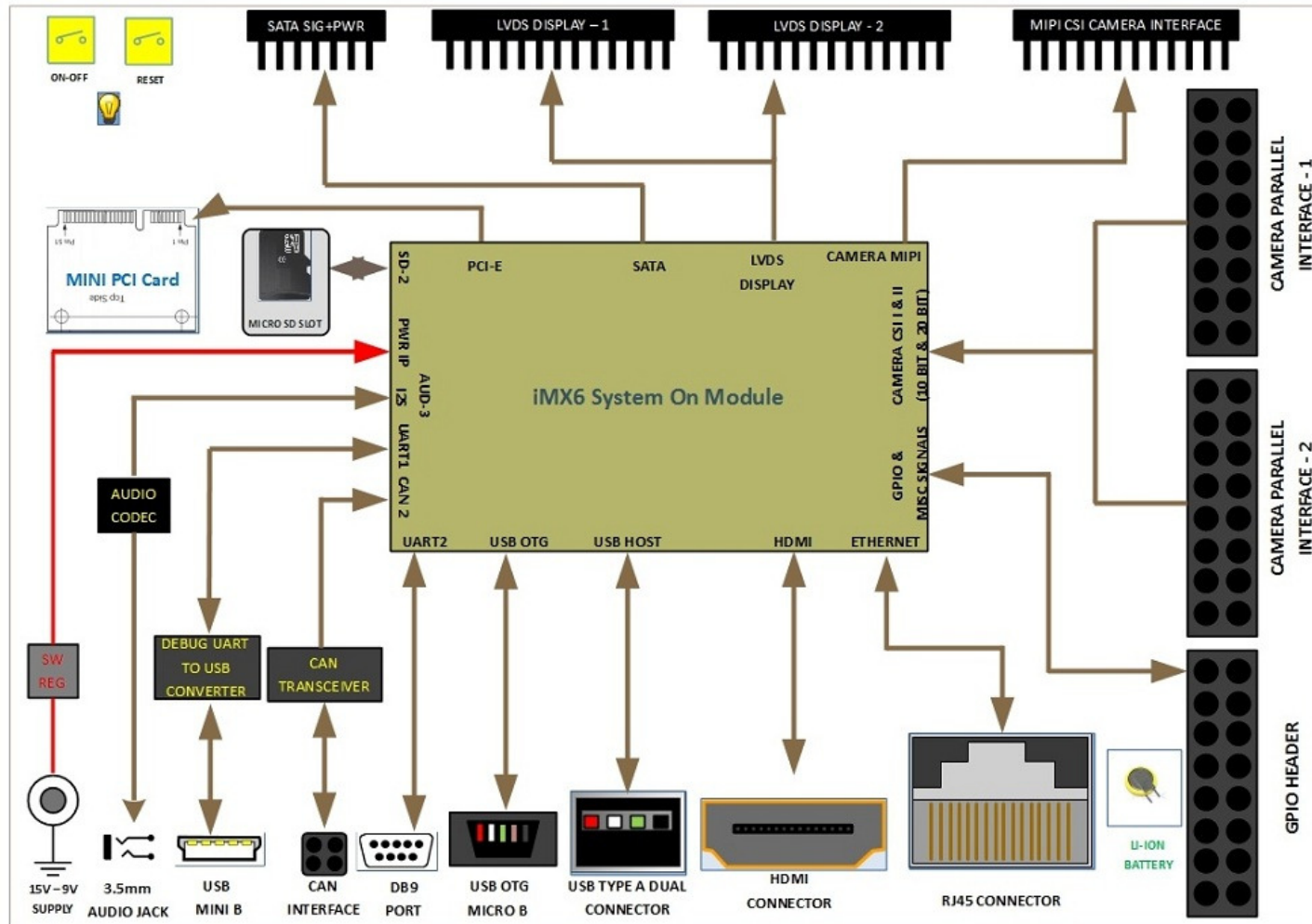
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BLOCK DIAGRAM

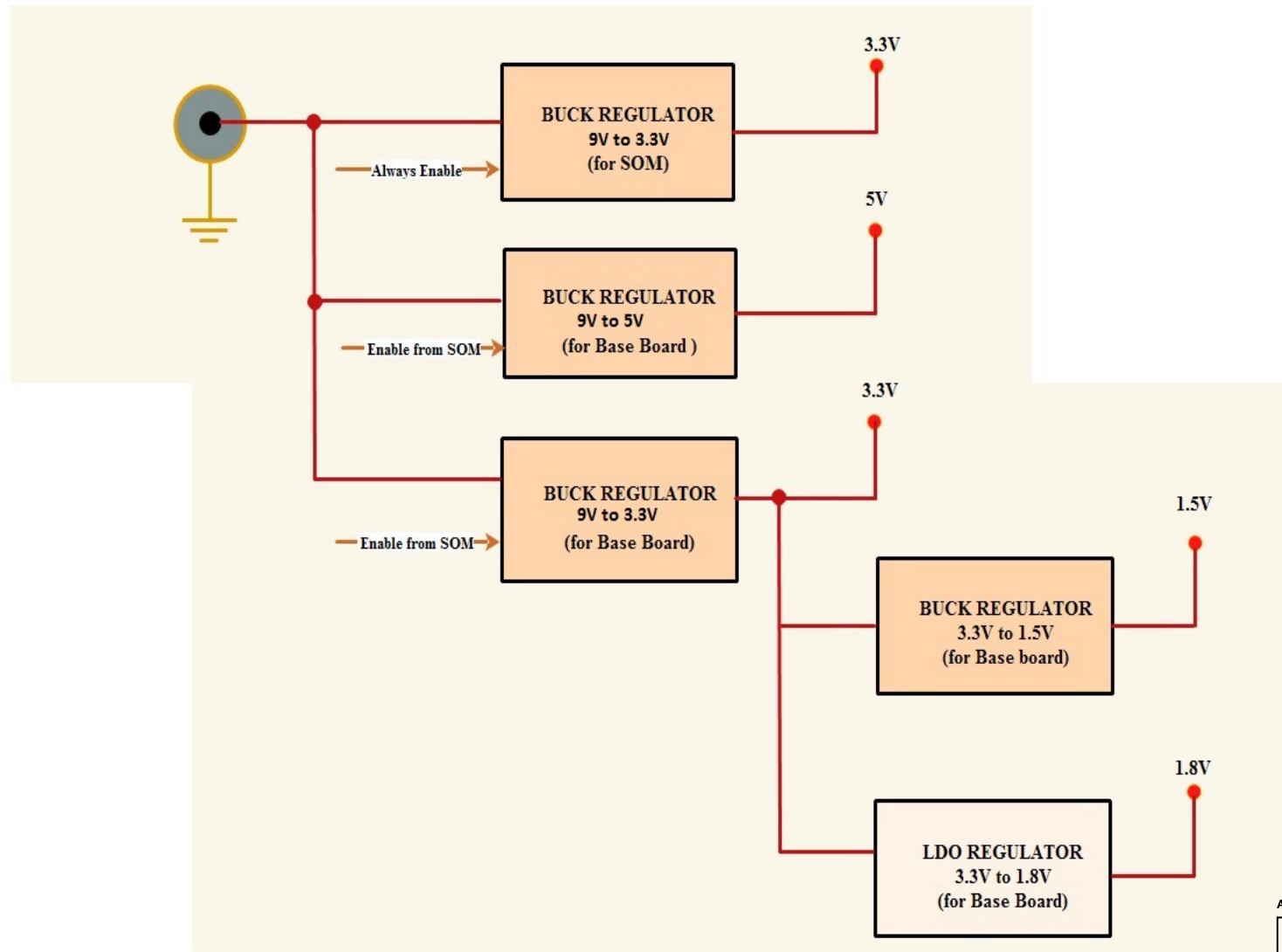


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POWER FLOW DIAGRAM



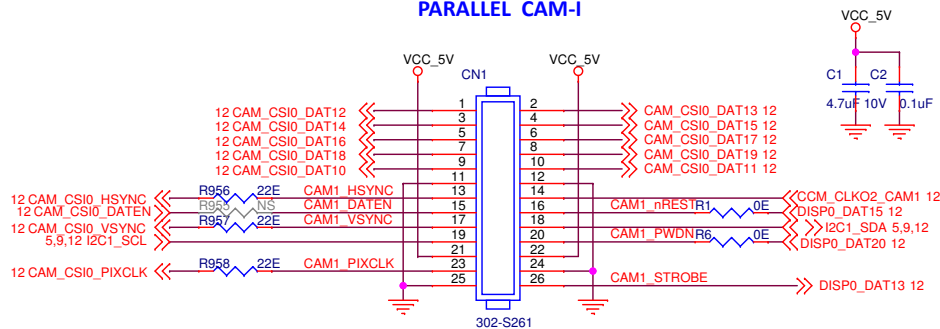
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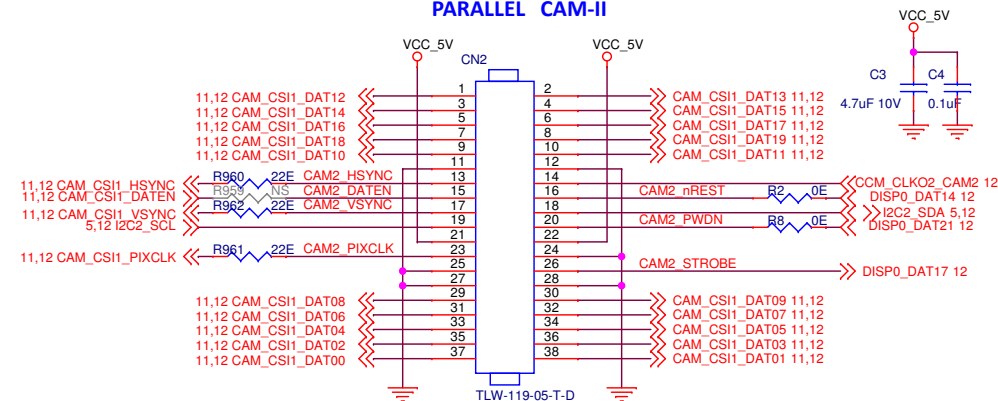
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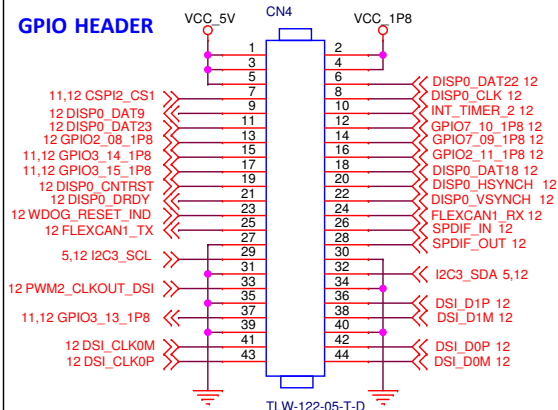
PARALLEL CAM-I



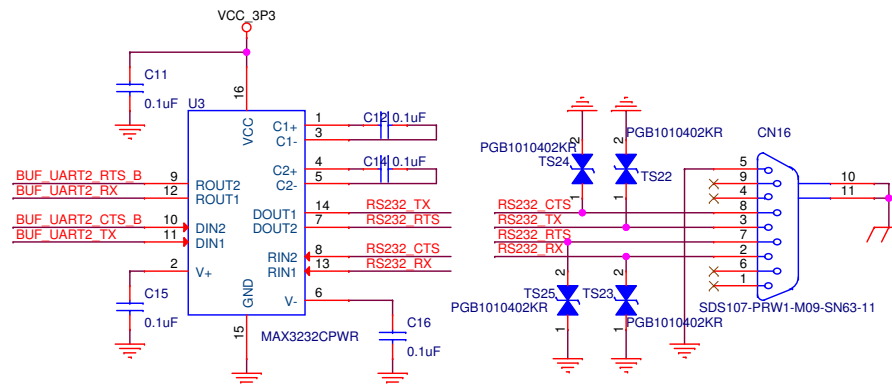
PARALLEL CAM-II



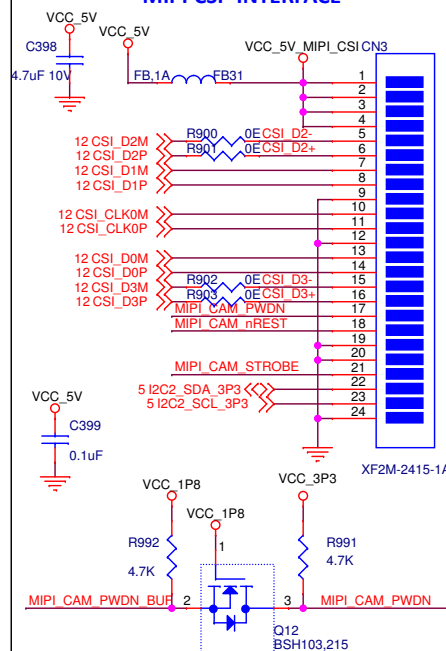
GPIO HEADER



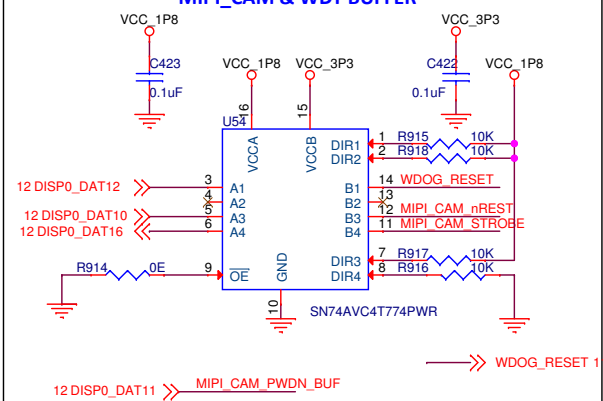
RS-232 INTERFACE



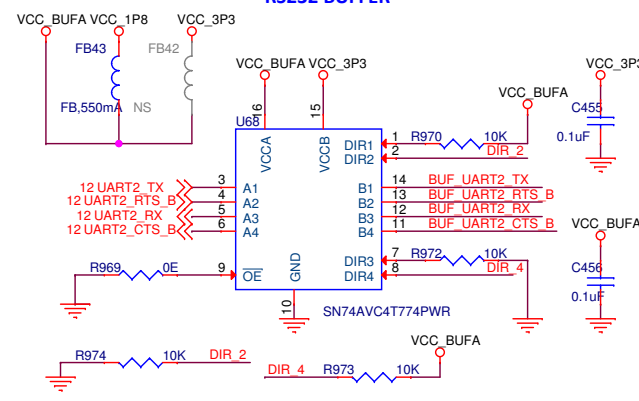
MIPI CSI INTERFACE



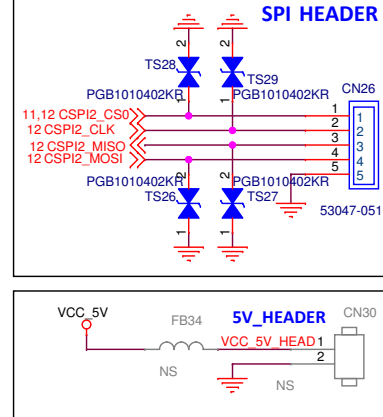
MIPI_CAM & WDT BUFFER



RS232 BUFFER



SPI HEADER



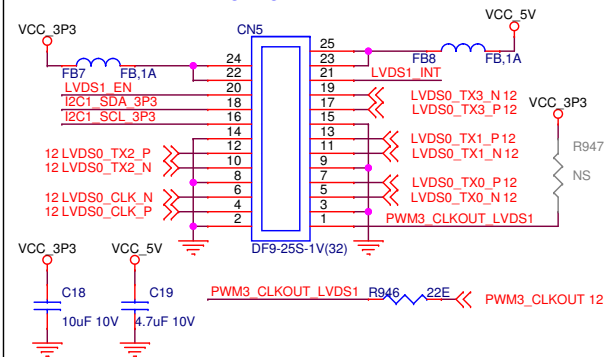
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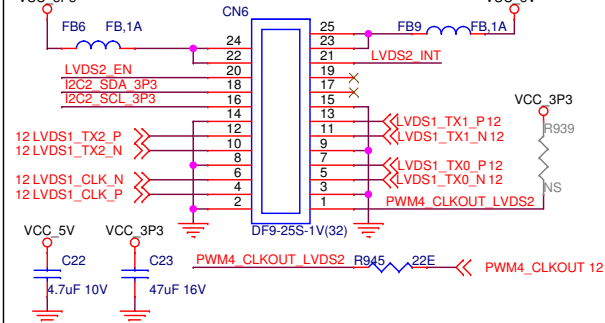
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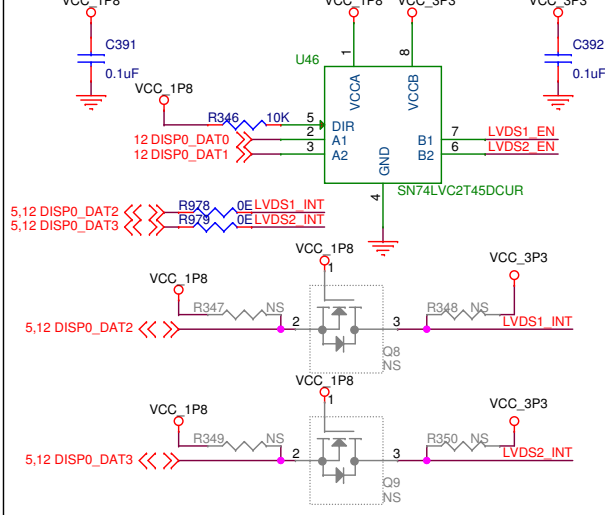
LVDS DISPLAY - 1



LVDS DISPLAY - 2

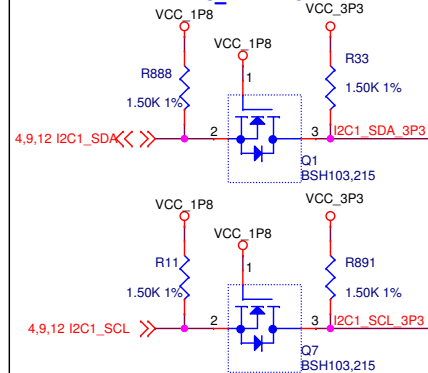


LVDS BUFFER

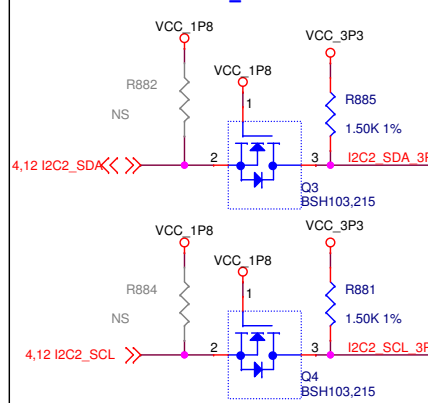


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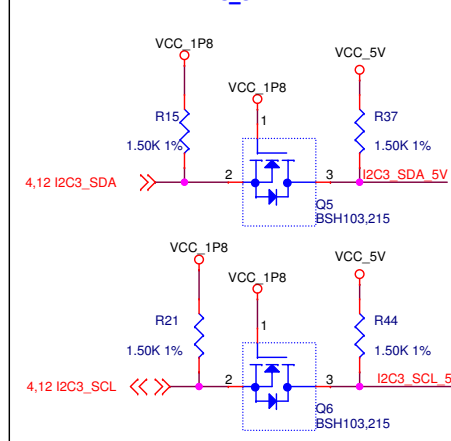
I2C_1 - LVDS 1



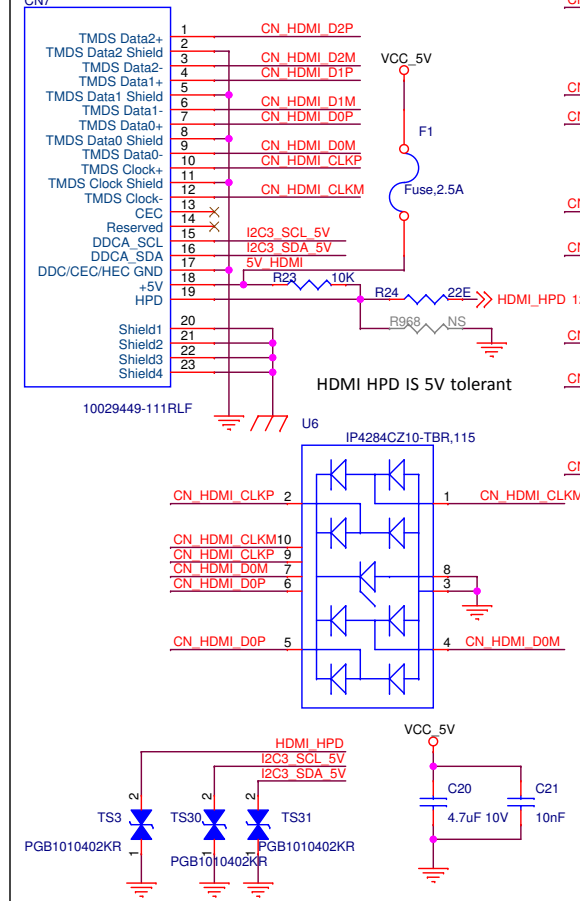
I2C_2 - LVDS 2



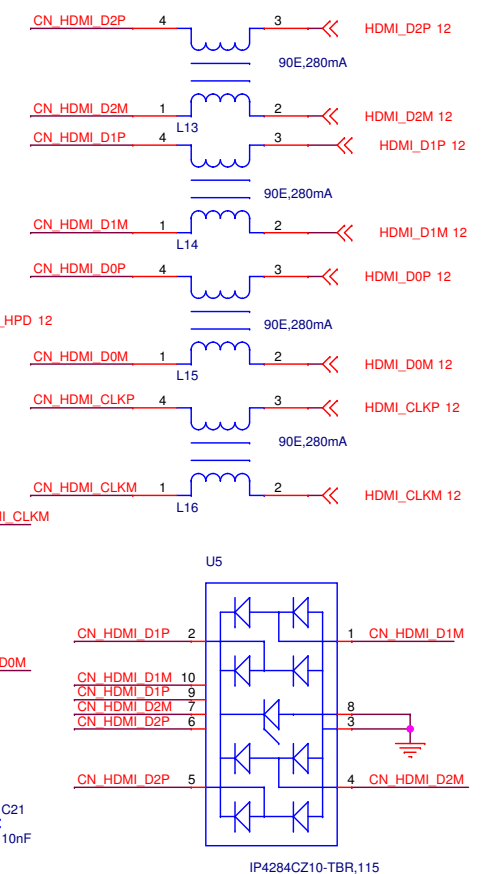
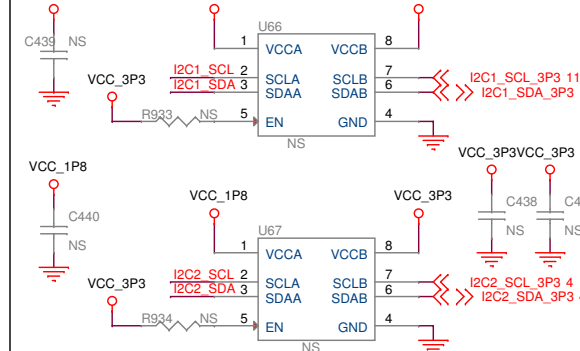
I2C_3 - HDMI



HDMI DISPLAY



OPTIONAL I2C BUFFER



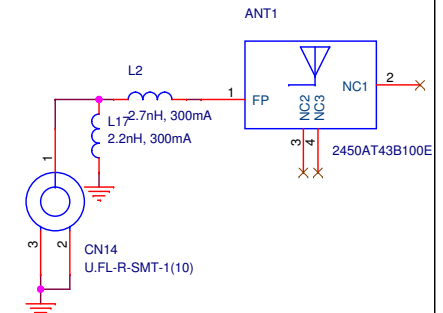
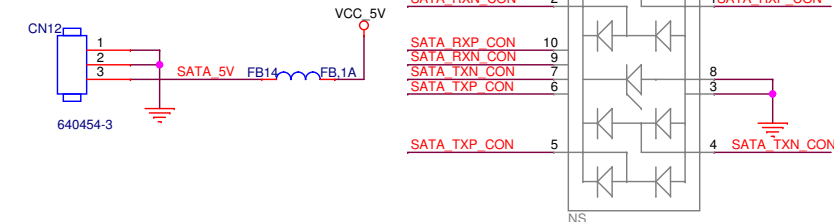
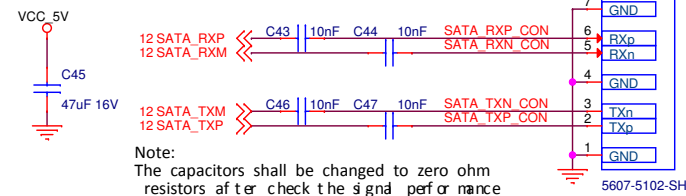
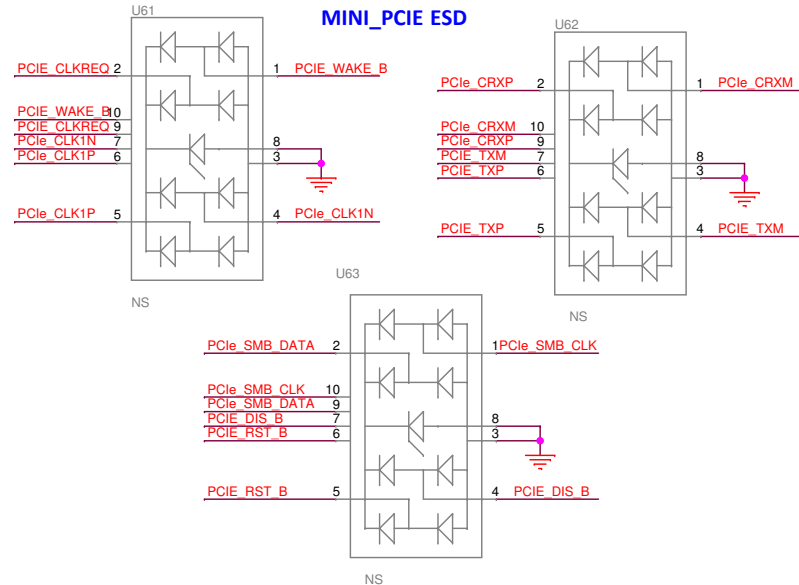
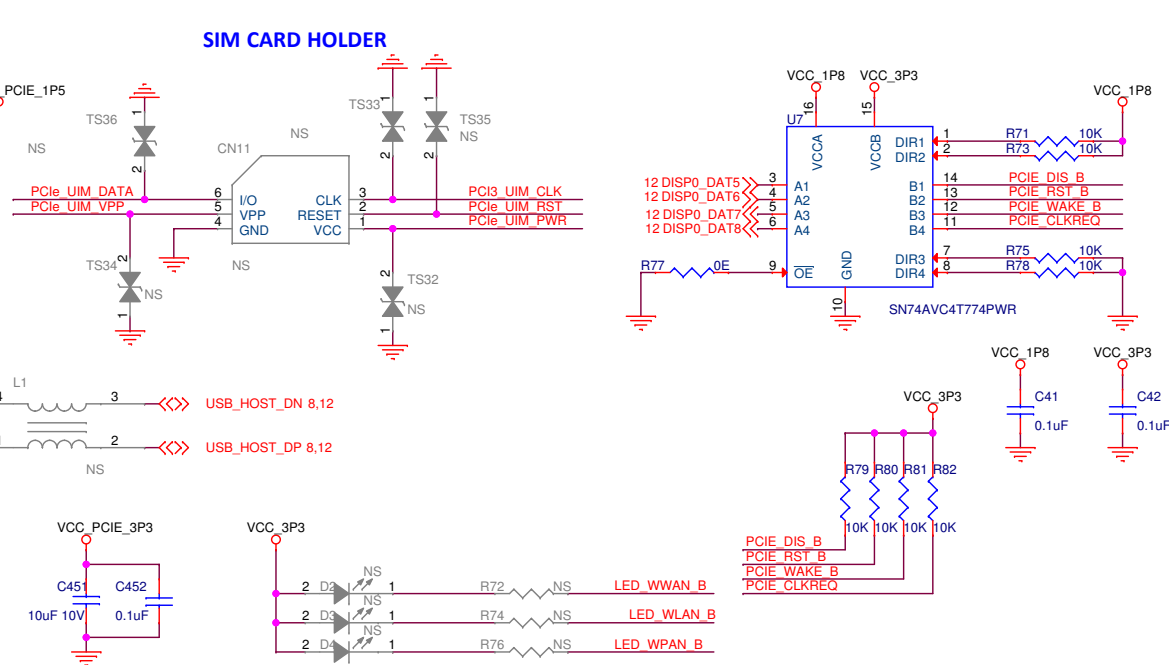
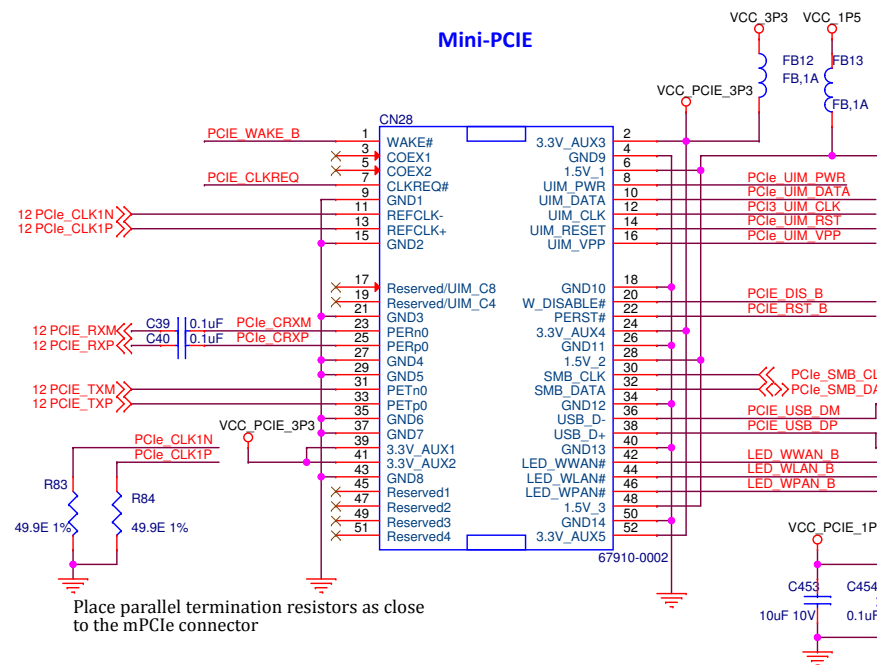
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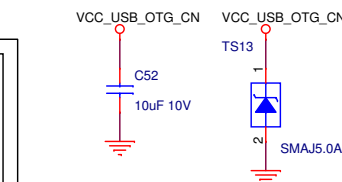
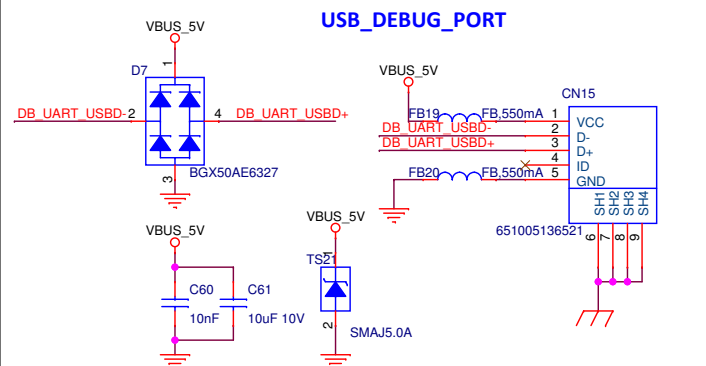
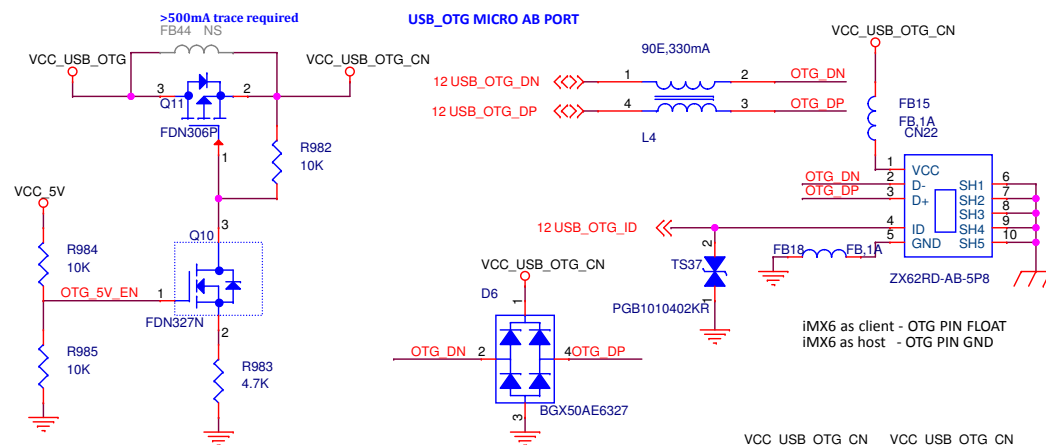
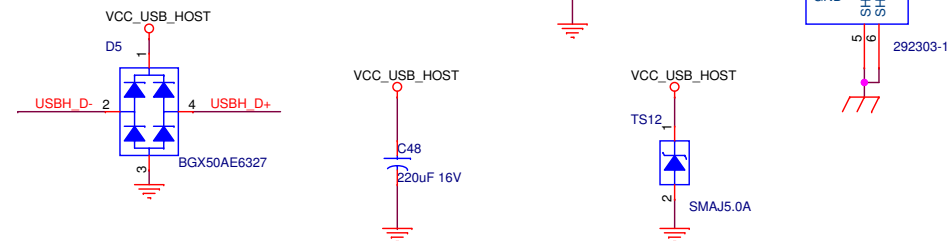
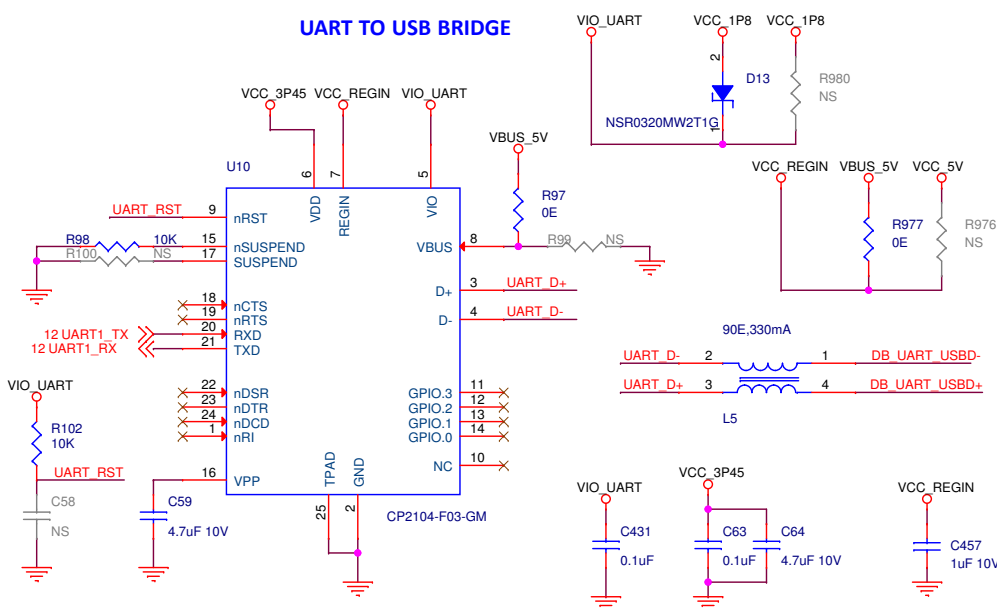
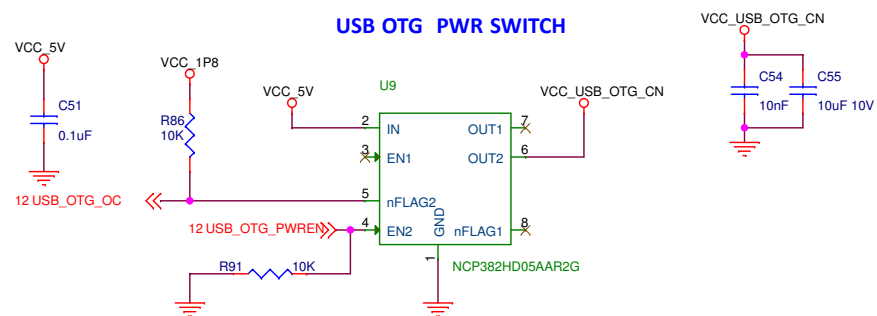
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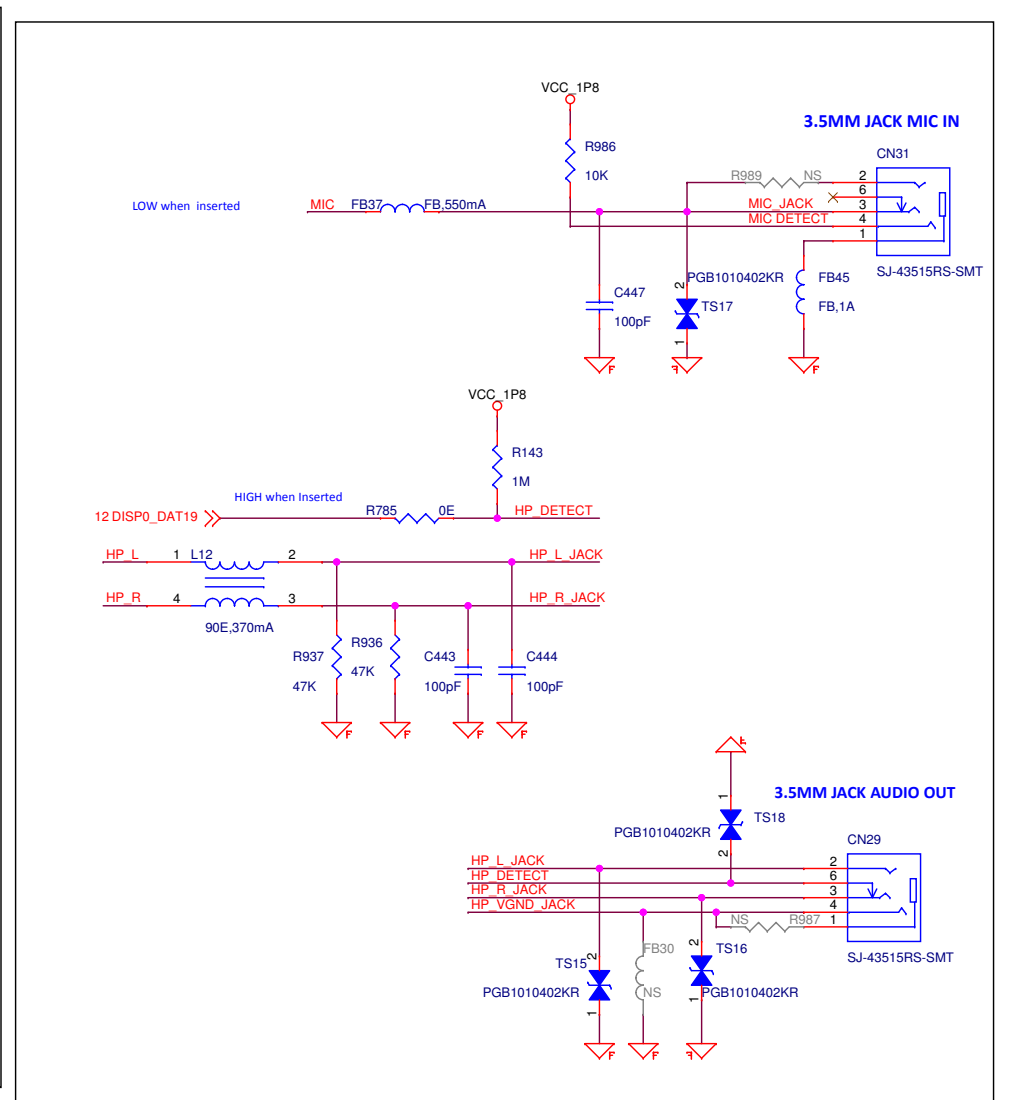
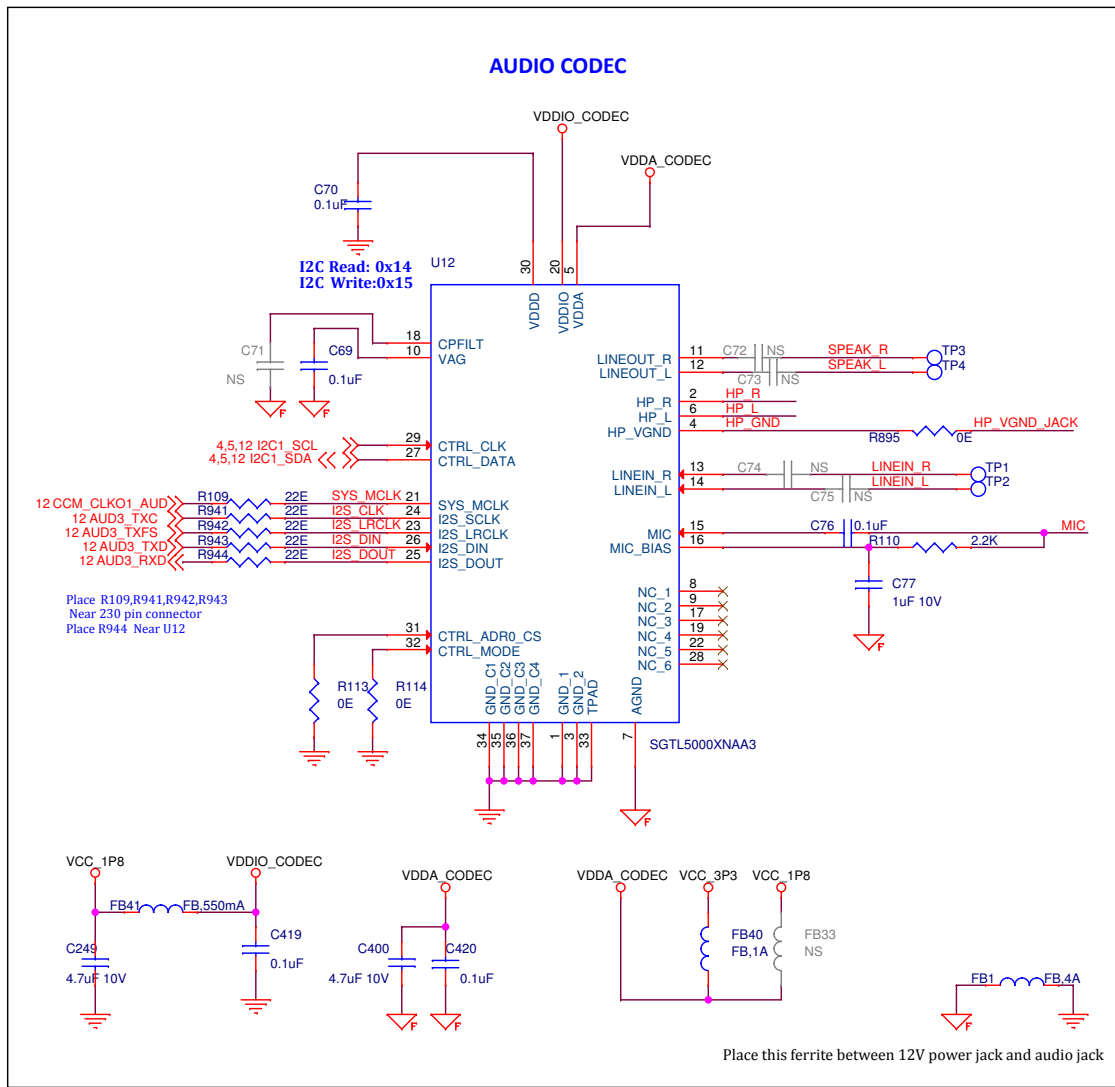


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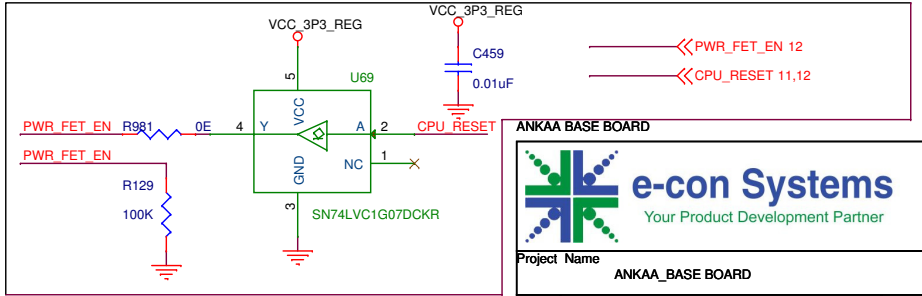
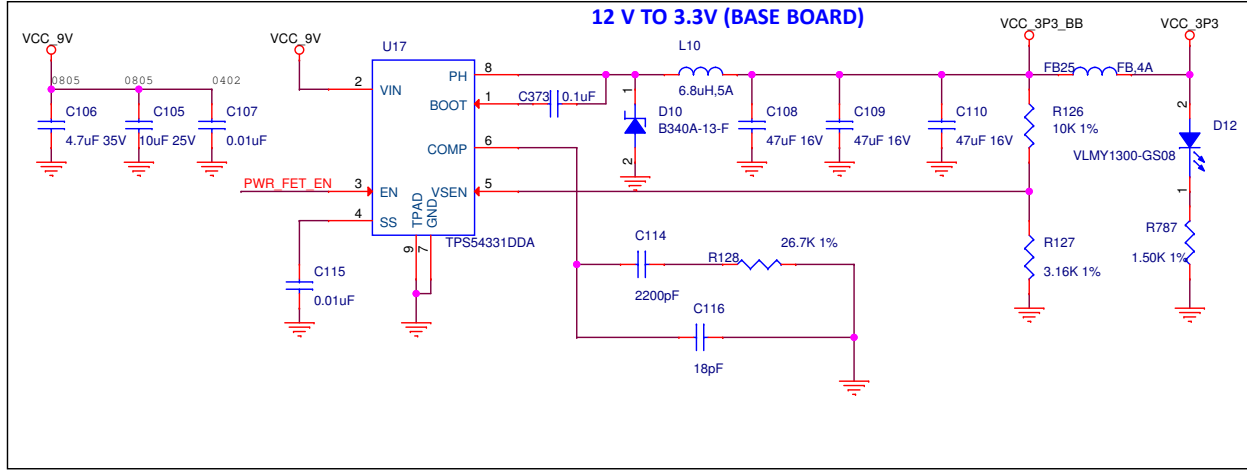
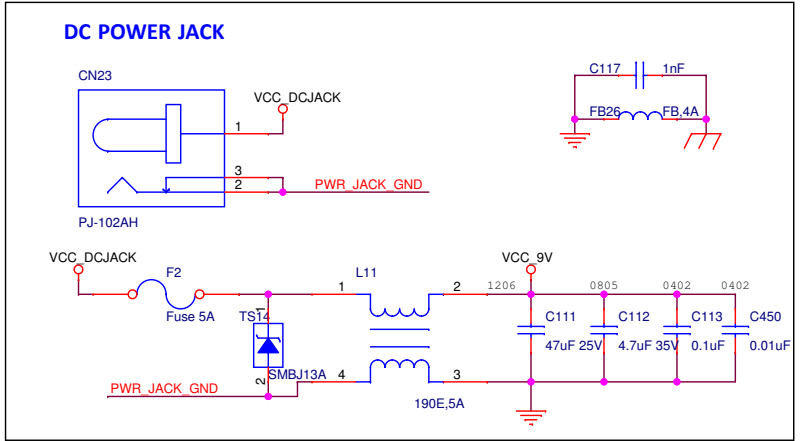
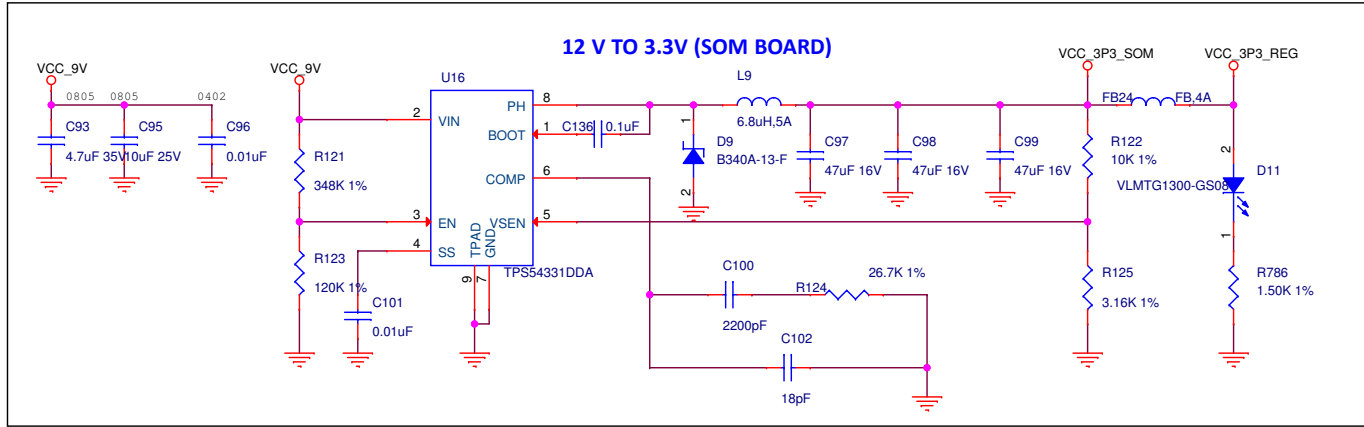
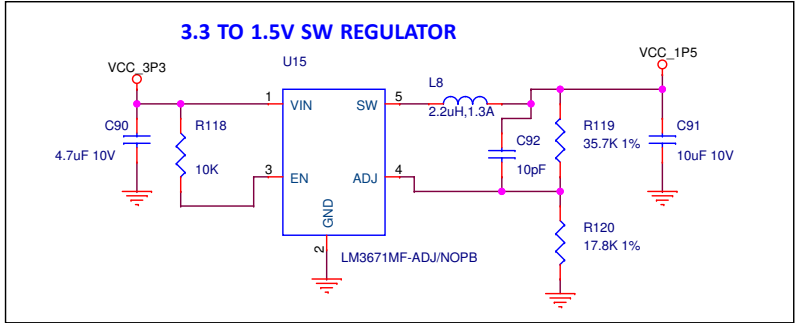
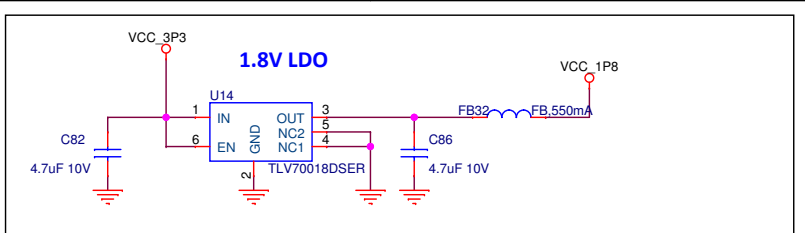
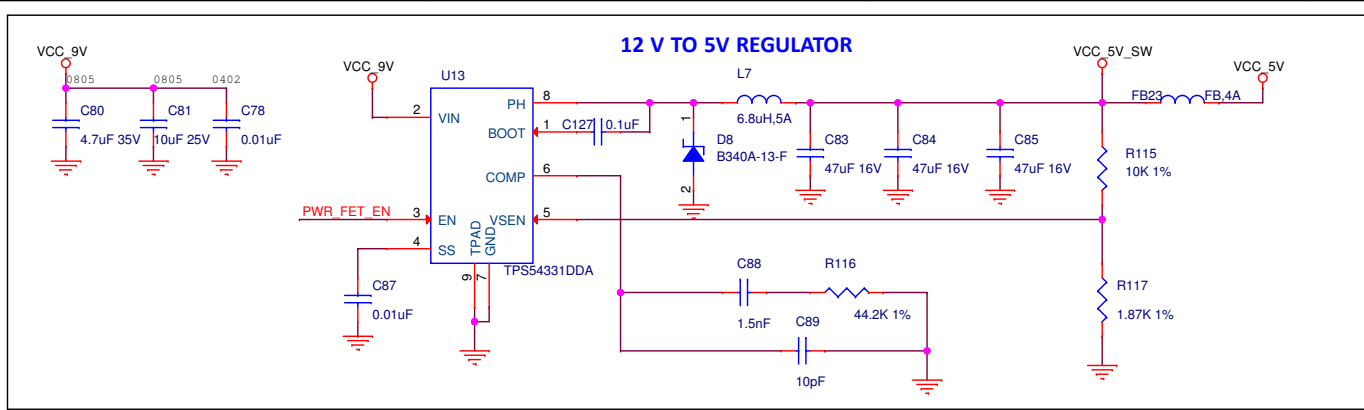




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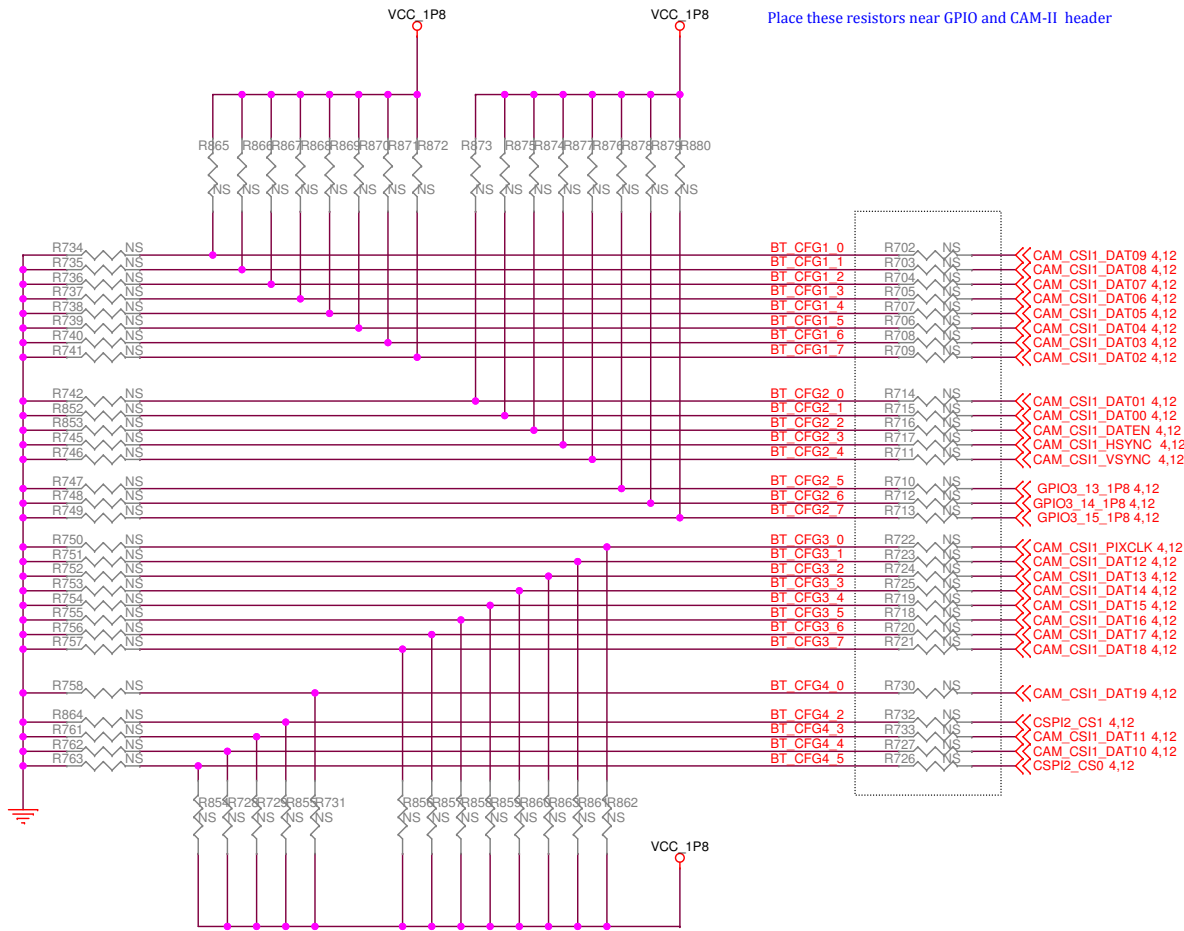


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	AUDIO CODEC ,OTG & SWITCHES	
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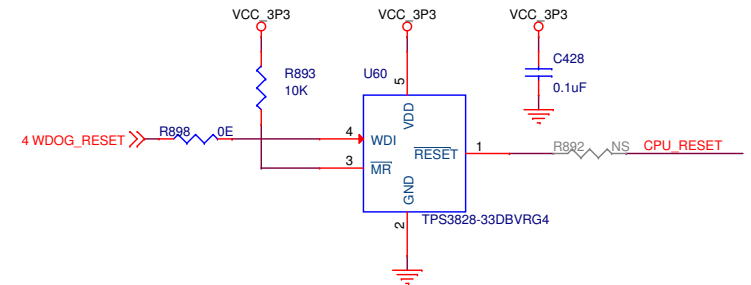


Boot Configuration Select

Place these resistors near GPIO and CAM-II header

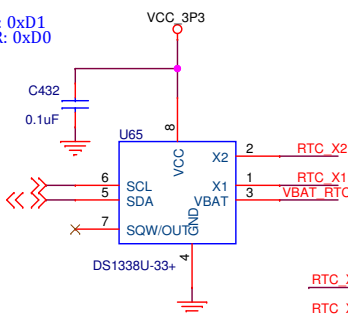


WATCH DOG RESET

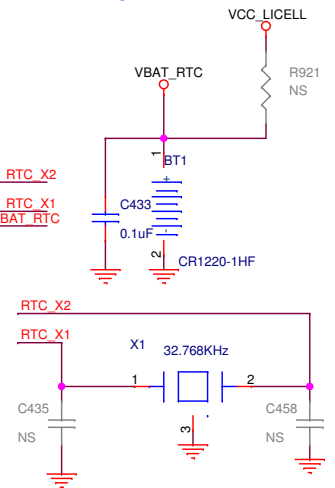


REAL TIME CLOCK

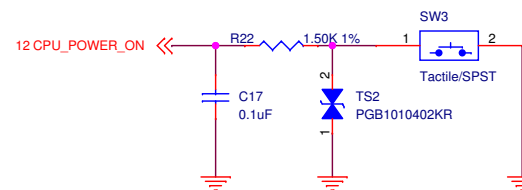
I2C READ ADDR : 0xD1
I2C WRITE ADDR: 0xD0



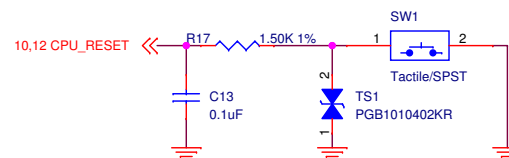
RTC BATTERY



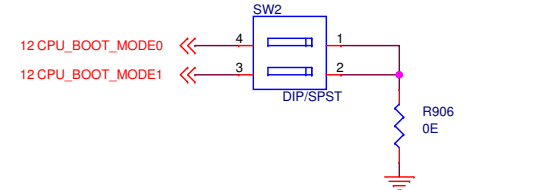
CPU ON/OFF SW



RESET INPUT



CPU BOOT MODE CONFIG



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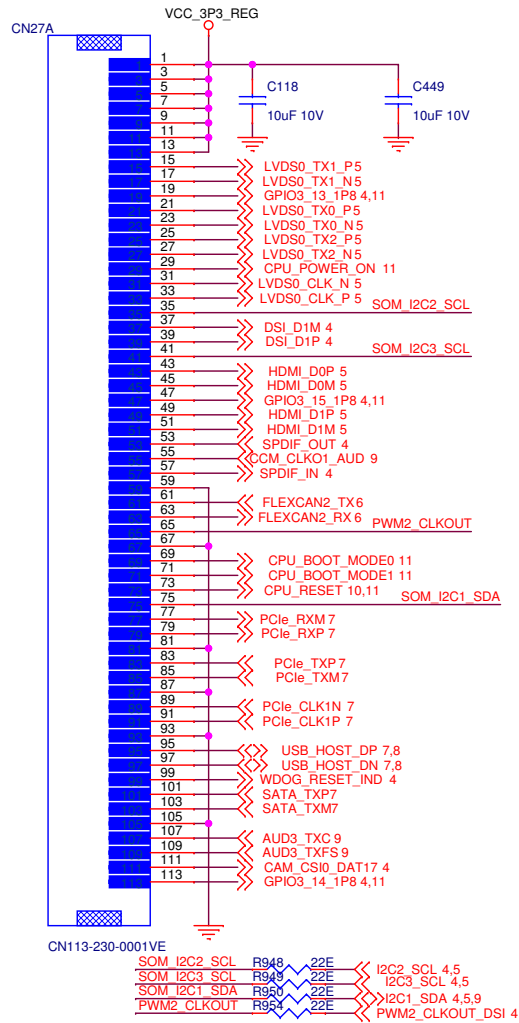
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BOOT CONFIGURATION

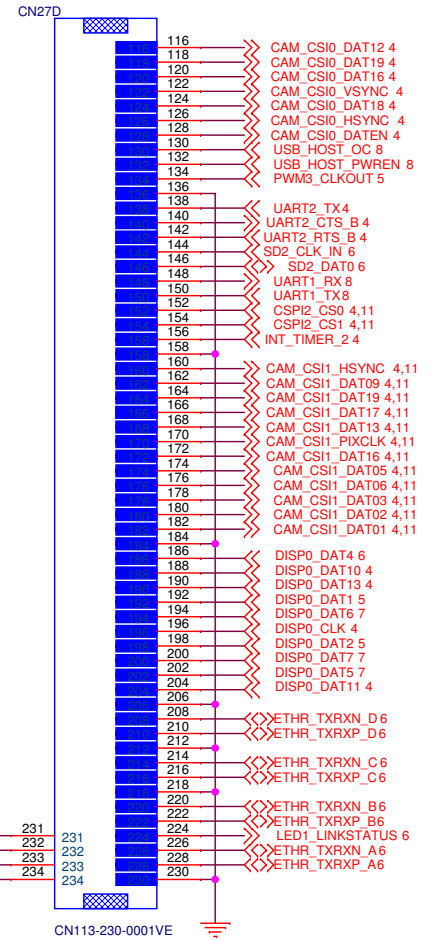
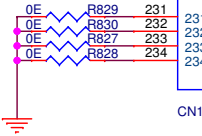
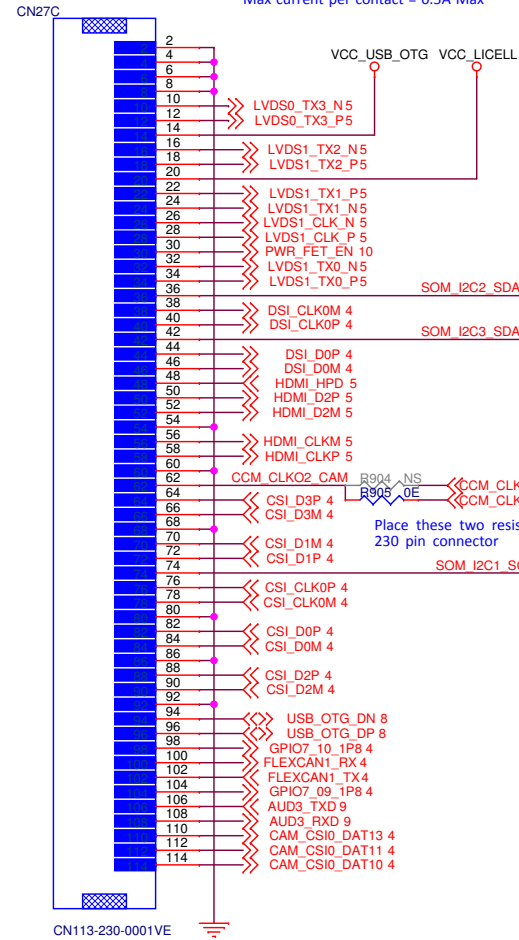
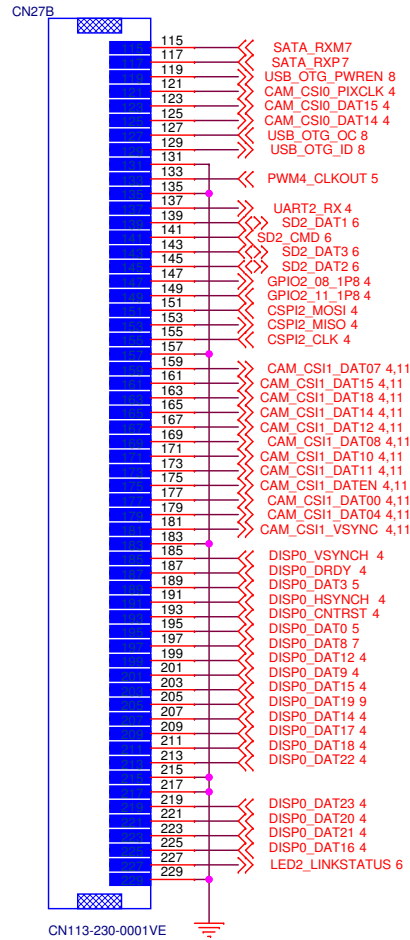
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Max current per contact = 0.5A Max



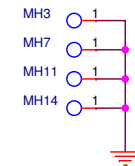
Max current per contact = 0.5A Max



BASE BRD MOUNTING HOLE



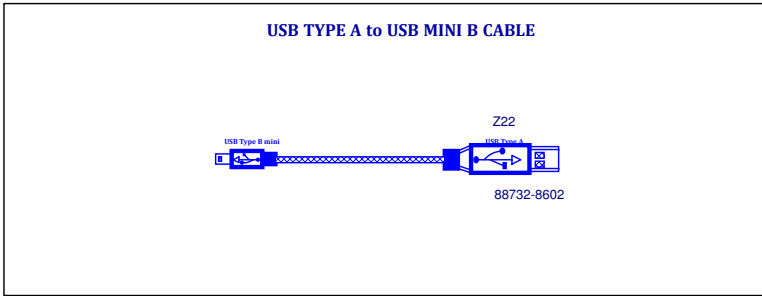
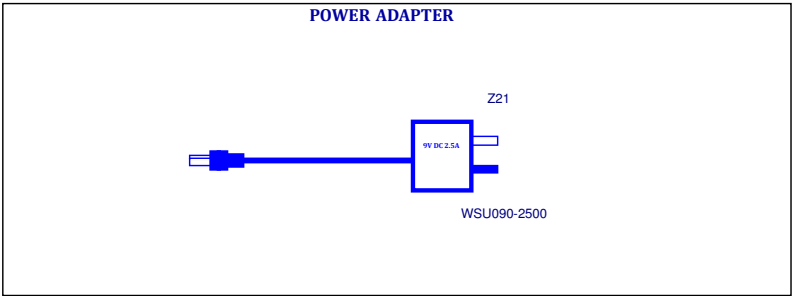
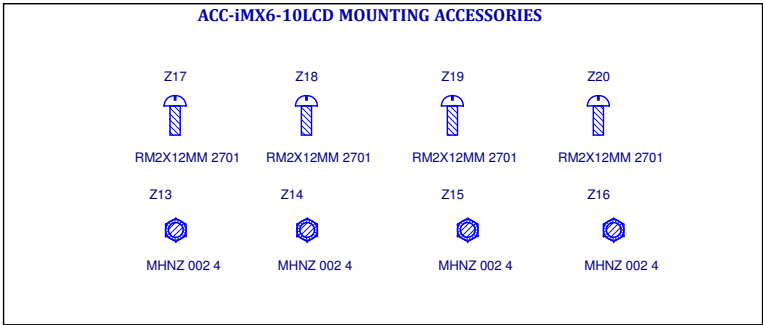
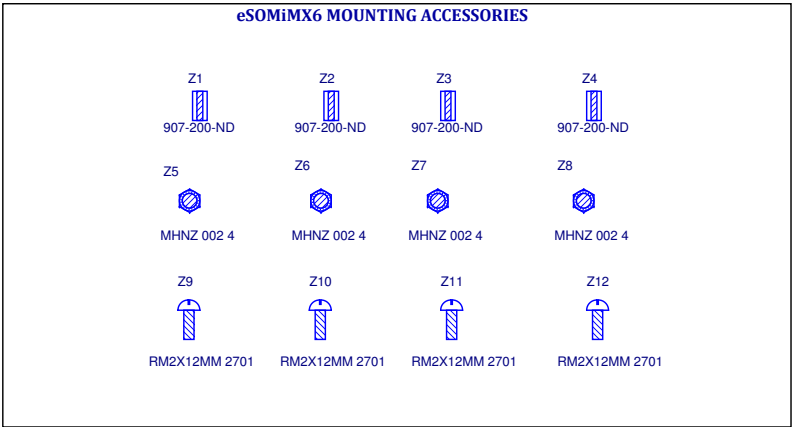
LVDS MOUNTING HOLE



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Rev No	Date	Descript i on	Remarks
A	12 SEP 2014	Initial Release	
B	16 OCT 2014	Page NO: 4 U68 , Level translator added for UART2 interface to provide option for 1.8V and 3.3V I/O FB43,FB42 ,C455,C456, R970,R972,R969,R974,R975,R971,R973 are added	
C	09 DEC 2014	Page NO: 5 LVDS1_INT and LVDS2_INT signals are changed to bidirectional. U46 changed from 4 bit to 2 bit buffer C18 changed from 47uF to 10uF R347,R348,R349,R350,R978,R979,Q8,Q7 are added Page NO: 8 UART Bridge changed from Self Powered to USB Bus powered D13, R980 added Page NO: 10 U69 , Open drain single bit buffer added to reset the audio codec when RESET switch is pressed R981 added	

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