SHIKHARA

Tapeout Signoff

**Table of Contents**

[1 Revision History 4](#_Toc472326490)

[2 Sign-off Approval 5](#_Toc472326491)

[3 Team 6](#_Toc472326492)

[4 Project Sign-off Description 7](#_Toc472326493)

[5 Bug Tracker Verdict / Waivers 10](#_Toc472326494)

[6 Logic Gate Counts and Memories – RFQ Vs Actual 13](#_Toc472326495)

[6.1. Module gate Count 13](#_Toc472326496)

[7 Final Review Checklist 15](#_Toc472326497)

[7.1 Functional Spec/HRM 15](#_Toc472326498)

[7.2 ASIC Architecture 15](#_Toc472326499)

[7.3 Micro-architecture 15](#_Toc472326500)

[7.4 ASIC Verification Plan 15](#_Toc472326501)

[7.5 ASIC Verification Results 16](#_Toc472326502)

[7.6 Functional coverage checklist 16](#_Toc472326503)

[7.7 ASIC Pin-out Review 16](#_Toc472326504)

[7.8 Package Review 17](#_Toc472326505)

[7.9 Synthesis and Final Netlist 17](#_Toc472326506)

[7.10 Software Architecture 18](#_Toc472326507)

[7.11 Software Code and Operations Review 18](#_Toc472326508)

[7.12 Software Reference Manual 18](#_Toc472326509)

[8 Compliance Reports 19](#_Toc472326510)

[9 Design Rule Checklist 20](#_Toc472326511)

[10 Package Details 26](#_Toc472326512)

[10.1 Pad List 26](#_Toc472326513)

[10.2 Pad Diagram 26](#_Toc472326514)

[10.3 Pin Diagram 26](#_Toc472326515)

[10.4 Pin Description 26](#_Toc472326516)

[10.5 Bonding Description 26](#_Toc472326517)

[10.6 Bonding Diagram 26](#_Toc472326518)

[11 Package Outline 27](#_Toc472326519)

[12 Verification Reports 28](#_Toc472326520)

[13 Application Testing Reports 28](#_Toc472326521)

[14 Performance Reports 28](#_Toc472326522)

[15 Synthesis Check-list/ Reports 28](#_Toc472326523)

[16 Shikhara Project Description 29](#_Toc472326524)

[17 Shikhara Project Features 31](#_Toc472326525)

[18 Shikhara Block Diagram 33](#_Toc472326526)

[19 Shikhara Core Partitions 35](#_Toc472326527)

[20 Bootstrap Pins 37](#_Toc472326528)

[21 Modes and Selections 38](#_Toc472326529)

[22 Paths 39](#_Toc472326530)

[23 Library Path 40](#_Toc472326531)

[24 ECO 41](#_Toc472326532)

[25 Area with Post Layout Database 42](#_Toc472326533)

[26 ATPG Coverage Analysis 43](#_Toc472326534)

[27 CLOCKS IN DESIGN: 43](#_Toc472326535)

[28 EEPROM Interface: 43](#_Toc472326536)

[29 Verification Reports 43](#_Toc472326537)

# Revision History

|  |  |  |
| --- | --- | --- |
| *Rev* | *Date* | *Description* |
| 0.1 | 16-01-2017 | Initial Version |
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# Sign-off Approval

|  |  |  |
| --- | --- | --- |
| ***Designation*** | ***Name*** | ***Signature & Date*** |
| **Project Manager** | Vishwanath Linga |  |
| **Design Manager** | Vishwanath Linga |  |
| **Verification Manager** | Narendar Raju |  |
| **Synthesis & STA Manager** | Prabhakar |  |
| **Software Manager** | Arivendu Bhardwaj |  |
| **Systems & Apps Manager** | Siva Prakasam |  |
| **Vice President – Engineering** | Vishwanath Linga |  |
| **Chief Financial Officer** |  |  |
| **Company Secretary** |  |  |
| **Managing Director / CTO** |  |  |

# Team

**ARCHITECTURE, DESIGN & VERIFICATION**

Vishwanath Linga (Vice President)

Bhanu Prakash

Ramu Cherkupally

Ganga Prasad

Sudhakar

Himavanth

Satya Rajeev

Narendar Raju (Manager)

Bala Raju

Viswanath S

Kiran

Shravan

Bhasakar

Vamsi

**SYNTHESIS & STA**

Prabhakar Moluguri (Manager)

Dhirender Singh

Indu Alasakani

Sumanth Pydi

Vishwanath Jeeligam

**SOFTWARE**

**SYSTEMS & APPLICATIONS**

# Project Sign-off Description

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Product Summary** | | | | | |
| Product Name / Part Number | | |  |  | |
| Number of Pins | | |  | | |
| Supply voltage(s) | | |  | | |
| Package Type | | |  | | |
| Function Description (Brief) | | |  | | |
| Competitor Part(s) | | |  | | |
| Compliance requirements with Industry Standards. | | |  | | |
| Compliance Verified/Waivers | | |  | | |
| Estimated Power Consumption | | |  | | |
| Geometry | | |  | | |
| Tapeout type | | |  | | |
| Cell Library | | |  | | |
| IPs used | | |  | | |
| Area (Total Gate Count) | | |  | | |
| Memories | | |  | | |
| Clock frequencies | | |  | | |
| Spares Capability for ECOs | | |  | | |
| BIST capabilities | | |  | | |
| Foundry/Fab | | |  | | |
| Test/debug hooks and features | | |  | | |
| Special Cells (if any) | | |  | | |
| **Design Process Checklist** | | | | | |
| RTL Verification Status | |  | | | |
| Code Coverage index | |  | | | |
| Lint Report | |  | | | |
| Regression Test Count (Attach list) | |  | | | |
| Design guide checklist (ATTACH LIST) Q&A | |  | | | |
| Synthesis & Post Layout Checklist (Attach list ) Q&A | |  | | | |
| Gate Level Sims status | |  | | | |
| FPGA Testing Status  (Attach Test matrix results ) | |  | | | |
| Performance Checks (if applicable) data | |  | | | |
| EXCEPTIONS, IF ANY, IN TEST PLAN (Specify in Appendix, if many to list here) | |  | | | |
| **Synthesis Checks** | | | | | |
| i) Critical Paths (enclose list) | |  | | | |
| ii) Clock skews (enclose list) | |  | | | |
| iii) Maximum Fan-out checks | |  | | | |
| iv) Static Timing Analysis  (attach report) | |  | | | |
| v) Synopsys Warnings report (final) attach list if any | |  | | | |
| vi) Final Gate Count | |  | | | |
| vii) Die Size estimate (final) | |  | | | |
| viii) Pad level AC timings (for System application) check | |  | | | |
| ix) ) Pad level DC timings (for System application) check | |  | | | |
| x) ) Pad level rise – fall timings (for System application) check | |  | | | |
| Power down mode checks (if applicable) | |  | | | |
| **Post Layout Simulation status** | | | | | |
| i) Fast | |  | | | |
| ii) Slow | |  | | | |
| iii) Post Layout Sims warning  checkout (attach list) | |  | | | |
| iv) Additional Relevant data on GL/Post layout Sims | |  | | | |
| Test Vectors | |  | | | |
| **Reset Phase Simulation Check** | | | | | |
| i) Clocks | |  | | | |
| ii) Pad Control Logic | |  | | | |
| iii) Internal Resets | |  | | | |
| **Simulation Models** | | Internal | | | External |
| Real world system correlation | |  | | |  |
|  | |  | | |  |
| **Explicit/Implicit Limitation Statement** | | | | | |
| None | | | | | |
| **Database and Archive Details** | | | | | |
| FPGA & ASIC RTL files congruency verified | Done | | | | |
| Bug List Status Open /Total |  | | | | |
| Final Net list Name |  | | | | |
| Database Directory Path |  | | | | |
| Synthesis Directory path |  | | | | |
| SW Drivers/Tests database path |  | | | | |
| Post Layout Simulation Warnings List |  | | | | |
| QA report |  | | | | |
| Composite Database Backup CD(s)Volume Name & number |  | | | | |

# Bug Tracker Verdict / Waivers

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ***Bug ID*** | ***Bug Status*** | ***Bug Description*** | ***Gating for Tapeout*** | ***Severity\**** | ***Remarks*** |
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| --- | --- |
| ***Severity\**** | ***Definition*** |
| blocker | Prevents function from being used, no work-around, blocking progress on multiple fronts |
| critical | Prevents function from being used, no work-around |
| major | Prevents function from being used, but a work-around is possible |
| normal | A problem making a function difficult to use but no special work-around is required |
| minor | A problem not affecting the actual function, but the behavior is not natural |
| trivial | A problem not affecting the actual function, a typo would be an example |
| Enhancement | Desirable feature |

# Logic Gate Counts and Memories – RFQ Vs Actual

|  |  |  |
| --- | --- | --- |
|  | **RFQ** | **Actual** |
| Digital gate count |  |  |
| Memory RAM bits |  |  |

|  |  |  |
| --- | --- | --- |
| ***Name*** | ***RFQ Gate count (K)*** | ***Actual Gate count (K)*** |
|  |  |  |
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Memories details can be found in the following document.

**Shikhara/doc/arch\_doc/Shikhara\_Memories.xls**

## Module gate Count

|  |  |  |
| --- | --- | --- |
| ***Instance Name*** | ***Gate Count***  ***(Including all IPs and Memories)*** | ***Gate Count***  ***(Excluding all IPs and Memories)*** |
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# Final Review Checklist

## Functional Spec/HRM

Remarks:

## ASIC Architecture

Remarks: NIL

## Micro-architecture

**List of all blocks/sections that are to be reviewed in the design**

|  |  |  |
| --- | --- | --- |
| ***Block/Design sections to be reviewed*** | ***Done*** | ***Remarks*** |
|  |  |  |
|  |  |  |
|  |  |  |
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## ASIC Verification Plan

## ASIC Verification Results

Review results checklist

|  |  |  |
| --- | --- | --- |
| ***Items*** | ***Done*** | ***Remarks*** |
| **Interface signals observation points** |  |  |
| **Interface electrical handshake observations**  Protocol handshake observations |  |  |
| **Clock distribution Block**  Internal clock source selection and muxing operations  Scan/Test mode selection |  |  |
| **Reset Control**  Internal Reset controller observations  Observation points to verify all of initialization operations |  |  |
| **Chip Interfaces – Bus Name**  Interface electrical handshake observations  Protocol handshake observations |  |  |

## Functional coverage checklist

|  |  |  |
| --- | --- | --- |
| ***Items*** | ***Done*** | ***Remarks*** |
| **Detailed Feature list as per the functional spec** |  |  |

## ASIC Pin-out Review

|  |  |  |
| --- | --- | --- |
| ***Items*** | ***Done*** | ***Remarks*** |
| **Bus/Functional Interfaces – no missing signals with reference to standard usage and external interconnecting devices** |  |  |
| **IO Types checked** |  |  |
| **Drive strength checked** |  |  |
| **Pull-down/pull-up requirements checked** |  |  |
| **Multiplexed modes checked** |  |  |
| **Scan mode pin definitions and muxing** |  |  |
| **Test mode pins and muxing** |  | . |
| **Clock pins** |  |  |
| **Power supply pins – core, IO, analog, reference, etc.** |  |  |

## Package Review

|  |  |  |
| --- | --- | --- |
| ***Items*** | ***Done*** | ***Remarks*** |
| **Pin/Ball assignments – functional pins completed** |  |  |
| **External Interfaces mappings/pin placements match with external components** |  |  |
| **Clock signal placements** |  |  |
| **Signal Integrity analysis for high speed interfaces and differential signals** |  |  |
| **Package thermal analysis meets the power requirement** |  |  |
| **Bonding options reviewed** |  |  |
| **All package options reviewed** |  |  |
| **Device Power estimation** |  |  |

## Synthesis and Final Netlist

|  |  |  |
| --- | --- | --- |
| ***Items*** | ***Done*** | ***Remarks*** |
| **Top-level synthesis constraints defined and reviewed** |  |  |
| **Clock domains defined and timing issues reviewed** |  |  |
| **Final chip gate count review** |  |  |
| **Timing closure review** |  |  |
| **DFT/Scan structure and timing review** |  |  |
| **BIST structure and timing review** |  |  |

## Software Architecture

Check list Completed: Yes

Remarks:

## Software Code and Operations Review

Check list Completed: Yes

Remarks:

## Software Reference Manual

# Compliance Reports

Detailed log files generated by the tool:

# Design Rule Checklist

All questions have to be answered with a YES or NO. Deviations should be fully explained in an Annexure at the end of the document.

1. Always have block diagram of the module with a) Clocks b) Reset paths, and timing waveforms CLEARLY drawn out.

|  |  |
| --- | --- |
| **YES** | NO |

2. Have a list of input and output ports with timing and Fan-out constraints.

|  |  |
| --- | --- |
| **YES** | NO |

3. Have the state transition diagrams of state machines clearly specified beforehand.

|  |  |
| --- | --- |
| **YES** | NO |

4. All module outputs must be registered, as far as possible. Ensure partitioning to this effect BEFORE RTL coding.

|  |  |
| --- | --- |
| **YES** | NO |

**Comment: Since this is an ASIC and all the modules are in under our control**

5. All module inputs must be registered except in special cases. Ensure partitioning to this effect BEFORE RTL coding.

|  |  |
| --- | --- |
| **YES** | NO |

**Comment: Since this is an ASIC and all the modules are in under our control**

6. All module outputs must have fan-out of 1. That is, an output should not drive any internal nodes.

|  |  |
| --- | --- |
| YES | NO |

7. Reset input to a module should be registered. Ensure that all resets are asynchronously applied and synchronously released. That is, the trailing edge of the reset should be synchronous with respect to the domain clock. EVERY MODULE, IDEALLY, MUST BE CAPABLE OF BEING INDEPENDENTLY RESET THROUGH A SOFTWARE BIT. THIS GREATLY FACILITATES THE SILICOON DEBUG PROCESS

|  |  |
| --- | --- |
| YES | NO |

8. All nodes must have fan-out less than 16.

|  |  |
| --- | --- |
| **YES** | NO |

9. No latches. This is to simplify timing analysis.

|  |  |
| --- | --- |
| YES | **NO** |

10. Clocks must not be locally buffered or synthesized, since clock tree balancing ends at a gate/flop.

|  |  |
| --- | --- |
| YES | NO |

11. Clocks must only go to positive edge triggered flops.

|  |  |
| --- | --- |
| **YES** | NO |

12. Chip periphery logic must be partitioned in a separate module. No Verilog code should exist outside the module level.

|  |  |
| --- | --- |
| **YES** | NO |

13. Use of tri state busses should be avoided. This is to avoid stray current paths and undefined levels from causing random logic behavior. If used, enables must be FULLY decoded and a disable input must be available as a primary input to prevent conflicts.

|  |  |
| --- | --- |
| YES | NO |

14. All independent clocks must be drive-able from an external pin in test mode.

|  |  |
| --- | --- |
| **YES** | NO |

15. Asynchronous outputs must be registered.

|  |  |
| --- | --- |
| **YES** | NO |

16. Asynchronous inputs must be registered. Control inputs must go through synchronizer logic.

|  |  |
| --- | --- |
| **YES** | NO |

17. Register to register path delays of asynchronous signals (the two previous rules convert all paths between two asynchronous clocks domains to be register-to-register paths) must be less than half clock period of the higher of the two clock periods. This applies to paths originating from either of the two clock domains.  This rule is required to allow the chip to run in synchronous fashion on the tester.

|  |  |
| --- | --- |
| YES | NO |

18. Write-through read is not allowed for any rams.

|  |  |
| --- | --- |
| YES | NO |

19. If using a ram as data buffer between two asynchronous clock domains, the output data should be registered before being used. The purpose is to ensure that asynchronous inputs transition synchronously with the destination clock domain.

|  |  |
| --- | --- |
| YES | NO |

20. All rams must be power-downed in any clock that they are not being read or written. Implement the signal even if you know that the targeted ram does not support power down.

|  |  |
| --- | --- |
| YES | NO |

21. No synchronous reset logic is allowed. This affects testability.

|  |  |
| --- | --- |
| YES | NO |

22. Target synthesis clock periods. Use a 25% clock guard band to account for PRE to POST layout timing differences. Allow a 500 ps clock skew and 500 s clock jitter for all clocks.  Synthesis Clock period = (True period)\*0.75 - 0.5 - 0.5.

|  |  |
| --- | --- |
| YES | NO |

23. If a set\_max\_delay constraint is needed for top level timing always have the origination point be from a clock.

|  |  |
| --- | --- |
| YES | NO |

24.  Implement 1 - hot state-machines wherever possible by explicitly instructing Synopsys that your state-machine is one hot. This will help making ECO implementation easier.

|  |  |
| --- | --- |
| YES | NO |

25. No multi-cycle paths: this enables at speed structural test.

|  |  |
| --- | --- |
| YES | NO |

26. All primary IO pins must be at the top level in the hierarchy

|  |  |
| --- | --- |
| YES | NO |

27. Avoid internally derived resets.

|  |  |
| --- | --- |
| YES | NO |

28. Avoid using structural, library specific instantiations. This will defeat the foundry independent nature of high level coding.

|  |  |
| --- | --- |
| YES | NO |

29. Avoid asynchronous feedback paths, self timed or self clocked logic.

|  |  |
| --- | --- |
| YES | NO |

30. There should be independent bypass clocks for each domain.

|  |  |
| --- | --- |
| YES | NO |

31. Use lint checking on your code. Make sure you understand all the warnings, and don’t turn these off unless you know what you are doing. HAVE A CERTIFIED COPY OF THE FINAL LINT RUN ON RTL ARCHIVED.

|  |  |
| --- | --- |
| YES | NO |

32. Always use synchronization AND handshake when signals have to communicate across clock domains. S1, from domain 1 on clk1, must be held and cleared only after ensuring that it is double synchronized, seen as S2 in domain 2 on clk2, and returns into domain 1 after re-synchronizing on clk1.

|  |  |
| --- | --- |
| YES | NO |

33. TAKE GREAT CARE WHEN SETTTING OR RESETTING CONTROL REGISTER BITS – ENSURE THAT SUCH CHANGES DO NOT AFFECT LEGAL STATE MACHINE OPERATIONS OR CAUSE ILLEGAL TRANSACTIONS ON SYSTEM INTERFACES, OR CAUSE LOGIC BLOCKS TO HANG OR ENTER INDETERMINATE CONDITIONS.AS FAR AS POSSIBLE, ‘GRACEFUL’ SYNCHRONIZED ASSERTION AND DEASSERTION SEQUENCES MUST BE IMPLEMENTED.

|  |  |
| --- | --- |
| YES | NO |

34. NO STATE MACHINE SHOULD HAVE MORE THAN 16 states. 20 is absolute maximum, under exceptional conditions.

|  |  |
| --- | --- |
| **YES** | NO |

35. As far as possible, avoid one clock wide pulse signaling to different logic functions. The pulse should be held and removed only when the destination logic block has seen it.

|  |  |
| --- | --- |
| YES | NO |

36. Identify signals with critical timings and delays clearly in the RTL. For every module, identify the clock frequency and maximum And minimum delays allowed for signals with that clock. PREPARE A LIST FOR SYNOPSYS.

|  |  |
| --- | --- |
| YES | NO |

37. Always try and use edge detection and generate pulses out of transitions for processing, avoid using levels for signal processing.

|  |  |
| --- | --- |
| YES | NO |

38. Never make design assumptions based on frequency of operation. If different frequencies (f1 & f2) are used, then test the following cases:

F1 and f2 at application frequencies

F1 very large, f2 very small

F1 very small, f2 very large

F1 and f2 very close to each other (at any one of the application Frequencies).

|  |  |
| --- | --- |
| YES | NO |

39. Plan for ECOs. Every module must have spare logic that has about 10 flip flops, 20 combinational gates of every type and reset and clock signals going into it. Put a DON’T TOUCH on this with SYNOPSIS so that spare gates are available for ECOs if needed. Take additional steps to inform the floor planners to distribute this logic evenly around the modules under consideration.

|  |  |
| --- | --- |
| YES | NO |

40. Always simulate the design as a device at the System Level realization (i.e with PADs and PAD control logic implemented) and the DUT representing a SYSTEM component. ENSURE THAT THE SIMULATION REPLICATES ACTUAL SYSTEM LEVEL BEHAVIOR. AT RESET (ESPECIALLY ON BUSSES) STUDY SEVERAL SYSTEM LEVEL SAMPLES OF TIMINGS USING LOGIC ANALYZER AND SCOPE AND IMPLEMENT ACCURATE MODELS. DO NOT CHANGE TIMINGS WITHOUT UNDERSTANDING WHY.

|  |  |
| --- | --- |
| YES | NO |

41. Evaluate and implement test buses that allow for internal nodes to be brought out on device pins WITHOUT affecting system behavior. This can be done by using a test mode register that muxes out internal signals from different modules onto device pins. Alternately, bring out state machine vectors onto registers that can be read through SW – this is useful in debugging ‘hang’ or lockup conditions, under certain situations.

|  |  |
| --- | --- |
| YES | NO |

42. Have interconnect to all IPs been verified and double checked and agreed to by Vendor?

|  |  |
| --- | --- |
| YES | NO |

43. Have verification models used in RTL been verified and correlated on an actual system? Have all varieties and vendors been modeled accurately?

|  |  |
| --- | --- |
| **YES** | NO |

44. Has the robustness of the design been evaluated with illegal and non confirming sequences but similar sequences – for e.g. correct sequence maybe 0011001100 for 2 microseconds each – this can be generated by having 1 microsecond pulse width or a sequence like 11001100 etc?

|  |  |
| --- | --- |
| YES | NO |

45. Has a conscious effort been made in simulation to verify state machine transitions through all allowed states. Check with the coverage tool if needed.

|  |  |
| --- | --- |
| YES | NO |

46. Has the list of simulation specific settings/assumptions (setting a bit specially for simulation, disabling/enabling a specific node, unused signals connected one way or other, specific Environment/logic design Alterations made to get simulation working without knowing why) been made?

|  |  |
| --- | --- |
| YES | NO |

# Package Details

## Pad List

## Pad Diagram

## Pin Diagram

## Pin Description

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| ***Pin No*** | ***Pin*** | ***Pad*** | ***Group*** | ***Frequency***  ***(MHz)*** | ***Load***  ***(pf)*** | ***Drive Strength***  ***(mA)*** |
|  |  |  |  |  |  |  |

## Bonding Description

## Bonding Diagram

# Package Outline

# Verification Reports

# Application Testing Reports

# Performance Reports

# Synthesis Check-list/ Reports

# Shikhara Project Description

Shikhara is a 32 bit high performance low power RISC microprocessor based SoC designed for mobile applications. This SoC supports upto 128 bit internal bus architecture. The internal bus architecture comprises of AHB, AXI and APB bus structures. It also includes hardware accelerators for video processing, audio processing, and supports graphics accelerator with MALI400 GPU.

The memory system has dual external memory ports. Static Memory Controller can be configured to interface with NAND Flash and SRAM/NOR-Flash. LPDDR2/DDR3 controller is used to interface with external DDR memory.

Shikhara also includes hardware peripherals such as

* LCD controller
* UART Controller
* 8-channel DMA
* Dual Timers
* Watchdog Timer
* Real Time Clock
* General Purpose I/O Ports
* I2S-Bus interface
* I2C-Bus interface
* USB3.0 Host Controller
* USB3.0 DRD Controller operating at Super speed (5Gbps), High speed (480Mbps) and Full speed(12Mbps)
* HDMI 1.4a Tx controller
* Graphics Processing Unit (MALI-400 MP)
* SD Host & High Speed Multi-Media Card Interface
* MIPI CSI-2 Interface
* MIPI DSI Interface
* CAN Interface
* GNSS
* SPI Controller
* KMI Interface
* PLLs for clock generation

Shikhara uses ARM Cortex A9 MPcore configured to dual core. It includes separate 32KB Instruction and 32KB data caches. It also includes a full MMU to handle virtual memory management. The ARM Cortex A9 MPcore includes support for JAVA acceleration. The Cortex-a9 Processor implements ARMv7-A architechture and runs 32-bit ARM instructions, 16-bit and 32-bit Thumb instructions, and 8-bit Java bytecodes in Jazelle state.The ARM Cortex A9 MPcore includes a dedicated vector floating point coprocessor allowing efficient implementation of various encryption schemes as well as high quality 3D graphics applications using Neon MPE. The standard AMBA bus architecture allows the Shikhara to support many of the industry standard Operating Systems.

# Shikhara Project Features

Following is the summary of Shikhara Project features:

**CPU Platform**

* ARM Cortex A9 dual core (800MHz – Processor subsystem), 32KB L1 D-Cache, 32KB L1 I-Cache, 512KB L2 Cache.

**Video Processing Unit**

* ARC700 (400MHz-Video Sub system)

**Internal On chip memories**

* 64 KB ROM & 64KB RAM, 512KB L2 Cache RAM
* 64 KB RAM for Video ARC 700

**External memory interfaces**

* NAND/NOR/SRAM memory, LPDDR2/DDR3 SDRAM, SDMMC and SDIO

**Communication & connectivity**

* USB 3.0 DRD Controller
* USB3.0 Host Controller
* HDMI 1.4a Tx Controller
* Four UARTs
* Four General purpose input outputs
* One I2S (Master)
* Three I2C
* Two SPI Controllers.
* One MIPI CSI-2 Receiver.
* One MIPI DSI Transmitter
* One CAN Controller.

**System functions**

* Multiple power domains
* Clock gating
* Power gating
* Two DMA Controllers
* Two Dual Timers
* Watch Dog Timer
* JTAG interface for ARM debug access
* Multi Format video codec provides encoding & decoding of MPEG-4/H.263/H.264 up to 30fps

# Shikhara Block Diagram

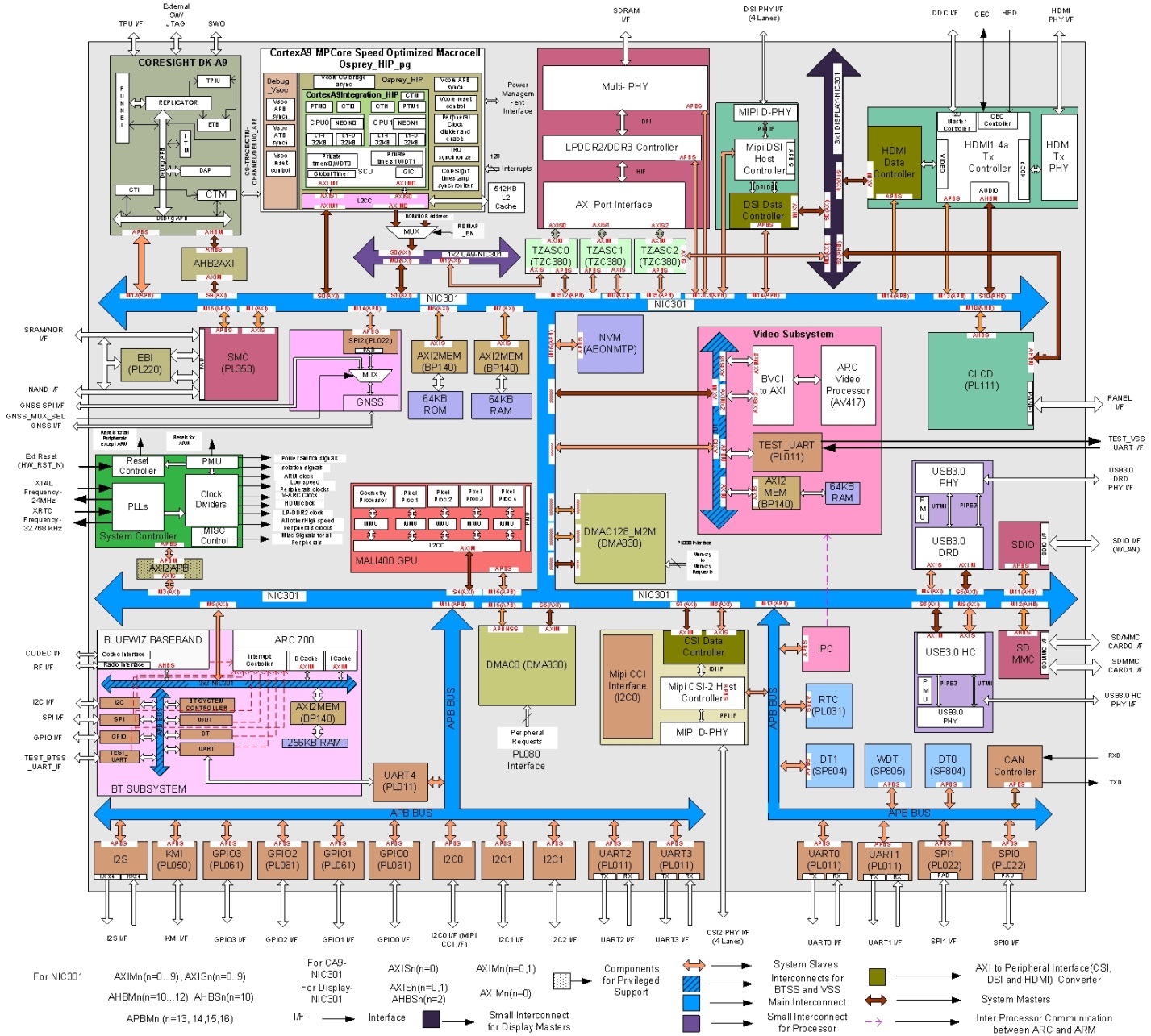


Figure 18.1 Shikhara SoC Architecture Diagram



Figure 18.2 Shikhara NIC connectivity

# Shikhara Core Partitions

Table 19.1 Shikhara Core Partitions

|  |  |  |  |
| --- | --- | --- | --- |
| **Sl. No:** | **Partition** | **Instantiated design files** | **Comments** |
| 1 | Shikhara\_core\_part1.v | m400\_mp\_toplevel.v |  |
| 2 | Shikhara\_core\_part2.v | video\_sub\_system.v |  |
| 3 | Shikhara\_core\_part3.v | DWC\_usb3\_drd\_top.v  DWC\_usb3\_host\_top.v |  |
| 4 | Shikhara\_core\_part4.v | SDIO\_DWC\_mobile\_storage.v  pl330\_dmac\_top.v  acc\_dbb2\_top.v(GNSS)  btSubSys.v |  |
| 5 | Shikhara\_core\_part5.v | pl353\_smc\_PL35xr2\_e41\_44221.v  pl330\_dmac128\_top.v  Ebi.v  SDMMC\_DWC\_mobile\_storage.v  Clcd.v  DWC\_hdmi\_tx\_top.v  Osprey.v (ARM hard macro)  DWC\_mipi\_csi2\_host\_top.v  DWC\_mipi\_dsi\_host\_top.v  pl301\_ahb2axi.v  pl301\_shikhara\_NIC301\_display.v |  |
| 6 | Shikhara\_core\_part6.v | lpddr2\_top.v  pl380\_tzasc\_TZC380r0p1\_3f1.v | 3 instances of pl380\_tzasc\_TZC380r0p1\_3f1 |



Figure 19.1 Shikhara Core Partition

# Bootstrap Pins

Table 20.1 Bootstrap Pins

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| ***Pin No.*** | ***Pin Name*** | **Boot Strap** | **External Connection** | **Internal Connection** | ***Description*** |
| 1 | CLD\_9 | debug\_  auth[3:0] -  Cortex-A9/Coresight Debug Authentication Signals | Not Connected | Pull Down | 0 - (SPNIDEN)Secure Privilege Non-  Invasive Debug Disabled 1 - (SPNIDEN)Secure Privilege Non-  Invasive Debug Enabled |
| 2 | CLD\_10 | Not Connected | Pull Down | 0 - (SPIDEN)Secure Privilege  Invasive Debug Disabled 1 - (SPIDEN)Secure Privilege  Invasive Debug Enabled |
| 3 | CLD\_11 | Not Connected | Pull Down | 0 - (NIDEN) Non-Invasive Debug  Disabled 1 - (NIDEN) Non-Invasive Debug  Enabled |
| 4 | CLD\_12 | Not Connected | Pull Down | 0 - (DBGEN) Debug Disabled 1 - (DBGEN) Debug Enabled |
| 5 | CLD\_13 | LPDDR/  DDR3 Select | Not Connected | Pull Down | Selects between LPDDR and DDR3 Memory Options '0' Select LPDDR '1' Select DDR3 |
| 6 | CLD\_14 | DEFAULT BOOT OPTION | Not Connected | Pull Down | 0 0 0 0  Production Level Booting  (From NOR ). 1 0 0 0  SPI flash booting from ROM. 1 0 0 1  NOR booting from ROM. 1 0 1 0  SD booting from ROM. 1 0 1 1  NAND 2KB 5 Cycle(0 bit Ecc)  booting from ROM. 1 1 0 0  NAND 2KB 5 Cycle(16 bit  Ecc) booting from ROM. 1 1 0 1  NAND 4KB 5 Cycle(8 bit Ecc)  booting from ROM. 1 1 1 0  NAND 512B 4 Cycle booting  from ROM. |
|  | CLD\_15 | Not Connected | Pull Down |
| 8 | CLD\_16 | Not Connected | Pull Down |
| 9 | CLD\_17 | Not Connected | Pull Down |

# Modes and Selections

Functional Mode Selection

Table 221.1 Functional Mode Selection

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Mode Selection** | SOC\_TEST\_EN | MODE\_SEL\_4 | MODE\_SEL\_3 | MODE\_SEL\_2 | MODE\_SEL\_1 | | MODE\_SEL\_0 |
| NORMAL\_MODE\_0 | 0 | 0 | x | x | 0 | 0 | |
| NORMAL\_MODE\_1 | 0 | 0 | x | x | 0 | 1 | |
| NORMAL\_MODE\_2 | 0 | 0 | x | x | 1 | 0 | |
| NORMAL\_MODE\_3 | 0 | 0 | x | x | 1 | 1 | |
| TB\_MODE | 0 | 1 | x | 0 | 0 | 0 | |
| TRACE\_MODE | 0 | 1 | x | 0 | 0 | 1 | |

Testability mode selection

Table 221.2 Test Mode Selection

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Mode Selection** | SOC\_TEST\_EN | MODE\_SEL\_4 | MODE\_SEL\_3 | MODE\_SEL\_2 | MODE\_SEL\_1 | MODE\_SEL\_0 |
| OSPREY\_DFT | 1 | 0 | 0 | 0 | 0 | 0 |
| L1\_MBIST | 1 | 0 | 0 | 0 | 0 | 1 |
| DFT MODE |  |  |  |  |  |  |
| BIST MODE |  |  |  |  |  |  |
| MBIST MODE |  |  |  |  |  |  |
| JTAG MODE |  |  |  |  |  |  |
| SCAN MODE |  |  |  |  |  |  |

# Paths

# Library Path

* /projects/shikhara\_ips/ips/golden\_version/guc/io\_models/TSMCHOME/digital/Front\_End/verilog/tphn40lpgv2od3\_sl\_210a/tphn40lpgv2od3\_sl\_pwr.v
* /projects/shikhara\_ips/ips/golden\_version/guc/io\_models/TSMCHOME/digital/Front\_End/verilog/tpan40lpgv2od3\_120a/tpan40lpgv2od3.v
* /projects/shikhara\_ips/ips/golden\_version/hdmi\_phy/tsmc\_40lp\_hdmi14txPHY\_3.04e/hdmitxio/tsmc\_40lp\_fc\_hdmitxio\_1.03d/vbm/hdmitxio.v
* /projects/shikhara\_ips/ips/golden\_version/guc/power\_cell\_models/ITCSTDS22A\_160/TSMCHOME/digital/Front\_End/verilog/tcbn40lpbwpcghvt\_130a/tcbn40lpbwpcghvt\_pwr.v
* /projects/shikhara\_ips/ips/golden\_version/guc/power\_cell\_models/ITCSTDS21A\_160\_NVT/TSMCHOME/digital/Front\_End/verilog/tcbn40lpbwpcg\_130a/tcbn40lpbwpcg\_pwr.v
* /projects/shikhara\_ips/ips/golden\_version/guc/power\_cell\_models/ITCSTDS22A\_160\_HVT/TSMCHOME/digital/Front\_End/verilog/tcbn40lpbwpcghvt\_130a/tcbn40lpbwpcghvt\_pwr.v
* /projects/shikhara\_ips/ips/golden\_version/guc/power\_cell\_models/ITCSTDS23A\_160\_LVT/TSMCHOME/digital/Front\_End/verilog/tcbn40lpbwpcglvt\_130a/tcbn40lpbwpcglvt\_pwr.v
* /projects/shikhara\_ips/ips/golden\_version/guc/core\_cell\_models/12track\_mod\_verilog\_models/tcbn40lpbwp12tm1pcg\_130a/tcbn40lpbwp12tm1pcg\_pwr.v
* /projects/shikhara\_ips/ips/golden\_version/guc/core\_cell\_models/12track\_mod\_verilog\_models/tcbn40lpbwp12tm1pcglvt\_130a/tcbn40lpbwp12tm1pcglvt\_pwr.v
* /projects/shikhara\_ips/ips/golden\_version/guc/core\_cell\_models/12track\_mod\_verilog\_models/tcbn40lpbwp12tm1p\_200a/tcbn40lpbwp12tm1p\_pwr.v
* /projects/shikhara\_ips/ips/golden\_version/guc/core\_cell\_models/12track\_mod\_verilog\_models/tcbn40lpbwp12tm1pcghvt\_130a/tcbn40lpbwp12tm1pcghvt\_pwr.v
* /projects/shikhara\_ips/ips/golden\_version/guc/core\_cell\_models/12track\_mod\_verilog\_models/tcbn40lpbwp12tm1plvt\_200a/tcbn40lpbwp12tm1plvt\_pwr.v
* /projects/shikhara\_ips/ips/golden\_version/guc/core\_cell\_models/ITCSTDS20A\_180/TSMCHOME/digital/Front\_End/verilog/tcbn40lpbwplvt\_120a/tcbn40lpbwplvt\_pwr.v
* /projects/shikhara\_ips/ips/golden\_version/guc/core\_cell\_models/ITCSTDS19A\_170/TSMCHOME/digital/Front\_End/verilog/tcbn40lpbwphvt\_120a/tcbn40lpbwphvt\_pwr.v

# ECO

Issue 1

Issue 2

* Muxes and Comb logic is replaced with the Clk Muxes
* Removed inverter between fb\_clk\_in0 and m\_clk0 and added a Phase delay of 50%
* Modified the DWC\_usb3\_pipe\_step\_gasket\_PIPE\_WIDTH4\_host\_0 and DWC\_usb3\_pipe\_step\_gasket\_PIPE\_WIDTH4\_drd\_0 with the below logic to make 2.3c version to 2.8b version of USB PHY

IND2D2BWP U48 (.A1 ( lane\_rx\_valid ) , .B1 (1'b0 ) , .ZN ( n57 ) ) ;

IND2D4BWP U49 (.A1 ( lane\_rx\_valid ) , .B1 ( 1'b0 ) , .ZN ( n58 ) ) ;

# Area with Post Layout Database

Analog IP:

Memory:

# ATPG Coverage Analysis

# CLOCKS IN DESIGN

Clocks in desing details can be found in the following document.

**Shikhara/doc/arch\_doc/Shikhara\_System\_Controller.doc**

# EEPROM Interface:

# Verification Reports

Post Layout Simulation Warnings List