DDR3 Demo for ECP5 VIP Processor Board

Demo User Guide

FPGA-UG-02024 Version 1.1

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DIP	Dual In-line Package
DDR	Double Data Rate
JTAG	Joint Test Action Group
OTF	On-the-Fly
SDRAM	Synchronous Dynamic Random-Access Memory
VIP	Video Interface Platform
USB	Universal Serial Bus

1. Introduction

This document provides technical information and instructions for using the ECP5™ DDR3 demo design. This demo design demonstrates the functionality of the Lattice DDR3 IP core operating at a speed of 400 MHz and 800 Mb/s using the Lattice ECP5 VIP Processor Board. The document includes description of the demo logic circuit, and instructions for running the DDR3 demo.

The ECP5 VIP Processor Board has onboard two modules of 16-bit DDR3 SDRAM. The demo design generates 16-bit test data, and writes it to the onboard DDR3 SDRAM. The design reads the DDR3 SDRAM data and compares it with original expected data. If there is a mismatch between the standard and read data, the design flags an error signal.

The demo design also allows the user to run the design with different parameters using onboard DIP switches.

The demo package includes the following:

- DDR3 IP core configuration files (.sbx)
- Verilog source code for the demo logic design
- Lattice Diamond® implementation project file (.ldf) and preference file (.lpf) for the demo project
- DDR3 demo bitstream file (.bit)

Figure 1.1 shows the top view of the ECP5 VIP processor board and its key components. Figure 1.2 on the next page shows the bottom view of the board.

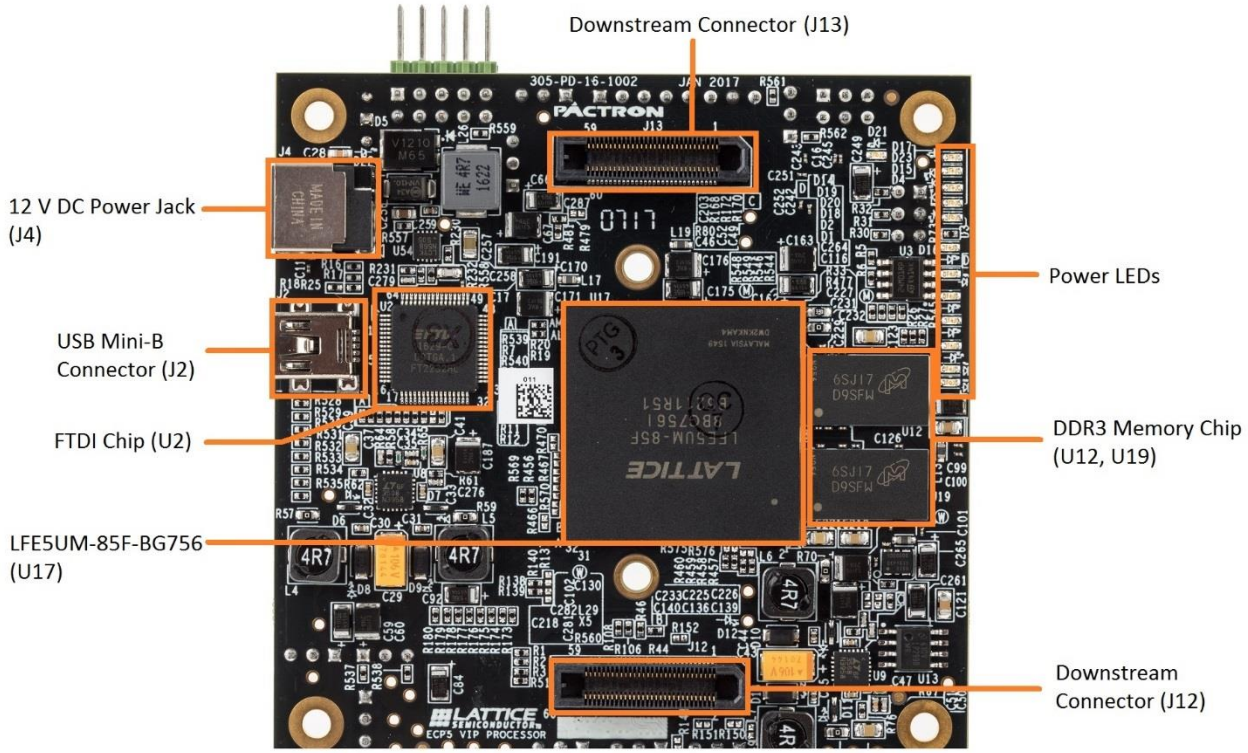

Figure 1.1. Top View of ECP5 VIP Processor Board and its Key Components

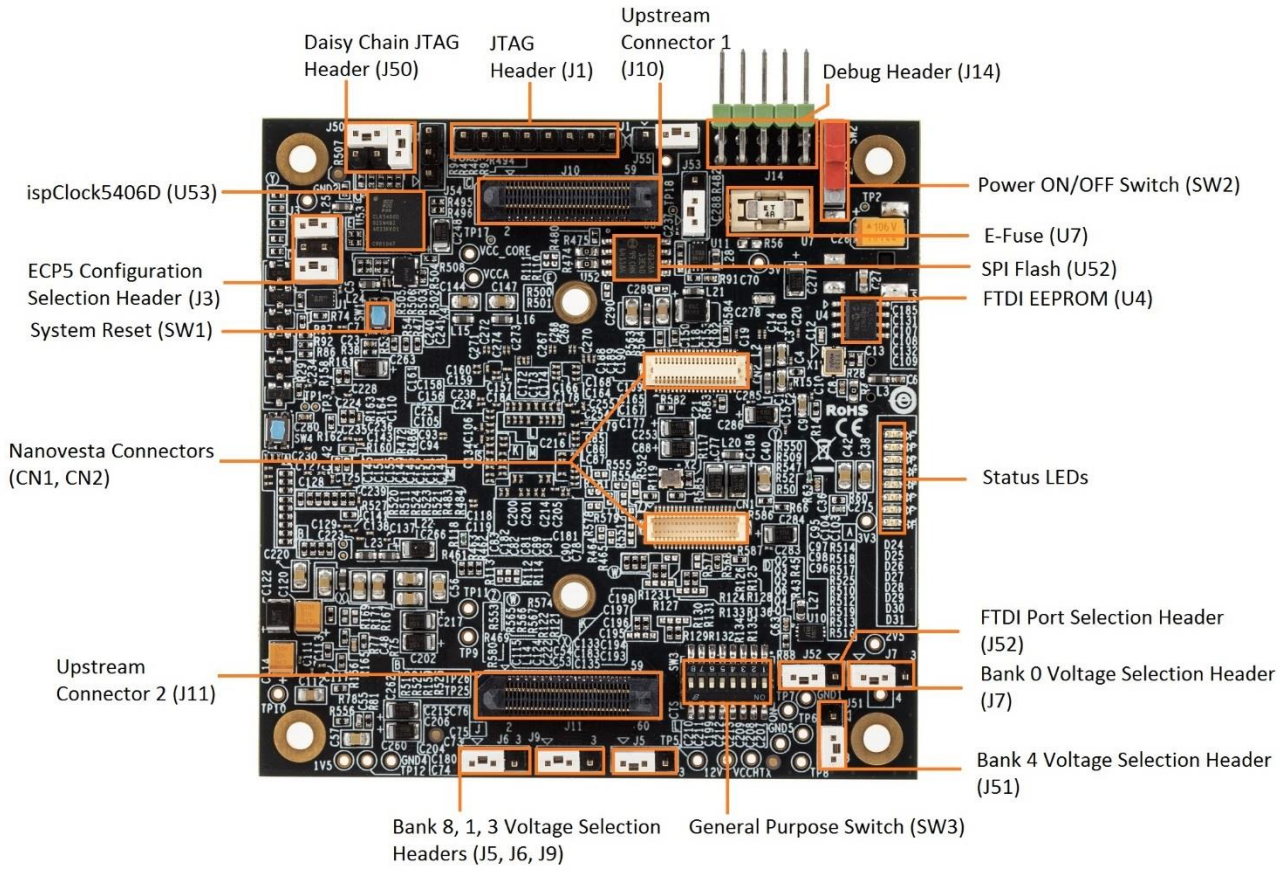

Figure 1.2. Bottom View of ECP5 VIP Processor Board

2. Functional Description

The DDR3 demo design consists of two major parts: a DDR3 controller IP core and the user logic block.

The DDR3 SDRAM controller IP core interfaces to the onboard external DDR3 SDRAM directly and performs control, read and write operations. The user logic block generates test data to be written to the SDRAM. The DDR3 controller then writes the data to the onboard DDR3 SDRAM. The DDR3 controller also reads the data from SDRAM, and passes it to the user logic block. The user logic block compares the read data with the expected data and flags an error if it detects a data mismatch.

The demo parameters can be modified using onboard DIP switches. The status of the running demo design is indicated with onboard LEDs.

The sections below describe the submodules in the user logic design in detail. Figure 2.1 shows the block diagram of the demo design.

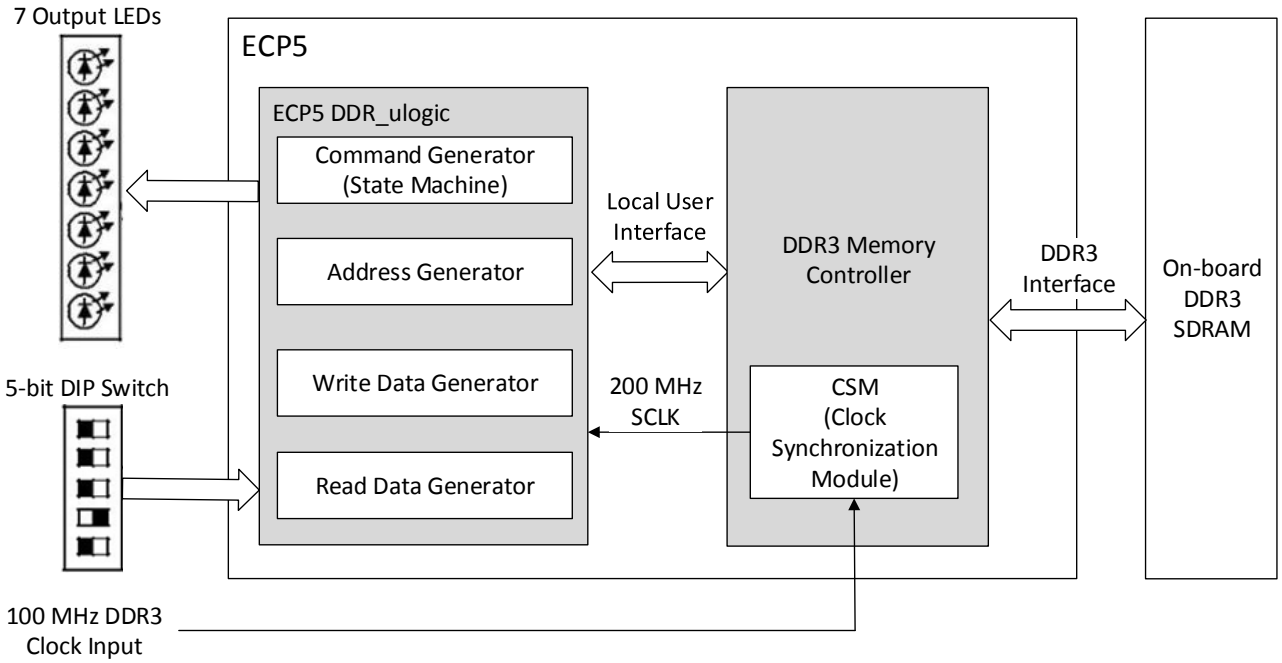

Figure 2.1. DDR3 Demo Block Diagram

2.1. DDR3 IP Core

This demo is supplied with a fully generated DDR3 SDRAM controller IP core. The IP core used to generate the DDR3 controller core is the DDR3 SDRAM controller IP core, version 3.1. You must install version 3.1 before updating and generating the IP core in the demo project. Refer to the Double Data Rate (DDR3) SDRAM Controller IP Core User's Guide (IPUG80) for details on generating the IP Core. The controller generated with this IP core interfaces directly with the external, onboard DDR3 SDRAM and performs control operations. The demo has been designed to support a DDR3 data bus width of 16 bits as the DDR3 memory module on the ECP5 VIP Processor Board is 16 bits wide.

2.2. User Logic

The user logic implemented in the DDR3 demo design provides the following functions:

- Command Generation State machine programs the mode registers and controls DDR3 read and write operation.
- Address generation
- Write data generation
- Read data validation
- Control and observation

2.2.1. Command Generator State Machine

The state machine controls the demo using the user control input through 5 switch inputs (part of the 8-bit DIP switch on the ECP5 VIP Processor Board). When the ECP5 device is programmed or a system reset is applied by pressing the SW1 switch, the state machine programs all DDR3 mode registers (MR0~MR3) based on the user test configuration (DIP switch setting). See Table 5.3 for details on the configuration settings.

Then, it generates a write command sequence. The write command may be repeated up to 32 times using either the command burst feature or multiples of single write commands depending on the user setting. After the write command sequence, a read command sequence is initiated. The read command sequence may also be repeated up to 32 times in the same way as the write command sequence. The read command sequence that follows the write command sequence always includes the same number of commands as the write command sequence. The state machine makes sure that both the write and the following read command sequences are always the same even when the user test configuration is changed at any time during the command sequences. This allows the DDR3 demo to be dynamically reconfigurable.

2.2.2. Address Generation

The address generation block provides the start address for the current user read/write command which is generated by the state machine. When the burst command mode is enabled, the address generation block automatically calculates the next address according to the demo control input.

2.2.3. Write Data Generation

The demo uses either PRBS or sequential data patterns. When PRBS is selected, a 128-bit PRBS pattern generator is connected to the local write data bus to generate a 16-bit DDR3 data pattern. For 16-bit DDR3 data, the lower 64 bits [63:0] of the 128-bit PRBS are allocated to the local data bus.

For the sequential data pattern, the demo design uses only a 32-bit sequential data pattern generator to provide 16-bit DDR3 data. This 32-bit data pattern is allocated to each 32-bit wide local data bus slot. For example, a 16-bit DDR3 bus requires a 64-bit local data bus which has two identically sequenced 32-bit patterns allocated on four 32-bit slots. The write data generation is enabled and driven by the datain_rdy signal assertions.

2.2.4. Read Data Validation

The Read Data Validator checks the read data from the DDR3 memory module. To do this, it generates the expected data patterns using exactly the same data sequences as the Write Data Generator block. The expected data generation is enabled and driven by the read_data_valid signal assertions.

The read data captured by read_data_valid is compared with the expected data generated by the Read Data Validator block. When there is a mismatch between both data patterns, the demo design will flag the error detection signal.

2.2.5. Control and Observation

The Control and Observation block includes the demo control input and result display functions. The demo control input uses 5 out of 8 DIP switches available on the ECP5 VIP Processor Board. The demo result is displayed through 7 LEDs on the board. See the Control and Observation Port Descriptions section and the Output Status LEDs section for descriptions of the demo control input switches and the result display LEDs.

3. Demo Kit Requirements

3.1. Hardware Requirements

To run the demo, the following hardware are required:

- ECP5 VIP Processor Board with ECP5-85 FPGA, 756-ball package
- 12 V DC power supply for the ECP5 VIP Processor Board
- Windows PC machine for implementing the demo project and downloading the bitstream
- USB cable for programming the ECP5 device

3.2. Software Requirements

To run the demo, the following software are required:

- Lattice Diamond design software, version 3.8 or later
- Programmer software for bitstream download

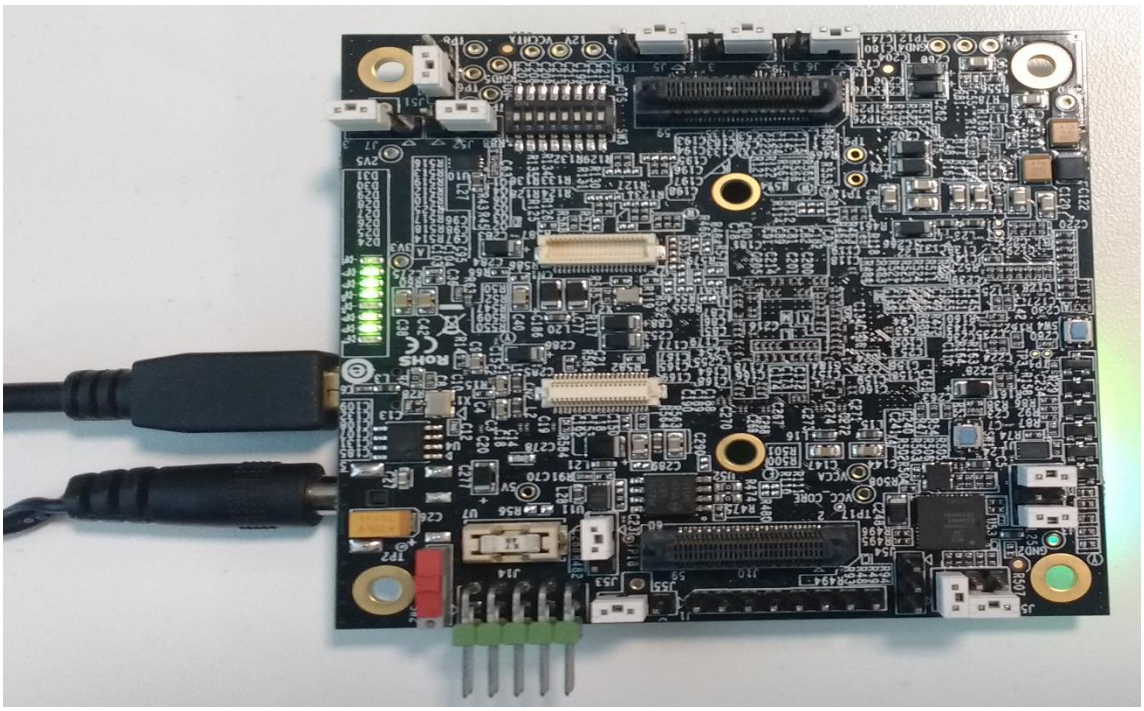

Figure 3.1. Demo Setup

4. ECP5 VIP Processor Board

This section describes how the ECP5 VIP Processor Board relates to the DDR3 demo.

4.1. DDR3 Memory

The ECP5 VIP Processor Board has onboard two 16-bit DDR3 memory modules. The DDR3 memory module on the board that is used for the DDR3 demo is a 96-pin unbuffered DDR3 SDRAM. The demo design uses up to 1 GB of memory space with one chip-select configuration.

4.2. Programming Cable Connections

The ECP5 device on the ECP5 VIP Processor Board can be programmed over JTAG via the USB port. This path can both program the device and be used with the Reveal™ logic analyzer to trace internal signal paths. The J52 header needs to be configured to enable the USB-to-JTAG path used by this demo. The instructions to set up the ECP5 VIP Processor Board for use with this demo are discussed in the Running the Demo section.

5. Port Assignments and Descriptions

Table 5.1 lists all the signals used by the DDR3 SDRAM controller IP core in the demo design to control and interface to the onboard DDR3 SDRAM. For details, refer to the Double Data Rate (DDR3) SDRAM Controller IP Core User's Guide (IPUG80).

Table 5.1. DDR3 Bus Interface

Port Name	Active	Direction	Description
em_ddr_reset_n	Low	Output	Asynchronous reset signal from the controller to the memory device. Asserted by the controller for the duration of power on reset or GSR_N
em_ddr_clk[CLKO_WIDTH-1:0]	—	Output	300 MHz memory clock generated by the controller
em_ ddr_clk_n[CLKO_WIDTH-1:0]	—	Output	300 MHz complimentary memory clock generated by the controller
em_ ddr_cke[CKE_WIDTH-1:0]	High	Output	Memory clock enable generated by the controller
em_ ddr_addr[ROW_WIDTH-1:0]	—	Output	Memory address bus, multiplexed row and column address for the memory
em_ ddr_ba[2:0]	—	Output	Memory bank address
em_ ddr_data[DATA_WIDTH-1:0]	—	In/Out	Memory bidirectional data bus
em_ ddr_dm[(DATA_WIDTH/8)-1:0]	High	Output	DDR3 memory write data mask
em_ ddr_dqs[DQS_WIDTH-1:0]	—	In/Out	Memory bidirectional data strobe
em_ ddr_dqs_n[DQS_WIDTH-1:0]	—	In/Out	Memory complementary bidirectional data strobe
em_ ddr_cs_n[CS_WIDTH-1:0]	Low	Output	Memory chip select
em_ ddr_cas_n	Low	Output	Memory column address strobe
em_ ddr_ras_n	Low	Output	Memory row address strobe
em_ ddr_we_n	Low	Output	Memory write enable
em_ ddr_odt[CS_WIDTH-1:0]	High	Output	Memory on-die termination control

Table 5.2 lists all the interfaces that are available to the user to either dynamically configure the parameters of the design (input mode) or observe the running status of the demo (output mode).

Table 5.2. Demo User Interface Ports

Port Name	Active	Direction	Description
clk_in	—	Input	Reference clock connected to a dedicated PLL clock input of the ECP5 FPGA.
reset_n	Low	Input	Asynchronous reset connected to the GSRN button (SW1). This resets the entire demo system including the DDR3 IP core when asserted.
dip_sw[4:0]	—	Input	User test configuration input. See the Control and Observation Port Descriptions section for further information.
oled[6:0]	—	Output	Demo result LED indicator output. See the Control and Observation Port Descriptions section for further information.

5.1. Control and Observation Port Descriptions

The Control and Observation Ports include the user interface ports as described in Table 5.2. This section describes in detail the two main control (DIP switch) and observation (LED) ports. Table 5.3 describes the functionality of each DIP switch on SW3 and how design parameters can be changed by changing the position of the switches.

The recommended default setting for the DIP switch is for all switches to be in the OFF position. The ON position is when the DIP switch level is towards ON that is printed on the DIP switch case.

Table 5.3. SW3 DIP Switch Definitions

Signal Name	DIP Switch Number	Assigned Function Control	DIP Switch Setting	Description
dip_sw[0]	SW3-1	Burst Length Selection	OFF	Set Burst Length to BL8
			ON	Set Burst Length to BC4
dip_sw[1]	SW3-2	On-the-Fly (OTF) Mode	OFF	Fixed burst size mode. The core is set to BL8 or BC4 during initialization depending on the Burst Length Selection setting.
			ON	OTF mode. Dynamic burst length change is controlled by the Burst Length Selection switch.
dip_sw[2]	SW3-3	Command Burst Disable	OFF	Enable command burst mode.
			ON	Disable command burst mode. Demo works in the single command mode. Manual single command repetitions are performed instead of using the command burst mode.
dip_sw[3]	SW3-4	Maximum Command Size	OFF	Use maximum command burst size/repetition The DDR3 core performs a 32 command burst (Command Burst Enabled) or the demo logic generates 32 consecutive single commands (Command Burst Disabled).
			ON	Use user-specified command burst size. Both command-burst and single-command-repetition modes use the burst size value (UsrCmdBrstCnt) defined in the ddr3_test_params.v file. The allowed values are 2, 4, 8, 16 or 32 with the default value set to 2.
dip_sw[4]	SW3-5	Data Mode	OFF	PRBS data patterns are used for the DDR3 demo. 128-bit pseudo random patterns are generated. In this demo (16-bit DDR3 SDRAM), the lower half [63:0] of the 128-bit PRBS data is used for the 64-bit local data bus.
			ON	Sequential data patterns. 32-bit sequential data pattern generators are used. For example, the 16-bit DDR3 demo has two 32-bit sequential patterns allocated to each 32-bit slot on a local data bus.

5.2. Output Status LEDs

Seven LEDs are used to indicate the demo progress and results. In Table 5.4, the Reference Designator column shows the diode reference designator printed on the ECP5 VIP Processor Board. Each LED indicates a particular status or condition of the DDR3 demo design, DDR3 controller core to be specific.

Table 5.4. Output LED Definitions

Signal Name	Reference Designator	Function	Status	Description
OLED[0]	D24	Heartbeat indicator	Blink	The board is on, and the core is receiving the clock Input.
			OFF	The core is unable to receive the clock signal.
OLED[1]	D25	DDR3 Transaction Indicator	Blink	DDR3 write-then-read operations are occurring. The more read data that comes in, the faster this LED blinks.
			OFF	No valid read data is detected.
OLED[2]	D26	Valid data indicator	Blink	Proper DDR3 read/write transactions are being performed with actual valid data.
			OFF	Received data is null (all 0 or 1).
	D31	Not used	—	—
OLED[3]	D27	Error Indicator	Blink	The first data mismatch error is detected. A system reset must be applied to clear this indicator.
			OFF	No error is detected.
OLED[4]	D28	INIT done and core ready indicator	ON	The core and memory initialization are complete, and the core is ready to accept user commands.
			OFF	The core is not ready to accept new command
OLED[5]	D29	Write indicator	ON	The core's write operation is properly working by detecting the datain_rdy signal assertions.
			OFF	The core is not ready to receive write data from the user.
OLED[6]	D30	Read indicator	ON	The core's read operation is properly working by detecting the read_data_valid signal assertions.
			OFF	Indicates invalid data on read-data bus.

6. Demo Package Directory Structure

The bitstream folder contains the demo bitstream for the ECP5 VIP Processor board. The DDR3_ project folder contains:

- *DDR3_project* (Demo design for ECP5 VIP Processor Board).
- The subfolder *ddr3_ecp5_impl* is the implementation folder for the ECP5 VIP Processor Kit.
- The subfolder *src* contains all the source files other than IP core.
- The subfolder *ddr3_ip_inst* is the generated IP core using Clarity Designer.

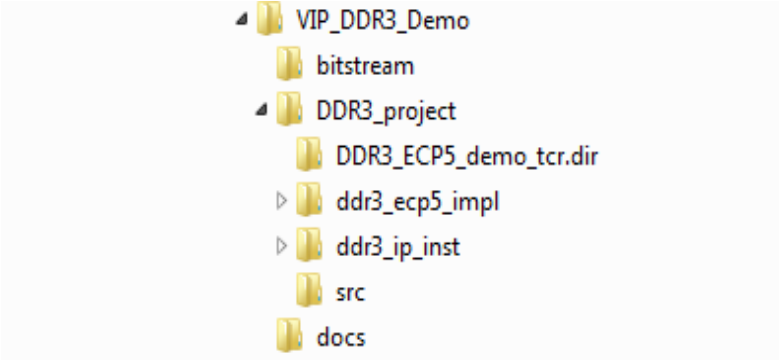

Figure 6.1. DDR3 Demo Package Directory Structure

7. Running the Demo

To run the demo:

1. Before the board is powered up, jumper pin #2 of J52 to pin #3. This puts ECP5 in the JTAG scan chain as the only device. Turn all positions of DIP switch SW3 to OFF.
2. Power up the board with 12 V power supply. Connect the board to a PC with a USB cable.
3. Launch the Lattice Diamond Programmer software.

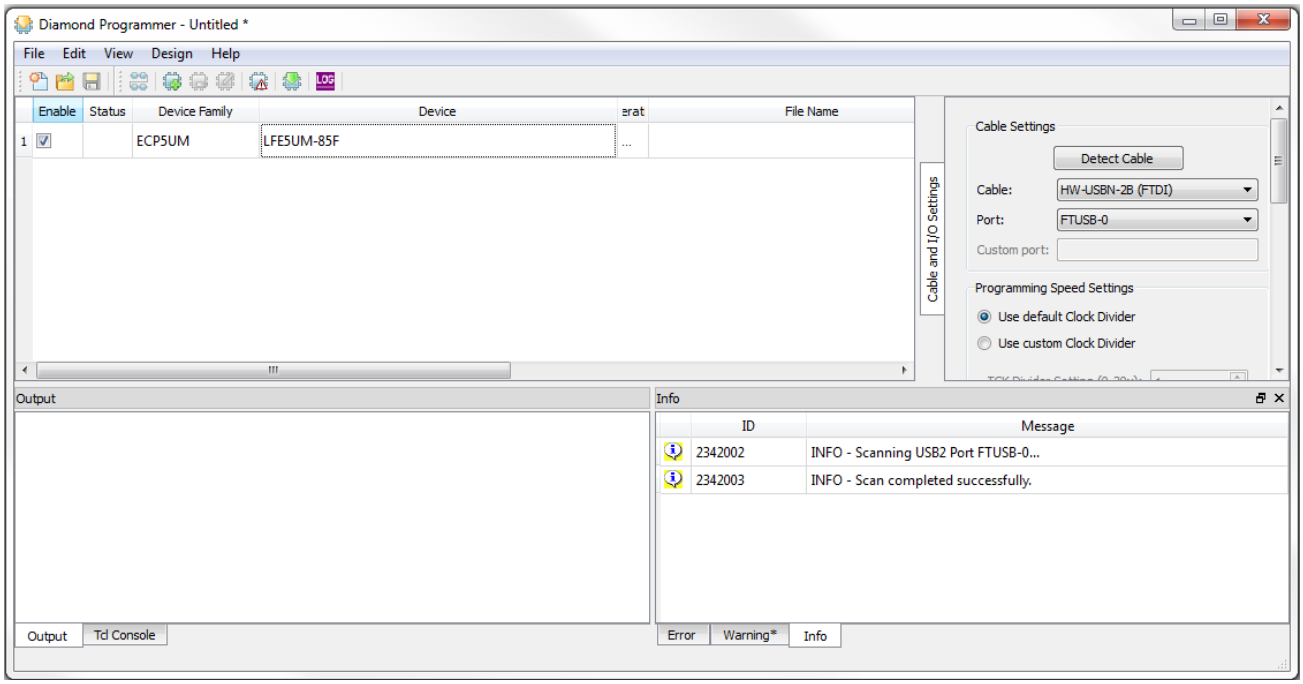

Figure 7.1. Getting Started

4. If the device is not detected, scan the JTAG chain by clicking the **Scan** button.
5. Select the **LFE5UM-85F** device.

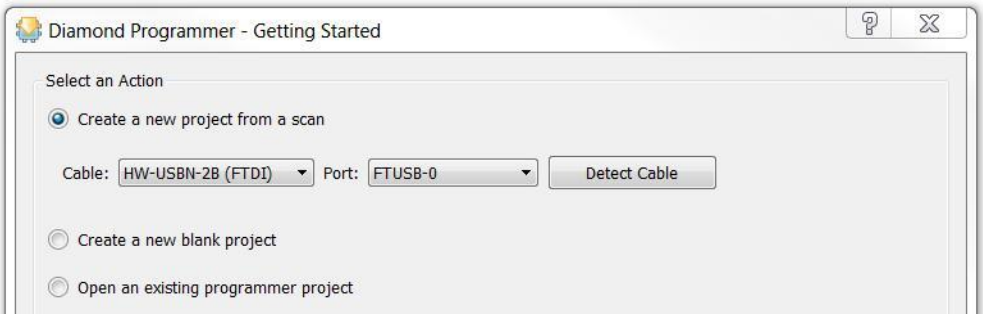

Figure 7.2. Detect Cable

6. For operation, select **Fast Program** as shown in Figure 7.3.
7. For the programming file, browse for the bitstream **VIP_ddr3_demo\bitstream\VIP_ddr3_demo.bit** to be programmed.
8. Click **OK** to start programming the device.

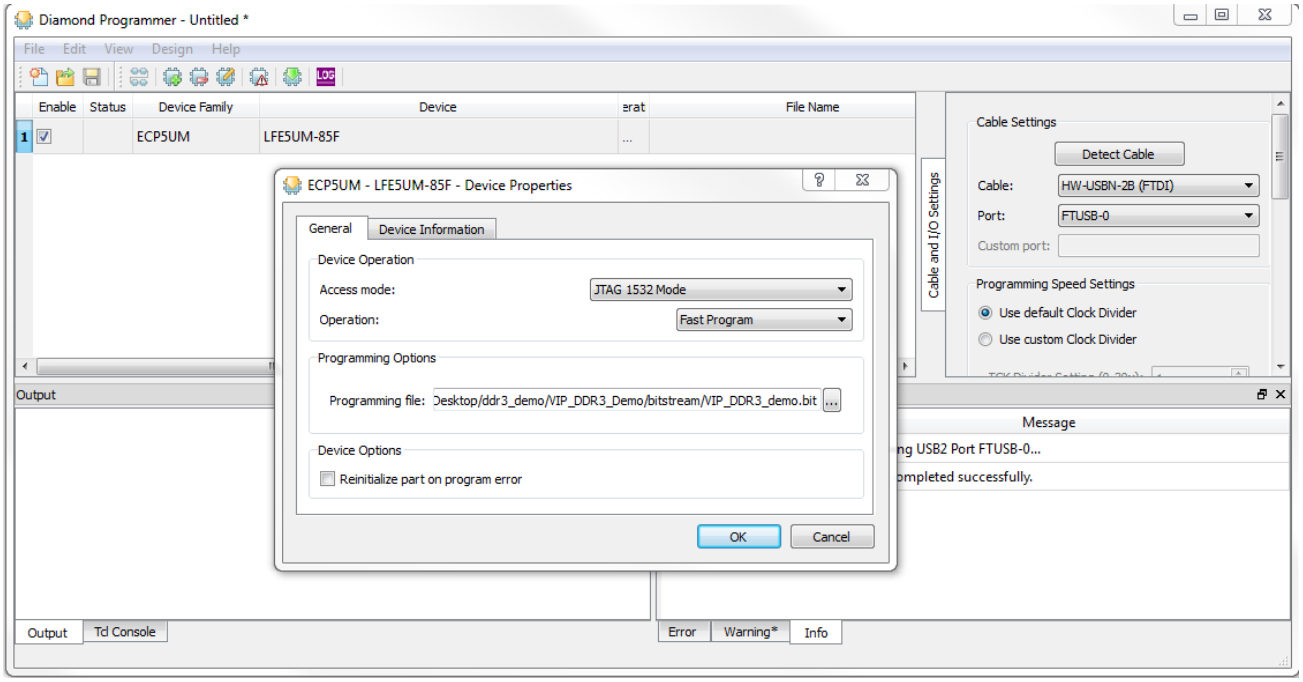

Figure 7.3. Device Properties

Status LEDs on the board should be illuminated or blinking when the FPGA programming is completed.

See Table 7.1 to verify whether LEDs are blinking as mentioned. If the green LED-D27 (Error) blinks, press the **GSRN** button (SW1) to clear the error counter and reset the design.

Table 7.1. Expected LED Status from Successful Demo

Name	Expected Status	Remark
D24 (Segment LED)	Rotating clockwise and character “0” pulse	Character “0” pulse rate is about 45 beats per second with SW3 all OFF position
D25	Blink	Green LED with constant blinking rate
D26	Blink	Green LED
D27	OFF	—
D28	ON	Green LED
D29	ON	Green LED
D30	ON	Green LED

8. Pinout Information

Table 8.1 lists the ECP5 pinouts used for the demo.

Table 8.1. ECP5 Pinouts

Port Name	Pin/Bank	Buffer Type	Site	Properties
BANK_6_VREF	V4/6	—	PL56B	VREF1_DRIVER
VREF1_BANK_7	J7/7	—	PL35C	VREF1_DRIVER
clk_in	C5/7	LVDS_IN	PL11A	Clamp: On
dip_sw[0]	B26/1	LVCMOS12_IN	PT112B	Pull: Down, Clamp: On
dip_sw[1]	C26/1	LVCMOS12_IN	PT114A	Pull: Down, Clamp: On
dip_sw[2]	D26/1	LVCMOS12_IN	PT114B	Pull: Down, Clamp: On
dip_sw[3]	A28/1	LVCMOS12_IN	PT116A	Pull: Down, Clamp: On
dip_sw[4]	A29/1	LVCMOS12_IN	PT116B	Pull: Down, Clamp: On
em_ddr_addr[0]	W4/6	SSTL15_I_OUT	PL74B	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[10]	W1/6	SSTL15_I_OUT	PL68D	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[11]	Y6/6	SSTL15_I_OUT	PL71B	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[12]	U1/6	SSTL15_I_OUT	PL68B	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[1]	Y5/6	SSTL15_I_OUT	PL71C	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[2]	AB6/6	SSTL15_I_OUT	PL77B	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[3]	P3/6	SSTL15_I_OUT	PL59B	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[4]	AB5/6	SSTL15_I_OUT	PL77A	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[5]	W5/6	SSTL15_I_OUT	PL71D	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[6]	AC6/6	SSTL15_I_OUT	PL74D	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[7]	Y7/6	SSTL15_I_OUT	PL71A	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[8]	AC7/6	SSTL15_I_OUT	PL77C	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_addr[9]	AD6/6	SSTL15_I_OUT	PL80A	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_ba[0]	U3/6	SSTL15_I_OUT	PL62D	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_ba[1]	Y4/6	SSTL15_I_OUT	PL74A	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_ba[2]	W3/6	SSTL15_I_OUT	PL65C	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_cas_n	T1/6	SSTL15_I_OUT	PL68A	Drive: 8 mA, Clamp: On, Slew: Fast
em_ddr_cke[0]	T2/6	SSTL15_I_OUT	PL65B	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_clk[0]	R3/6	SSTL15D_I_OUT	PL59C	Drive: 8 mA, Clamp: On, Slew: Fast
em_ddr_cs_n[0]	P2/6	SSTL15_I_OUT	PL59A	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_data[0]	AC5/6	SSTL15_I_BIDI	PL83C	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[10]	V7/6	SSTL15_I_BIDI	PL56D	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[11]	T7/6	SSTL15_I_BIDI	PL47D	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[12]	U6/6	SSTL15_I_BIDI	PL50C	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[13]	T4/6	SSTL15_I_BIDI	PL53C	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[14]	U7/6	SSTL15_I_BIDI	PL50D	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[15]	U4/6	SSTL15_I_BIDI	PL56A	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[1]	AC2/6	SSTL15_I_BIDI	PL89C	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[2]	AB4/6	SSTL15_I_BIDI	PL83B	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[3]	AE3/6	SSTL15_I_BIDI	PL86D	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[4]	W2/6	SSTL15_I_BIDI	PL86A	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[5]	AD4/6	SSTL15_I_BIDI	PL83D	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[6]	Y1/6	SSTL15_I_BIDI	PL86B	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[7]	AB1/6	SSTL15_I_BIDI	PL92A	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[8]	V6/6	SSTL15_I_BIDI	PL56C	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD
em_ddr_data[9]	P4/6	SSTL15_I_BIDI	PL47B	Drive: 8 mA, Clamp: On, Slew: Fast, VREF1_LOAD

Table 8.1. ECP5 Pinouts *(Continued)*

Port Name	Pin/Bank	Buffer Type	Site	Properties
em_ddr_dm[0]	AB3/6	SSTL15_I_OUT	PL83A	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_dm[1]	R6/6	SSTL15_I_OUT	PL50A	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_dqs[0]	AC3/6	SSTL15D_I_BIDI	PL89A	Drive: 8 mA, Clamp: On, Slew: Fast, Diffresistor: 100
em_ddr_dqs[1]	R4/6	SSTL15D_I_BIDI	PL53A	Drive: 8 mA, Clamp: On, Slew: Fast, Diffresistor: 100
em_ddr_odt[0]	V1/6	SSTL15_I_OUT	PL68C	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_ras_n	C2/7	SSTL15_I_OUT	PL17B	Drive: 8 mA, Clamp: On, Slew: Fast
em_ddr_reset_n	C4/7	SSTL15_I_OUT	PL11C	Drive: 8 mA, Clamp: On, Slew: Slow
em_ddr_we_n	P1/6	SSTL15_I_OUT	PL62B	Drive: 8 mA, Clamp: On, Slew: Fast
oled[0]	AG30/4	LVCMOS15_OUT	PB114B	Drive: 8 mA, Clamp: On, Slew: Slow
oled[1]	AK29/4	LVCMOS15_OUT	PB116A	Drive: 8 mA, Clamp: On, Slew: Slow
oled[2]	AK30/4	LVCMOS15_OUT	PB116B	Drive: 8 mA, Clamp: On, Slew: Slow
oled[3]	AH32/4	LVCMOS15_OUT	PB119A	Drive: 8 mA, Clamp: On, Slew: Slow
oled[4]	AG32/4	LVCMOS15_OUT	PB119B	Drive: 8 mA, Clamp: On, Slew: Slow
oled[5]	AJ29/4	LVCMOS15_OUT	PB121A	Drive: 8 mA, Clamp: On, Slew: Slow
oled[6]	AM28/4	LVCMOS15_OUT	PB96A	Drive: 8 mA, Clamp: On, Slew: Slow
out_test1	B1/7	SSTL15_I_OUT	PL17A	Drive: 8 mA, Clamp: On, Slew: Slow
reset_n	AH1/8	LVCMOS25_IN	PB4B	Pull: Down, Clamp: On, Hysteresis: On
test1	F5/7	SSTL15_I_IN	PL14D	Clamp: On, VREF1_LOAD

Notes:

- As VREF is shared for both memory chips, you need to drive both VREF to get the voltage level of 0.75 V, so that single memory (U12) works properly.
- For two-memory (U12 and U19) modification, refer to the ECP5 VIP Processor Board Evaluation Board User Guide (FPGA-EB-02001).

Important

For the ECP5 demo, the bitstream included with the demo design has been developed for Revision B of ECP5 VIP Processor Board.

The demo bitstreams have been built with Lattice Diamond v3.8 for using with Revision B of ECP5 VIP Processor Board.

References

For more information, refer to:

- FPGA-DS-02012 (previously DS1044), ECP5 and ECP5-5G Family Data Sheet
- IPUG80, Double Data Rate (DDR3) SDRAM Controller IP Core User's Guide

For schematics, refer to:

- FPGA-EB-02001, ECP5 VIP Processor Board Evaluation Board User Guide

Technical Support

For assistance, submit a technical support case at www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
July 2017	1.1	• Updated Introduction section. • Updated Figure 2.1. DDR3 Demo Block Diagram. • Updated Table 8.1. ECP5 Pinouts.
May 2017	1.0	Initial release.

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