

# Xilinx Project Synthesis on Vivado (EE354)

This document is to provide design flow steps in using Xilinx Vivado to synthesize, implement, and generate a bitstream file (.bit file). We will be using NEXYS 4 (ARTIX-7) [2] as the development board during labs. In each lab, you will be first required to finish the design in Vivado toolkit and generate the configuration bitstream file (.bit file). Then you need to download the bitstream file onto the NEXYS 4 board using some programming tools (Vivado Hardware Manager, Digilent Adept). Figure 1 shows the design flow.

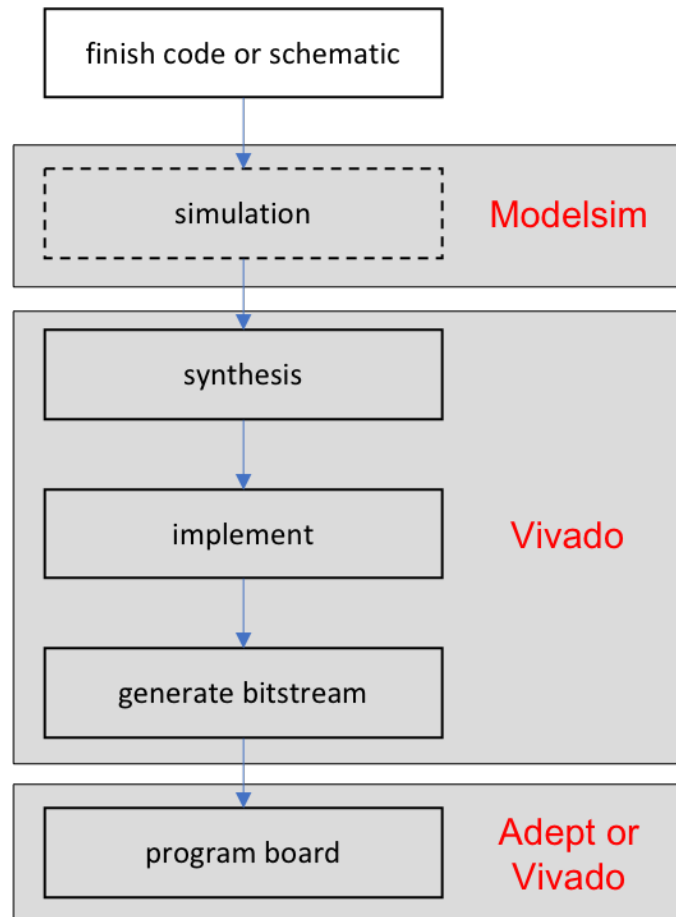


Figure 1 Design flow with Vivado

## 1 Preparation

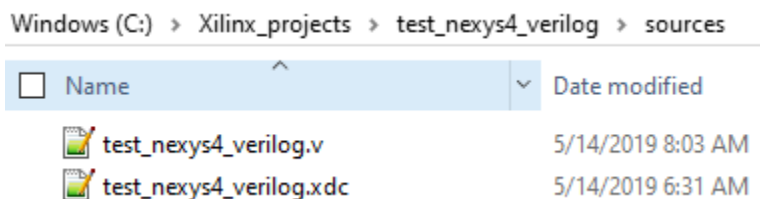
- First finish installing the Xilinx Vivado synthesis and implementation tool as per steps provided to you [1].
- Install Adept
- Receive a Nexys 4 board from your TA. Please do not disturb the jumper placement on the NEXYS 4 board. Jumpers were already set in the right fashion. The Nexys 4 reference manual [2] talks about functionality of these jumpers but you do not have to go through the same.

## 2 Design Steps

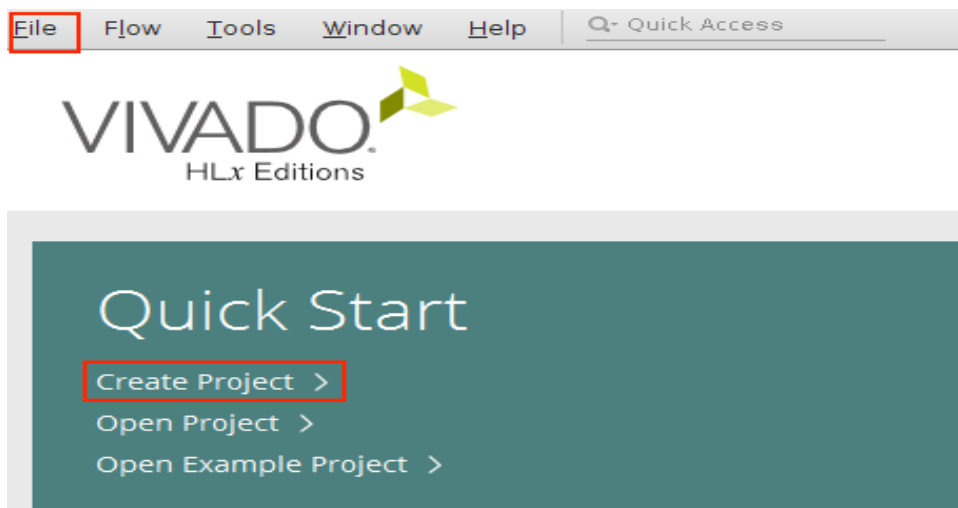
In this section, we break down the design flow into a couple of small steps to give you a basic idea of digital circuit design in Vivado.

### 2.1 Phase 1: Create a project

- **Create a project folder** called test\_nexys4\_verilog under C:\Xilinx\_projects. Create a subdirectory called sources. Download from [test nexys4 verilog sources only](#) the two source files:  
Verilog design source file: test\_nexys4\_verilog.v  
Xilinx Design Constraints file (.xdc file): test\_nexys4\_verilog.xdc



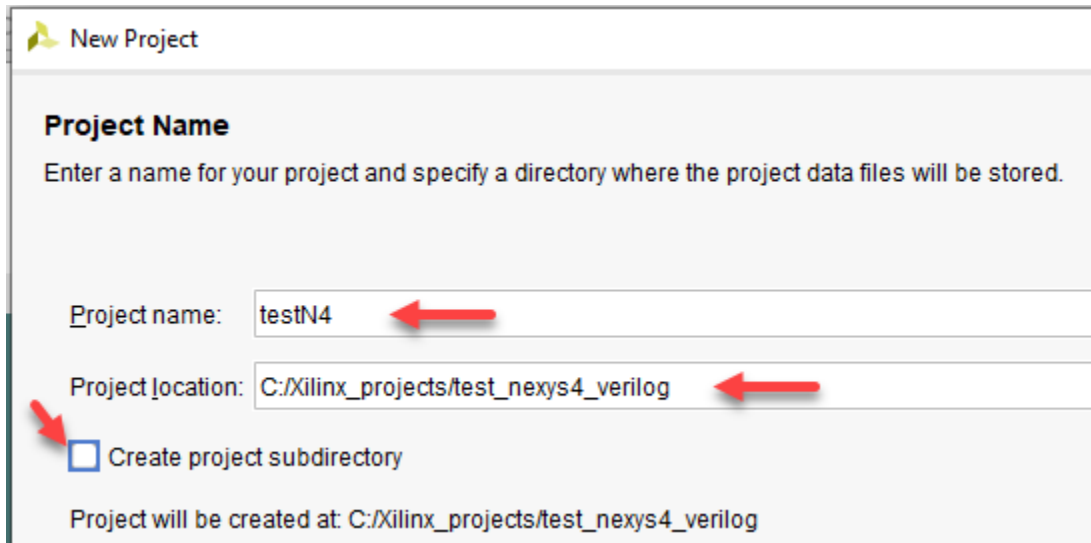
- **Open the Vivado tool** on your windows laptop or on VDI
- **Create a Vivado project** Let us call it testN4.
- 



You can click the **Create Project** in the Quick Start, or you can alternatively go to **File->Project->New**.  
Click **Next**.

- **Specify project name and location**

Let us call it testN4. The location is C:\Xilinx\_projects\test\_nexys4\_verilog



**New Project**

**Project Name**  
Enter a name for your project and specify a directory where the project data files will be stored.

Project name: testN4

Project location: C:/Xilinx\_projects/test\_nexys4\_verilog

☐ Create project subdirectory

Project will be created at: C:/Xilinx\_projects/test\_nexys4\_verilog

Click **Next** and choose **RTL Project**. Click **Next**.



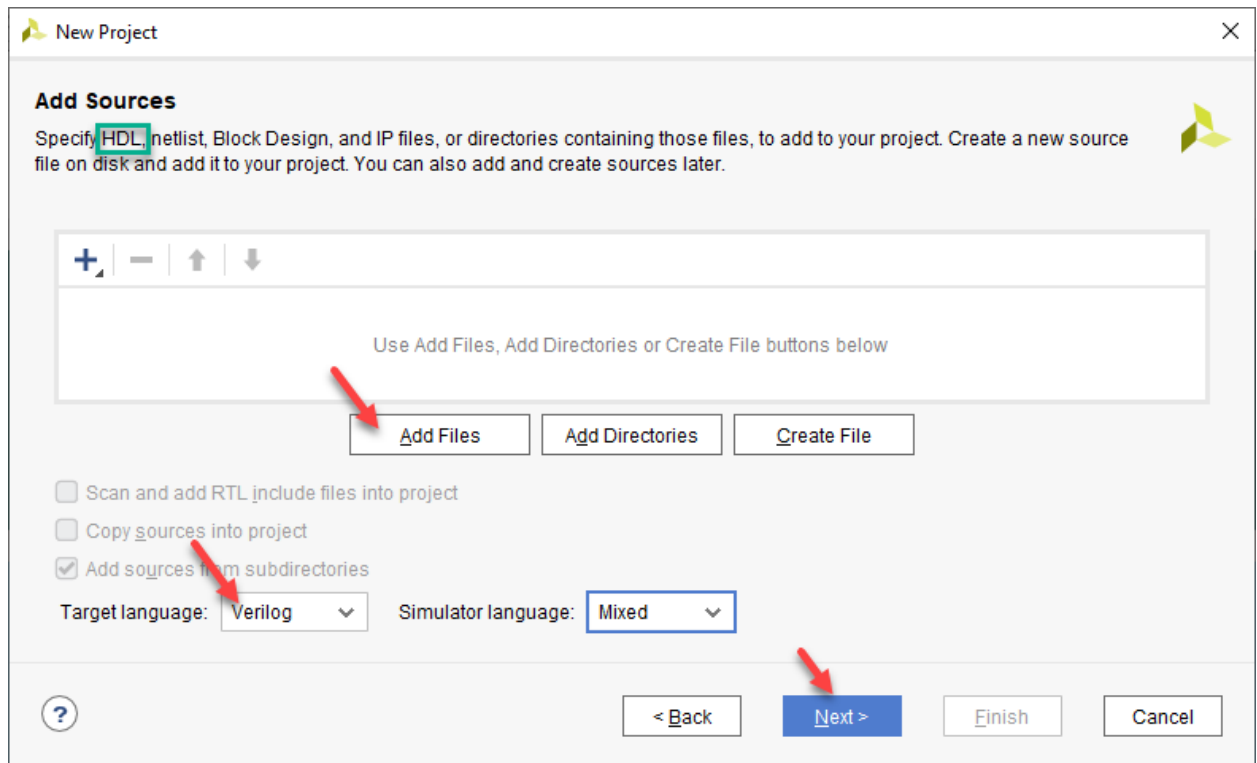
**New Project** [X]

**Project Type**  
Specify the type of project to create.

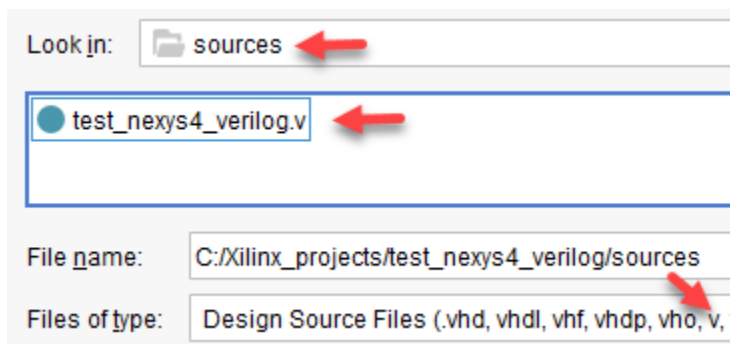
☒ **RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☐ Do not specify sources at this time

- **Add files**

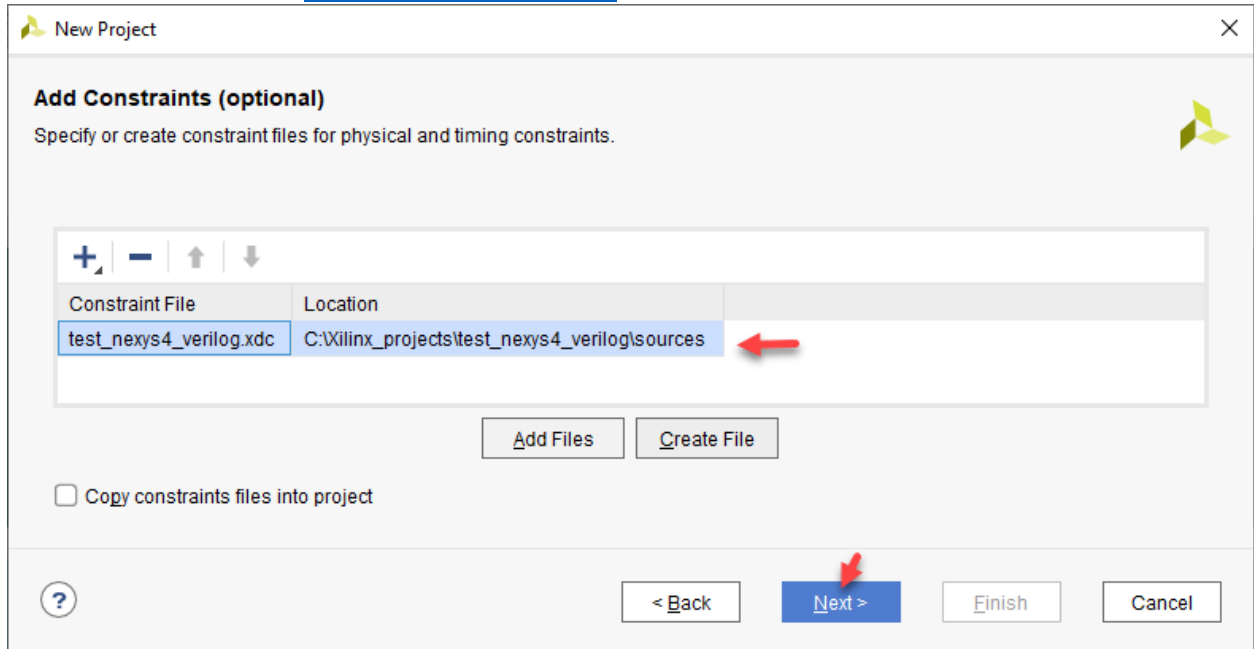


You can choose to **Add Files** from some reference source or you can **Create File** from scratch. Here we choose to load a previously completed test file (test\_nexts4\_verilog.v). Click **Next**.



- **Add constraints**

This step is very important. Xilinx Design Constraint files (.xdc) specifies pins associated with your input and output ports (**pin assignment**) and **clock frequency**, which is critical for following synthesis, implement (which includes timing design) and generating bitstream file. A master constraints file ([Nexys4 Master xdc.zip](#)) has been posted. One needs to uncomment the needed lines and also revise the signal names (labels). In most occasions, we will give you a completed constraint file during each lab. For example, we are giving you for the first week's lab [test\\_nexys4\\_verilog.xdc](#).



Click **Next**.

**Note:** Source files can be found in

[http://www-classes.usc.edu/engr/ee-s/254/ee254/lab\\_manual/test\\_nexys4\\_verilog\\_sources\\_only/](http://www-classes.usc.edu/engr/ee-s/254/ee254/lab_manual/test_nexys4_verilog_sources_only/).

Though a complete project is also provided in [http://www-classes.usc.edu/engr/ee-s/254/ee254/lab\\_manual/test\\_nexys4\\_verilog.zip](http://www-classes.usc.edu/engr/ee-s/254/ee254/lab_manual/test_nexys4_verilog.zip), we highly recommend you to start from scratch and create your own projects.

- For the next step we can either **Choose the Part** (the hard way) or **Choose the board** (the easy way).

### Choose the Part (the hard way)

New Project

Default Part

Choose a default Xilinx part or board for your project.

Parts | Boards

Reset All Filters

Category: General Purpose

Family: Artix-7

Package: csg324

Speed: -1

Temperature: All Remaining

Static power: All Remaining

Search: Q-

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs	GI
xc7a15tcsg324-1	324	210	10400	20800	25	0	45	0
xc7a35tcsg324-1	324	210	20800	41600	50	0	90	0
xc7a50tcsg324-1	324	210	32600	65200	75	0	120	0
xc7a75tcsg324-1	324	210	47200	94400	105	0	180	0
xc7a100tcsg324-1	324	210	63400	126800	135	0	240	0

?

< Back

Next >

Finish

Cancel

Now let us show you the **Choose the board** (the easy way) method

**New Project**

**Default Part**  
Choose a default Xilinx part or board for your project.

Parts | **Boards**

[Reset All Filters](#) [Update Board Repositories](#)

Vendor:  Name:  Board Rev:

Search:

Display Name	Preview	Vendor	File Version	Pa
Nexys4		digilentinc.com	1.1	xc7

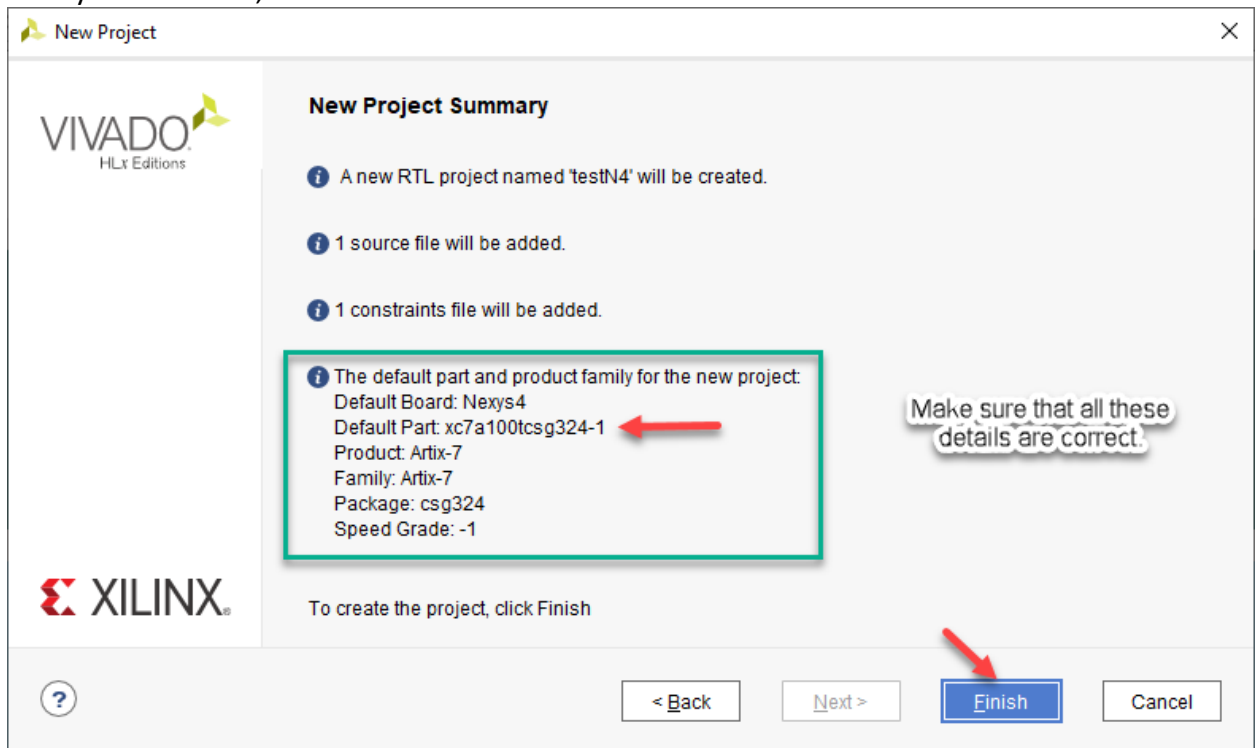
[? < Back](#) [Next >](#) [Finish](#) [Cancel](#)

Recall that we added the Nexys 4 board file during installation. If we didn't add board file, we have to choose the part *xct100tcsg324-1* in **Parts**. i.e. **Choose the Part** (the hard way)

Click **Next**.

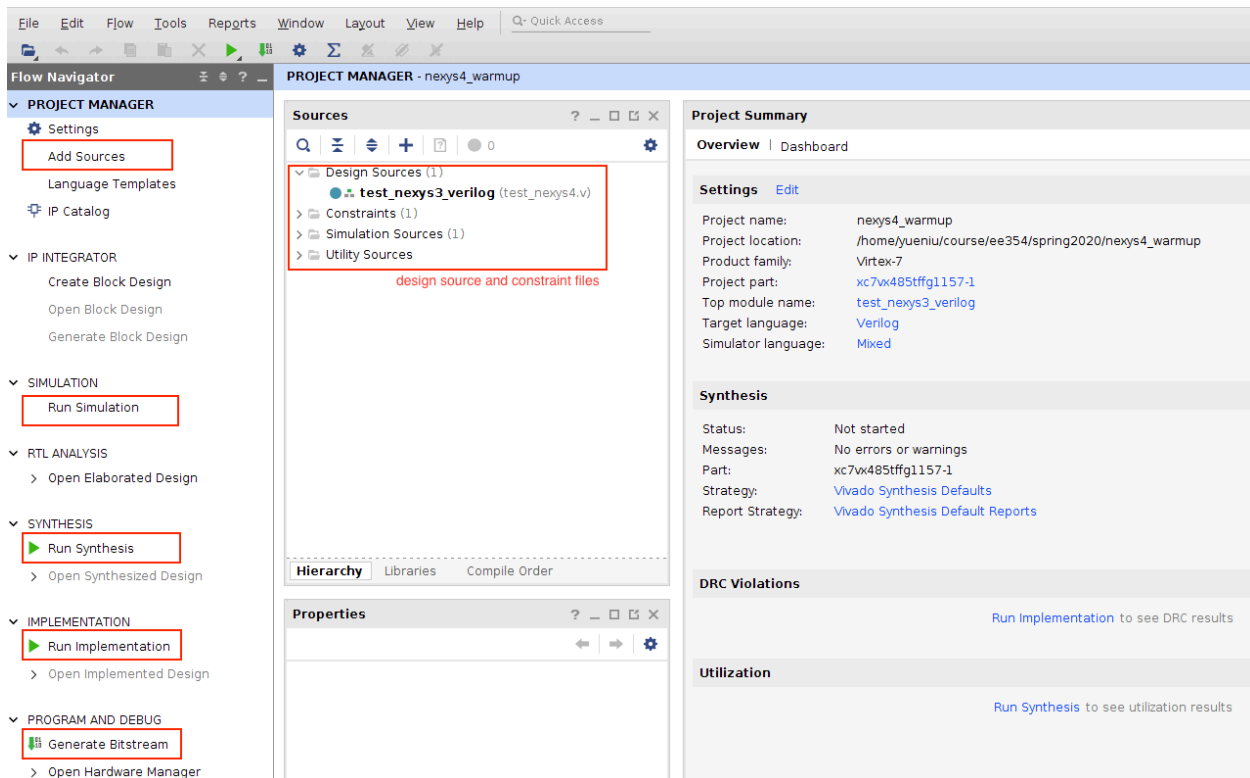
- All set

Now you are all set, click **Finish**.



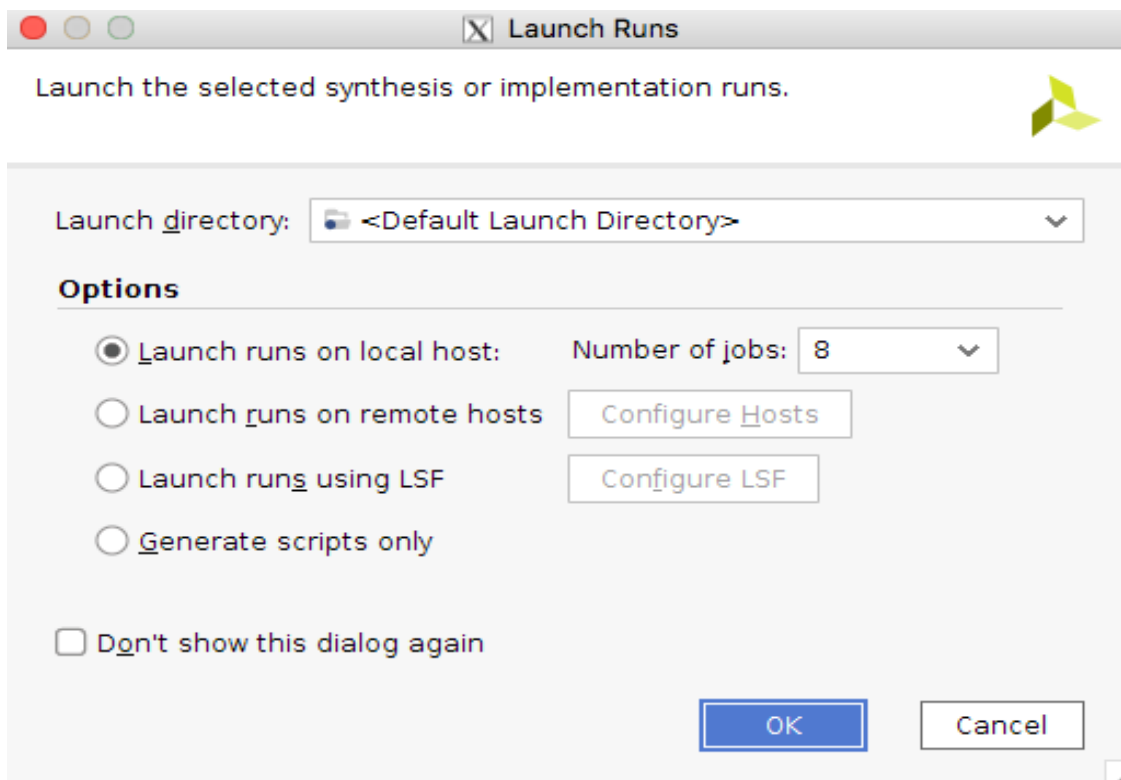
## 2.2 Phase 2: Generate Bitstream





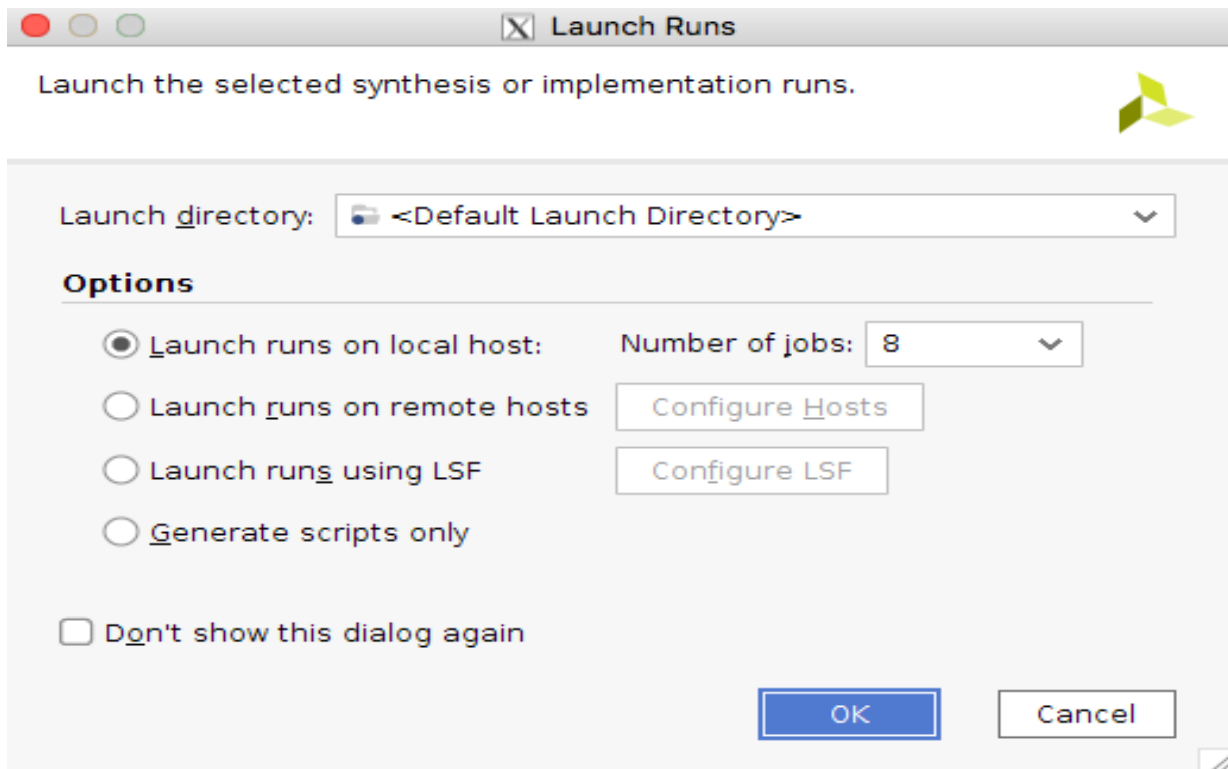
This is a typical window after creating a project. Buttons in the left column are the commands you can run. The middle column is the **Project Manager** which lists the source files and constraint files. The right column is the **Project Summary**. To generate bitstream to program NEXYS 4 board, you need to finish the three steps ( **Run Synthesis**, **Run Implementation**, **Generate Bitstream** ) one by one in that order or all in one stroke by selecting to do the last step **Generate Bitstream**, which will cause the prior steps also to be run. Shown below is one step-at-a-time option.

## ▪ Run Synthesis



There are options you can configure to run synthesis. For now, you can just keep all options as the default.

- **Run Implementation**



- **Generate Bitstream**

If no errors found in previous steps, you can now generate the configuration bitstream to program the board. You can go to the **Project Dir/nexys4\_test.runs/impl\_1/** to get the \*.bit file.

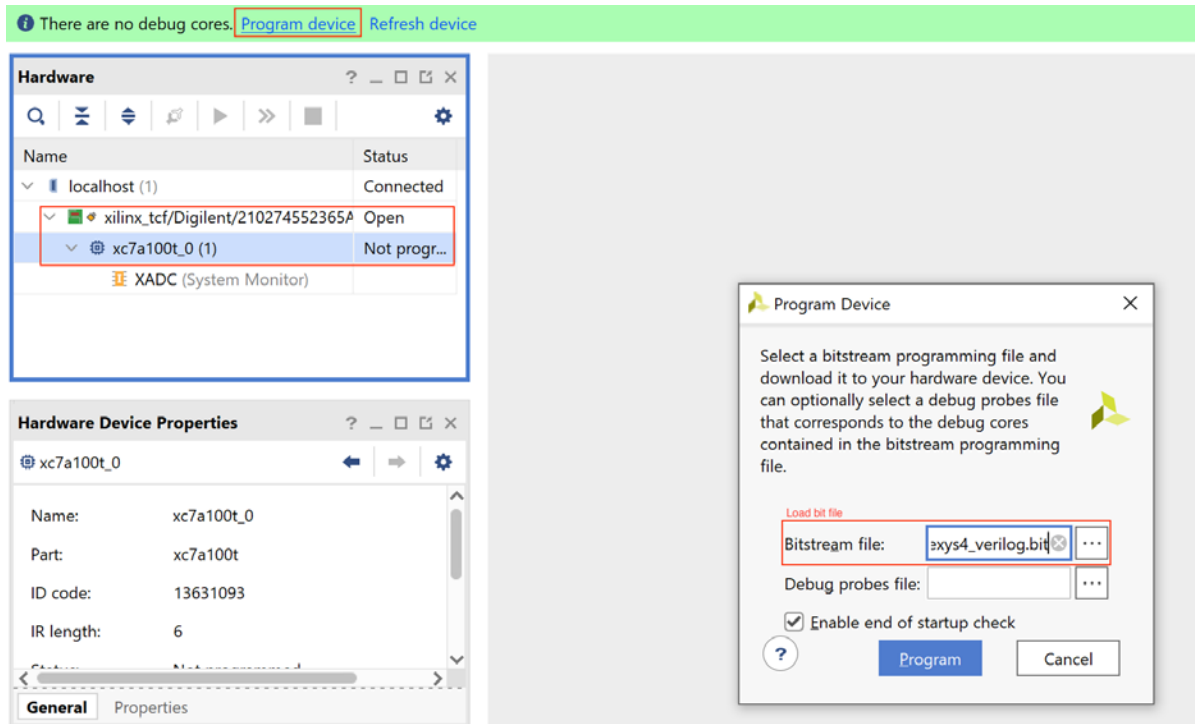
- **Program board**

Connect the Nexys 4 board to your laptop using the given USB cable and turn on the board.

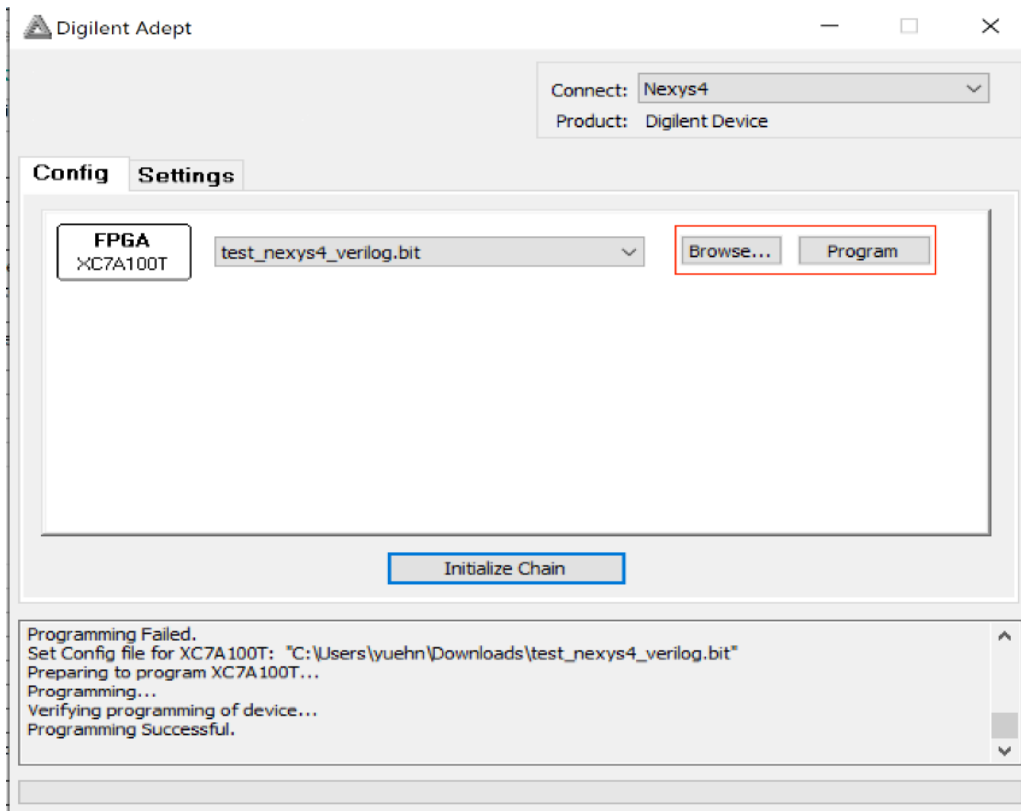
You can use Adept tool by Digilent or the Vivado Hardware Manager to download the .bit file to the board.

Vivado Hardware Manager is always preferred to program the board. You can click **Open Hardware Manager** in the project window. After it detects your board, click **Program device** to program your board and load the bitstream file, then click **Program**.

**Note:** You don't have to add anything in the **Debug probes file** blank, which is for hardware debugging purpose. For now, we don't need it.



If, for some reason, you failed to program your board in **Hardware Manager**, you can also switch to **Digilent Adept** [3]. First **Browse** the bit file, then **Program** the board.



If you manage to download the bit stream file, you should see 16 LEDs displaying a walking LED pattern, dot points flashing and the 8 SSDs (7-Segment Displays) displaying the TRUE and Complemented value of the 16 switches in hexadecimal notation. Try pressing the 5 buttons.

Congratulations!

## References

- [1] Vivado Installation steps [.docx](#) [.pdf](#)
- [2] Nexys 4 reference manual [.pdf](#)
- [3] Digilent Adept [Go here](#)
- [4] (This document) Xilinx Project Synthesis on Vivado [.docx](#) [.pdf](#) [.mp4](#)