



## **SCHOOL OF ENGINEERING AND NATURAL SCIENCES**

**Computer Engineering**

**Digital Logic Design**

**Final Project**

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**Department, ID:** CoE, 64240051

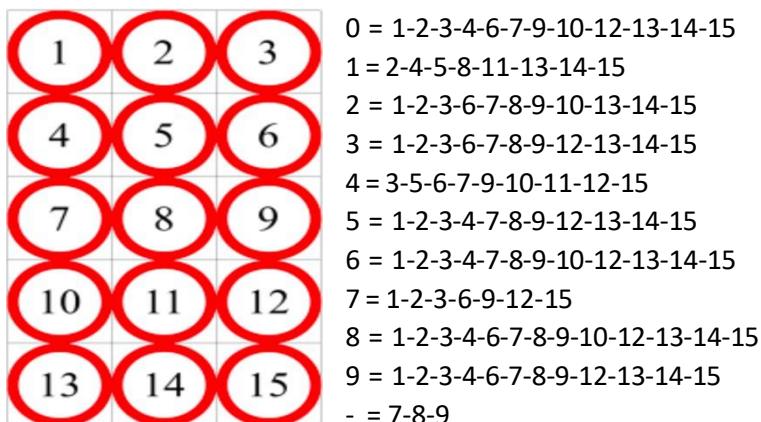
## 1. General Description

In this project, a 15-pixel display system consisting of a 5x3 LED matrix designed on a breadboard has been developed. The system includes a control mechanism that displays the digits derived from the student numbers in a sequential manner. For each digit, it is represented by a binary code. Using basic logic gates, the display of digits is provided by the activation of certain LEDs. A truth table has been created that defines all combinations of LEDs for the representation of numbers.

The timing structure of the system is provided by an ID code generator, which is synchronized with a clock signal operating at a frequency of 1 Hz and is designed as a finite state machine. This generator creates an automatic loop so that the digits in the student numbers are displayed sequentially. All components were simulated on the TinkerCAD platform, which was used to visualize the circuit and test its accuracy.

## **2. Part 1 : Design of 5x3 Pixel LED Display Adapter**

A truth table was created using the binary equivalents of the numbers. To determine the activation of the 5x3 pixel LEDs generated, the Karnaugh map of each LED was created using the truth table. Boolean expressions were obtained using K-maps. Circuit diagrams were created using LogiSim. The TinkerCad circuit is built using the obtained Boolean expressions. A, B, C and D inputs were provided with the circuit using binary codes logic 1 and logic 0 inputs, and the decimal values of the binary codes were observed with LEDs.



**Figure 1.** 15-pixel LED display

**Table 1.** The truth table of first part

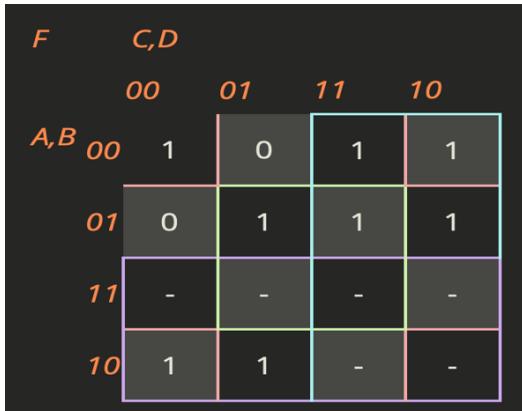


Figure 2. The K-map of LED1



Figure 3. The K-map of LED2



Figure 4. The K-map of LED3

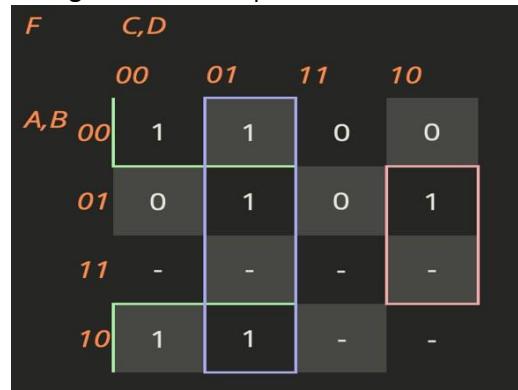


Figure 5. The K-map of LED4

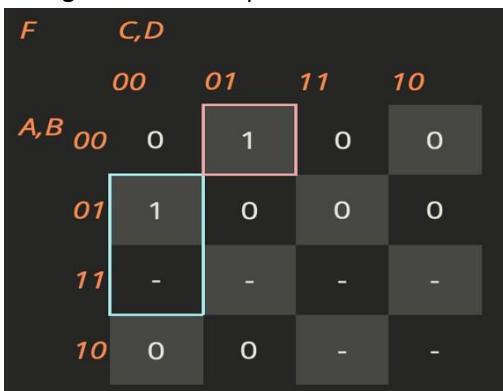


Figure 6. The K-map of LED5



Figure 7. The K-map of LED6



Figure 8. The K-map of LED7

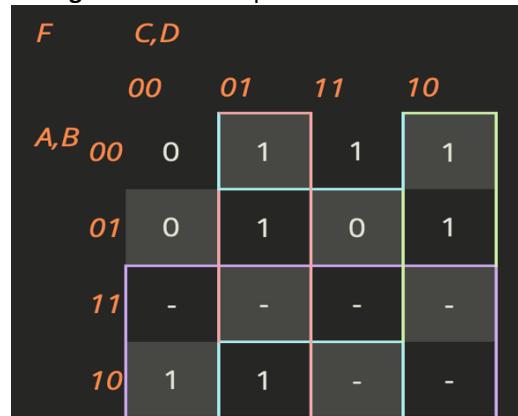


Figure 9. The K-map of LED8



Figure 10. The K-map of LED9

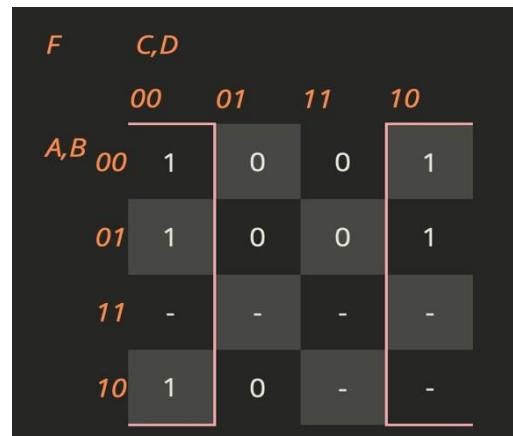


Figure 11. The K-map of LED10

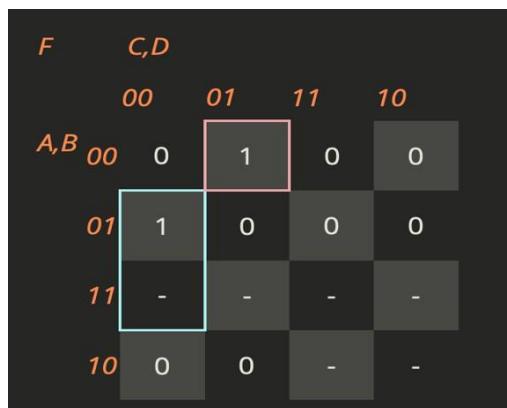


Figure 12. The K-map of LED11

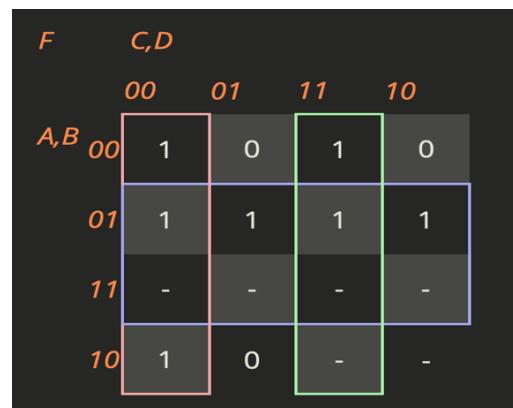


Figure 13. The K-map of LED12



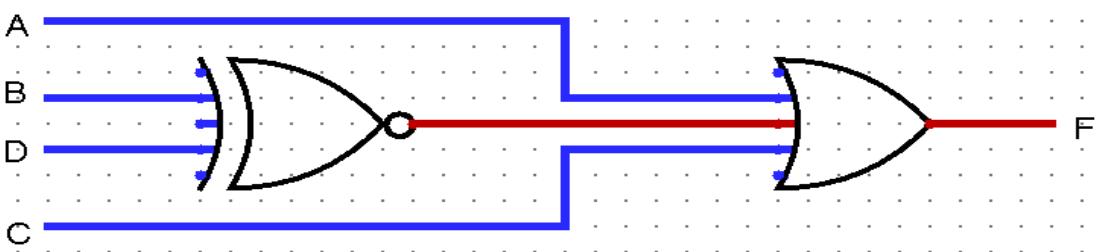
Figure 14. The K-map of LED13



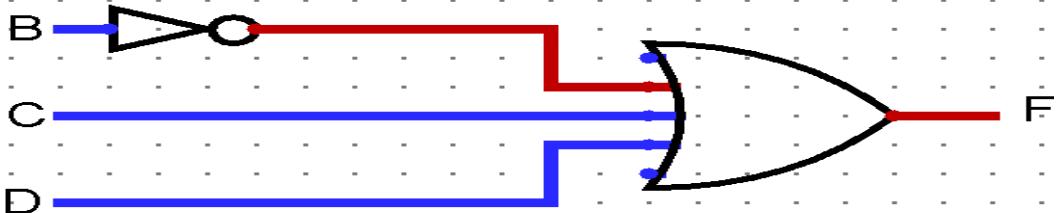
Figure 15. The K-map of LED14



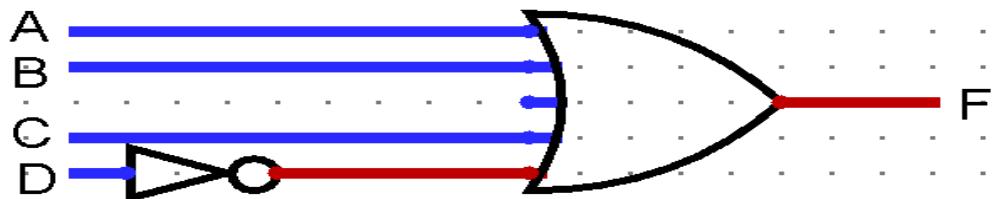
Figure 16. The K-map of LED15



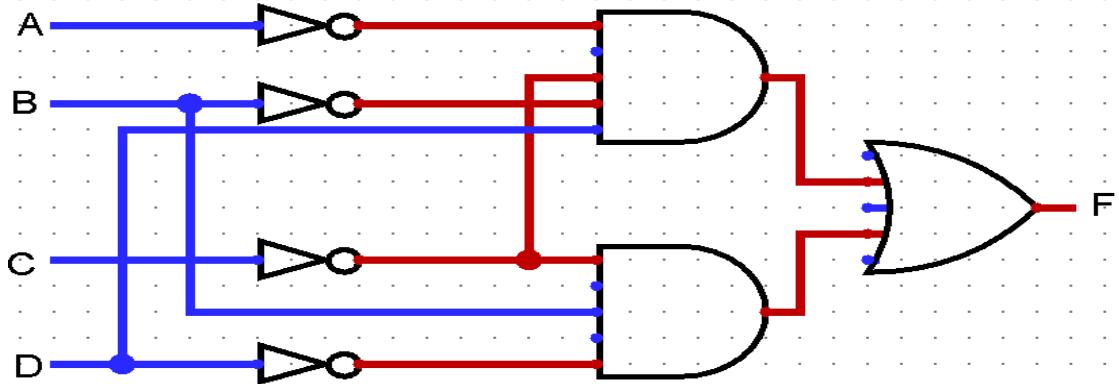
**Figure 17.** LED1 :  $F = B'D' + C + BD + A$



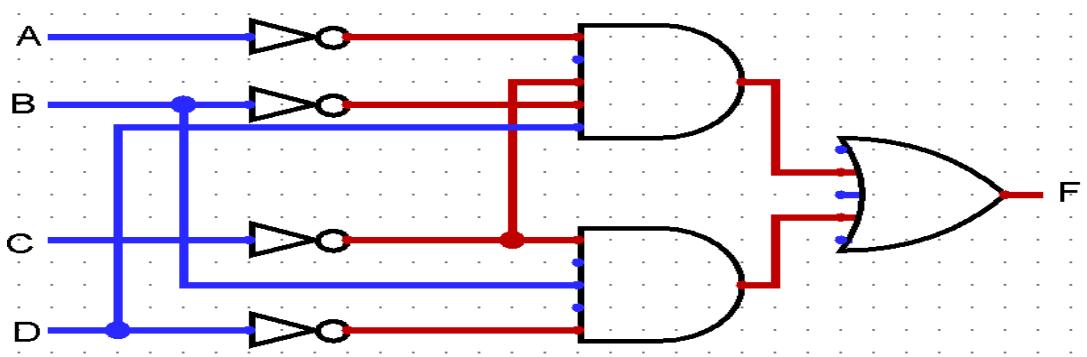
**Figure 18.** LED2 :  $F = B' + D + C$



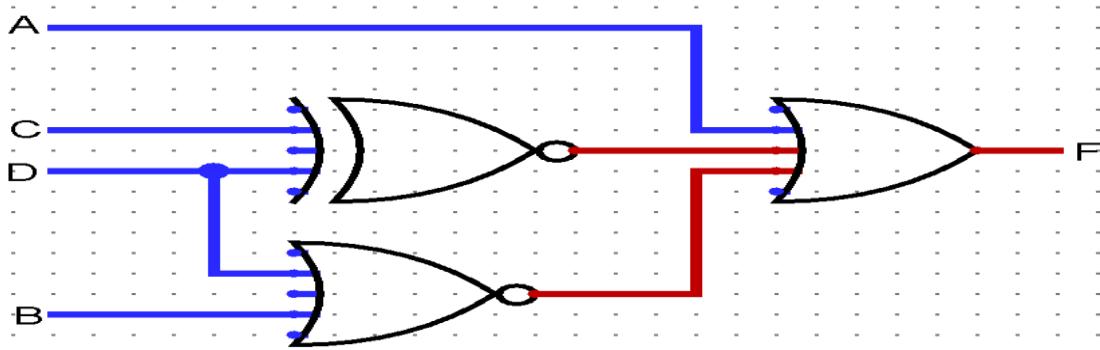
**Figure 19.** LED3 :  $F = D' + C + B + A$



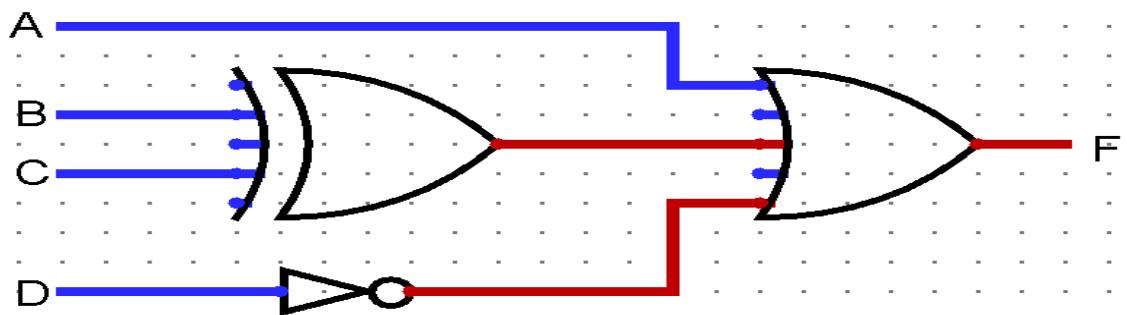
**Figure 20.** LED4 :  $F = B'C' + C'D + BCD'$



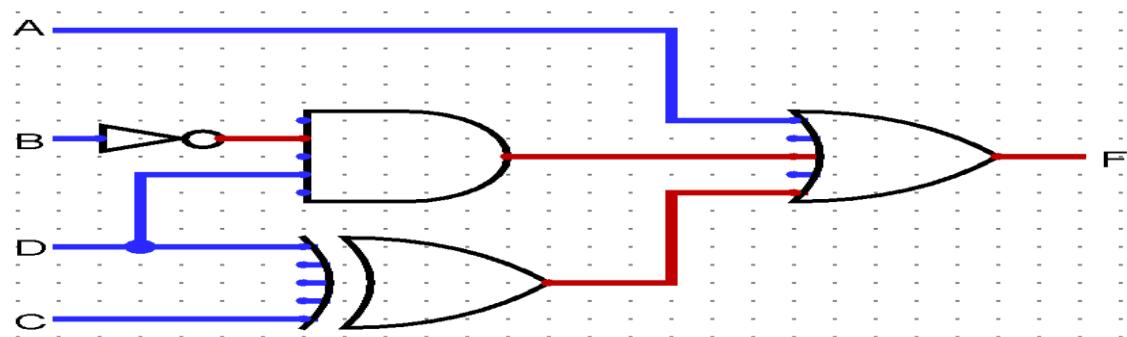
**Figure 21. LED5 :**  $F = A'B'C'D + BC'D'$



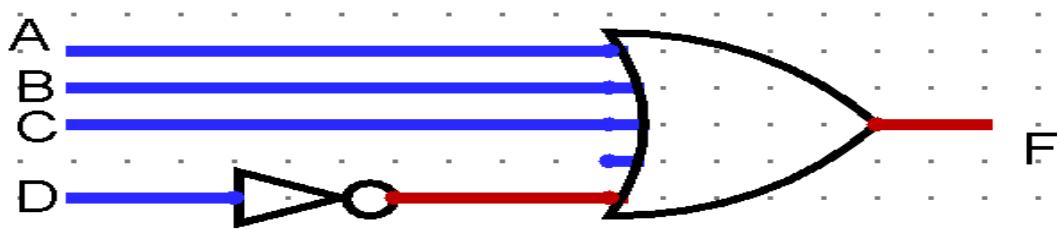
**Figure 22. LED6 :**  $F = C'D' + CD + A + B'D'$



**Figure 23. LED7 :**  $F = D' + B'C + BC' + A$



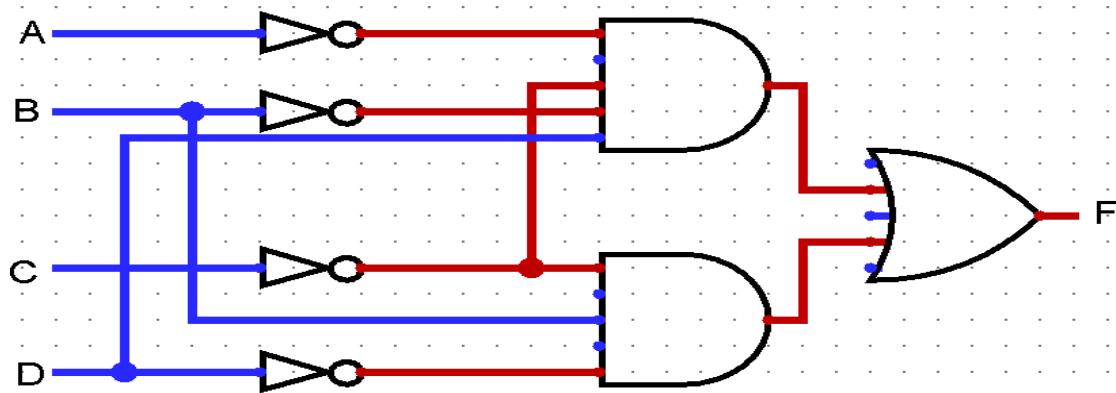
**Figure 24. LED8 :**  $F = CD' + C'D + B'D + A$



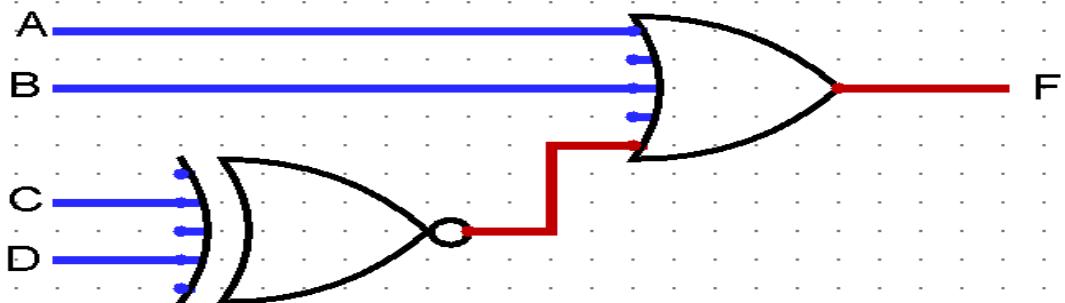
**Figure 25.** LED9 :  $F = D' + C + B + A$



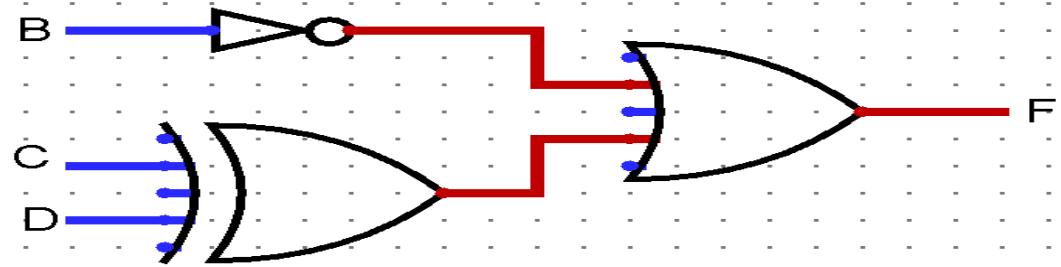
**Figure 26.** LED10 :  $F = D'$



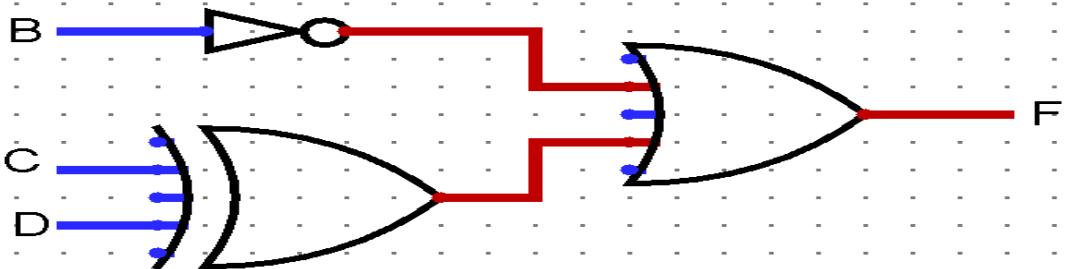
**Figure 27.** LED11 :  $F = A'B'C'D + BC'D'$



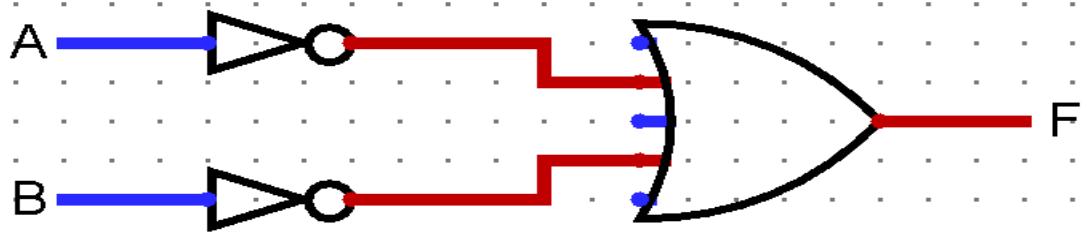
**Figure 28.** LED12 :  $F = C'D' + CD + B + A$



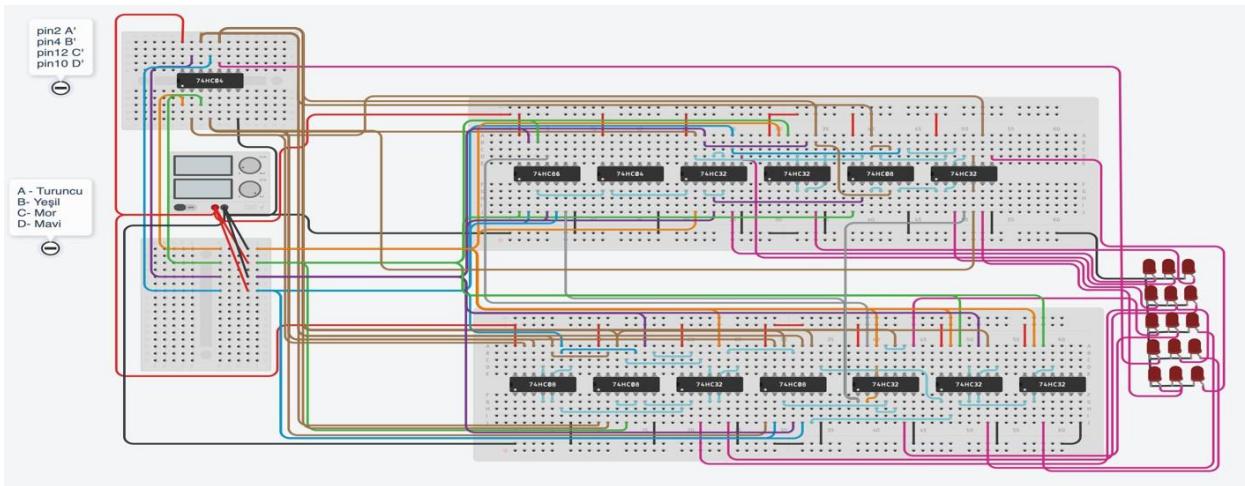
**Figure 29.** LED13 :  $F = B' + C'D + CD'$



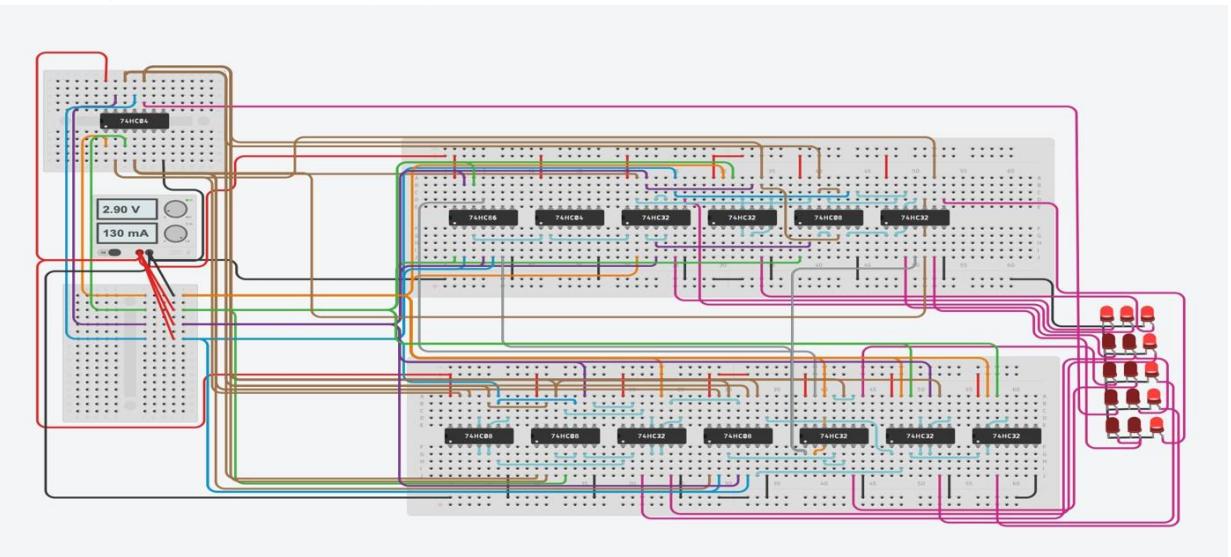
**Figure 30.** LED14 :  $F = B' + C'D + CD'$



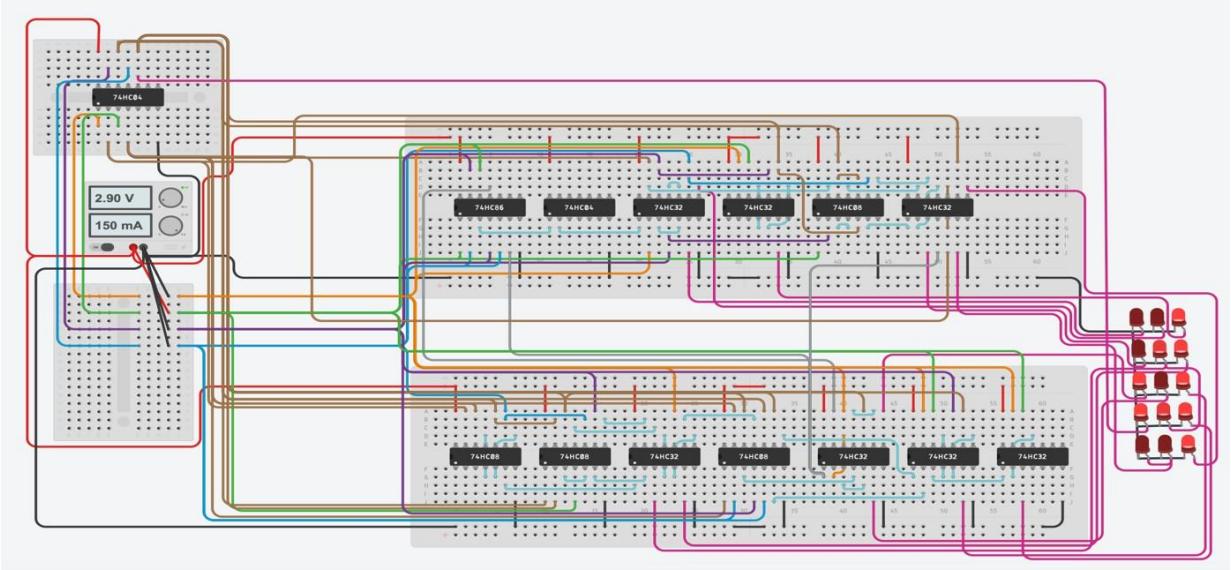
**Figure 31.** LED15 :  $F = A' + B'$



**Figure 32.** The circuit set up for part 1 in TinkerCAD



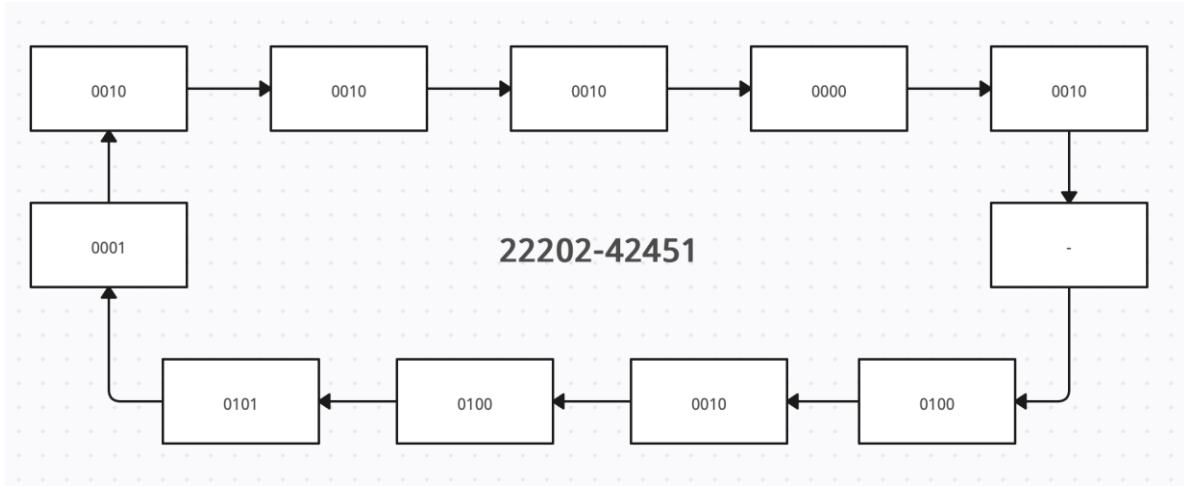
**Figure 33.** Displaying "7" on 15-pixel LED display for part 1 in TinkerCAD



**Figure 34.** Displaying "4" on 15-pixel LED display for part 1 in TinkerCAD

### **3. Part 2 : Design of ID Code Generator**

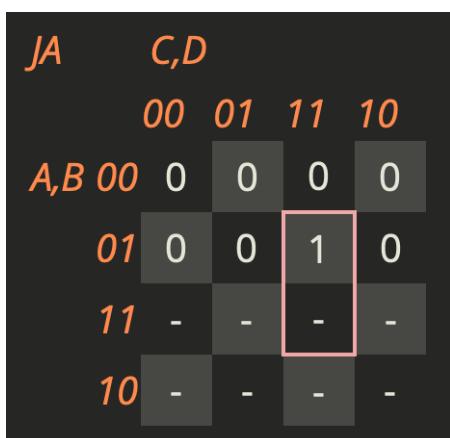
The initial step undertaken in this part of the project was to design a comprehensive state diagram. This diagram was crucial for determining the precise order in which the digits 22202-42451 would be displayed. This systematic approach allowed for the visualization of the process flow and served as a foundational guide for implementing the digit display mechanism.



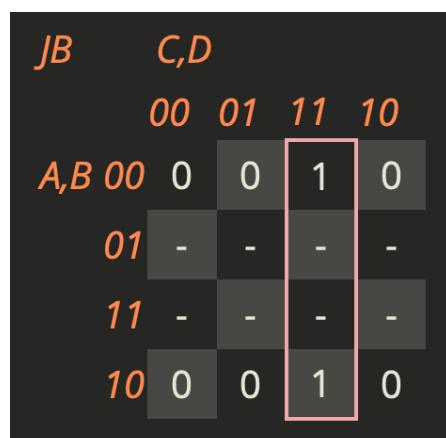
**Figure 35.** State diagram of part 2

**Table 2.** The truth table of second part

Current State				Next State				Output				A Flip-Flop		B Flip-Flop		C Flip-Flop		D Flip-Flop		
A	B	C	D	A*	B*	C*	D*	W	X	Y	Z	JA	KA	JB	KB	JC	KC	JD	KD	
0	0	0	0	0	0	0	1	0	0	1	0	0	X	0	X	0	X	1	X	
0	0	0	1	0	0	1	0	0	0	1	0	0	X	0	X	1	X	X	1	
0	0	1	0	0	0	1	1	0	0	0	1	0	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	0	0	0	0	X	1	X	X	1	X	1	
0	1	0	0	0	1	0	1	0	0	0	1	0	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	X	X	X	X	0	X	X	0	1	X	X	1	
0	1	1	0	0	1	1	1	0	1	0	0	0	X	X	0	X	0	1	X	
0	1	1	1	1	0	0	0	0	0	0	1	0	0	X	X	1	X	1	X	
1	0	0	0	1	1	0	0	1	0	1	0	0	X	0	0	X	0	X	1	
1	0	0	1	1	0	1	0	0	1	0	1	0	X	0	0	X	1	X	1	
1	0	1	0	1	0	1	1	0	0	0	0	1	X	0	0	X	0	1	X	
1	0	1	1	1	1	1	0	0	X	X	X	X	X	0	1	X	X	1	X	
1	1	0	0	1	1	0	1	X	X	X	X	X	0	X	0	0	X	1	X	
1	1	0	1	1	1	1	0	X	X	X	X	X	0	X	0	1	X	X	1	
1	1	1	0	1	1	1	1	X	X	X	X	X	0	X	0	X	0	1	X	
1	1	1	1	0	0	0	0	X	X	X	X	X	1	X	1	X	1	X	1	



**Figure 36.** K-map of JA



**Figure 37.** K-map of JB

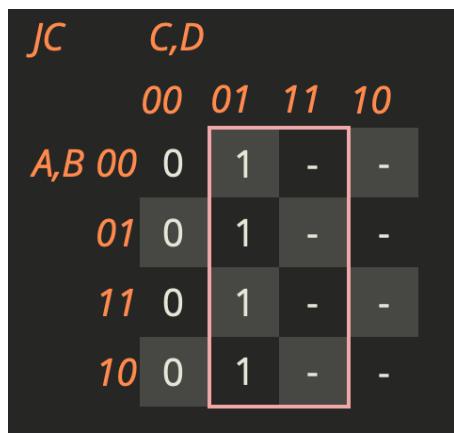


Figure 38. K-map of  $JC$

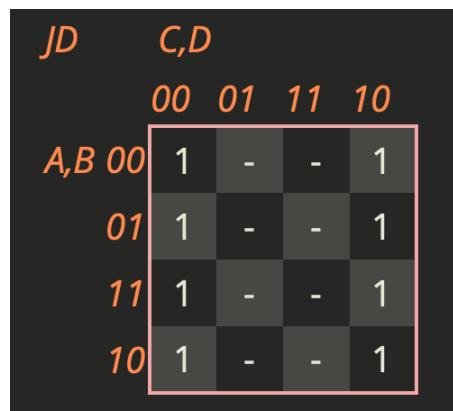


Figure 39. K-map of  $JD$

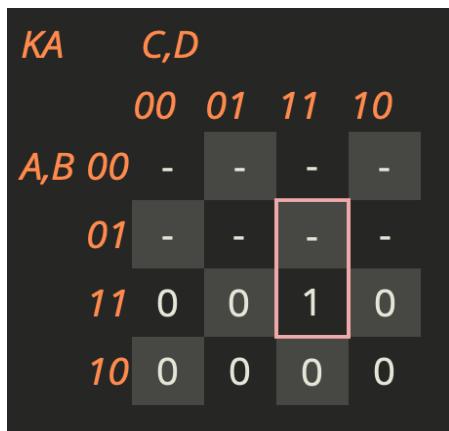


Figure 40. K-map of  $KA$

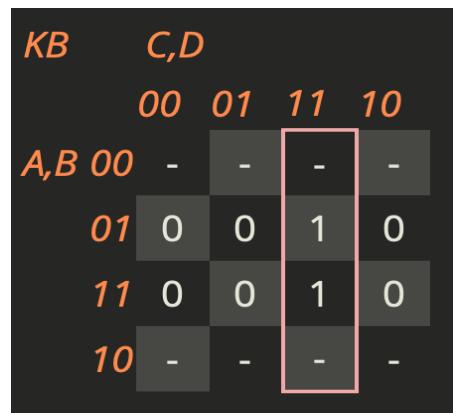


Figure 41. K-map of  $KB$

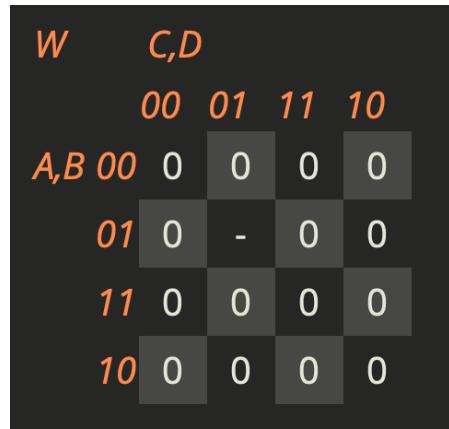


Figure 42. K-map of  $W$

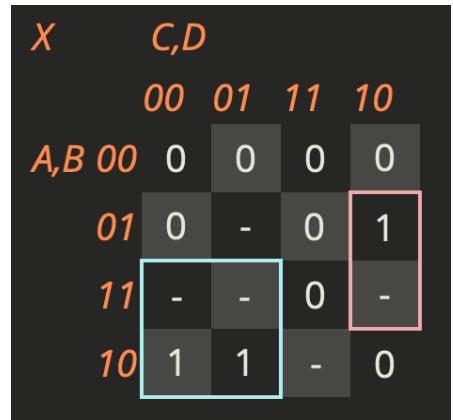


Figure 43. K-map of  $X$

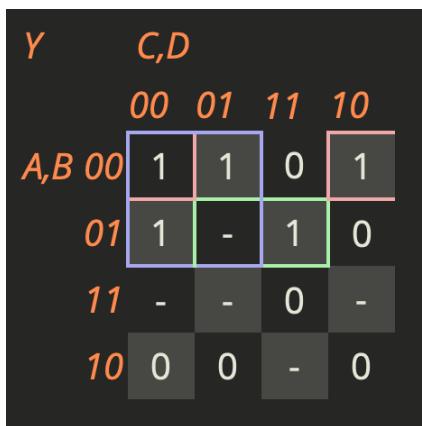


Figure 44. K-map of Y

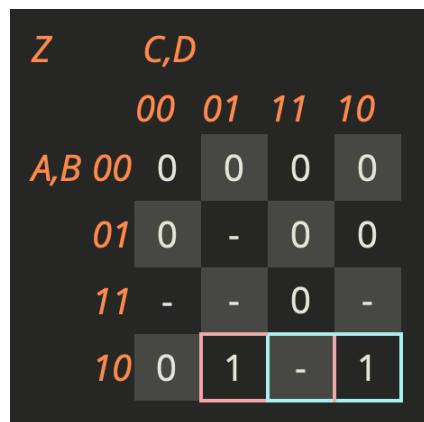


Figure 45. K-map of Z

Table 3. The displayed numbers according to their order of digit

Order of the Digit	Display Number
1	2
2	2
3	2
4	0
5	2
6	4
7	2
8	4
9	5
10	1

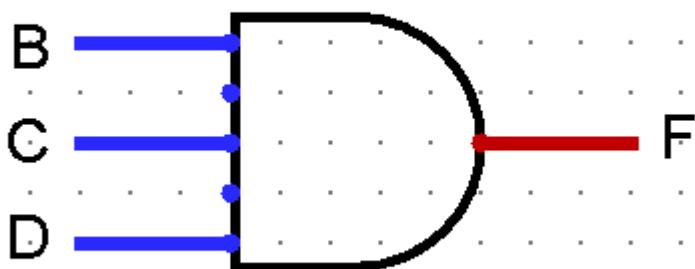
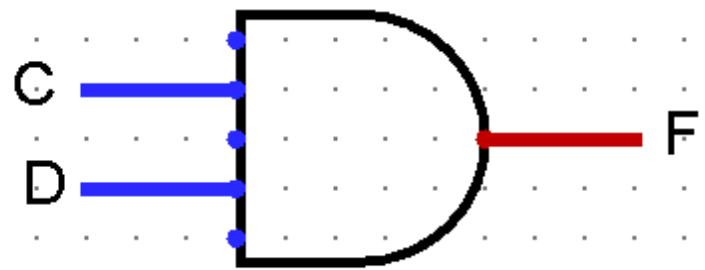


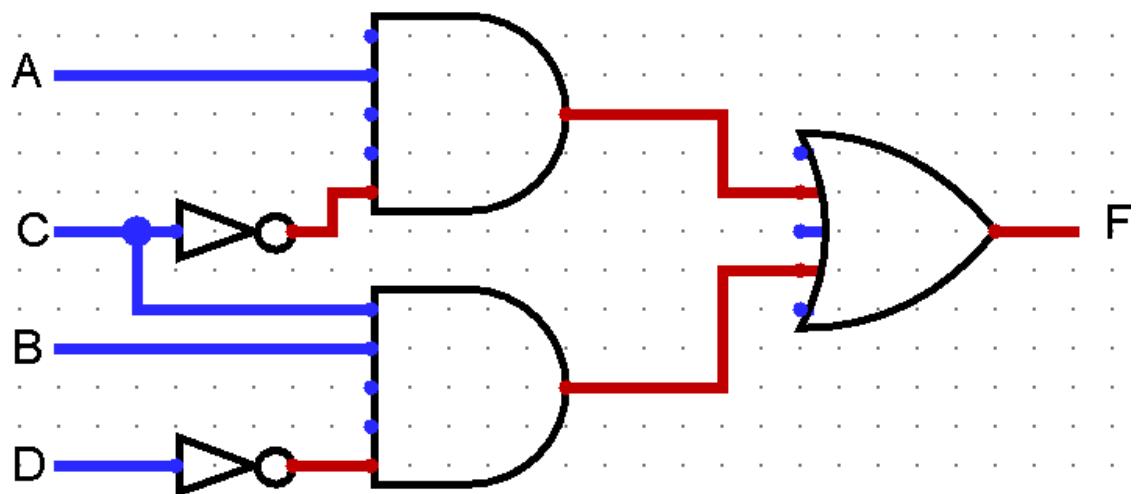
Figure 46. JA, KA circuit diagram



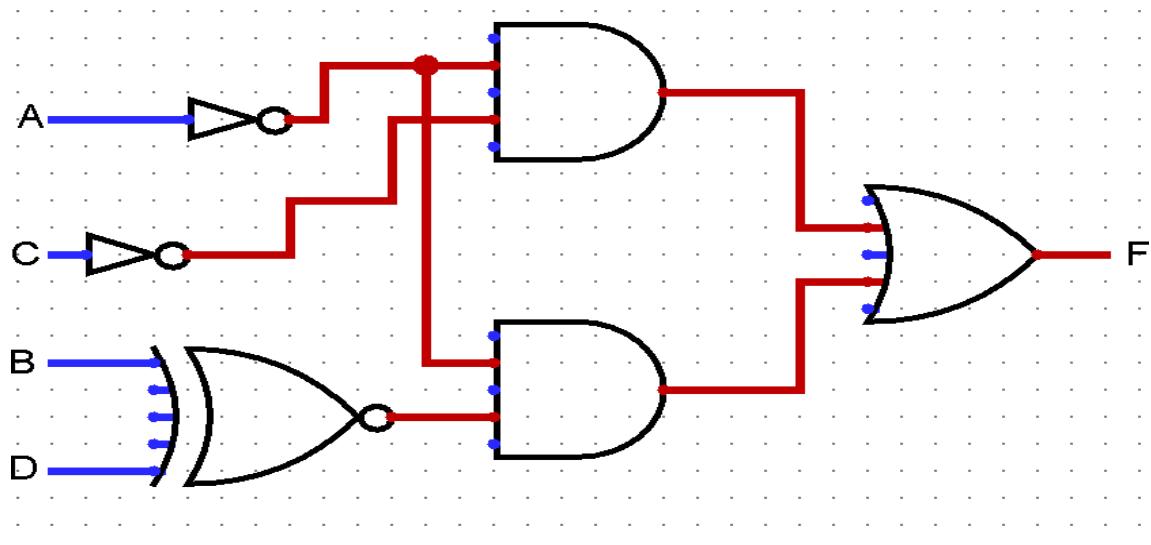
**Figure 47.** JB, KB circuit diagram



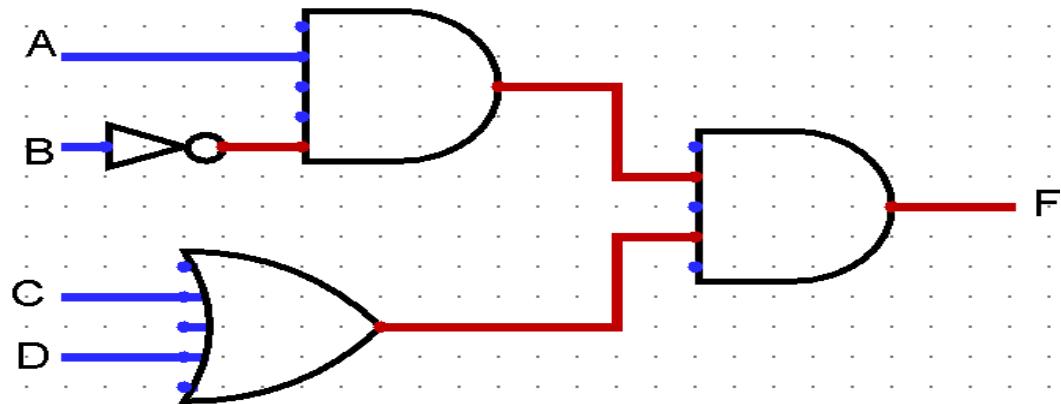
**Figure 48.** JC, KC circuit diagram



**Figure 49.** X's circuit diagram



**Figure 50.** Y's circuit diagram



**Figure 51.** Z's circuit diagram