PES University, Bangalore

(Established under Karnataka Act No. 16 of 2013)

UE21EC251B – Digital VLSI Design

DVD – Project

Session: Jan-May 2023

Question: **CMOS Inverter with balanced rise and fall time**

Branch: **ECE**

Semester & Section: **Semester 4, Section A**

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Name of the Course Instructor :

Signature of the Course Instructor

(with Date) : _____

Introduction:

An inverter is a logic circuit that implements binary logical negation, and converts high logic levels to low logic level, and vice versa, i.e invert the input signal and generate its complement as output. The input signal can be a logical high or logical low, represented by a voltage level in digital electronics.

There are different types of inverter circuits available, including CMOS (Complementary Metal-Oxide-Semiconductor), NMOS (Negative Metal-Oxide-Semiconductor), and resistive load inverters.

The CMOS inverter consists of a P-channel MOS transistor and an N-channel MOS transistor that are connected in series between the power supply voltage and ground. The output of the inverter is obtained at the junction of the two transistors, and the input signal is applied to the combined gate terminal of the two transistors. When the input signal is logical low, the P-channel MOSFET is turned on, and the N-channel MOSFET is turned off. Conversely, when the input signal is logical high, the P-channel MOSFET is turned off, and the N-channel MOSFET is turned on.

CMOS inverters are preferred over other types of inverters due to high noise immunity, low power consumption, and high output drive capability. CMOS technology also allows implementation of complex logic gates and circuits with low power consumption.

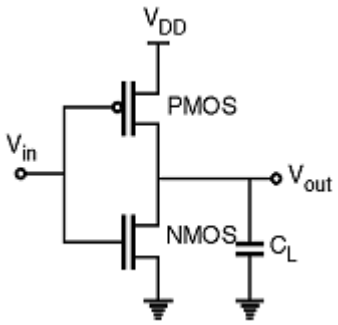


Fig: CMOS Inverter

Timing Characteristics:

A CMOS inverter has the following timing characteristics:

- Rise Time (t_r):
  - Time required to increase the output voltage from 10% to 90%.
- Fall Time (t_f):
  - Time required to decrease the output voltage from 10% to 90%.
- High-Low Propagation delay (t_{pHL}):
  - Time delay between 50% of V_{OH} transition of rising input and 50% of the falling output
- Low-High Propagation delay (t_{pLH}):
  - Time delay between 50% of V_{OH} transition of falling input and 50% of the rising output
- Contamination Delay (t_{cd}):
  - It is the smallest time from the 50% input crossing to the 50% output crossing.

Aim:

To find inverter characteristics for an inverter with equivalent Rise time and fall time

Formulae:

$$\tau_f = \frac{2(0.1V_{OH} - V_{th})}{K_n(V_{OH} - V_{th})^2} - \frac{C_{Load}}{K_n(V_{OH} - V_{th})} \ln\left(\frac{1.9V_{OH} - 2V_{th}}{0.1V_{OH}}\right)$$

Fall time

$$\tau_r = \frac{2(0.1V_{OH} - |V_{th}|)}{K_p(V_{OH} - |V_{th}|)^2} - \frac{C_{Load}}{K_p(V_{OH} - |V_{th}|)} \ln\left(\frac{1.9V_{OH} - 2|V_{th}|}{0.1V_{OH}}\right)$$

Rise time

Values:

- $V_{tn} = 542.077\, mV$
- $V_{tp} = -507.834\, mV$
- $C_{Load} = 100\, fF$
- $\mu_n C_{ox} = 503.3304\ \frac{\mu A}{V^2}$
- $\mu_p C_{ox} = 96.3072\ \frac{\mu A}{V^2}$

$$\tau_r = \frac{2(0.1 \times 1\ -\ 507.834 \times 10^{-3})}{K_p(1\ -\ 507.834 \times 10^{-3})^2} - \frac{100 \times 10^{-15}}{K_p(1\ -\ 507.834 \times 10^{-3})} \ln\left(\frac{1.9\ -\ 2 \times 507.834 \times 10^{-3}}{0.1}\right)$$

$$\tau_r = -\frac{3.367365111}{K_p}$$

$$\tau_f = \frac{2(0.1 \times 1\ -\ 542.077 \times 10^{-3})}{K_n(1\ -\ 542.077 \times 10^{-3})^2} - \frac{100 \times 10^{-15}}{K_n(1\ -\ 542.077 \times 10^{-3})} \ln\left(\frac{1.9\ -\ 2 \times 542.077 \times 10^{-3}}{0.1}\right)$$

$$\tau_f = \frac{-4.216411619}{K_n}$$

$$\frac{K_p}{K_n} = \frac{-4.216411619}{-3.36736511} = 1.252139724$$

$$\frac{\mu_p C_{ox} W_p}{\mu_n C_{ox} W_n} = 1.252139724$$

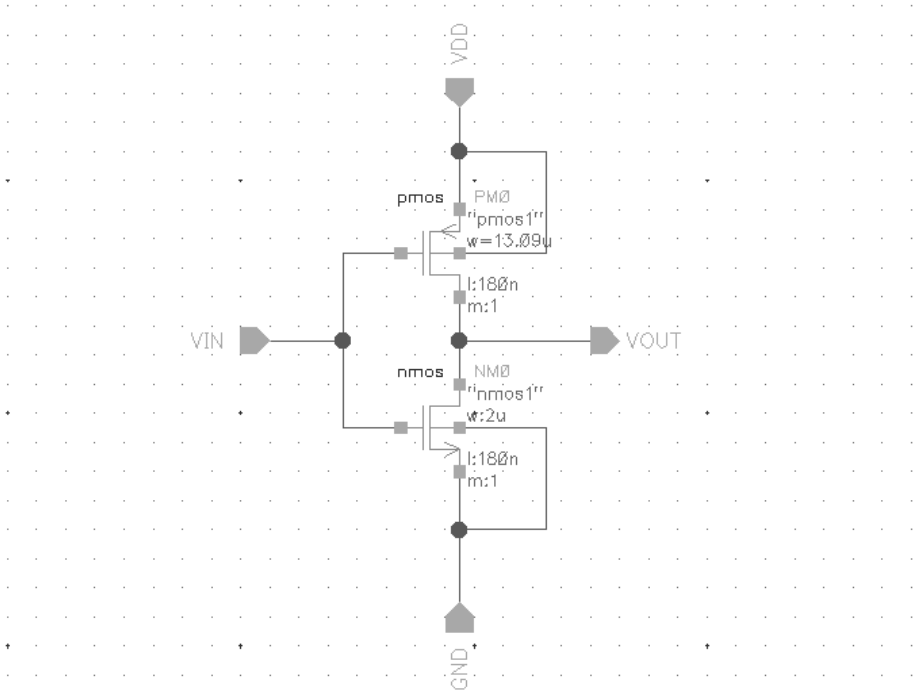
$$\frac{W_p}{W_n} = 6.544058888$$

$$W_p = 6.544058888 \times W_n$$

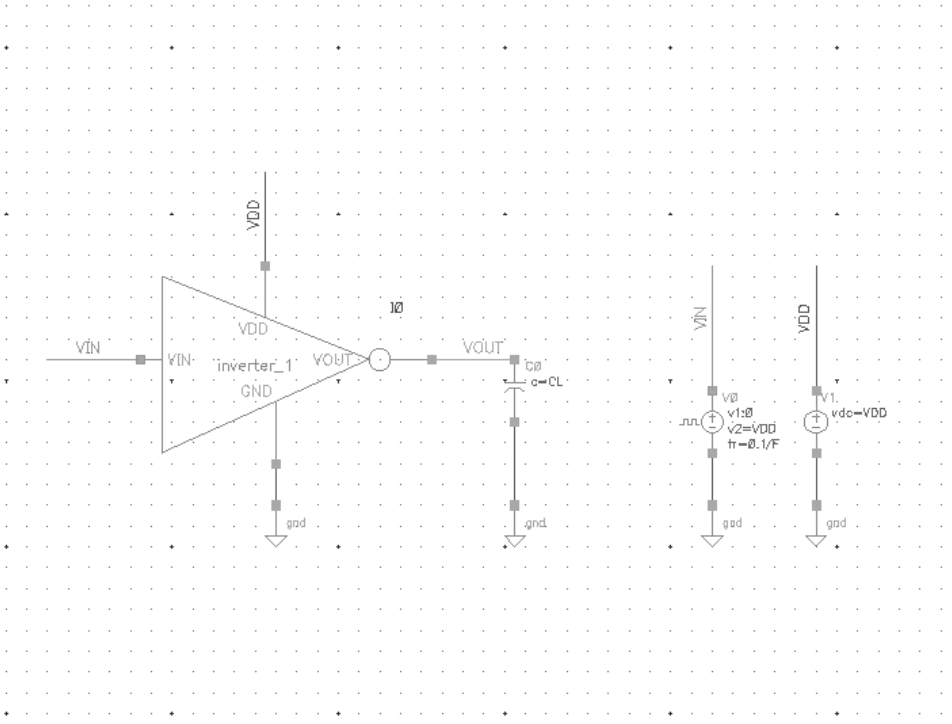
Let $W_n = 2\mu m$, then

$$W_p = 13.08811778\ \mu m$$

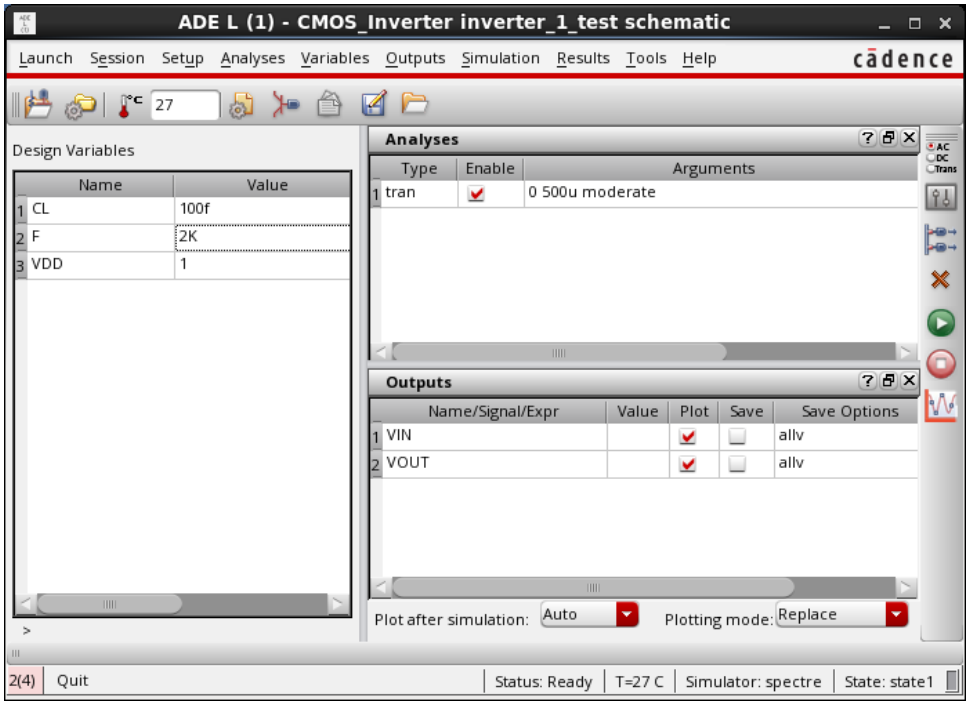
Circuit:



CMOS Inverter



CMOS Test Circuit



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Output Graph: