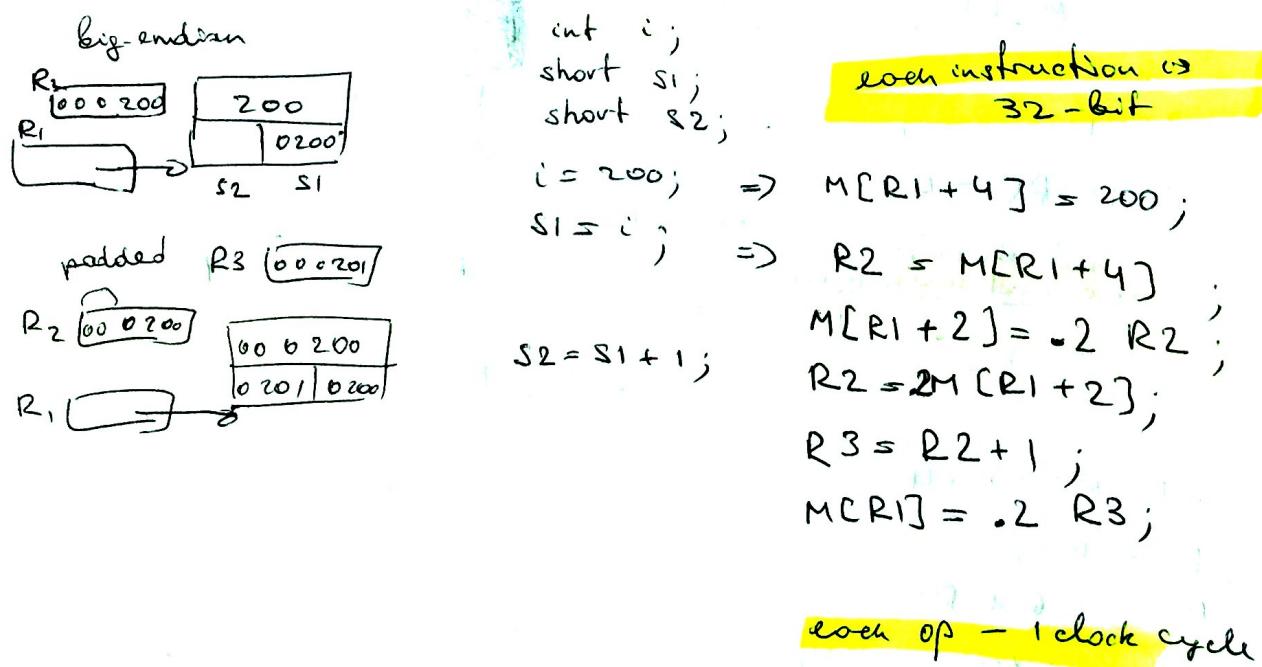
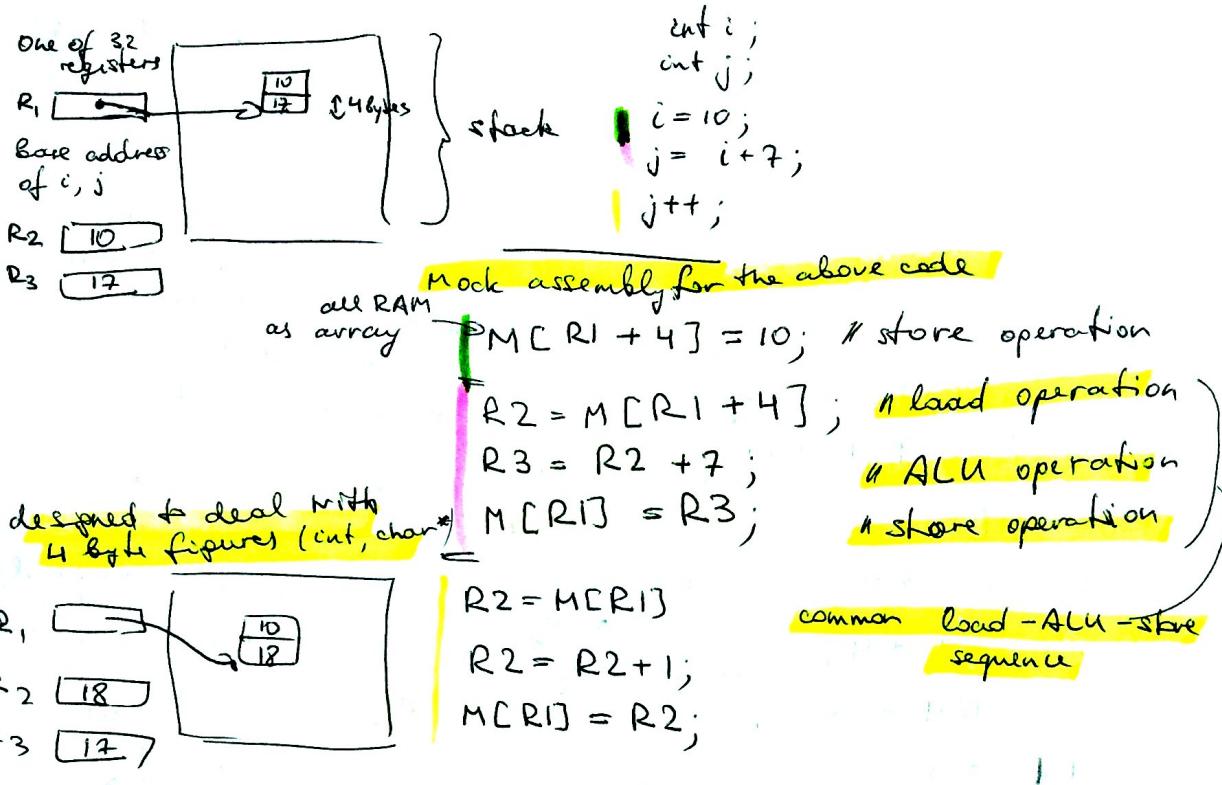


## CS 107 Lecture 9 Assembly

①



```

int array [4];
int i;

```

```

for (i=0; i<4; i++) {
    array[i] = 0;
}
i--;

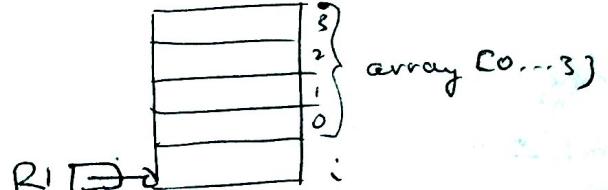
```

```

= M[R1] = 0;           reload after
                      JMP
= R2 = M[R1];          program counter
                      (address of currently
                      executed instr.)
B GE R2, 4, PC+40     greater or
                      equal branching
R3 = M[R1]; { i < reload to be context
                      insensitive
R4 = R3 * 4; } offset
                      in bytes
R5 = R1 + 4; { base
                      address
R6 = R4 + R5;         array[i] = 0;
M[R6] = 0;             jump when
                      test passes
= R2 = M[R1];          reload to
                      be context
                      insensitive
R2 = R2 + 1;           i++
M[R1] = R2;             i--;
JMP PC - 40;           (10 instructions,
                      each 4 bytes)

```

each i is used, reload it to keep context insensitivity



The hardware makes sure that base address of an relevant activation record is stored in a register (e.g. R1)

### Branch instruction

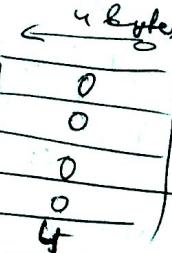
B EQ (equal)

B NE (not equal)

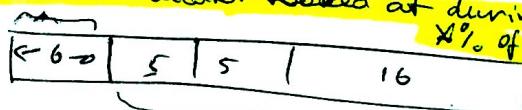
B LE (less equal to)

B GT (greater than)

B GE (greater equal to)



Encoding of instructions: instruction structure indicator loaded at during first  $\frac{X}{Y}$  % of clock cycle



R1 = M[R2 + 4]; 000 000

R1 = 100; 000 001

R3 = R6 \* R10; 010011

M[R1 - 20] = R19; 111 111

fill out the instruction structure (example numbers)

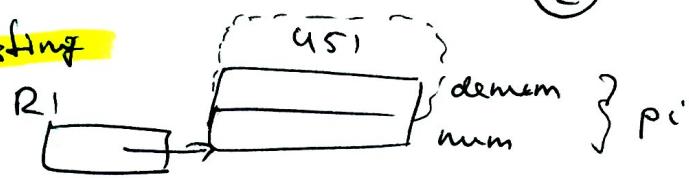
e.g. Huffman encoding

CS 107 Lecture 9

2

## Struct and pointers, casting

struct fraction {  
    int num;  
    int denom;  
};



street fraction pi;

$$\text{pi. num} = 22; \Rightarrow \text{M[R1]} = 22;$$

$$\text{Pr. denum} = 7'; \Rightarrow M[R1 + 4] = 7;$$

(struct fraction \*) & p1. denom ) -> denom = 451;

$$\Rightarrow M[R1 + 8] = 451;$$

A cart does not add code; if computer allows to generate code that it would otherwise not generate.