COA Group-4

1.Which of the following is a characteristic of Von Neumann architecture

a.Separate data and instruction memory

b.Shared data and instuction memory

c. Parallel processing of instructions

d.Uses only cache memory

Ans=b

2.The time taken to access a memory location and obtain its contents is called:

1. Cycle time
2. Latency time
3. Access time
4. Seek time

Answer: C Access time

3.A cache memory uses 4-way set-associative mapping with 256 sets. How many blocks can be stored in the cache?

A) 64

B) 256

C) 1024

D) 2048

Answer: C) 1024

4.Register renaming is done in pipelined processors \_\_\_\_\_\_\_\_\_

1. As an alternative to register allocation at compile time
2. For efficient access to function parameters and local variables
3. To handle certain kinds of hazards
4. As part of address translation

ANS: C)

5.The process of mapping a logical address to a physical address is called:

1. Address translation
2. Address binding
3. Address mapping
4. Address allocation

Ans: A) Address translation

6.\_\_\_\_\_\_\_ is a special type of memory that works like both RAM and ROM.

1)Register memory

2)Secondary memory

3)Flash memory

4)Cache memory

Ans -3

7.A computer system with a direct-mapped cache has 128 blocks and a block size of 16 bytes. If the total memory size is 64 KB, how many bits are used for the tag field?

A) 6

B) 7

C) 9

D) 10

Answer: C) 9

8.Which of the following is a non-volatile memory?

1. DRAM
2. SRAM
3. PROM
4. Cache memory

Answer: C. PROM

9.Consider a non-pipelined processor with a clock rate of 2.5 gigahertz and average cycles per instruction of four. The same processor is upgraded to a pipelined processor with five stages; but due to the Intemal pipeline delay, the clock speed is reduced to 2 gigahertz. Assume that there are no stalls in the pipeline. The speedup achieved in this pipelined processor is

A 3.2

B. 3.0

C. 2.2

1. 2.0

ANS: A

10.If each address space represents one byte of storage space, how many address lines are needed to access RAM chips arranged in a 4 x 6 array, where each chip is 8K x 4 bits ?

A)13

B)15

C)16

D)17

Ans: D)17

11.The dynamic hazard problem occurs in

1. Combinational circult alone
2. Sequential circuit only
3. Both (A) and (B)
4. None of the above

ANS: C

12.Which of the following register automatically increments its contents during the instruction Execution?

1. Instruction Register(IR)

(b) Program Counter(PC)

c)General Purpose Register

(d) Link Register

Ans)b

13.Pipelining can introduce hazards in CPU execution. Which of the following is NOT a hazard

Typically encountered in pipelined architectures?

a) Structural hazard

b) Data hazard

c) Control hazard

d) Logical hazard

Ans: d) Logical hazard