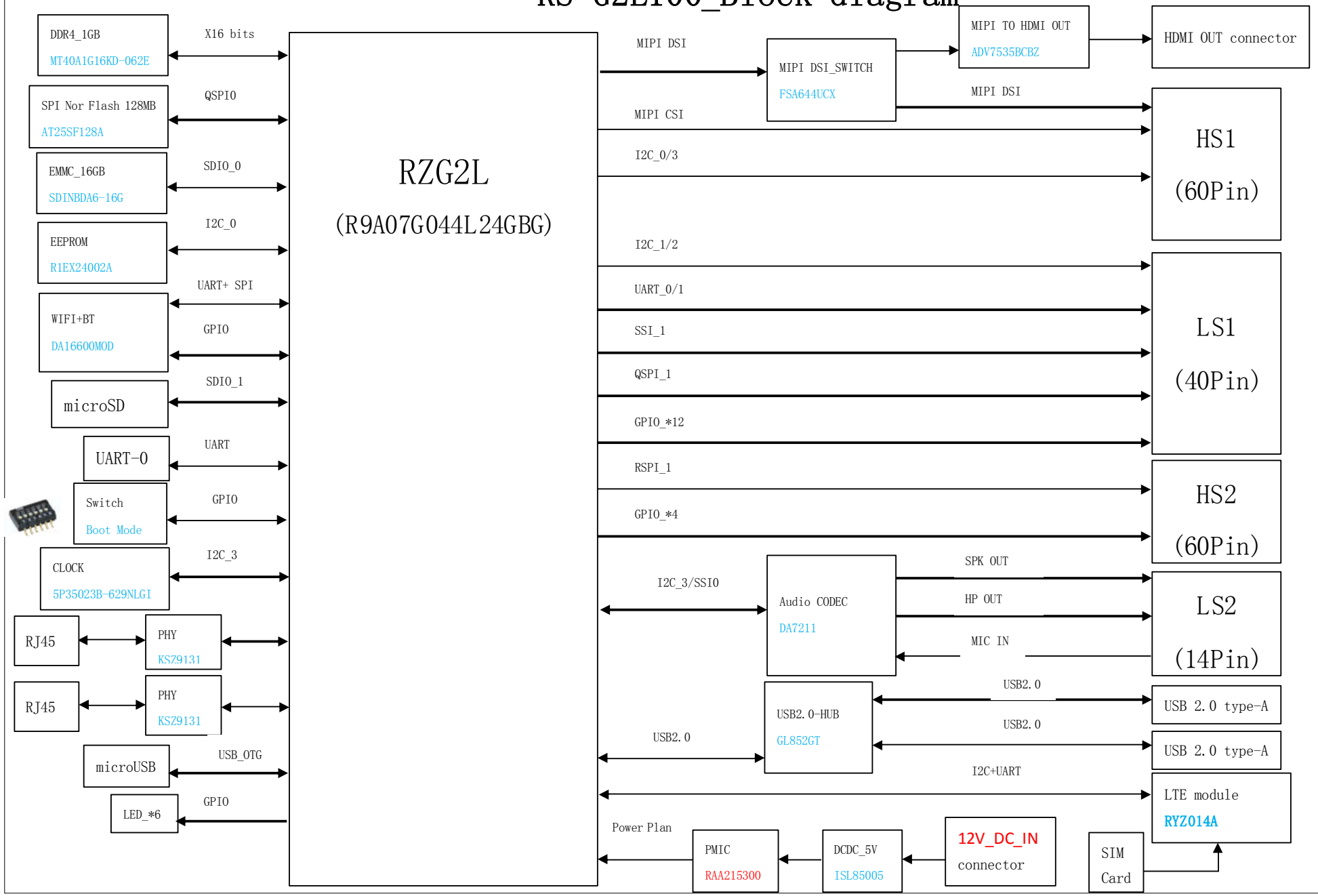
RZ/G2L 15mmPKG 96Boards-CE

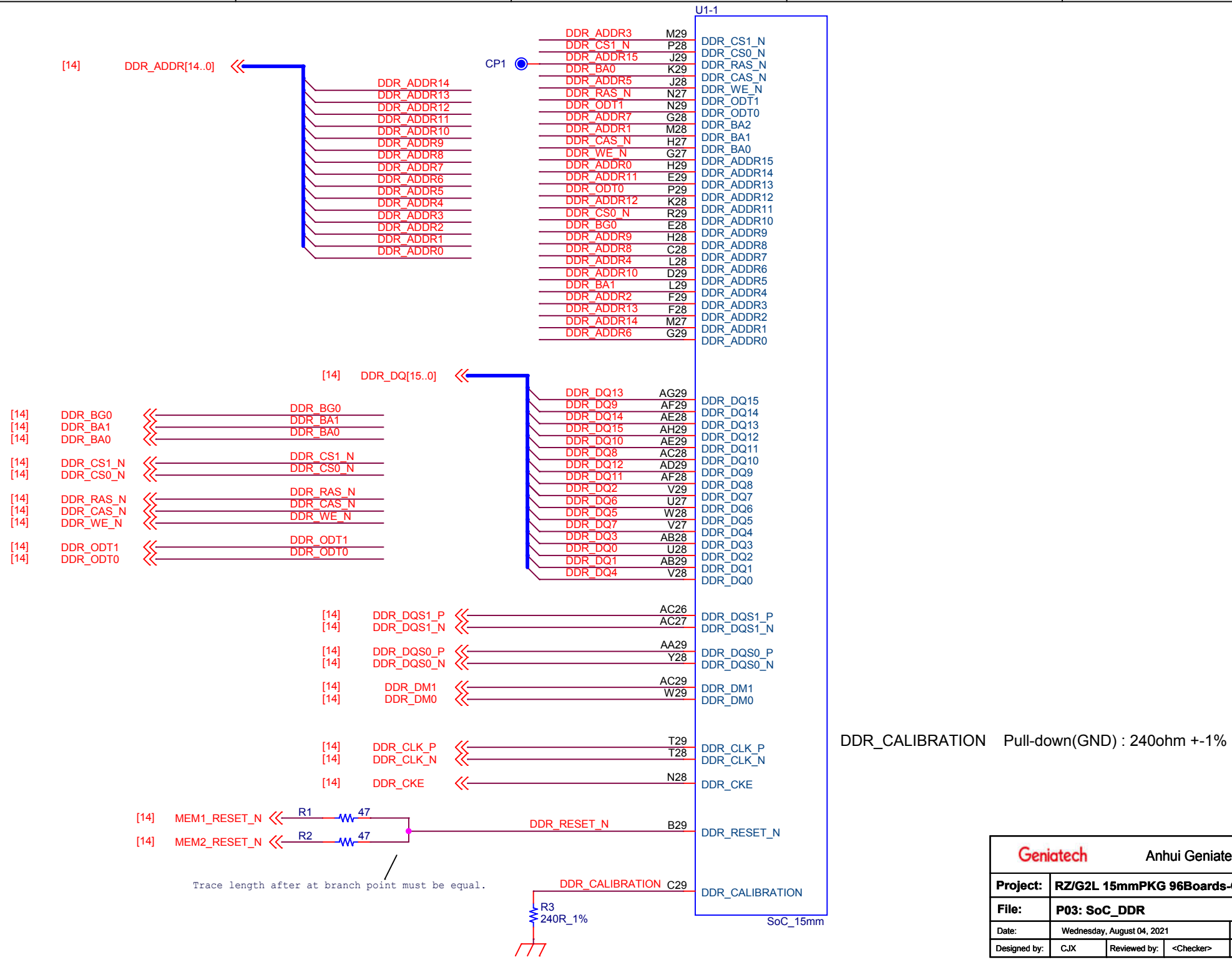
Rev:1.0

Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P01: TITLE				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	1 of 24

RS-G2L100_Block diagram



Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P02: Block diagram				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	2 of 24



Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P03: SoC_DDR				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	3 of 24

SoC SD0/1 I/F

SD0_PVDD=1.8V
SD1_PVDD=3.3V

U1-7

P18_0/SD0_CD/GTIOC0A/RIIC3_SDA/MTIOC2A
SD0_CLK
SD0_CMD
SD0_DATA0
SD0_DATA1
SD0_DATA2
SD0_DATA3
SD0_DATA4
SD0_DATA5
SD0_DATA6
SD0_DATA7
SD0_RST_N
P18_1/SD0_WP/GTIOC0B/RIIC3_SCL/MTIOC2B

P19_0/SD1_CD/GTIOC3A/MTIOC1A/RIIC2_SDA
SD1_CLK
SD1_CMD
SD1_DATA0
SD1_DATA1
SD1_DATA2
SD1_DATA3
P19_1/SD1_WP/GTIOC3B/MTIOC1B/RIIC2_SCL

SoC_15mm

D3.3V_M
R4 2.2K R0402
R5 2.2K R0402
RIIC3_SDA [6,10,16]
RIIC3_SCL [6,10,16]

SD0 (CLK,CMD,DAT[7:0])
(1) Matched trace length.
(2) Single ended impedance = 50ohm
SD1 (CLK,CMD,DAT[3:0])
(1) Matched trace length.
(2) Single ended impedance = 50ohm

D3.3V_M
R9 10K R0402
R10 10K R0402
R14 0R R0402 P19_1_LS1_GPIO-G

SD0 I/F (EMMC)

VDD_SD0_M
R6 4.7K R0402
R7 4.7K R0402
R8 4.7K R0402
SD0_DATA0
SD0_DATA1
SD0_DATA2
SD0_DATA3
SD0_DATA4
SD0_DATA5
SD0_DATA6
SD0_DATA7
SD0_CMD
SD0_CLK
SD0_RST_N
R11 22R R0402 eMMC_CLK
R12 0R R0402 eMMC_RST

D3.3V_M
C1 4.7uF C0402
C2 100nF C0402
C3 100nF C0402
E6 F5 J10 K9 VCC1 VCC2 VCC3 VCC4

U2A
SDINBDA6-16G
DAT0 DAT1 DAT2 DAT3 DAT4 DAT5 DAT6 DAT7 CMD CLK RST
VCCQ1 VCCQ2 VCCQ3 VCCQ4 VCCQ5 VDDIM
VSSQ1 VSSQ2 VSSQ3 VSSQ4 VSSQ5 DS
VSS1 VSS2 VSS3 VSS4 VSS5 VSS6

VDD_SD0_M
C4 100nF C0402
C5 100nF C0402
C6 100nF C0402
C7 4.7uF C0402
C8 100nF C0402
C9 4.7uF C0402
eMMC_VDDIM
eMMC_DQS
R13 NC R0402

SD1 I/F (MicroSD)

U2B
SDINBDA6-16G

VDD_SD1_M
R15 NC R0402
R16 10K R0402
R17 10K R0402
R18 10K R0402
R19 10K R0402
R20 10K R0402
HS1_SD1_CLK
HS1_SD1_CMD
HS1_SD1_DATA0
HS1_SD1_DATA1
HS1_SD1_DATA2
HS1_SD1_DATA3
R21 NC SD1_CLK
R22 NC SD1_CMD
R23 NC SD1_DATA0
R24 NC SD1_DATA1
R25 NC SD1_DATA2
R26 NC SD1_DATA3

D3.3V_M
R28 4.7K R0402
U3
PCA9306DC1
GND EN
VREF1 VREF2
MSCL SSCL
MSDA SSDA
VSSOP8
RIIC3_SCL
RIIC3_SDA
D1.8V_M
R29 200K R0402
R30 10K R0402
R31 10K R0402
HS1_I2C3_SCL
HS1_I2C3_SDA

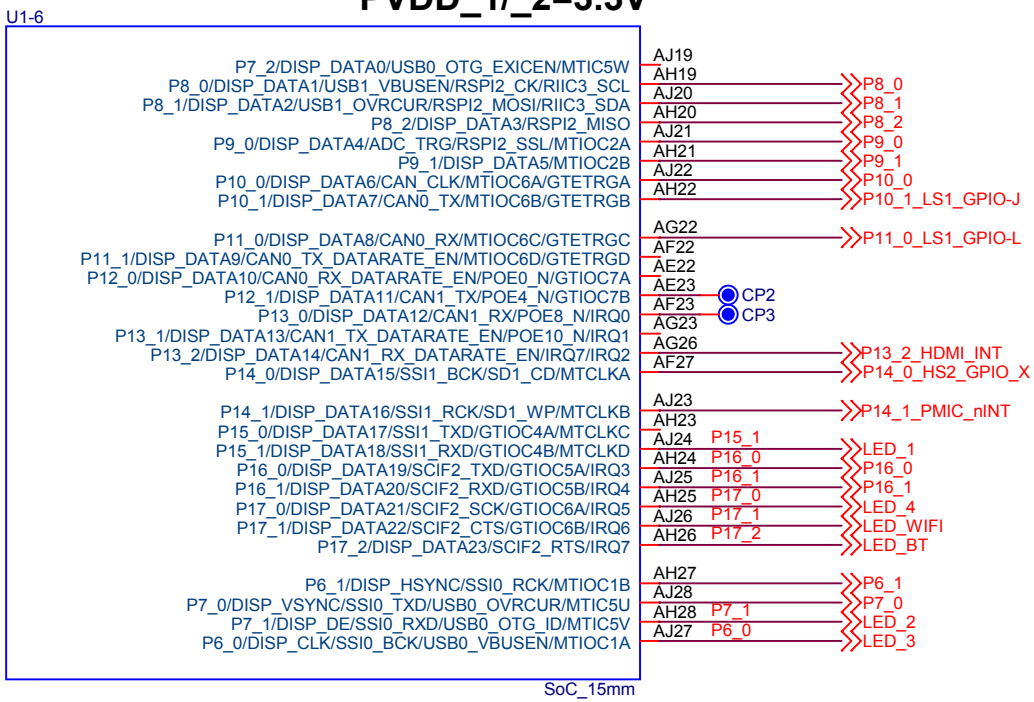
D3.3V_M
Q1
AO3402
SOT-23
C10 10uF C0603
C11 1uF C0402
C12 100nF C0402
[9] SD1_PWR_EN
R27 10K R0402

J1
SD1_CD
SD1_CMD
SD1_CLK
SD1_DATA0
SD1_DATA1
SD1_DATA2
SD1_DATA3
DET
CMD CLK DAT0 DAT1 DAT2 CD/DAT3
VDD VSS
GND3 GND4 GND2 GND1 GND5
CONN_SD_CARD 9
TF_CARD

Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P04: SoC_SD0/1				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	4 of 24

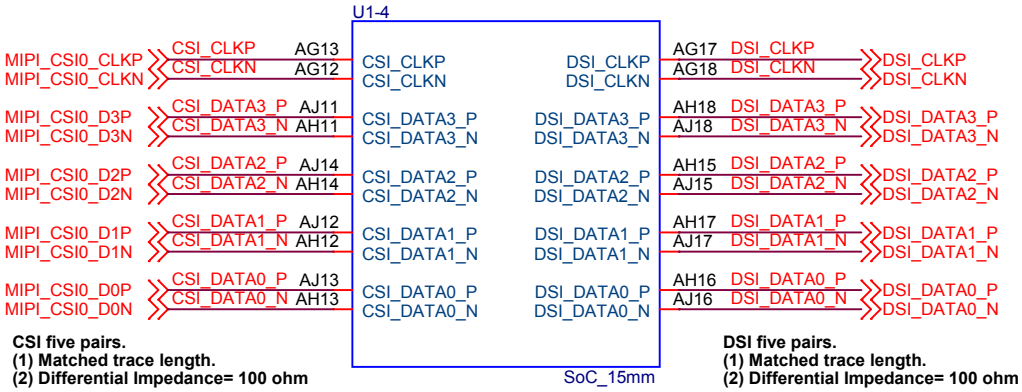
SoC DISP I/F

PVDD_1/_2=3.3V



SoC CSI/DSI I/F

CSI_VDD/DSI_VDD=1.8V



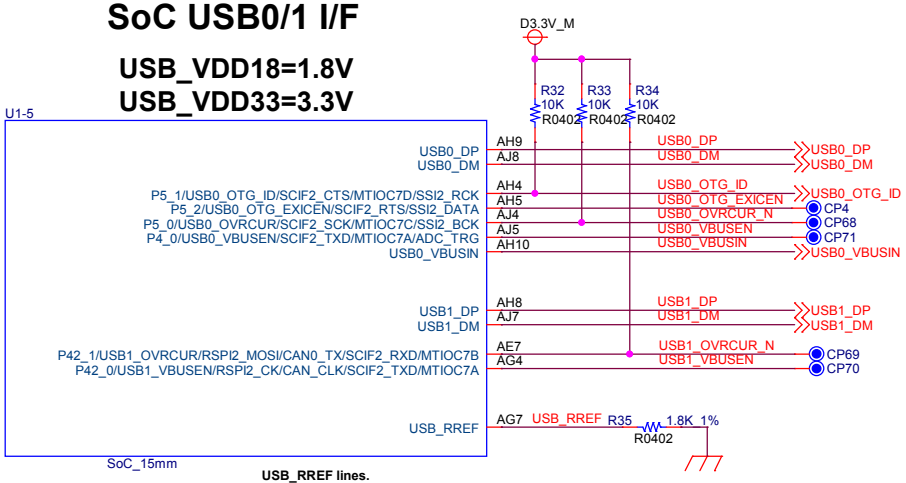
CSI five pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

DSI five pairs.
(1) Matched trace length.
(2) Differential Impedance= 100 ohm

Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P05: SoC_CSI/DSI_DISP				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	5 of 24

SoC USB0/1 I/F

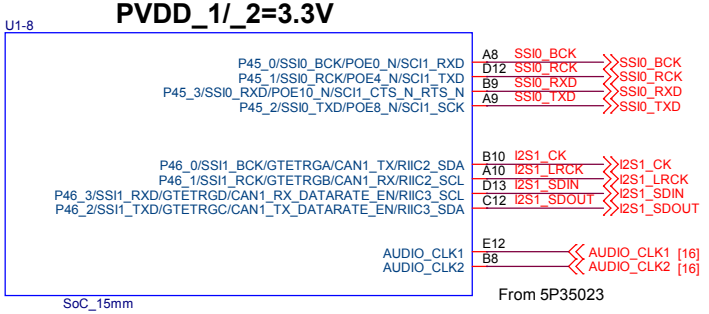
USB_VDD18=1.8V
USB_VDD33=3.3V



USB_RREF lines.
(1) Place the RREF resistor near the IC
and design the RREF wiring to be 0.5ohm or less.

SoC SSI0/1 I/F

PVDD_1/_2=3.3V

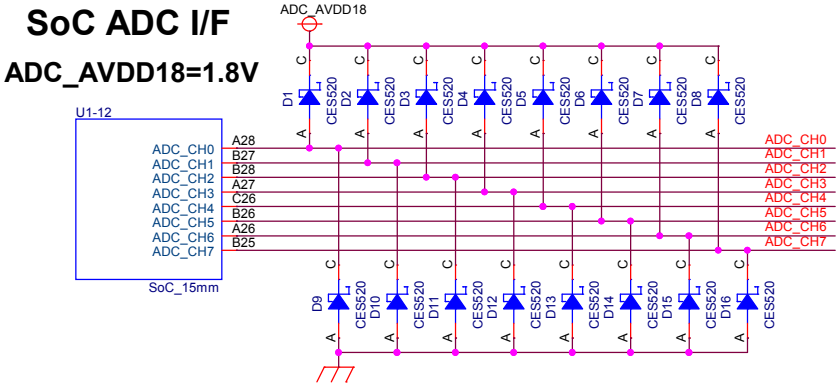


From 5P35023

AUDIO_CLK1 : 11.2896MHz(used as CD sampling rate 44.1KHz refclock)
AUDIO_CLK2 : 12.2880MHz(used as DVD sampling rate 48.0KHz refclock)

SoC ADC I/F

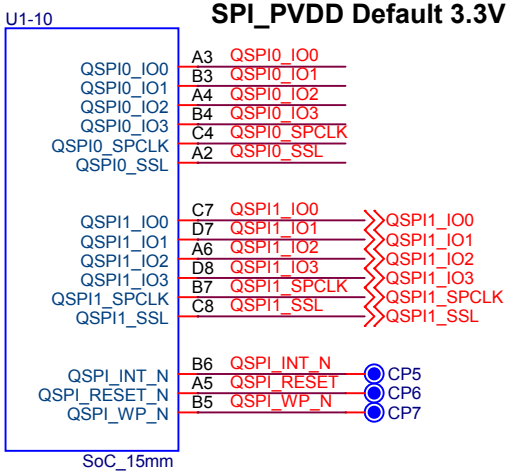
ADC_AVDD18=1.8V

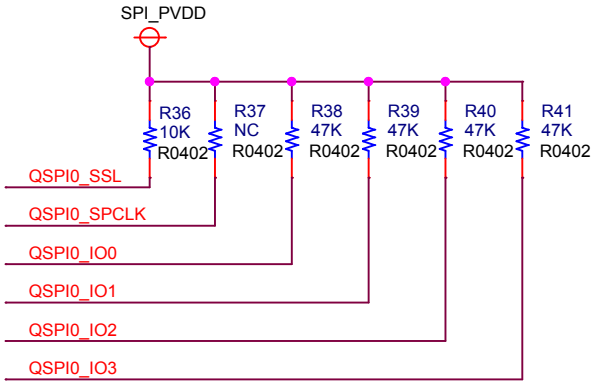


Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P06: SoC_SSI/ADC/USB				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	6 of 24

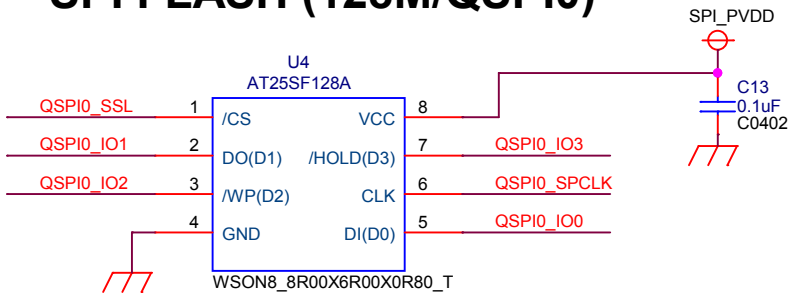
SoC SPI I/F

SPI_PVDD Default 3.3V





SPI FLASH (128M/QSPI0)



SoC ETHER0/1 I/F

ETHER0_PVDD--->ETHER_IO_VDD=1.8V
ETHER1_PVDD--->ETHER_IO_VDD=1.8V

Ether ET0 (RX_CTL,RXC,RXD[3:0],RX_ERR,TX_CTL,TXC,TX_COL,TX_CRS,TX_ERR,TXD[3:0])
(1) Matched trace length.
(2) Single ended impedance = 50ohm

R591-R596
Place near RZ/G2L
Wire with the same length

Layout Note:
Following signals need Ground guard.

ETHER_PHY1_CLK, ET0_TXC, ET0_RXC

Layout Note:
Matched Trace Length from SoC to KSZ9131RNX(Sub Board).
(max 250Mbps/pin) and Single ended impedance 50ohm.

Group 1
ET0_TXC
ET0_TX_CTL
ET0_TXD[3:0]
ET0_TX_COL
ET0_TX_CRS
ET0_TX_ERR
Group 2
ET0_RXC
ET0_RX_CTL
ET0_RXD[3:0]
ET0_RX_ERR

Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P07: SoC_QSPI/ETHER				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	7 of 24

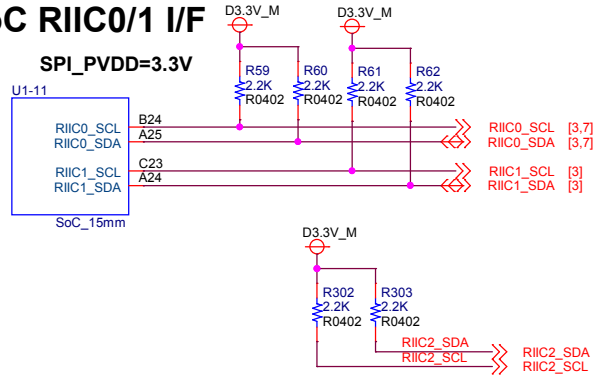
SoC Other I/F

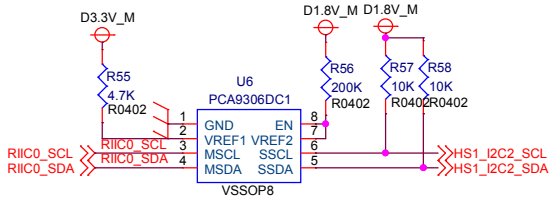
PVDD_1/_2=3.3V

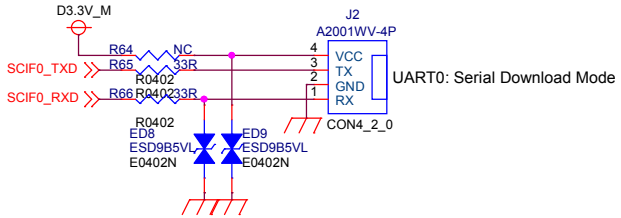
SCIF3_TXD : WIFI
SCIF3_RXD : WIFI
ET0_INTB(P1_0 IRQ2) : Connect to INT_N pin of KSZ9131RNX EtherPhy IC_0, used as IRQ2, CN C
ET1_INTB(P1_1 IRQ3) : Connect to INT_N pin of KSZ9131RNX EtherPhy IC_1, used as IRQ3, CN D
SCIF4_TXD : Connected to LTE
SCIF4_RXD : Connected to LTE
P3_0 : Connected to LS1
P3_1 : Connected to LS1
SCIF0_TXD : Serial Download Mode with UART to USB for Debug
SCIF0_RXD : Serial Download Mode with UART to USB for Debug
P39_0 : Connected to LS1
P39_1 : Connected to LS1
SD1_PWR_EN(P39_2) : used as "SD1_PWR_ON" to control SD1 card body 3.3V on-off
P4_1: Connected to MIPI DSI_SWITCH
SCIF1_TXD : Connected to LS1
SCIF1_RXD : Connected to LS1
P40_2 : Connected to LS1 HP_DET
P41_0 : SCIF1_CTS : Connected to LS1
P41_1 : SCIF1_RTS : Connected to LS1
P42_2 : Connected to LS1
P42_3 : RIIC2_SDA
P42_4 : RIIC2_SCL
P43_0 : Connected to LS1
P43_1 : Connected to LS1
P43_2 : Connected to LS1
P43_3 : Connected to LS1
RSPI1_CK : Connected to HS2
RSPI1_MOSI : Connected to HS2
RSPI1_MISO : Connected to HS2
RSPI1_SSL : Connected to HS2
P47_0 : Connected to LS1
P47_1 : Connected to HS2
P47_2 : Connected to HS2
P47_3 : Connected to HS2
SCIF2_TXD : Connected to LTE
SCIF2_RXD : Connected to LTE
P48_2 : Connected to LS1
SCIF2_CTS : Connected to LTE
SCIF2_RTS : Connected to LTE

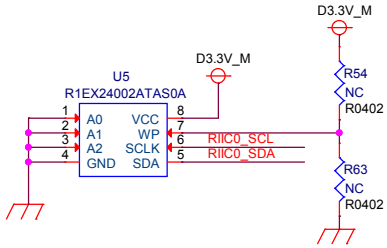
SoC RIIC0/1 I/F

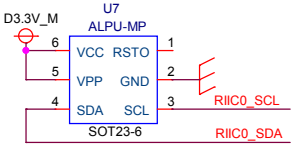
SPI_PVDD=3.3V



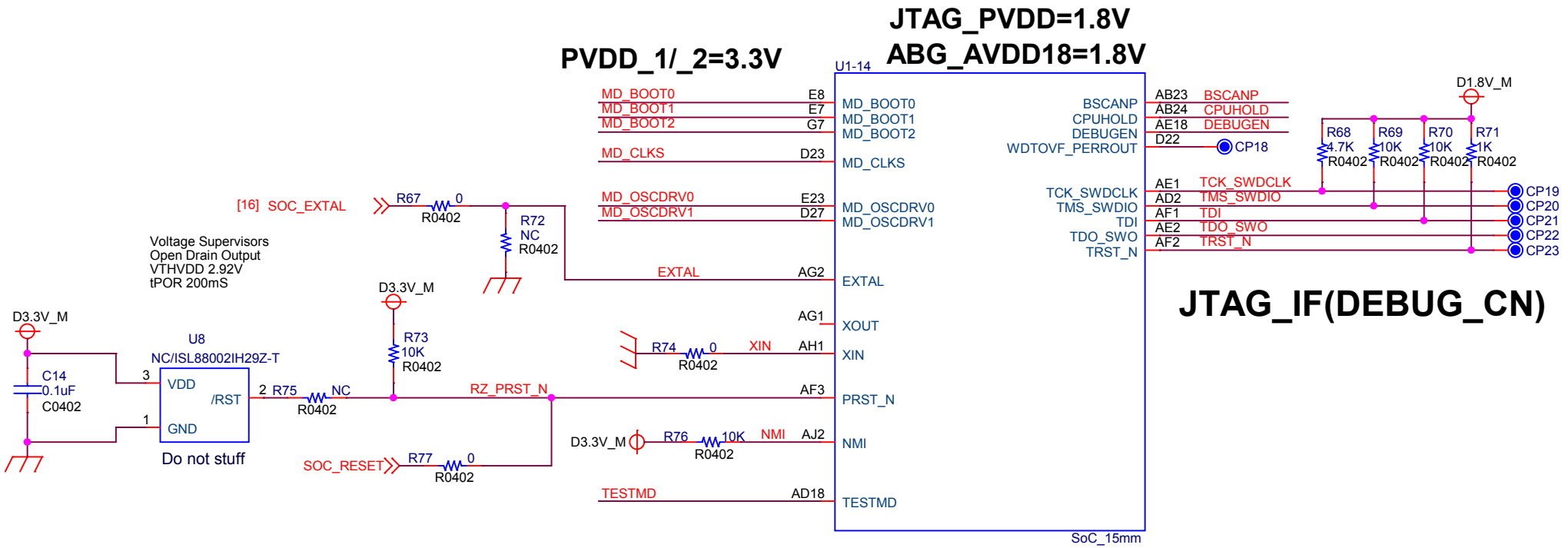


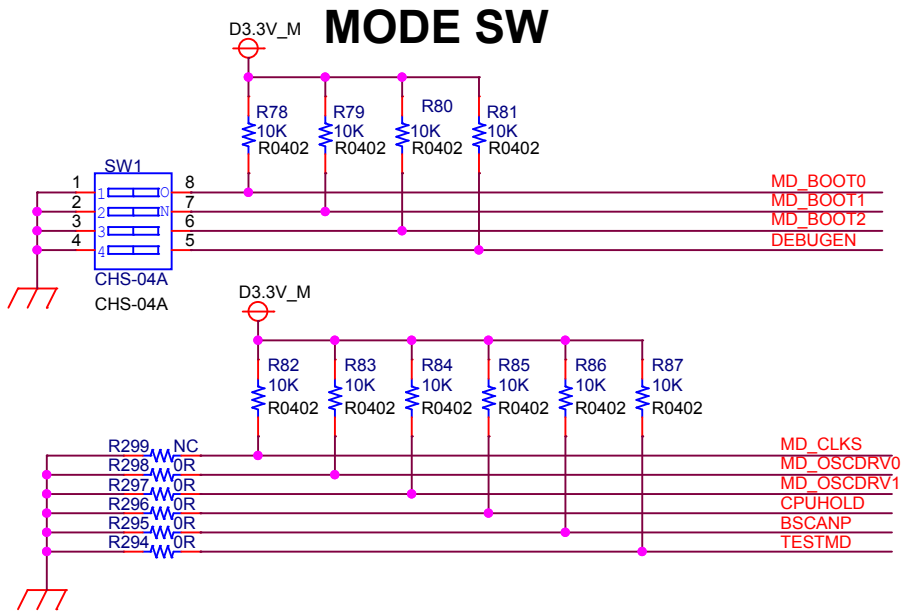




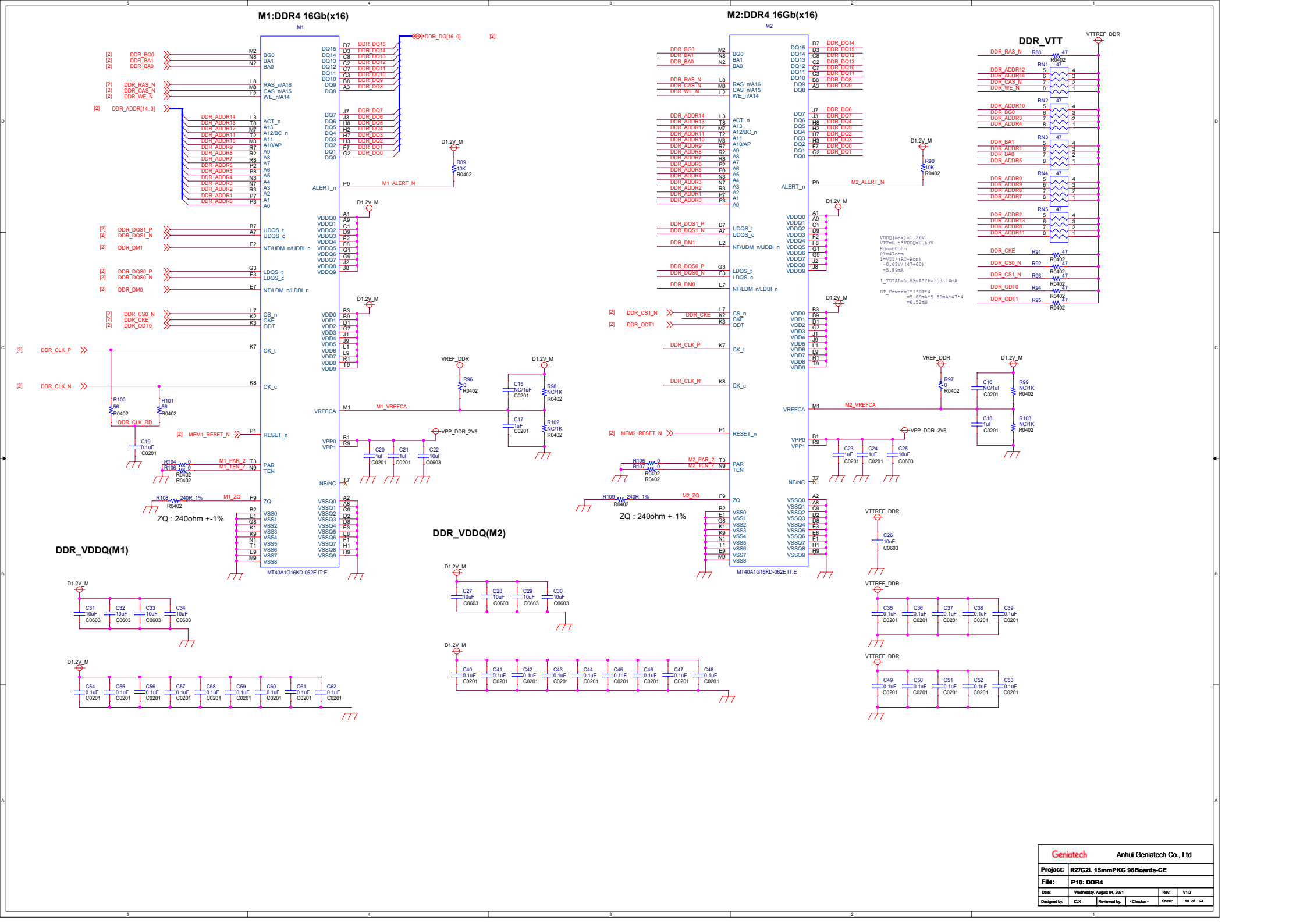


Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P08: SoC_GPIO/I2C				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	8 of 24





Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P09: SoC_MODE_JTAG				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	9 of 24


M1:DDR4 16Gb(x16)
M2:DDR4 16Gb(x16)
DDR_VTT
DDR_VDDQ(M1)
DDR_VDDQ(M2)
ZQ : 240ohm +-1%
ZQ : 240ohm +-1%
MT40A1G16KD-062E IT:E
MT40A1G16KD-062E IT:E
VDDQ(max)=1.26V
VTT=0.5*VDDQ=0.63V
Ron=60ohm
RT=47ohm
I=VTT/(RT+Ron)
=0.63V/(47+60)
=5.89mA
I_TOTAL=5.89mA*26=153.14mA
RT_Power=I*I*RT*4
=5.89mA*5.89mA*47*4
=6.52mW
Geniatech
Anhui Geniatech Co., Ltd
Project: RZ/G2L 15mmPKG 96Boards-CE
File: P10: DDR4
Date: Wednesday, August 04, 2021
Rev: V1.0
Designed by: CJX
Reviewed by: <Checker>
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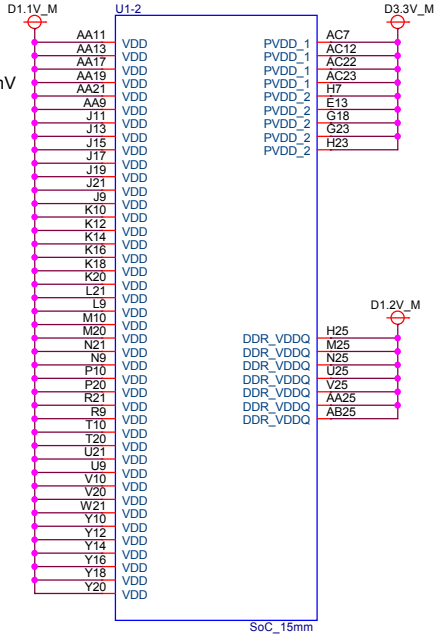
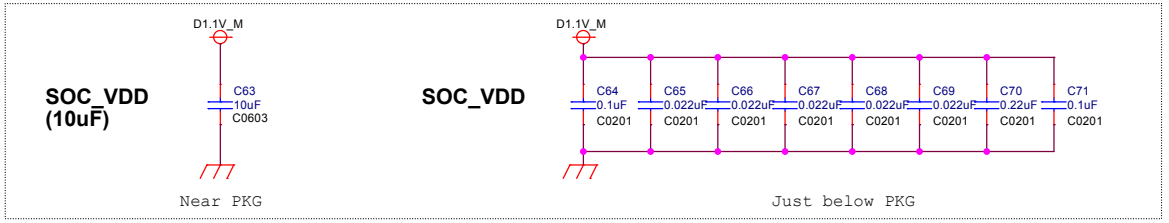
VDD=1.1V+50mV/-100mV
Max 3A

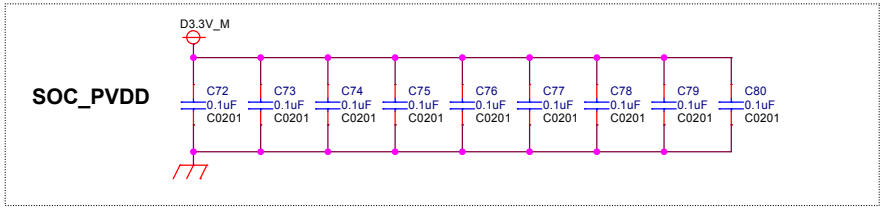


[VDD]

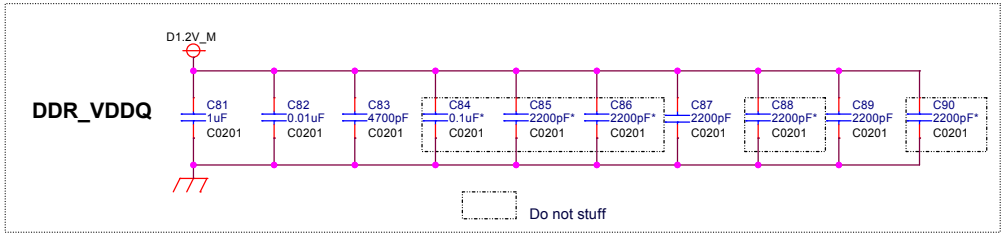


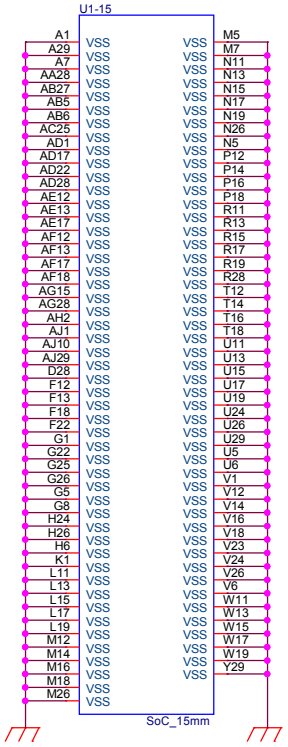
[PVDD]

TargetZ
1KHz-20MHz 50mohm
20MHz-1GHz 200mohm

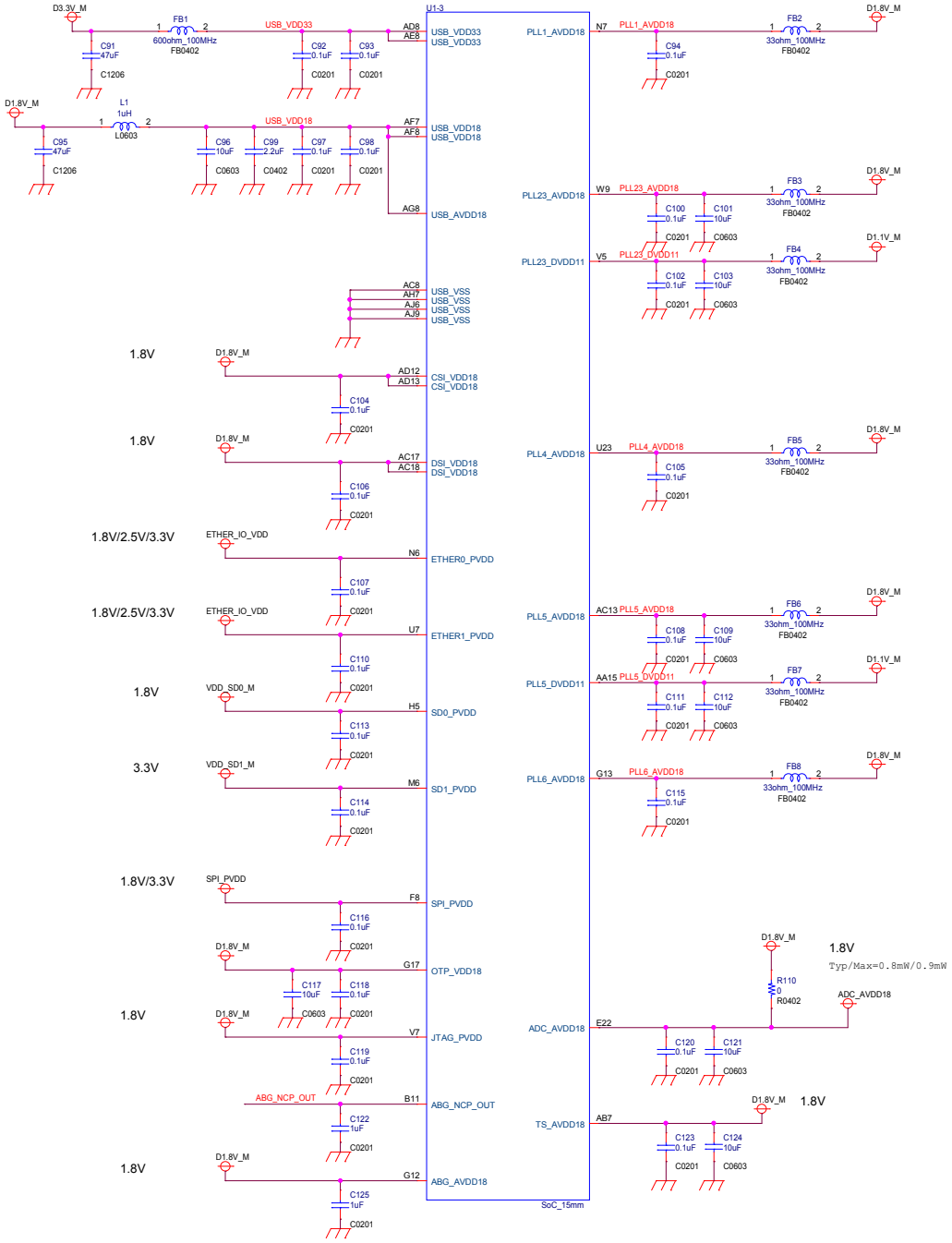


[DDR_VDDQ]

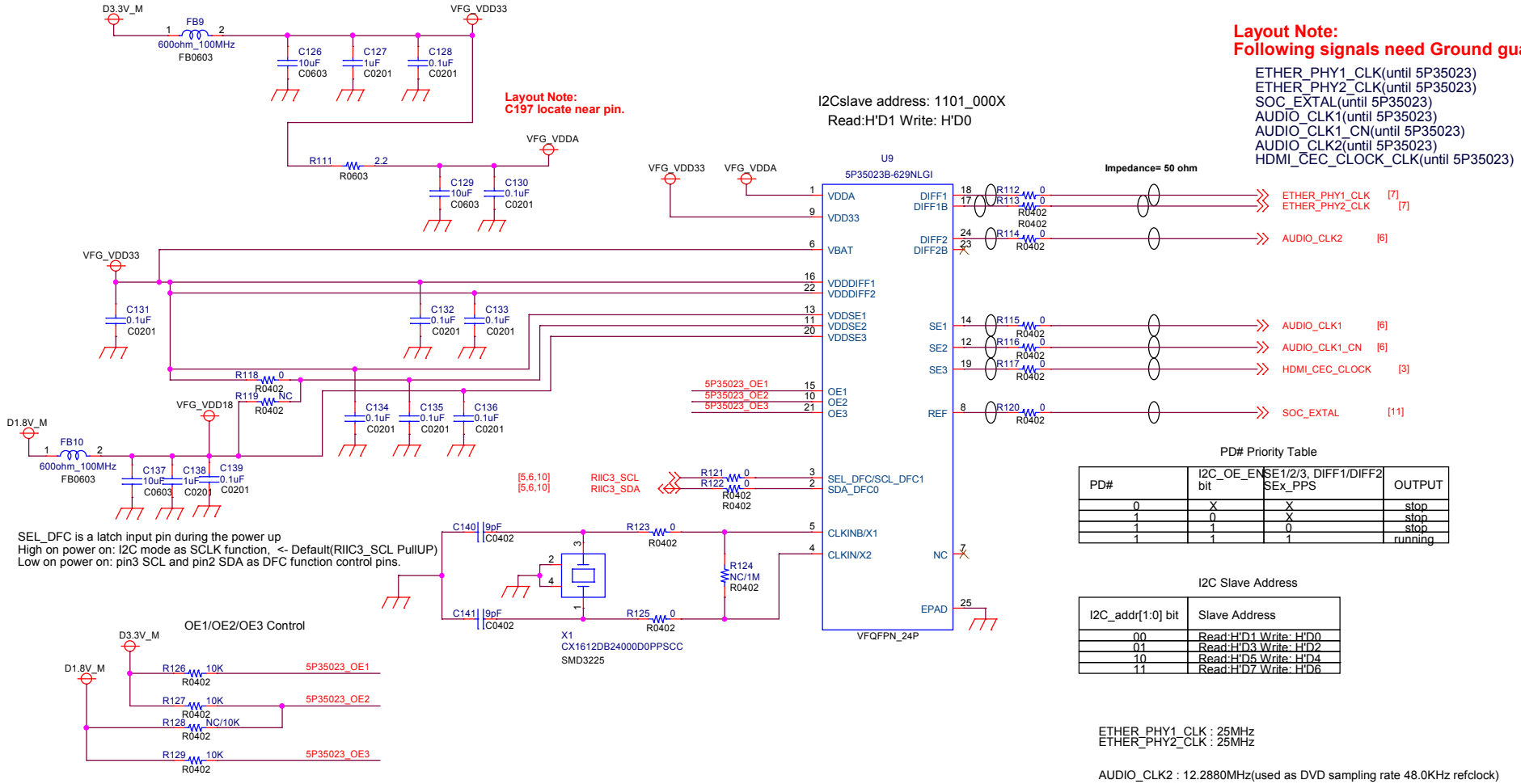




Geniatech	Anhui Geniatech Co., Ltd		
Project:	RZ/G2L 15mmPKG 96Boards-CE		
File:	P11: SoC_POWER1		
Date:	Wednesday, August 04, 2021	Rev:	V1.0
Designed by: CJX	Reviewed by: <Checker>	Sheet:	11 of 24



Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P12: SoC_POWER2				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	12 of 24



Layout Note:
Following signals need Ground guard.

ETHER_PHY1_CLK(until 5P35023)
ETHER_PHY2_CLK(until 5P35023)
SOC_EXTAL(until 5P35023)
AUDIO_CLK1(until 5P35023)
AUDIO_CLK1_CN(until 5P35023)
AUDIO_CLK2(until 5P35023)
HDMI_CEC_CLOCK_CLK(until 5P35023)

PD# Priority Table

PD#	I2C_OE_EN bit	SE1/2/3, DIFF1/DIFF2 SEx_PPS	OUTPUT
0	X	X	stop
1	0	X	stop
1	1	0	stop
1	1	1	running

I2C Slave Address

I2C_addr[1:0] bit	Slave Address
00	Read:H'D1 Write: H'D0
01	Read:H'D3 Write: H'D2
10	Read:H'D5 Write: H'D4
11	Read:H'D7 Write: H'D6

ETHER_PHY1_CLK : 25MHz
ETHER_PHY2_CLK : 25MHz

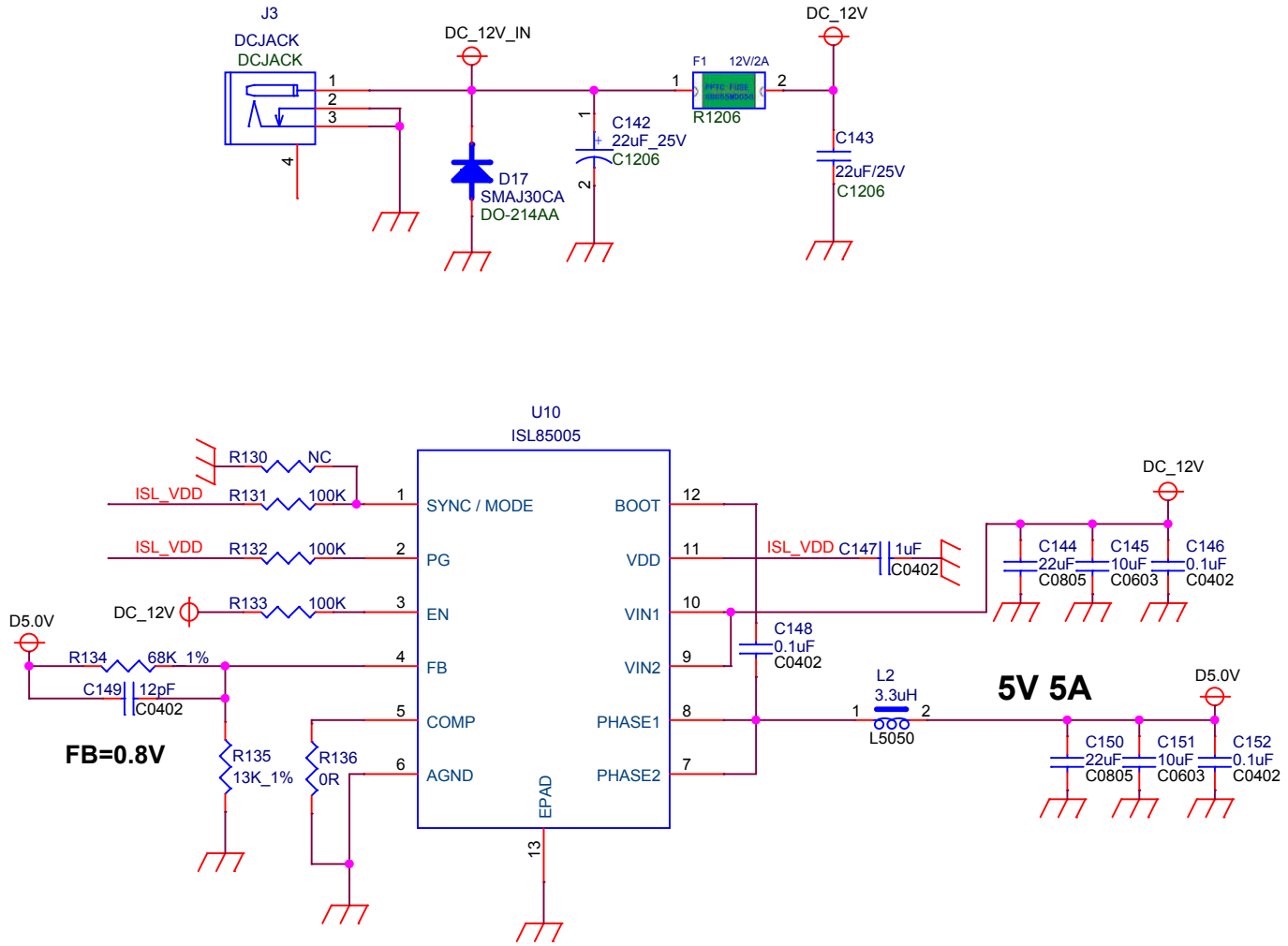
AUDIO_CLK2 : 12.2880MHz(used as DVD sampling rate 48.0KHz refclock)

AUDIO_CLK1 : 11.2896MHz(used as CD sampling rate 44.1KHz refclock)
AUDIO_CLK1_CN : 11.2896MHz(used as CD sampling rate 44.1KHz refclock)

HDMI_CEC_CLOCK : 12MHz (D1.8V_M level)

SOC_EXTAL : 24MHz

Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P13: CLOCK				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	13 of 24



Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P14: POWER_5V				
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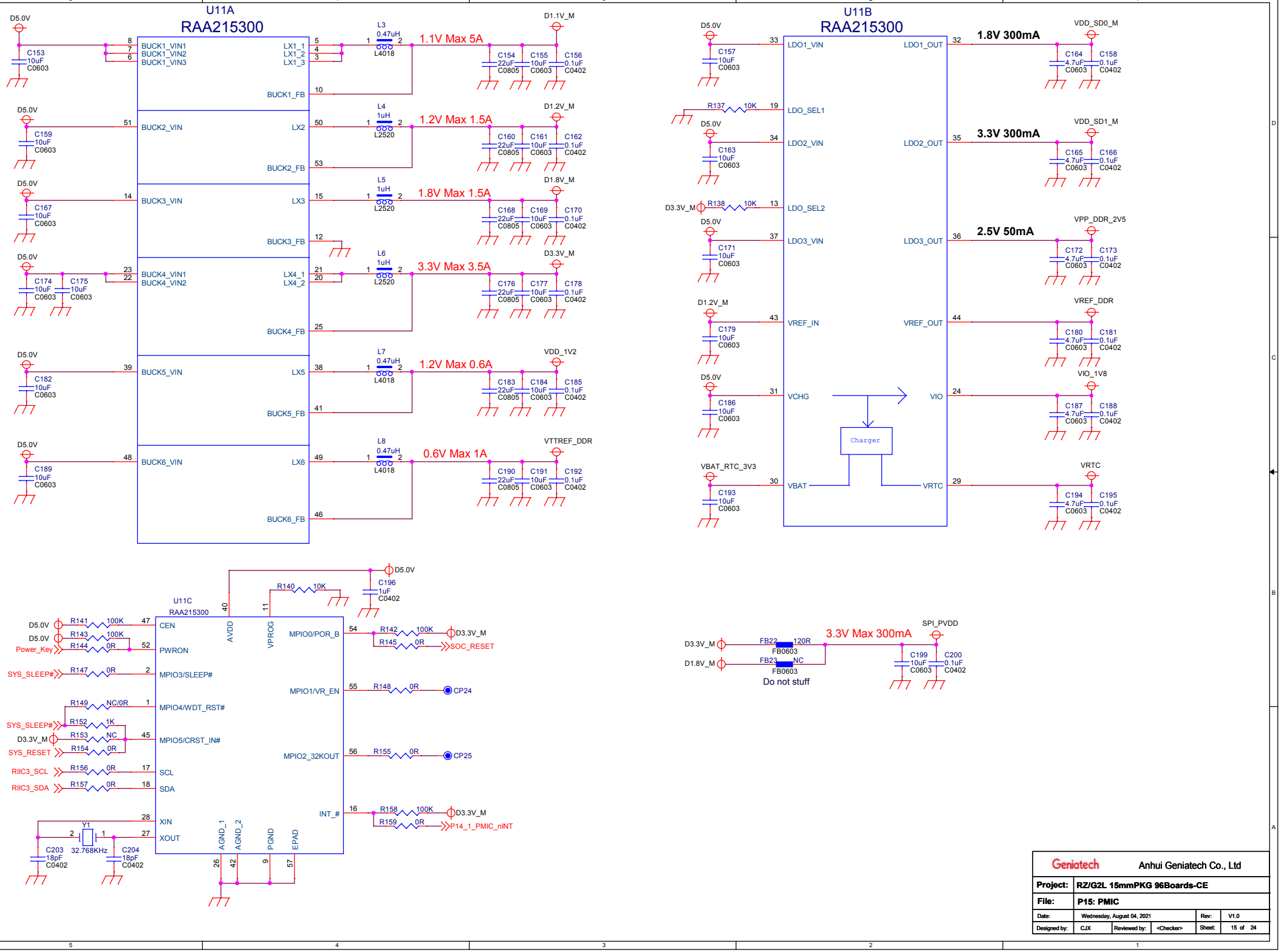
U11A
RAA215300
BUCK1_VIN1
BUCK1_VIN2
BUCK1_VIN3
LX1_1
LX1_2
LX1_3
BUCK1_FB
L3
0.47uH
L4018
1.1V Max 5A
D1.1V_M
BUCK2_VIN
LX2
BUCK2_FB
L4
1uH
L2520
1.2V Max 1.5A
D1.2V_M
BUCK3_VIN
LX3
BUCK3_FB
L5
1uH
L2520
1.8V Max 1.5A
D1.8V_M
BUCK4_VIN1
BUCK4_VIN2
LX4_1
LX4_2
BUCK4_FB
L6
1uH
L2520
3.3V Max 3.5A
D3.3V_M
BUCK5_VIN
LX5
BUCK5_FB
L7
0.47uH
L4018
1.2V Max 0.6A
VDD_1V2
BUCK6_VIN
LX6
BUCK6_FB
L8
0.47uH
L4018
0.6V Max 1A
VTTREF_DDR
D5.0V
U11B
RAA215300
LDO1_VIN
LDO1_OUT
1.8V 300mA
VDD_SD0_M
LDO_SEL1
LDO2_VIN
LDO2_OUT
3.3V 300mA
VDD_SD1_M
LDO_SEL2
LDO3_VIN
LDO3_OUT
2.5V 50mA
VPP_DDR_2V5
VREF_IN
VREF_OUT
VREF_DDR
VCHG
VIO
VIO_1V8
Charger
VBAT
VRTC
VBAT_RTC_3V3
U11C
RAA215300
CEN
PWRON
MPIO3/SLEEP#
MPIO4/WDT_RST#
MPIO5/CRST_IN#
SCL
SDA
XIN
XOUT
AVDD
VPROG
MPIO0/POR_B
MPIO1/VR_EN
MPIO2_32KOUT
INT_#
AGND_1
AGND_2
PGND
EPAD
SOC_RESET
CP24
CP25
P14_1_PMIC_nINT
Power_Key
SYS_SLEEP#
SYS_RESET
RIIC3_SCL
RIIC3_SDA
32.768KHz
3.3V Max 300mA
Do not stuff
SPI_PVDD
Geniatech
Anhui Geniatech Co., Ltd
Project: RZ/G2L 15mmPKG 96Boards-CE
File: P15: PMIC
Date: Wednesday, August 04, 2021
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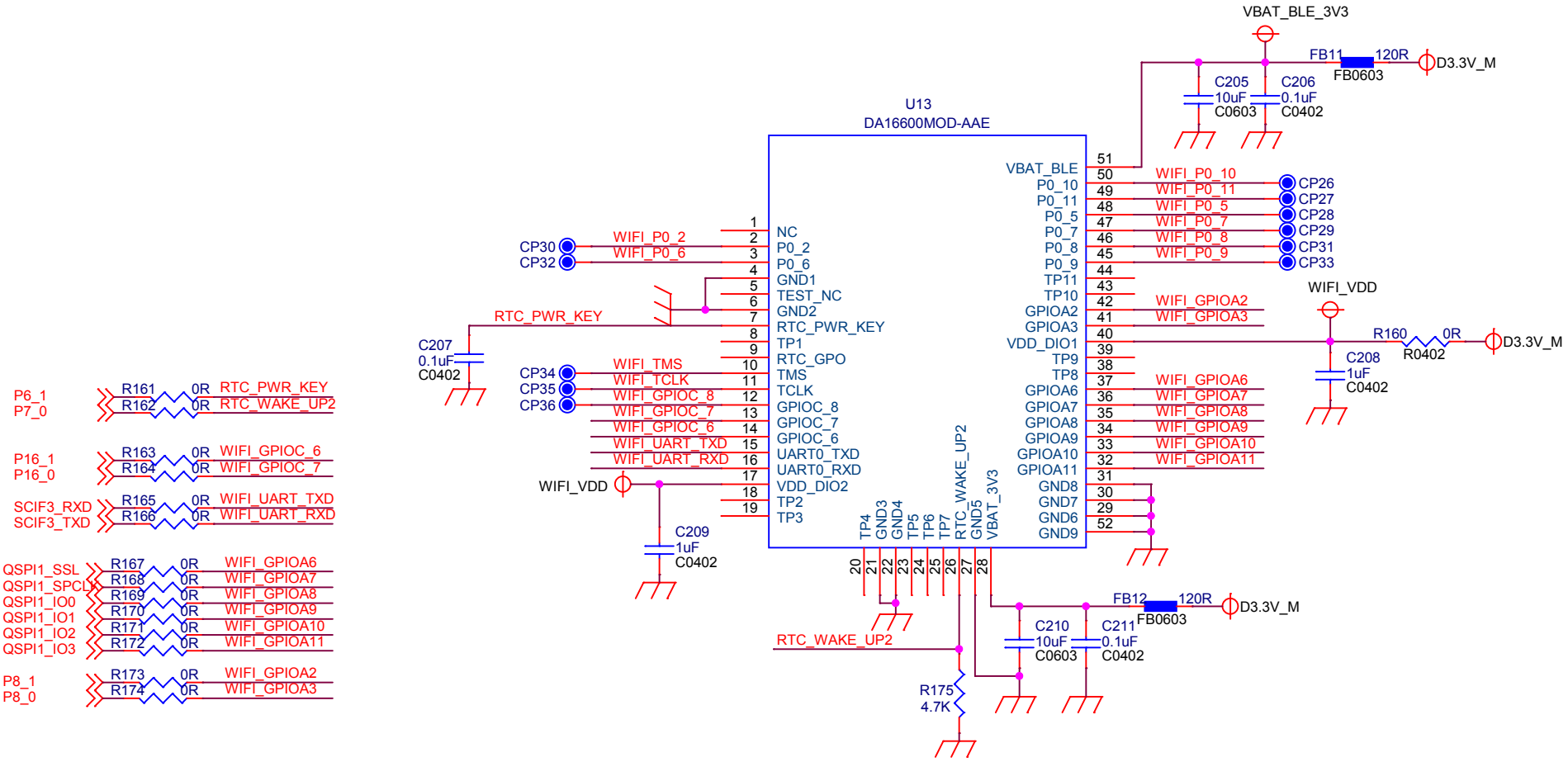

Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P16: WIFI_BT				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
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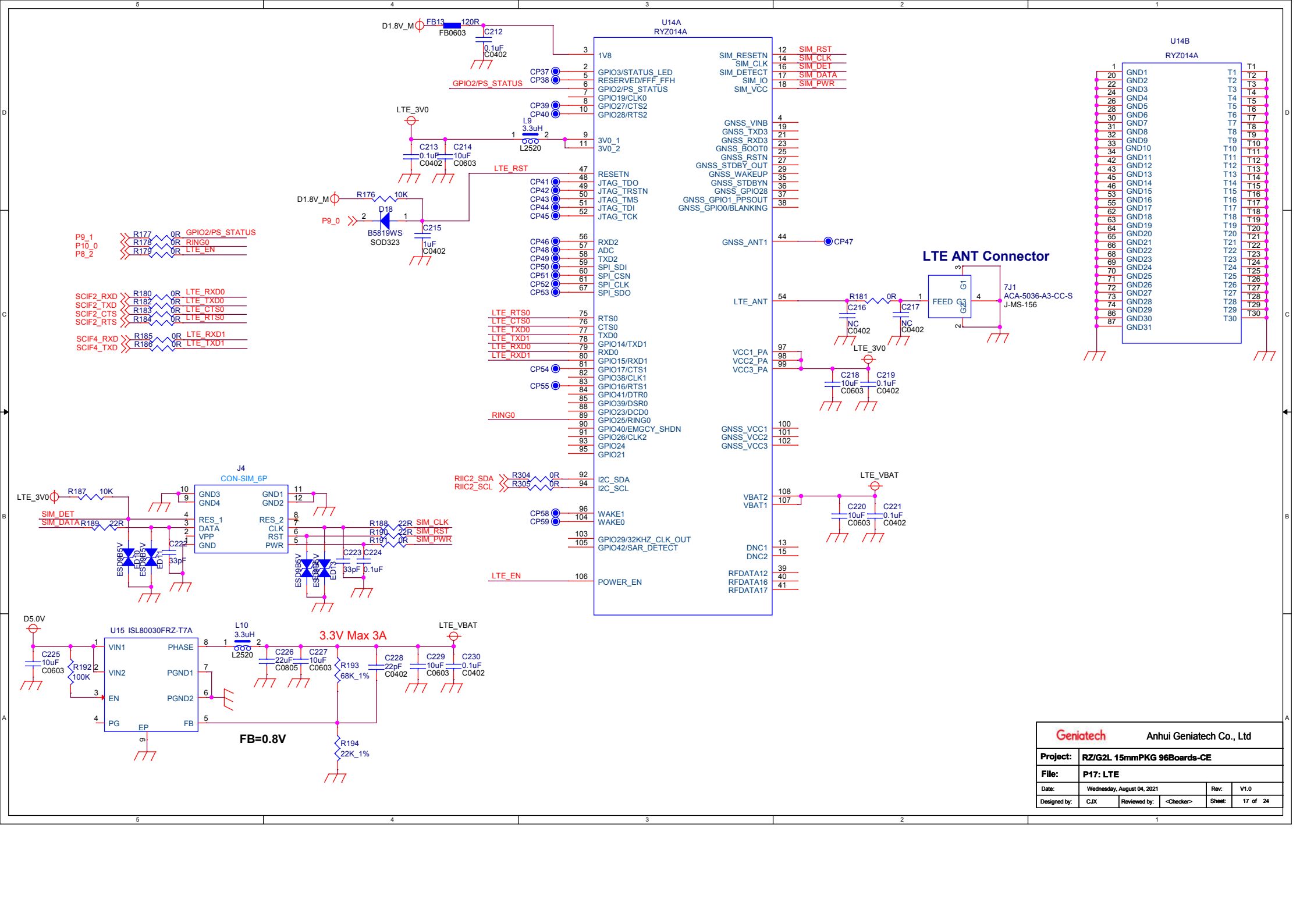
U14A
RYZ014A
U14B
RYZ014A
LTE ANT Connector
7J1
ACA-5036-A3-CC-S
J-MS-156
J4
CON-SIM_6P
U15 ISL80030FRZ-T7A
3.3V Max 3A
FB=0.8V
Geniatech
Anhui Geniatech Co., Ltd
Project: RZ/G2L 15mmPKG 96Boards-CE
File: P17: LTE
Date: Wednesday, August 04, 2021
Rev: V1.0
Designed by: CJX
Reviewed by: <Checker>
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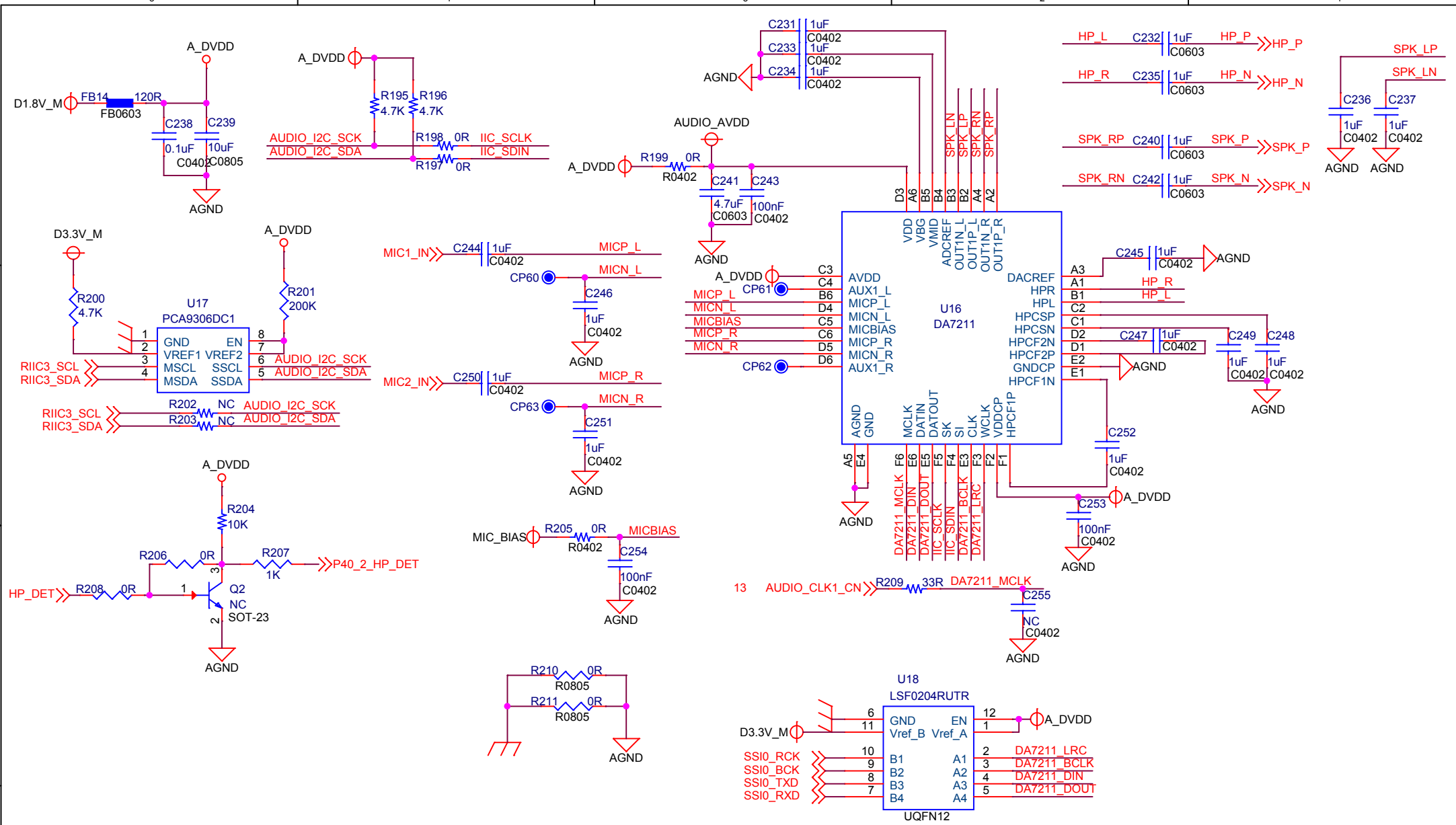
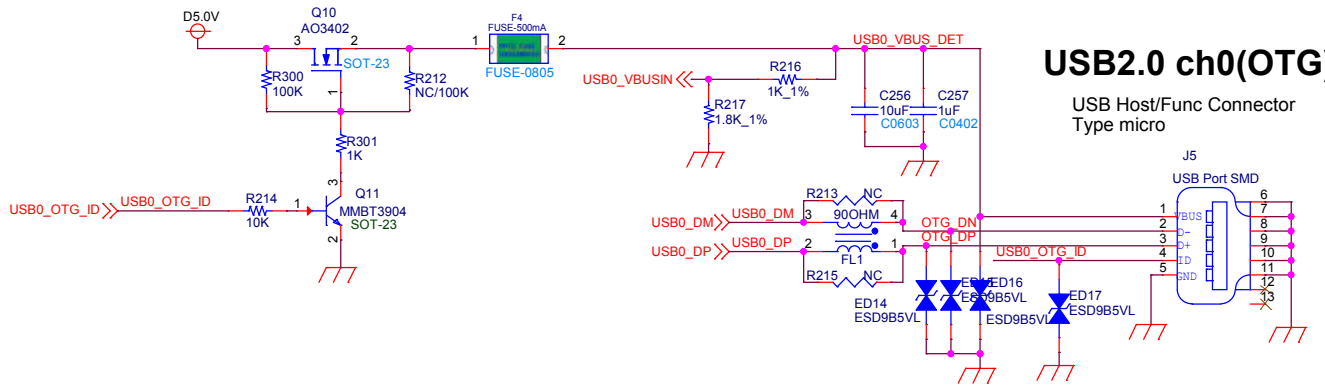
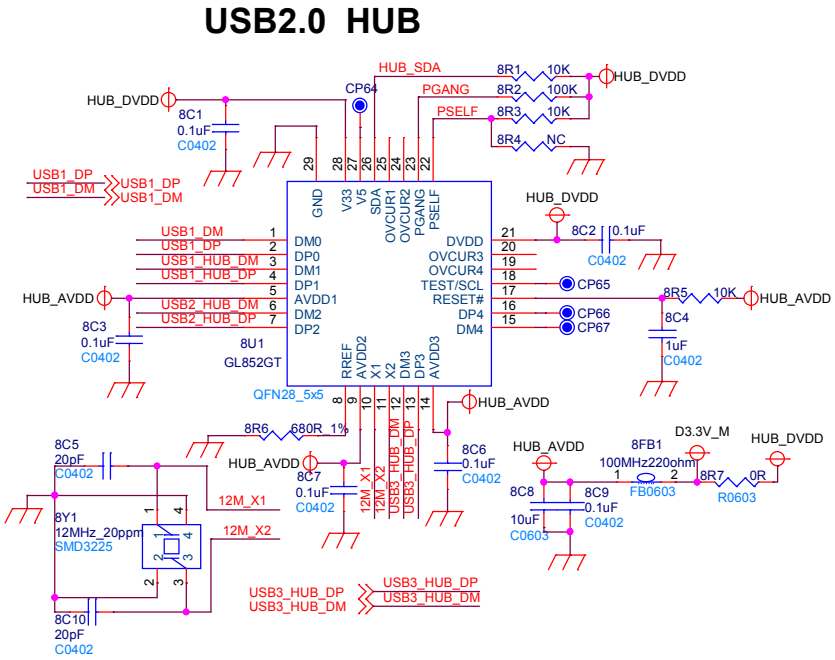
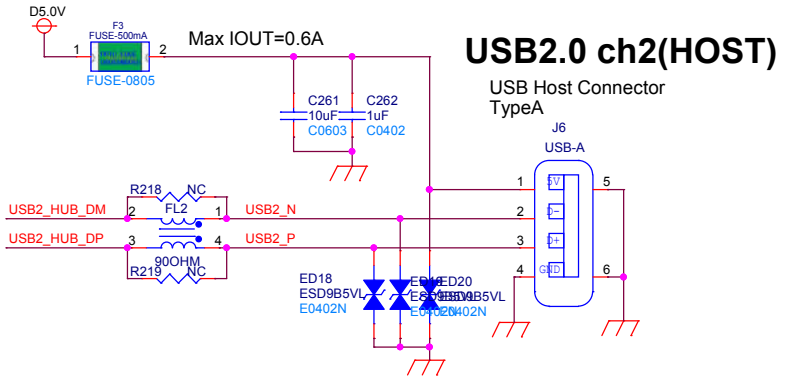
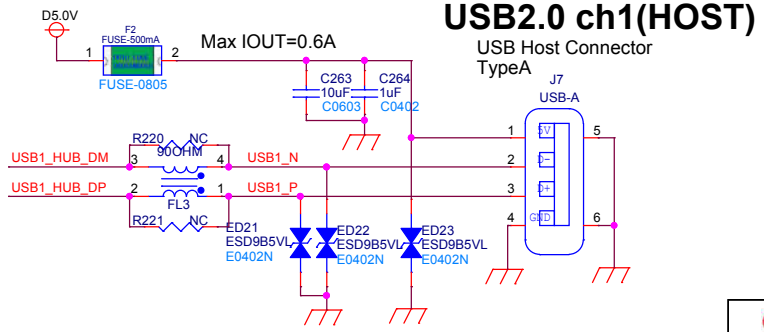


Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P18: Audio CODEC				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	18 of 24

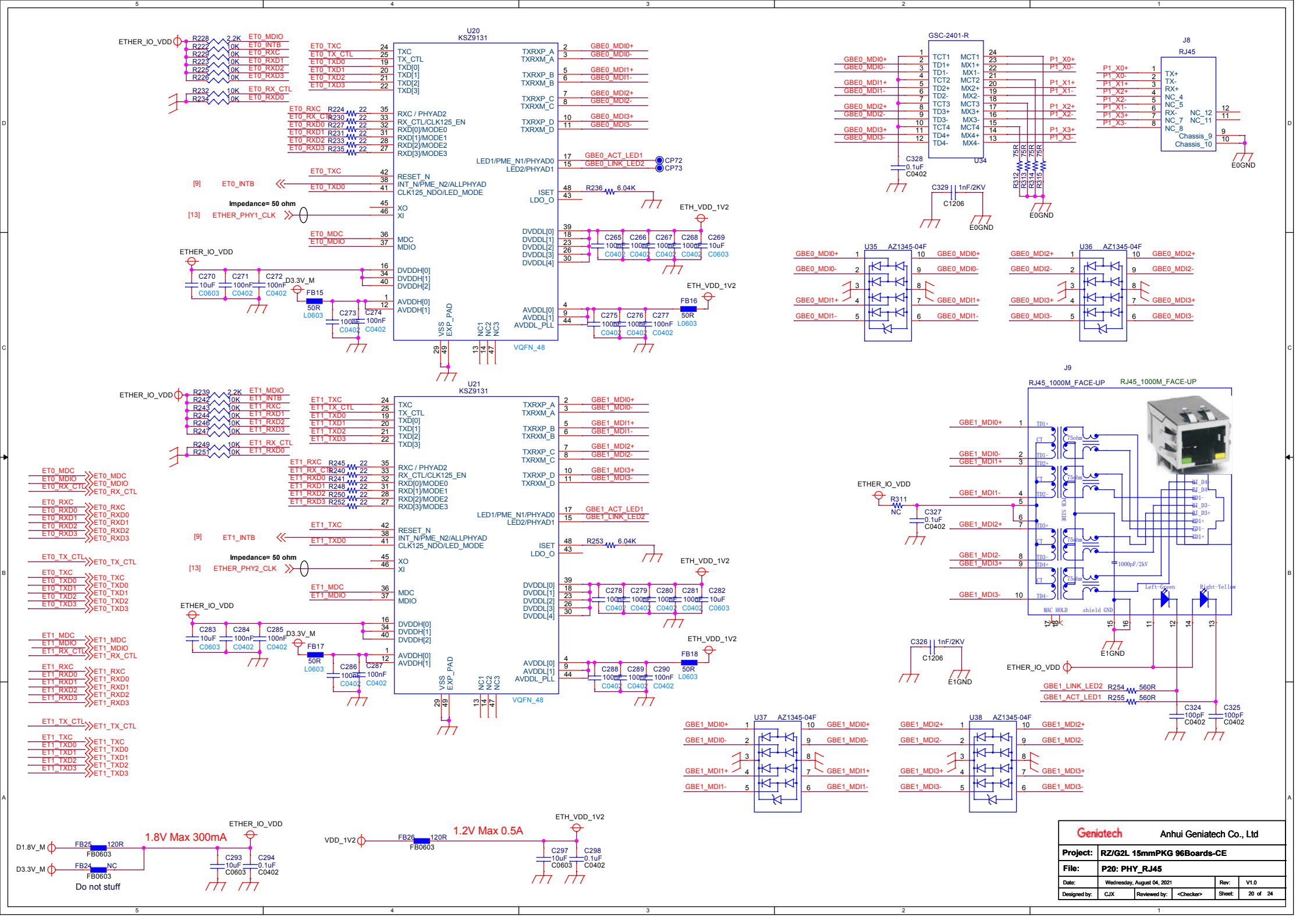








Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P19: USB				
Date:	Friday, August 06, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	19 of 24


U20
KSZ9131
U21
KSZ9131
GSC-2401-R
U34
J8
RJ45
U35 AZ1345-04F
U36 AZ1345-04F
U37 AZ1345-04F
U38 AZ1345-04F
J9
RJ45_1000M_FACE-UP
RJ45_1000M_FACE-UP
ETHER_IO_VDD
ETH_VDD_1V2
D3.3V_M
D1.8V_M
VDD_1V2
E0GND
E1GND
VQFN_48
1.8V Max 300mA
1.2V Max 0.5A
Do not stuff
Geniatech
Anhui Geniatech Co., Ltd
Project: RZ/G2L 15mmPKG 96Boards-CE
File: P20: PHY_RJ45
Date: Wednesday, August 04, 2021
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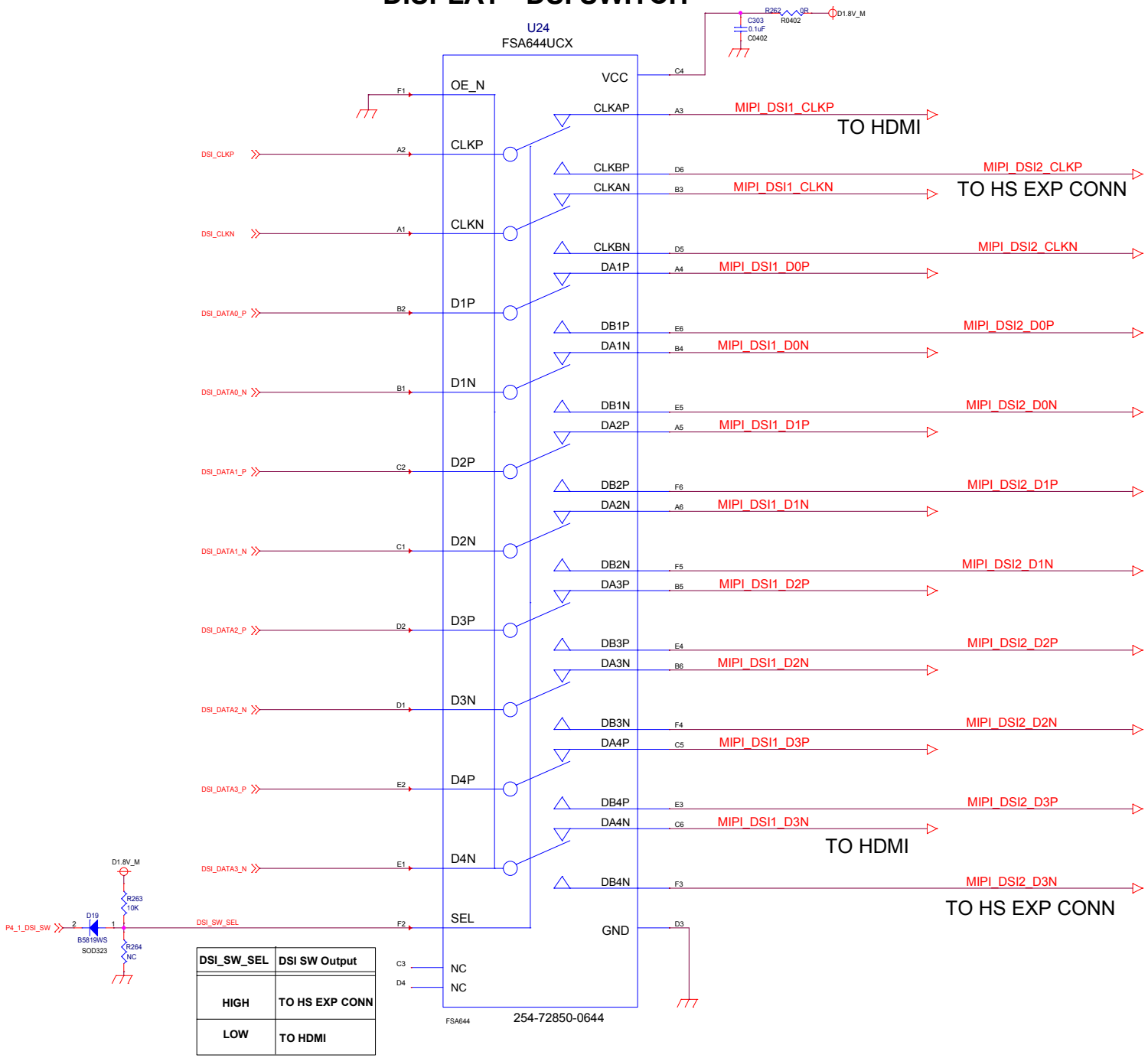
DISPLAY - DSI SWITCH



DSI_SW_SEL	DSI SW Output
HIGH	TO HS EXP CONN
LOW	TO HDMI

Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P21: MIPI DSI_SWITCH				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
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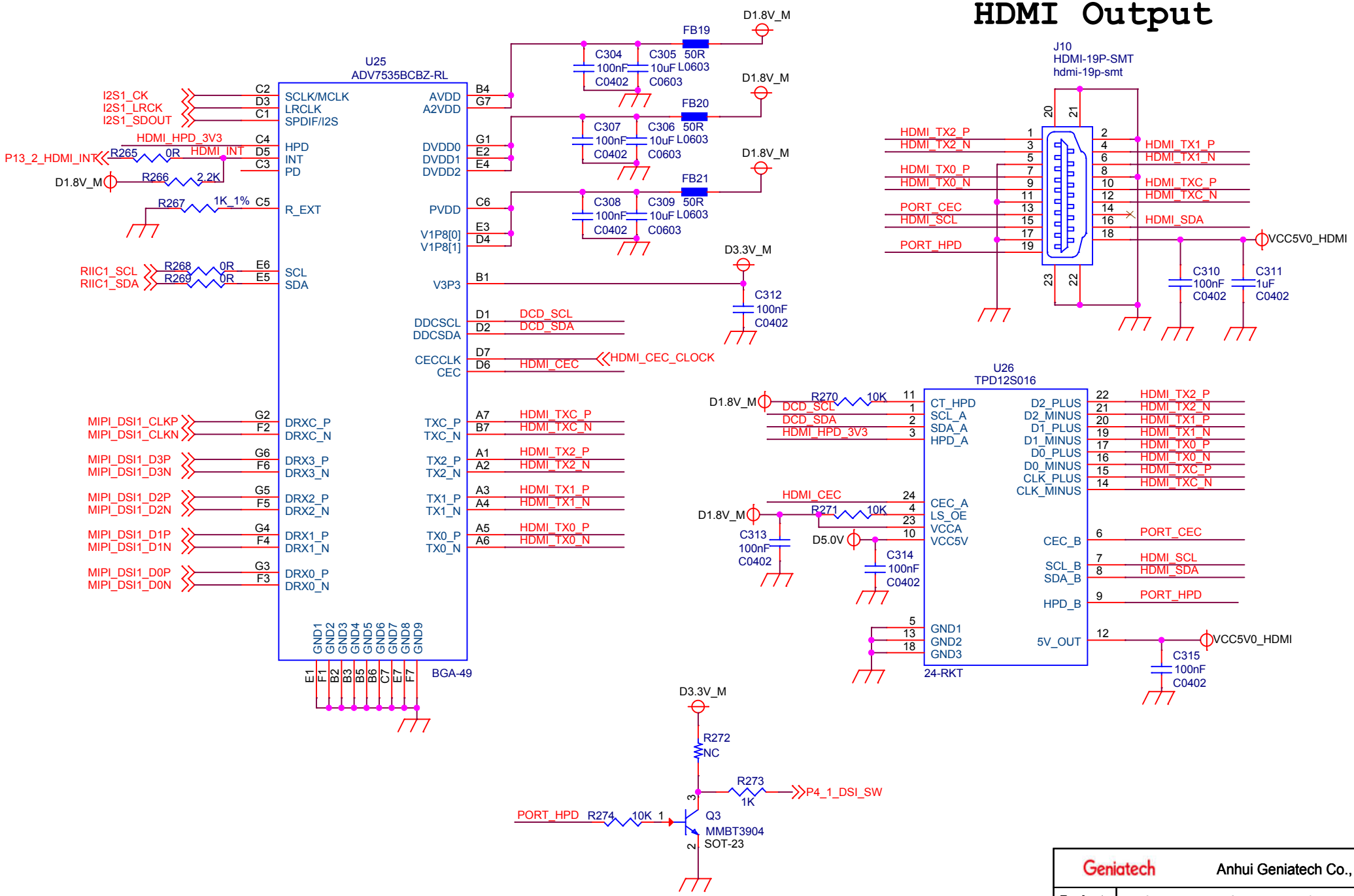
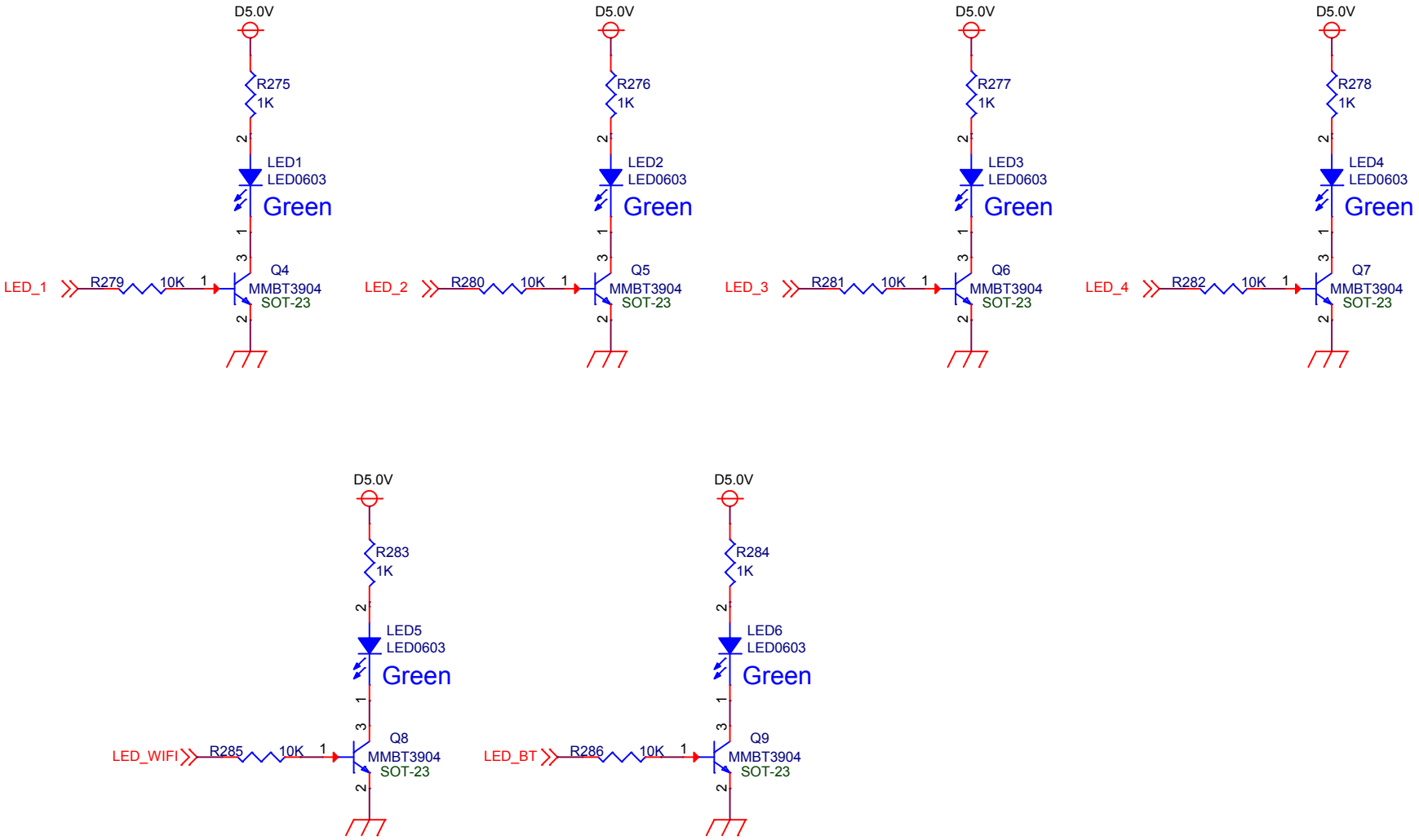
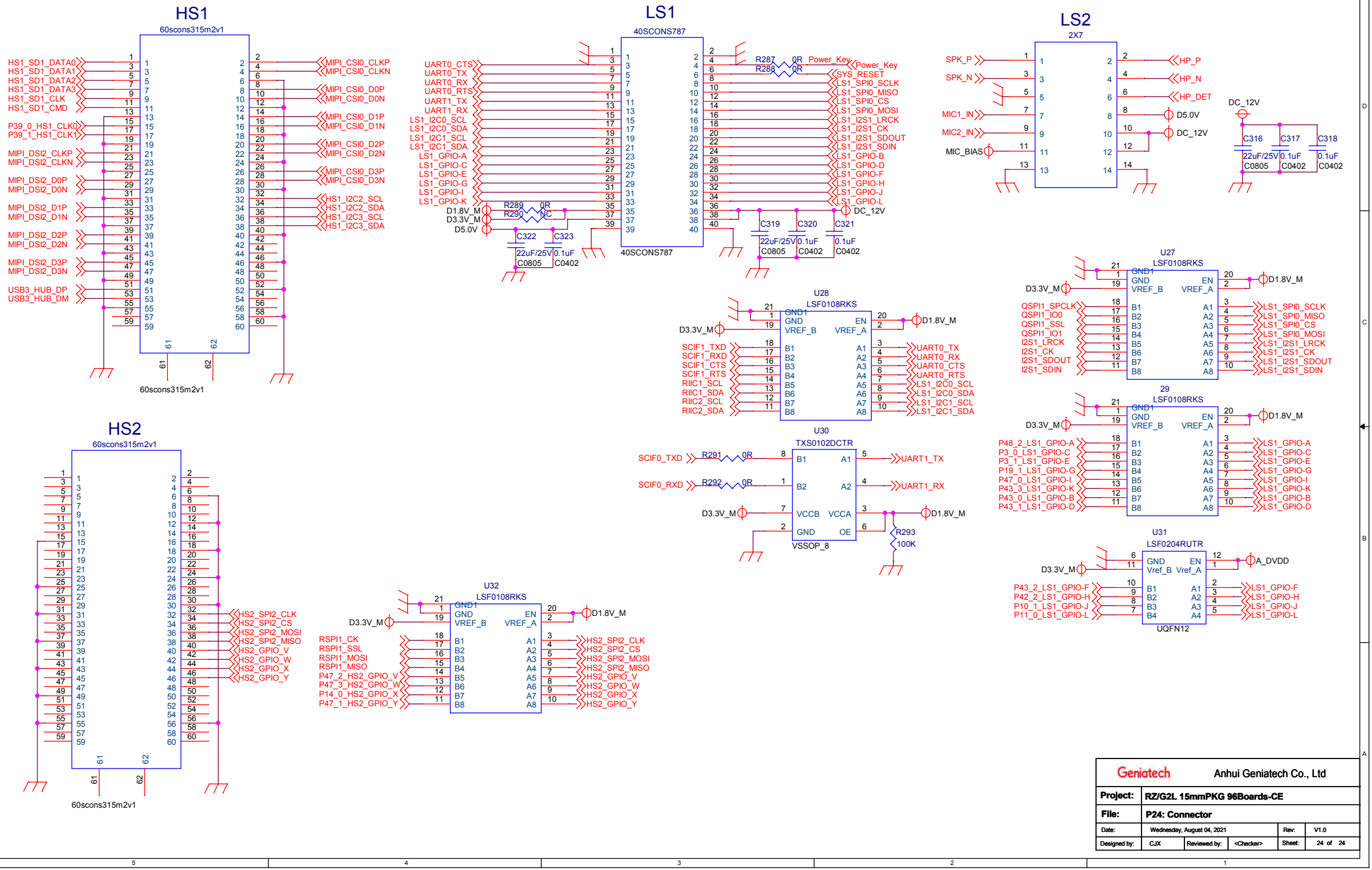
HDMI Output



Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P22: HDMI_OUT				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	22 of 24



Geniatech	Anhui Geniatech Co., Ltd				
Project:	**RZ/G2L 15mmPKG 96Boards-CE**				
File:	**P23: LED**				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	23 of 24



Geniatech	Anhui Geniatech Co., Ltd				
Project:	RZ/G2L 15mmPKG 96Boards-CE				
File:	P24: Connector				
Date:	Wednesday, August 04, 2021			Rev:	V1.0
Designed by:	CJX	Reviewed by:	<Checker>	Sheet:	24 of 24