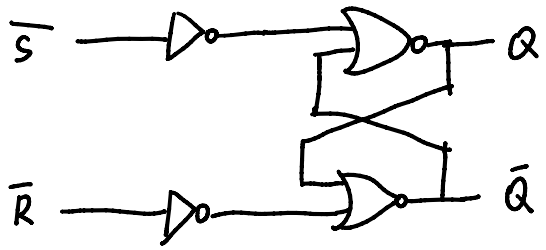
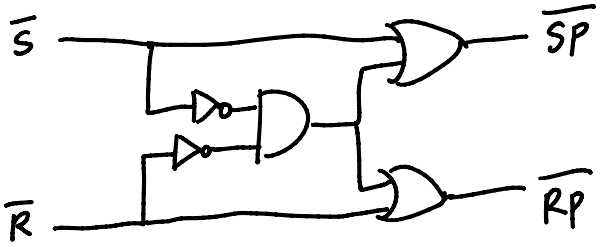
Homework 2 Part A

2022年10月24日 20:21

A.1.1

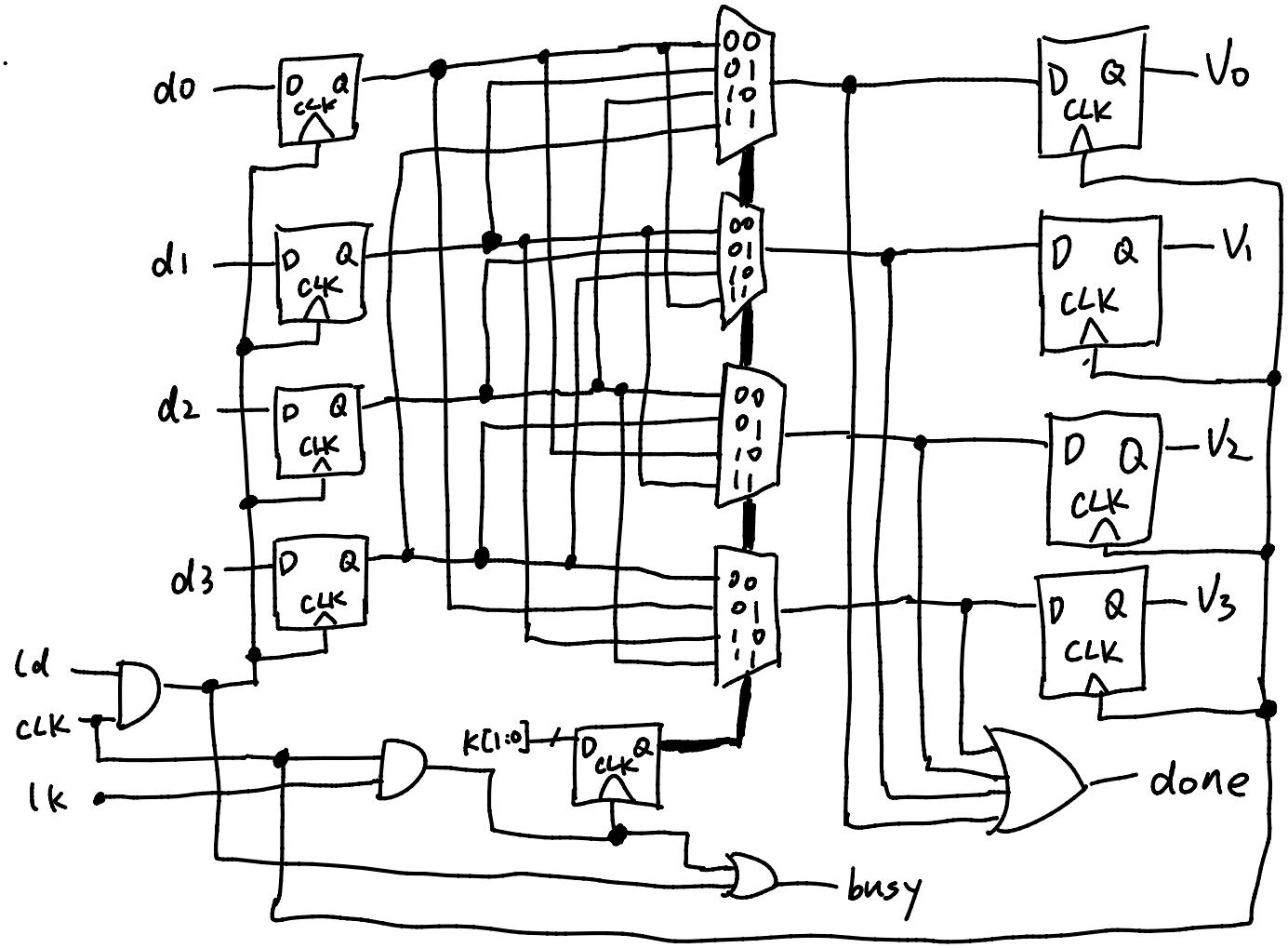


A.1.2.



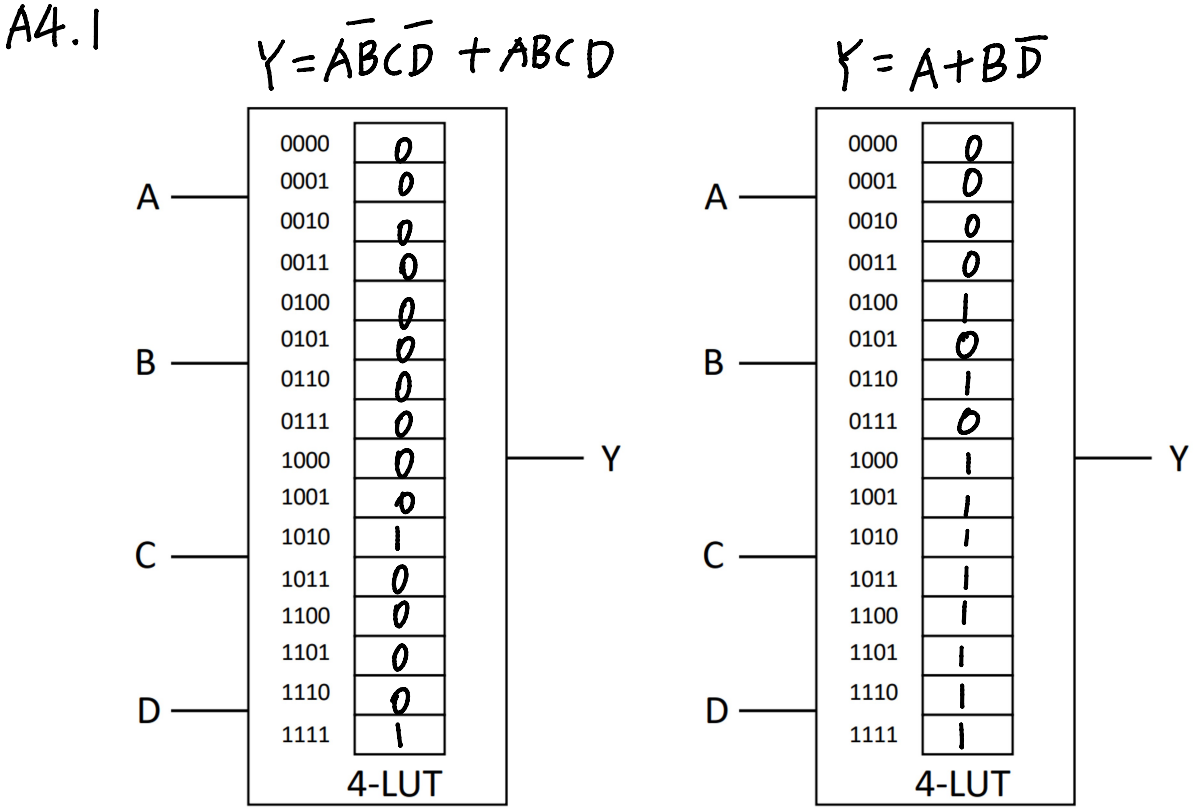
A2. There should be two counters and three inputs nodes. The reset bit should reset synchronized which means it should be reset when the clock is in rising edge.

A3.



The ld and clk connect together with a AND gate to let the ld is change only when the rising-edge of clock. The lk is also connect to the clk to perform identically. d0 - d3 are four inputs signals connected to four D-flip-flop under the control of clock signal. They all connected to four 4-1 MUX to perform the rotation calculation. The number of bits rotated will be controlled by the k input. The output of the four MUXs will also connected to four D-flip-flops to perform output controlled by rising-edge of clock. The OR gate at the end will be true when the signals are transferred into end.

A4.1



A4.2