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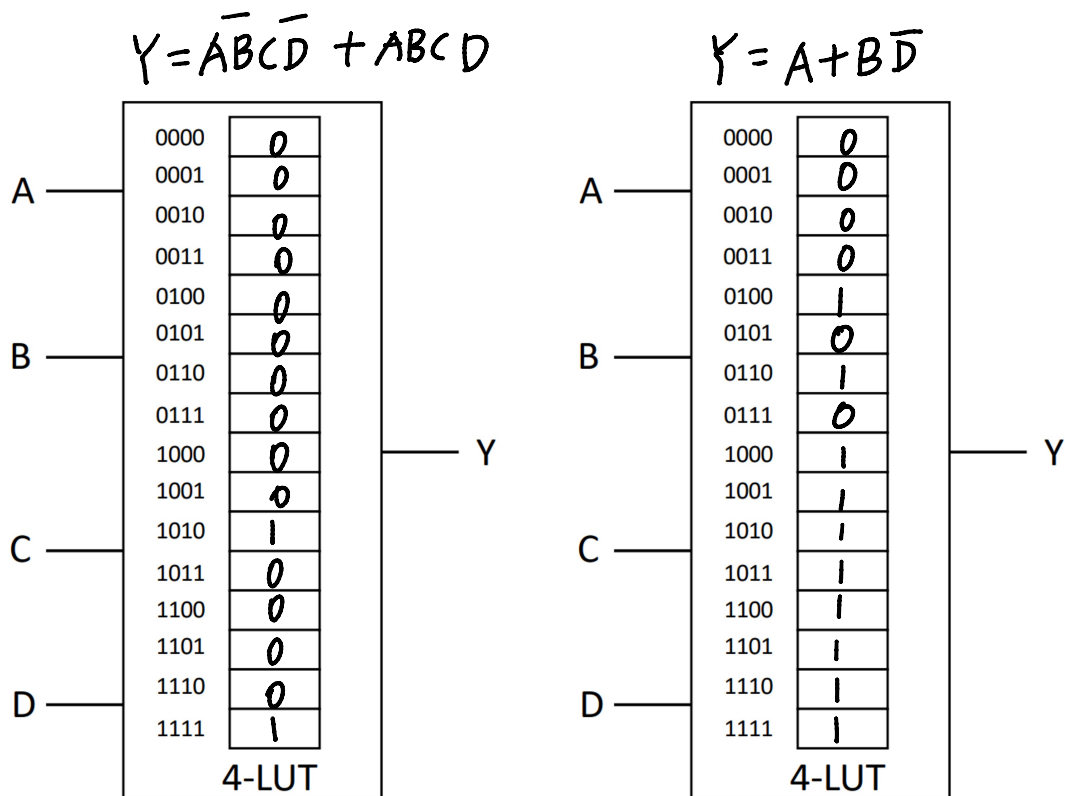
A2. There should be two counters and three inputs nodes. The reset bit should reset synchronized which means it should be reset when the clock is in rising edge.

A3.

Hand-drawn logic diagram of a 4-bit ripple-carry adder. The circuit includes four input registers ( $d_0, d_1, d_2, d_3$ ) and four output registers ( $V_0, V_1, V_2, V_3$ ), each implemented as a D flip-flop with a clock input. The inputs are connected to a 4-bit ripple-carry adder structure. The carry-in is connected to a D flip-flop labeled  $K[1:0]$ . The carry-out is connected to the  $done$  signal. The  $busy$  signal is the output of an OR gate that combines the carry-in and the carry-out of the  $K[1:0]$  register. The  $done$  signal is the output of an OR gate that combines the carry-out of the  $K[1:0]$  register and the carry-out of the final adder stage.

The Id and clk connect together with a AND gate to let the Id is change only when the rising-edge of clock. The Ik is also connect to the clk to perform identically. d0 - d3 are four inputs signals connected to four D-flip-flop under the control of clock signal. They all connected to four 4-1 MUX to perform the rotation calculation. The number of bits rotated will be controlled by the k input. The output of the four MUXs will also connected to four D-flip-flops to perform output controlled by rising-edge of clock. The OR gate at the end will be true when the signals are transferred into end.

A4.1



A4.2

