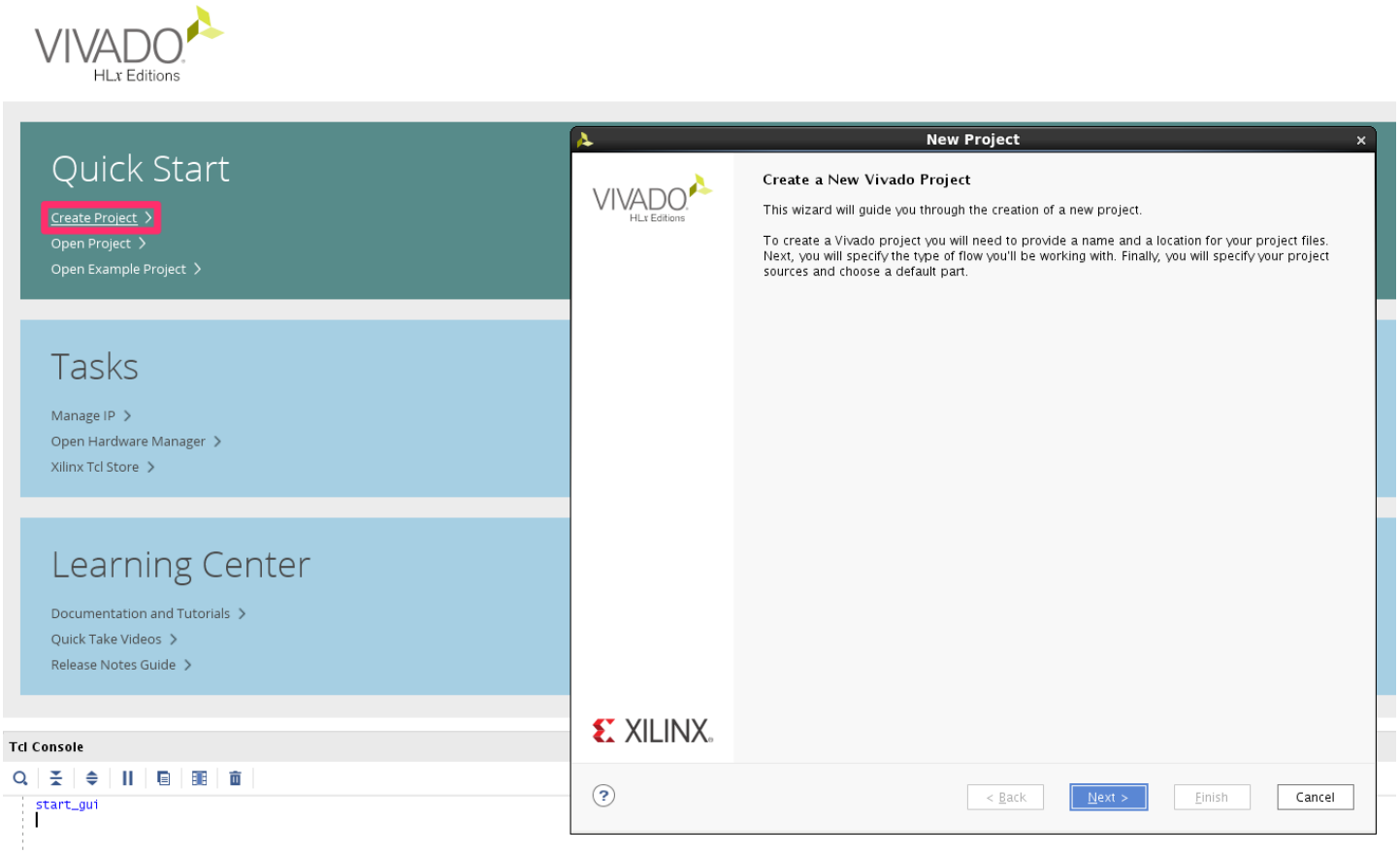
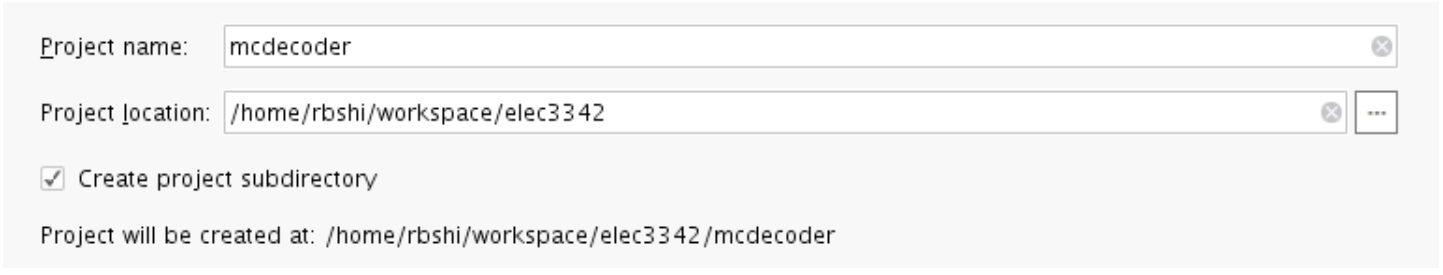
ELEC3342 Tutorial: Homework1-B

STEP1: Open Vivado and create a new project.

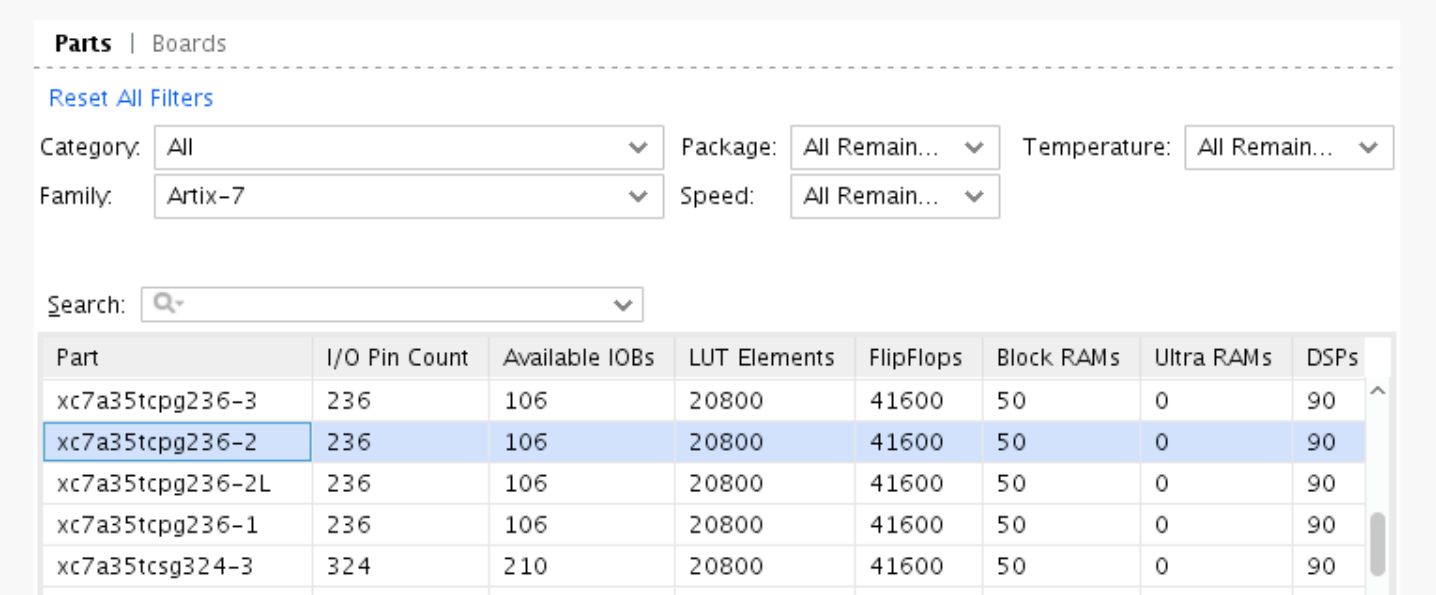


STEP2: Name the project and check *Create project subdirectory.*

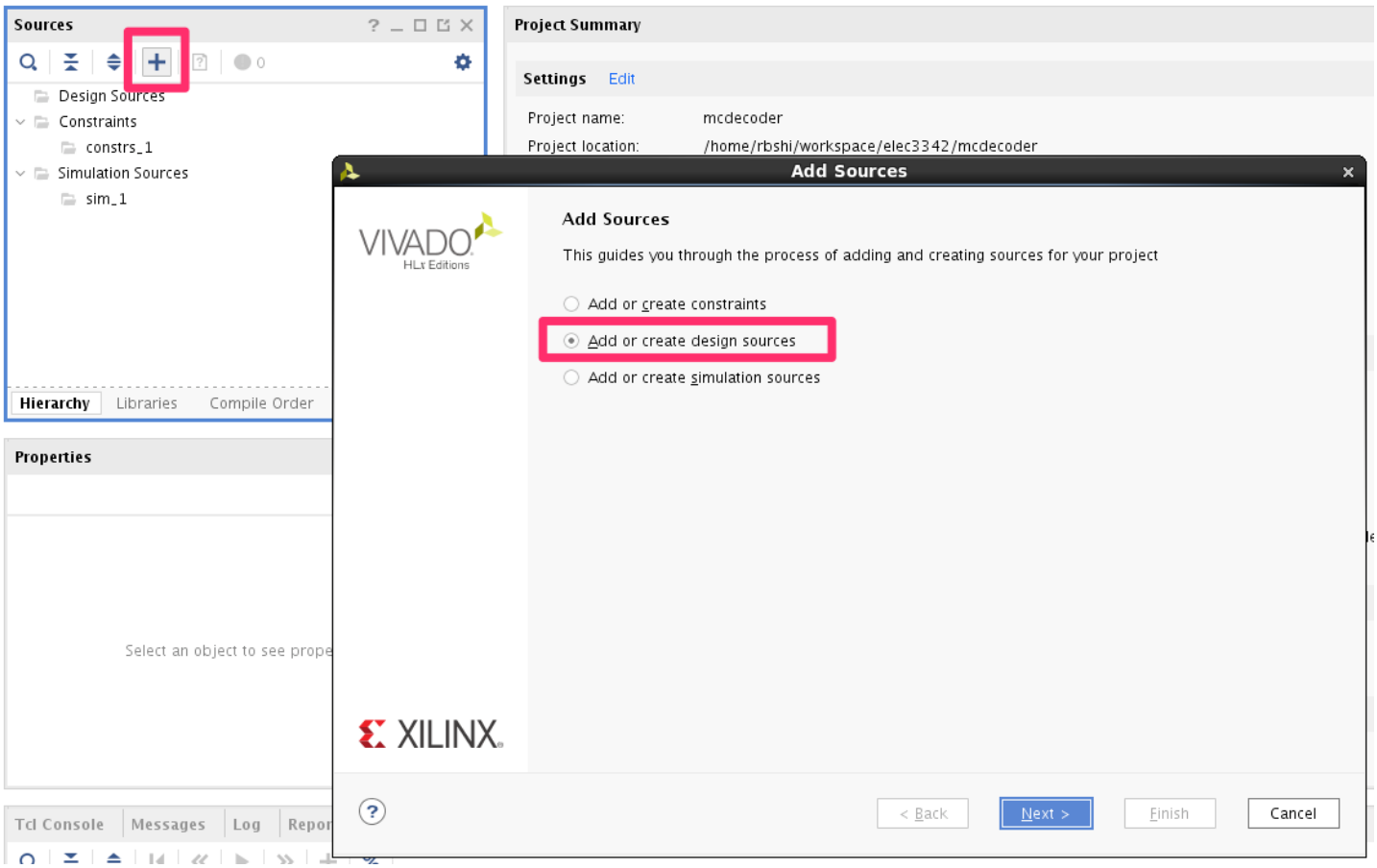


STEP3: Select the RTL Project and check *Do not specify sources at this time*.

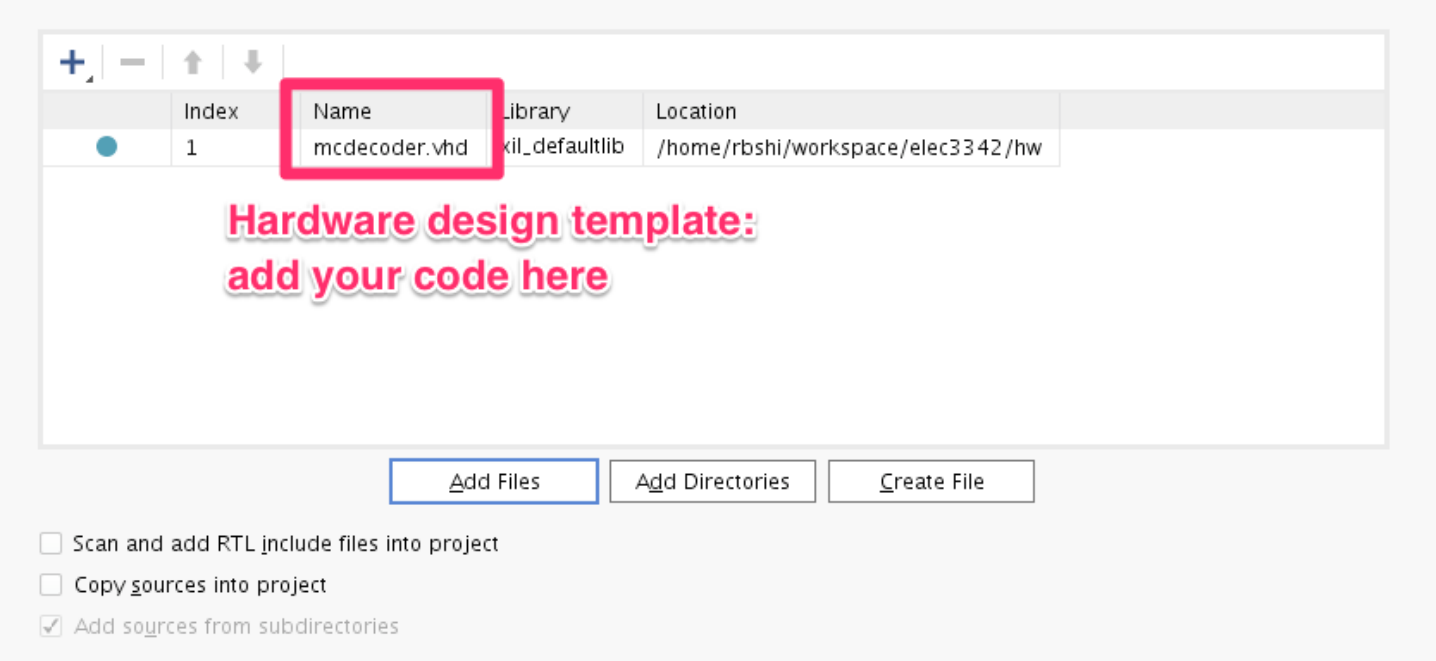
STEP4: Select the proper FPGA device for this project as in the following figure.



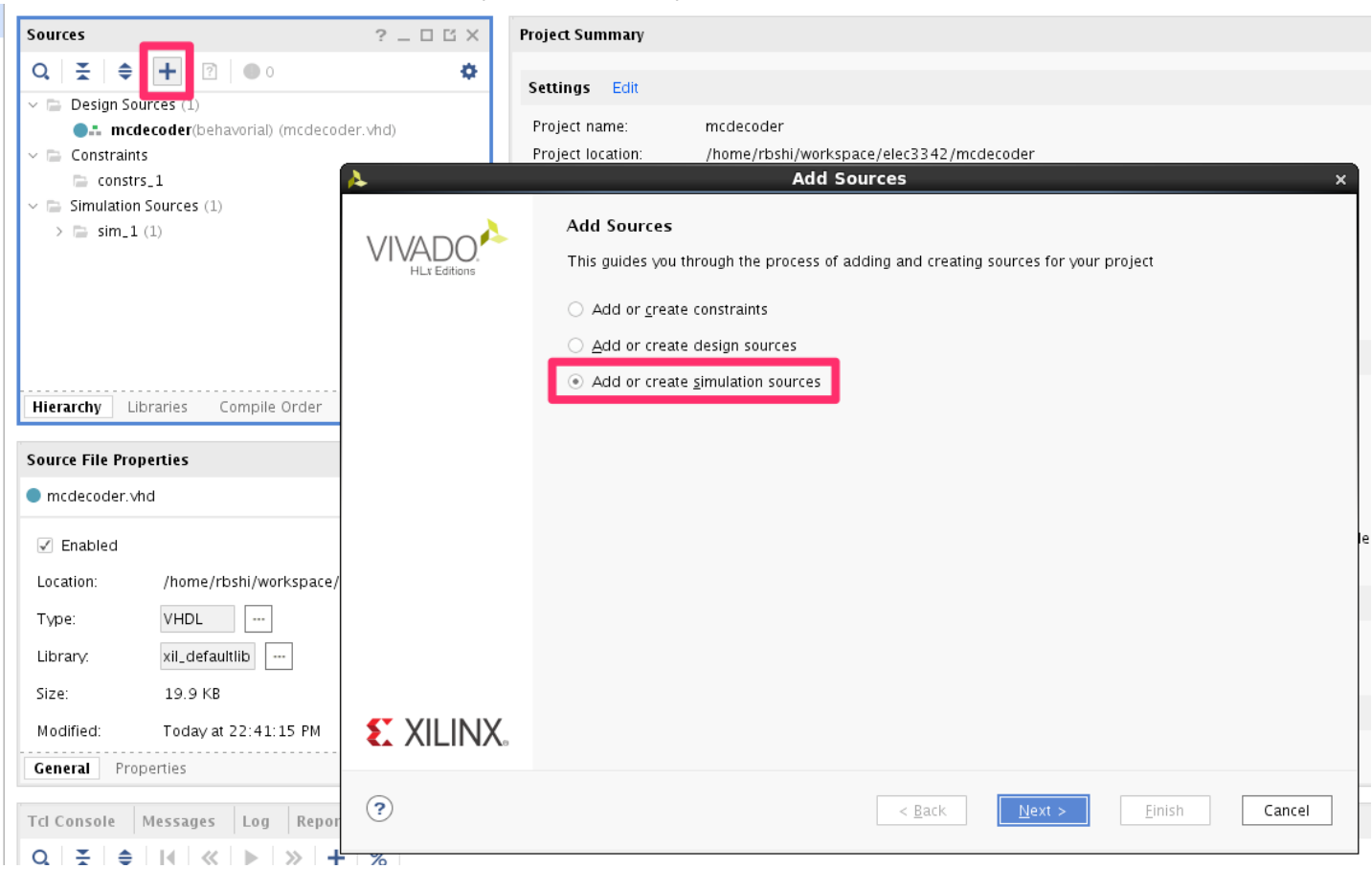
STEP5: Add the *design source file.*



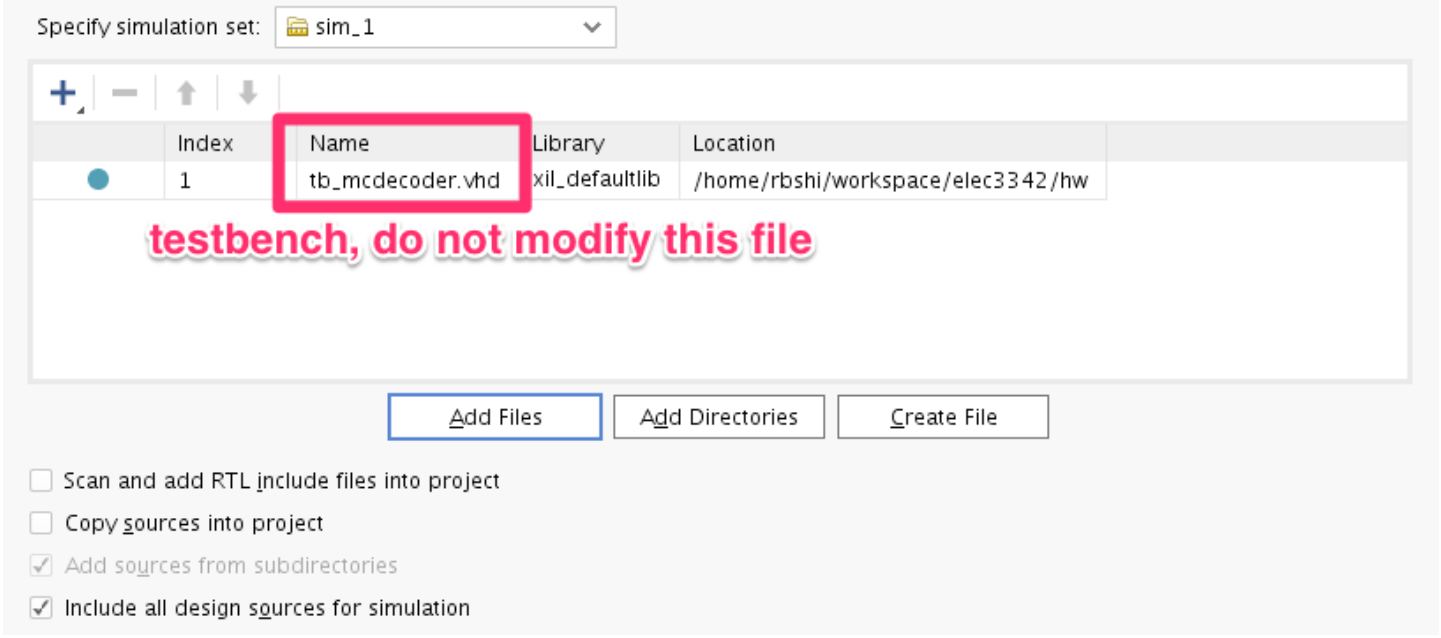
STEP6: Select the file mcdecoder.vhd from your computer. It is the hardware design *template* with I/O port definitions and hints to complete your work; **You should add your own hardware design into this file**.



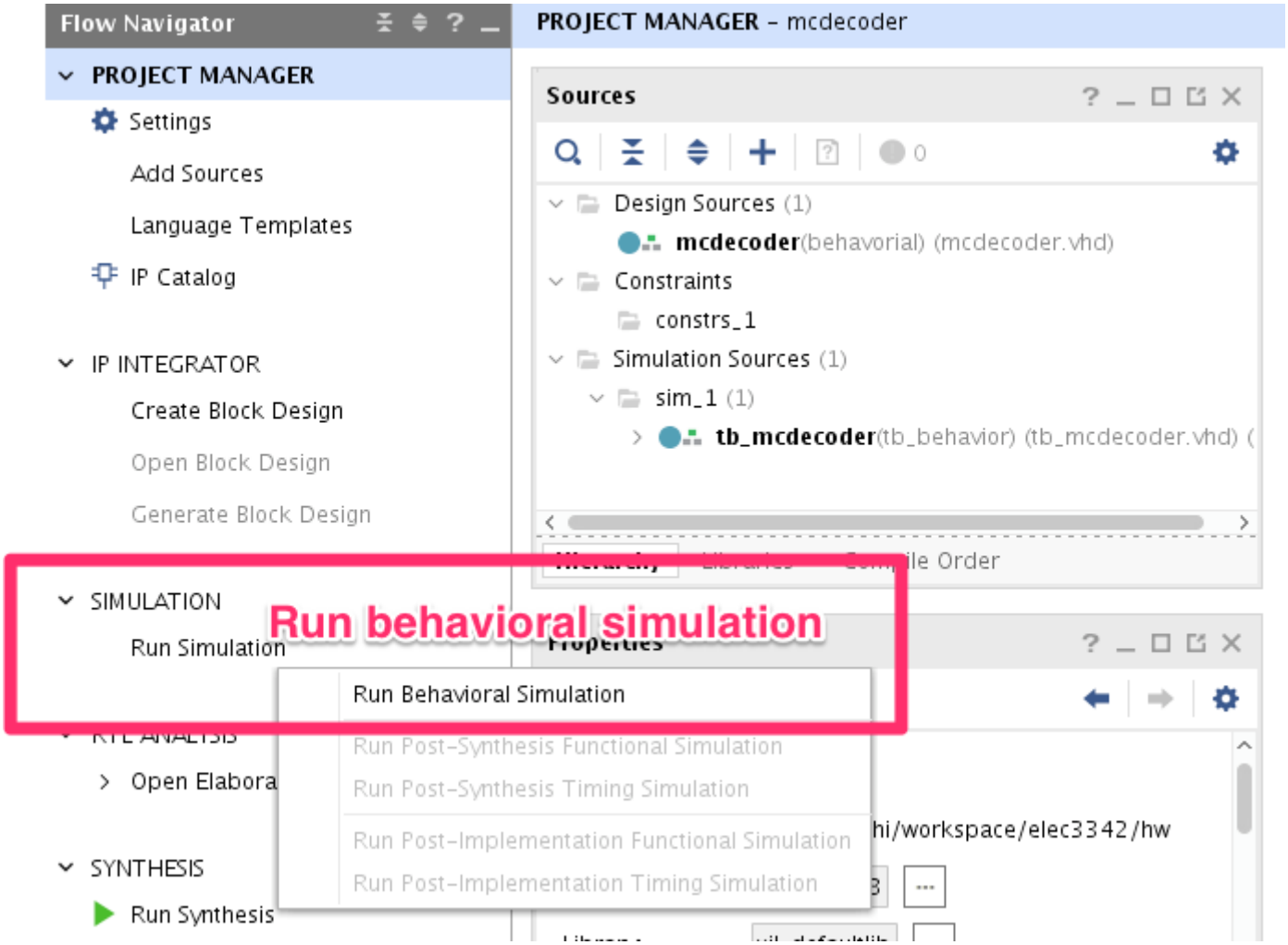
STEP7: Add the *simulation source file (testbench code).*



STEP8: Select the file tb_mcdecoder.vhd, which contains completed testbench code with test signals that will test your design. Do not modify this file.

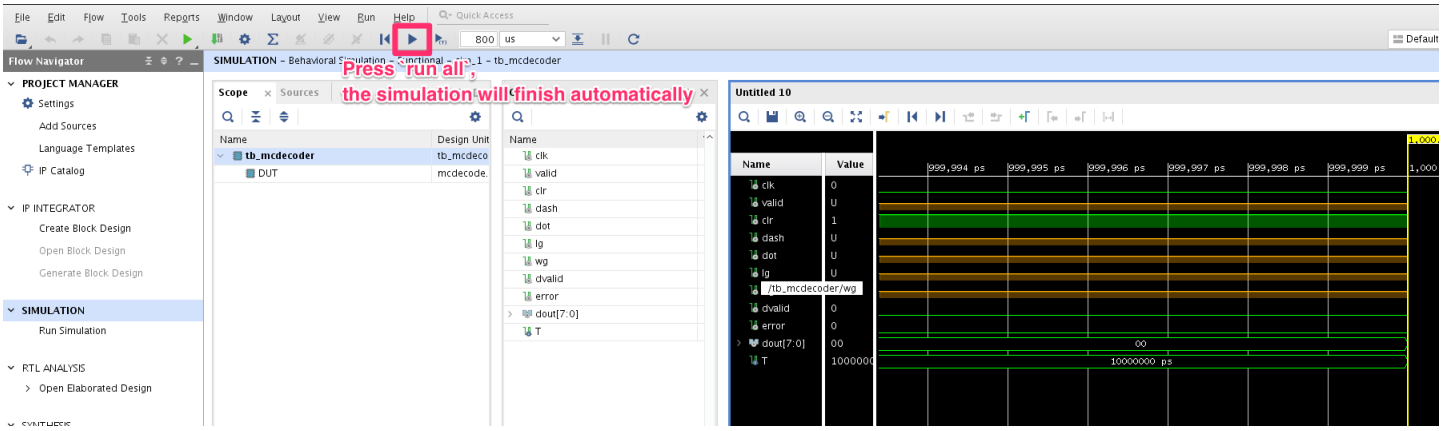


STEP9: Run a hardware behavioral simulation to verify the design function.



STEP10: Press the *run all* button to start the simulation. During the simulation, the testbench produces a sample Morse code signal to your hardware and collects the decoded results. It takes a few seconds and will finish automatically. The *wave window* can be used for tracing the bugs during design iterations.

Once you have changed your code (in mcdecoder.vhd), you can run the simulation by closing the simulation window and repeat **STEP9** again.



STEP11: To help verify the behavior, the decoded results (`*dout*`) indicated by high-value of `*dvalid*` signal are printed out in sequential, as the following figure. For this experiment, there are four ASCII codes are printed corresponding to (A,T,spcae,M) respectively. Note that the ASCII codes are in decimal format.