A1.1

$$T_c \geq t_{pcq} + t_{pd} + t_{setup}$$

$$= 60ps + 5 \times 100ps + 57ps$$

$$= 617ps.$$

$$f_{max} = \frac{1}{T_{cmin}} = \frac{1}{617ps} = 1.62GHz$$

A1.2:

$$T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew}$$

$$\Rightarrow t_{skew} \leq T_c - t_{pcq} - t_{pd} - t_{setup}$$

$$= \frac{1}{1.6GHz} - 60ps - 5 \times 100ps - 57ps$$

$$= 8ps.$$

A1.3.

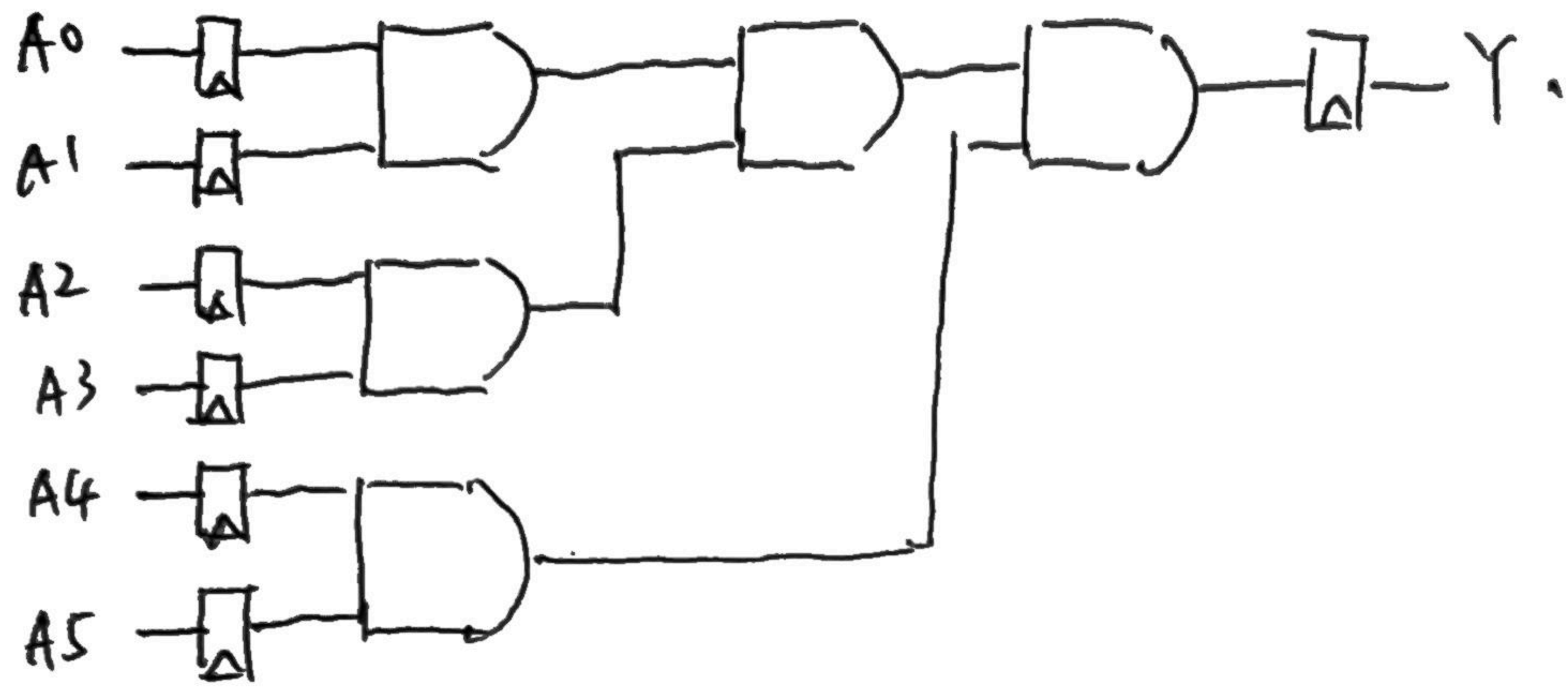
$$t_{ccq} + t_{cd} \geq t_{hold} + t_{skew}$$

$$\Rightarrow t_{skew} \leq t_{ccq} + t_{cd} - t_{hold}$$

$$= 40ps + 45ps - 17ps$$

$$= 68ps.$$

A 1.4. To increase the tolerate of clock skew, Increase t_{cd}. Decrease t_{pd}.



$t_{pd} = 3 \times 100ps = 300ps$.

$t_{cd} = 2 \times 45ps = 90ps$.

$T_c \geq t_{pcq} + t_{pd} + t_{setup}$

$= 60ps + 300ps + 57ps$.

$= 417 ps$.

$f_{max} = \frac{1}{T_{cmin}} = \frac{1}{417ps} = 2.40 GHz$.

$t_{skew} \leq t_{ccq} + t_{cd} - t_{hold}$

$= 40ps + 90ps - 17ps$

$= 113 ps$.

A2 :

$$P(\text{failure})$$

$$= \frac{1}{MTBF} = \frac{1}{1\ \text{year}} = \frac{1}{365 \times 24 \times 3600}$$

$$= 3.17 \times 10^{-8}$$

As $N = 4$ times. To satisfy the MTBF :

$$P(\text{failure}) = \frac{1}{4} P(\text{failure})$$

$$= \frac{1}{4} \times 3.17 \times 10^{-8} = 7.927 \times 10^{-9}$$

$$P = \frac{T_0}{T_c} e^{-\frac{T_c - t_{setup}}{\tau}}$$

$$\Rightarrow 7.927 \times 10^{-9} = \frac{110\,ps}{T_c} \exp\left(\frac{-(T_c - 70\,ps)}{100\,ps}\right)$$

$$\Rightarrow T_c = 1.6637\ ns$$

$$t = T_c - t_{setup}$$

$$= 1663.7\,ps - 70\,ps$$

$$= 1593.7\,ps.$$

A3.1 (a)

(i) $\Sigma t_{pd} = t_{pd} + 4t_{pd} + t_{pd} + t_{pd} + t_{pd}$

$= 8t_{pd}$.

$f_{max} = \frac{1}{T_{cmin}} = \frac{1}{t_{pcq} + 8t_{pd} + t_{setup}}$

(ii) Infinitely slow

(iii) throughput $= f_{max} = \frac{1}{t_{pcq} + 8t_{pd} + t_{setup}}$

(iv) latency $= 1$ cycle.

(b) (i) $\Sigma t_{pd} = \max(t_{pd} + 4t_{pd} + t_{pd} + t_{pd},\ t_{pd})$

$= 7t_{pd}$.

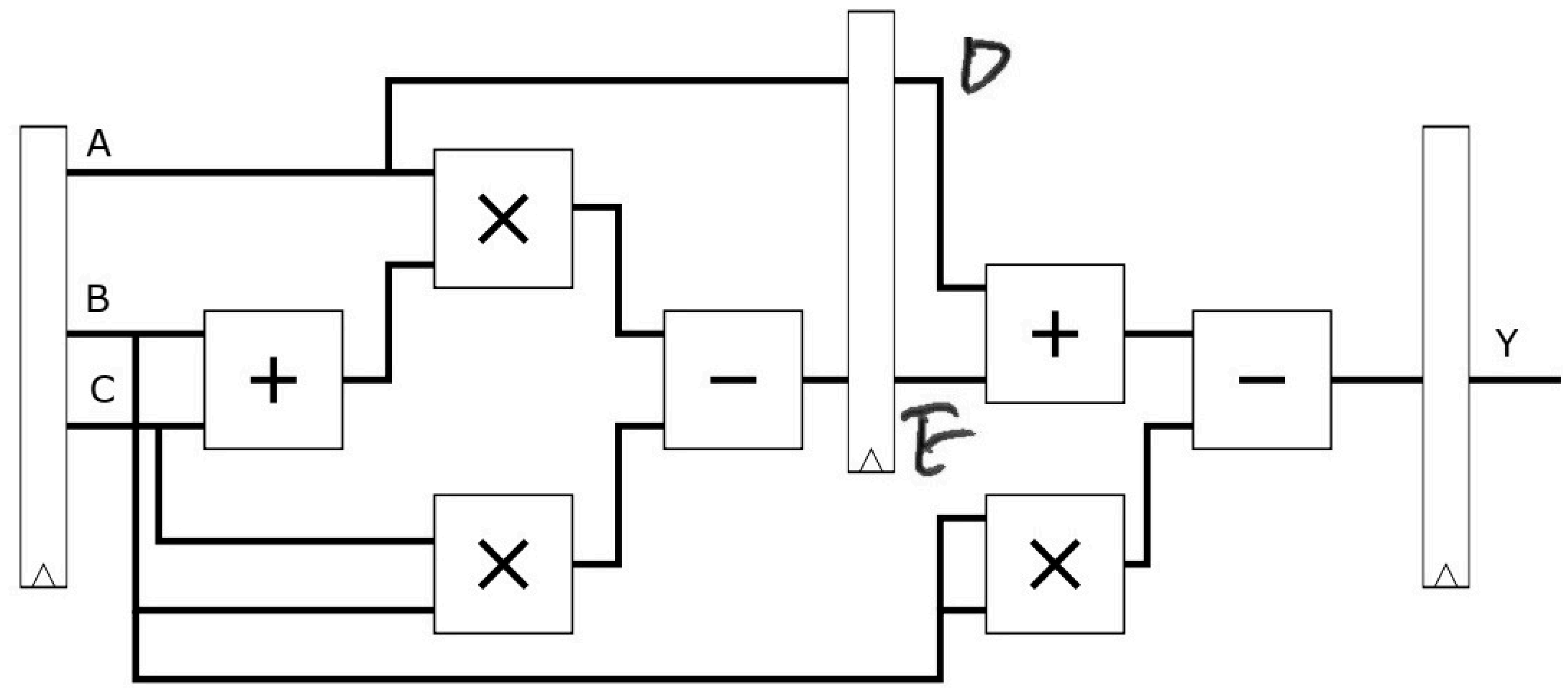
$f_{max} = \frac{1}{T_{cmin}} = \frac{1}{t_{pcq} + 7t_{pd} + t_{setup}}$

(ii) Infinity slow

(iii) throughput $= f_{max} = \frac{1}{t_{pcq} + 7t_{pd} + t_{setup}}$.

(iv) latency $= 2$ cycles.

A 3.2.



$$Y[n] = D[n-1] + E[n-1] - B[n] \cdot B[n]$$

$$= A[n-1] + A[n-1] \times \left[B[n-1] + C[n-1] \right] -$$

$$B[n-1] \cdot C[n-1] - B[n] \cdot B[n].$$

$\Rightarrow$ sequence doesn't match.

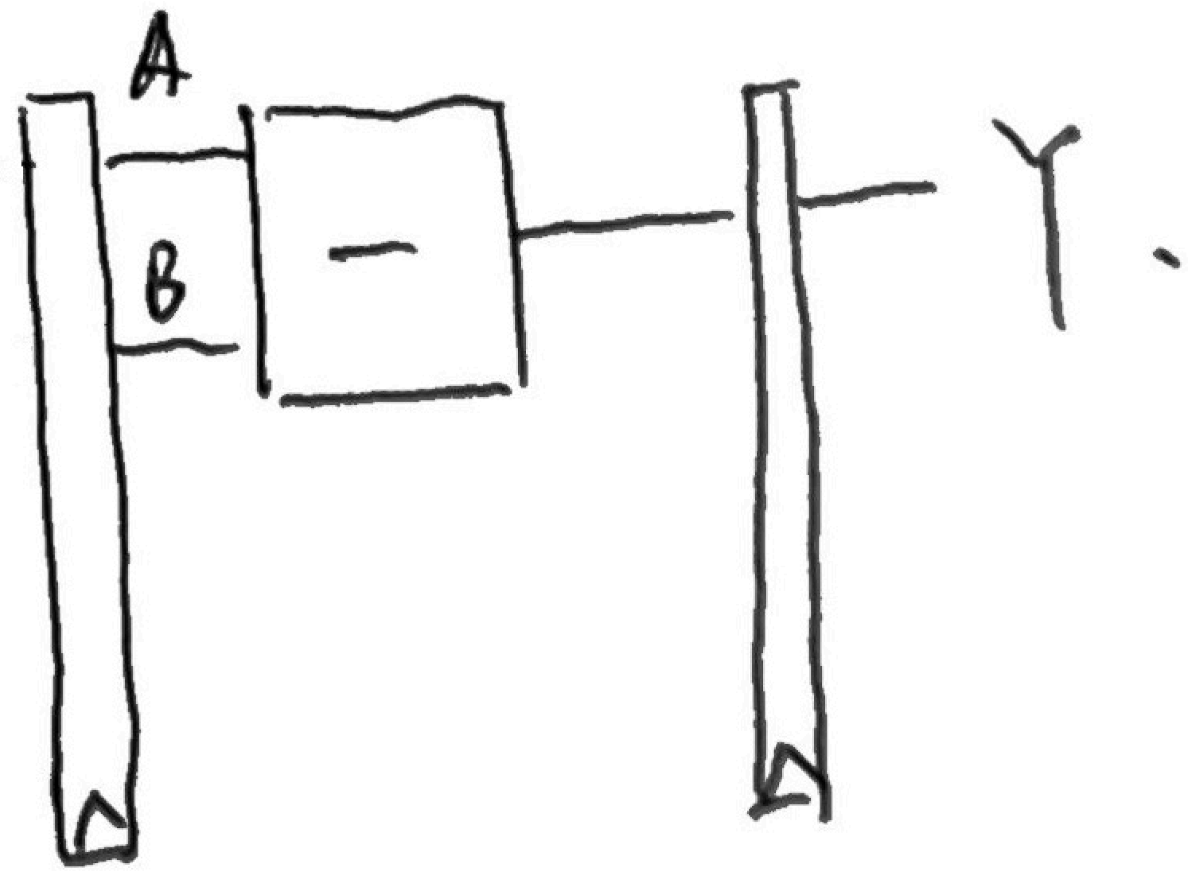
A 3.3.

$$Y = A(B+C) - BC + A - B \cdot B$$

$$= AB + AC - BC + A - B \cdot B$$

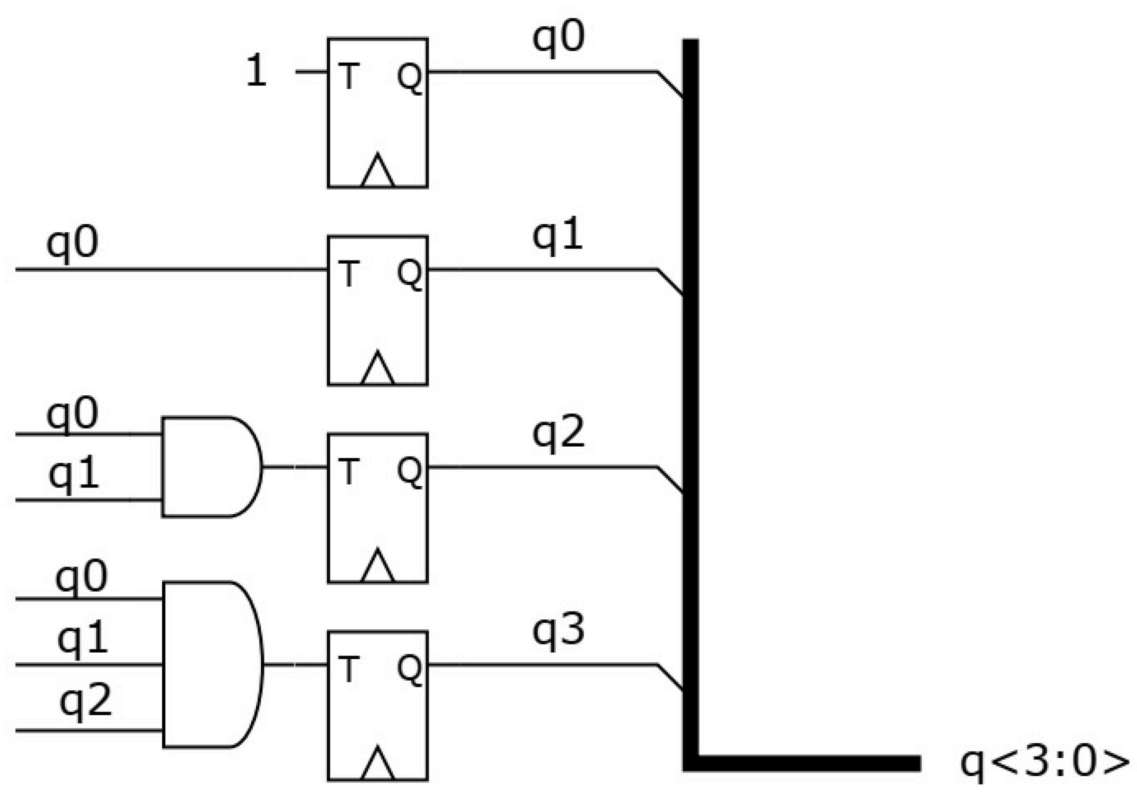
$$= A - B(B+C)$$

$$= A - B.$$



$$\text{throughput} = f_{max} = \frac{1}{t_{pcq} + t_{pd} + t_{setup}}$$

A 4.1



the critical path is the 4th T-FF.

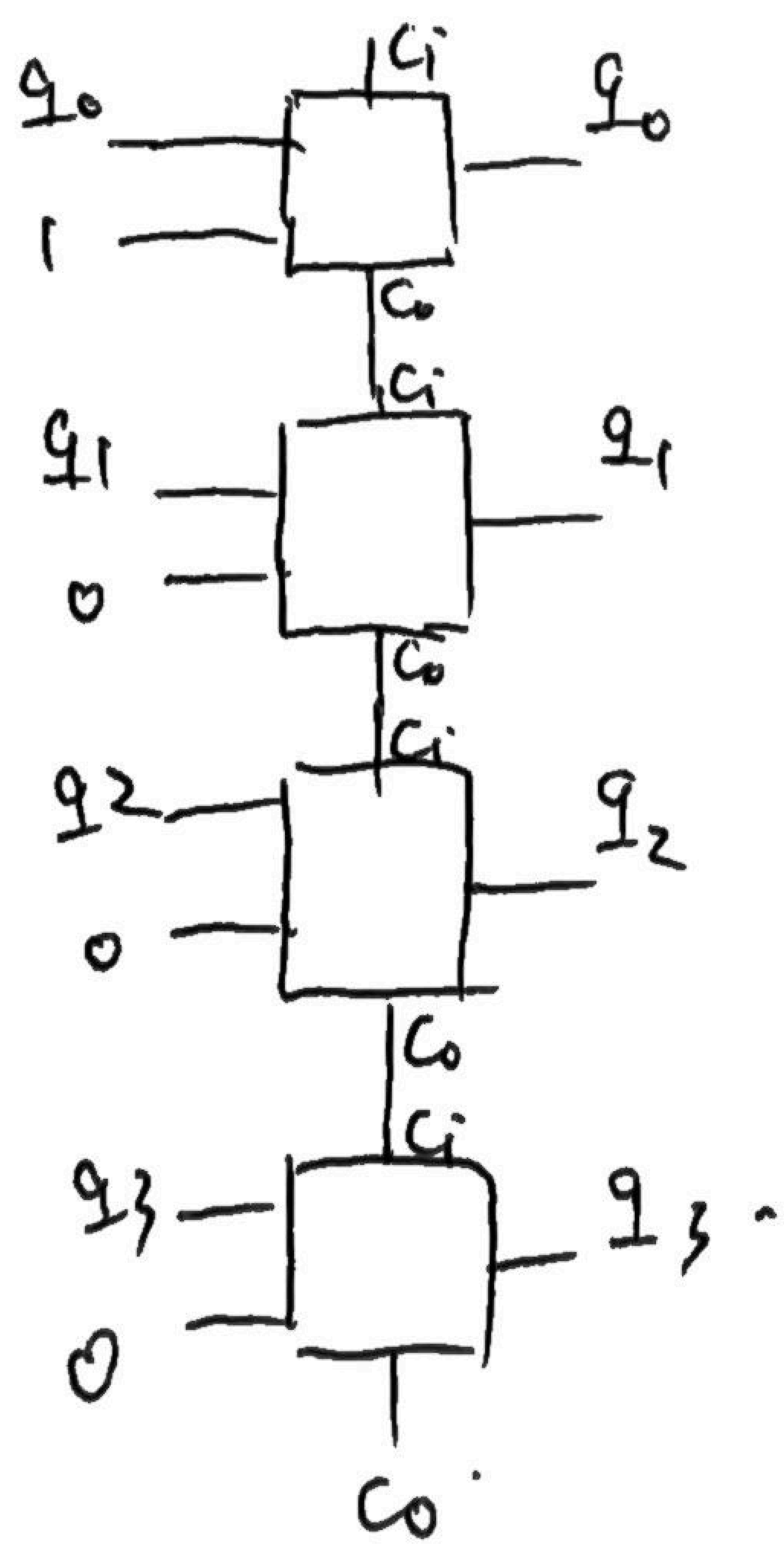
$t_{pd} = t_{pd,3}$.

$$f_{max} = \frac{1}{T_{cmin}} = \frac{1}{t_{pcq} + t_{pd} + t_{setup}}$$

$$= \frac{1}{2ns + 25ns + 7ns}$$

$$= 29.412\ MHz.$$

A 4.2:



Critical path is from the input of 1st FA to the output of 4th FA.

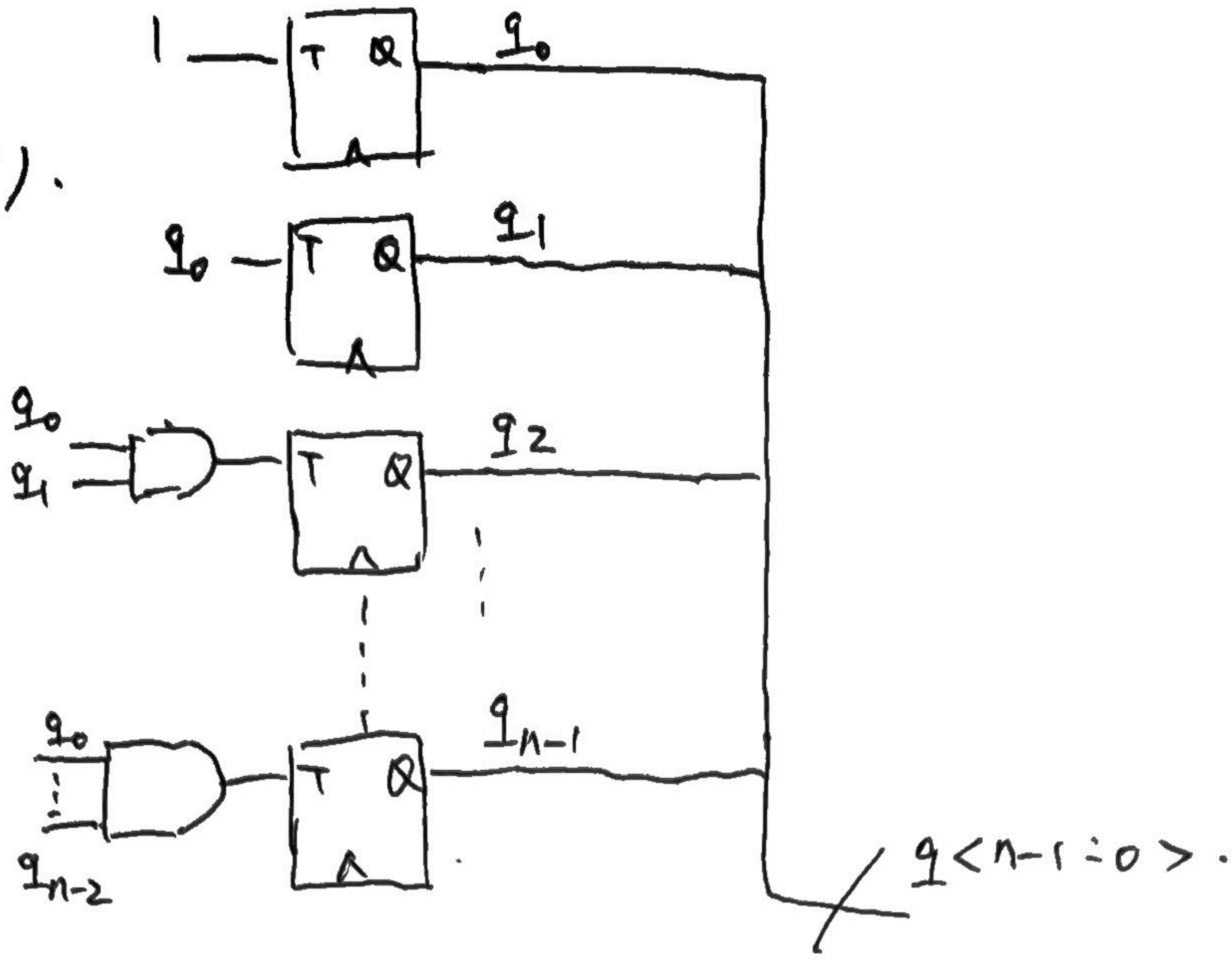
$$f_{max} = \frac{1}{T_{cmin}}$$

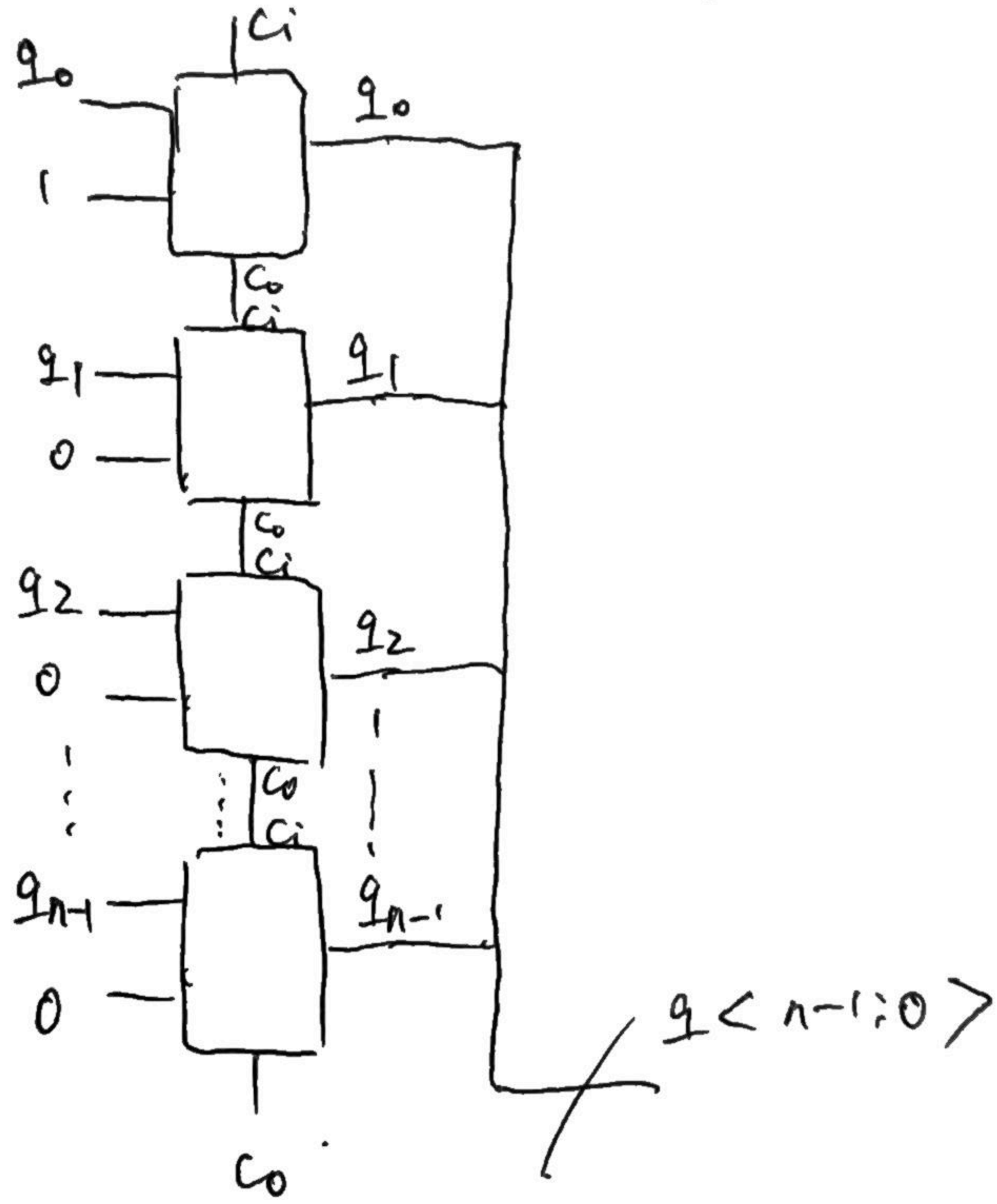
$$= \frac{1}{t_{pcq} + t_{pd} + t_{setup}}$$

$$= \frac{1}{2ns + 4 \times 20ns + 3ns}$$

$$= 11.765\ MHz.$$

A4.3. (i).





(2). Critical path of CntrP is the nth T-FF

Critical path of CntrA is from the input of 1st FA to the output of the last FA.

CntrP: $f_{max} = \frac{1}{T_{cmin}} = \frac{1}{2ns + (5+10\times 2^{n-1-2})ns + 7ns}$

$= \left[14 + 10\times 2^{n-3}\right]^{-1}$ GHz.

CntrA: $f_{max} = \frac{1}{T_{cmin}} = \frac{1}{2ns + 20n\,ns + 3ns} = \frac{1}{20n+5}$ GHz.

(3)

$$\frac{1}{20n+5} = \frac{1}{14+10\times 2^{n-3}}$$

$$\Rightarrow 20n+5 = 14+10\times 2^{n-3}$$

$$\Rightarrow \begin{cases} n_1 = 0.5409 \\ n_2 = 6.6269 \end{cases}$$

$\Rightarrow$ when $0.5409 < n < 6.6269$:

$20n+5 > 10\times 2^{n-3}+14$

$\Rightarrow$ when $n \geq 7$:

CntrA has higher frequency.