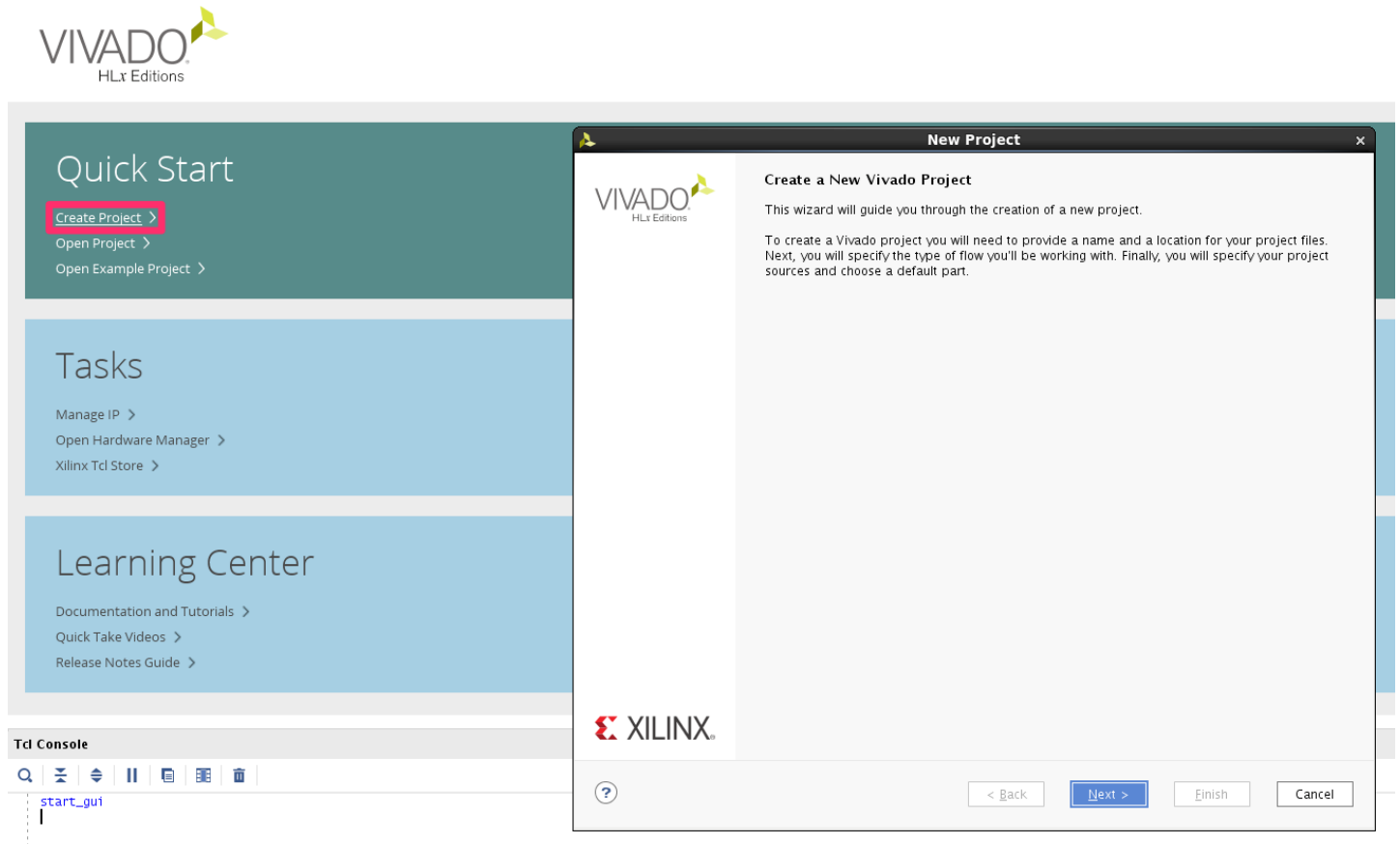


ELEC3342 Tutorial: Homework1-B

STEP1: Open Vivado and create a new project.



STEP2: Name the project and check *Create project subdirectory*.

Project name:

Project location:

☒ Create project subdirectory

Project will be created at: /home/rbshi/workspace/elec3342/mcdecoder

STEP3: Select the RTL Project and check *Do not specify sources at this time*.

☒ RTL Project
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☒ Do not specify sources at this time

STEP4: Select the proper FPGA device for this project as in the following figure.

Parts | Boards

[Reset All Filters](#)

Category: Package: Temperature:

Family: Speed:

Search:

Part	I/O Pin Count	Available IOBs	LUT Elements	FlipFlops	Block RAMs	Ultra RAMs	DSPs
xc7a35tcbpg236-3	236	106	20800	41600	50	0	90
xc7a35tcbpg236-2	236	106	20800	41600	50	0	90
xc7a35tcbpg236-2L	236	106	20800	41600	50	0	90
xc7a35tcbpg236-1	236	106	20800	41600	50	0	90
xc7a35tcbpg324-3	324	210	20800	41600	50	0	90

STEP5: Add the *design source file*.

Sources | Project Summary

Settings | [Edit](#)

Project name: mcdecoder
Project location: /home/rbshi/workspace/elec3342/mcdecoder

Add Sources

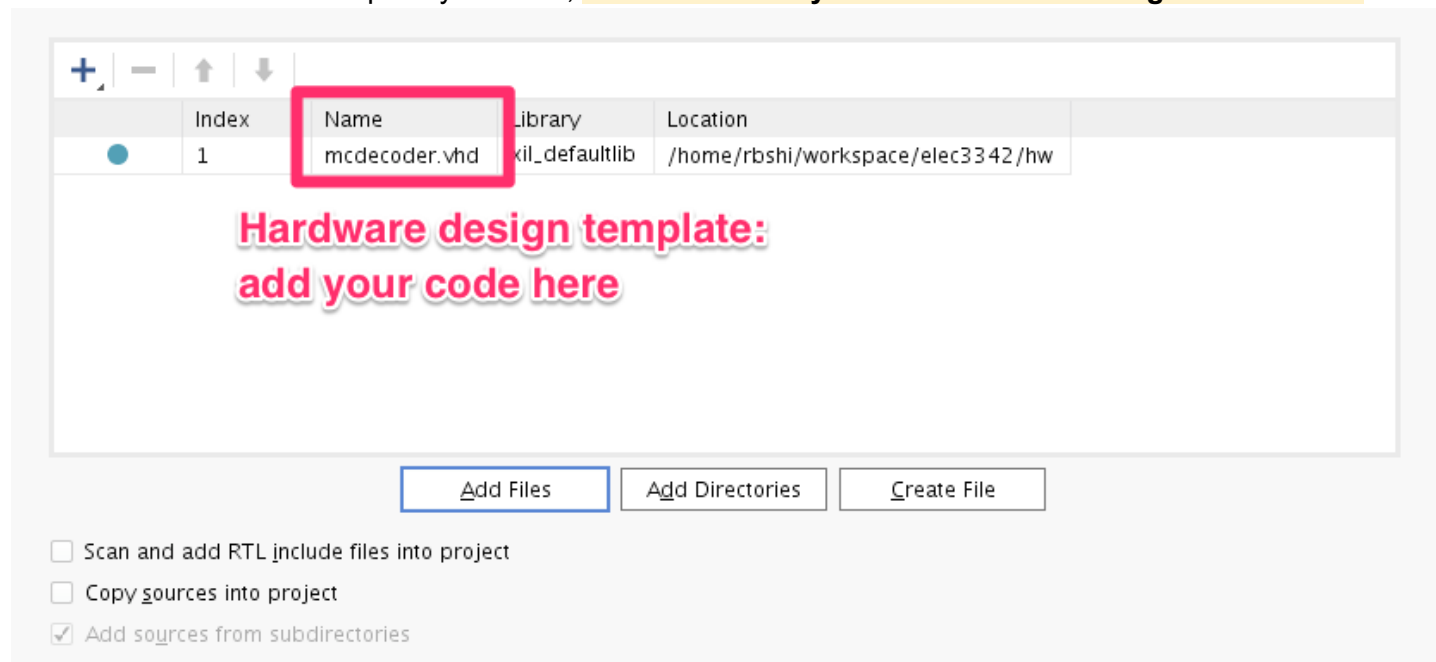
This guides you through the process of adding and creating sources for your project

- ☐ Add or create constraints
- ☒ Add or create design sources
- ☐ Add or create simulation sources

XILINX

[< Back](#) [Next >](#) [Finish](#) [Cancel](#)

STEP6: Select the file `mcdecoder.vhd` from your computer. It is the hardware design *template* with I/O port definitions and hints to complete your work; **You should add your own hardware design into this file.**



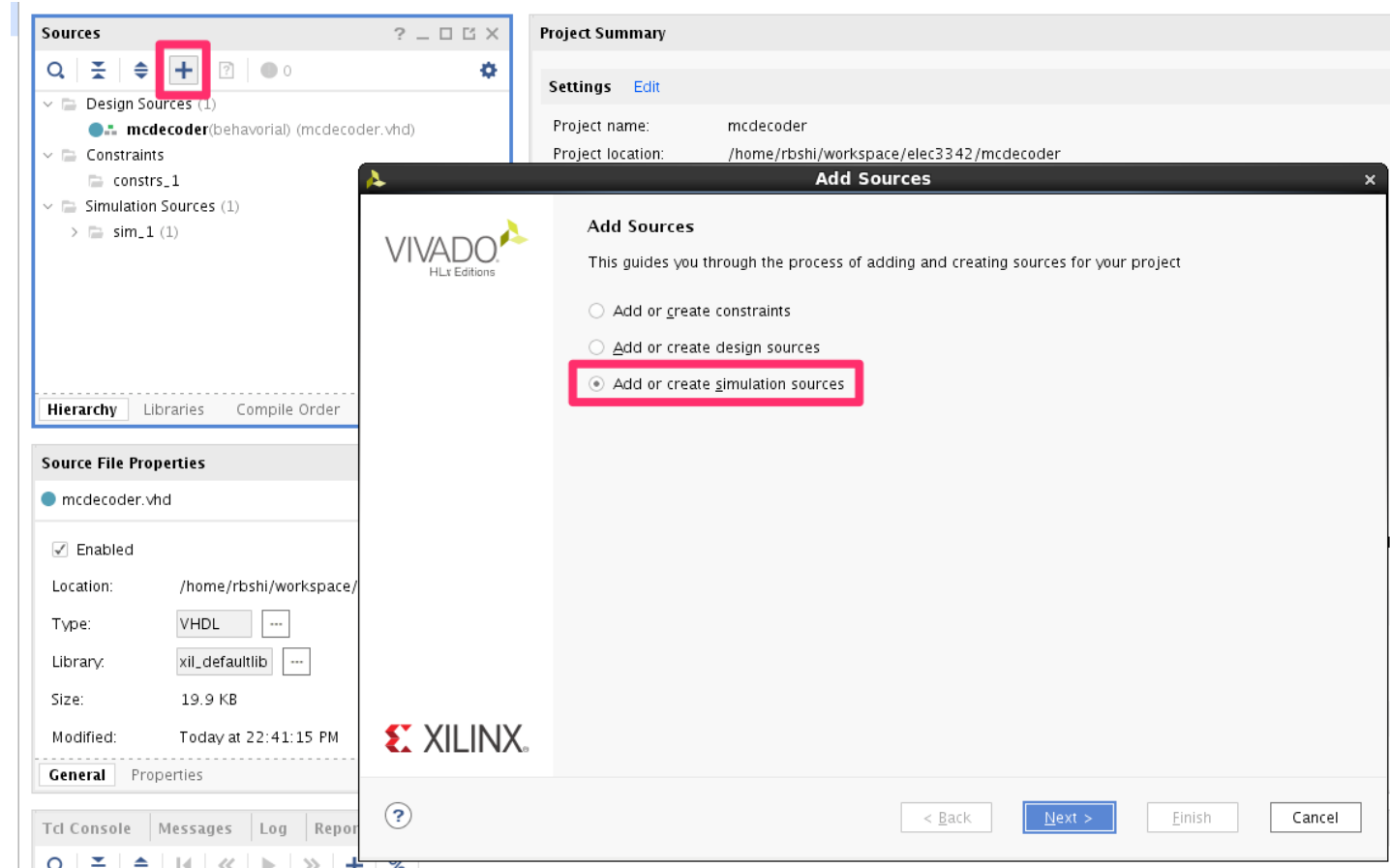
Index	Name	Library	Location
1	mcdecoder.vhd	xil_defaultlib	/home/rbshi/workspace/elec3342/hw

**Hardware design template:
add your code here**

[Add Files](#) [Add Directories](#) [Create File](#)

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories

STEP7: Add the *simulation source file (testbench code)*.



Sources

- Design Sources (1)
 - mcdecoder (behavioral) (mcdecoder.vhd)
- Constraints
 - constrs_1
- Simulation Sources (1)
 - sim_1 (1)

Project Summary

Settings Edit

Project name: mcdecoder
Project location: /home/rbshi/workspace/elec3342/mcdecoder

Add Sources

This guides you through the process of adding and creating sources for your project

- ☐ Add or create constraints
- ☐ Add or create design sources
- ☒ Add or create simulation sources

Source File Properties

mcdecoder.vhd

☒ Enabled

Location: /home/rbshi/workspace/

Type: VHDL

Library: xil_defaultlib

Size: 19.9 KB

Modified: Today at 22:41:15 PM

General Properties

Tcl Console Messages Log Report

< Back Next > Finish Cancel

STEP8: Select the file `tb_mcdecoder.vhd`, which contains completed testbench code with test signals that will test your design. Do not modify this file.

Specify simulation set: sim_1

	Index	Name	Library	Location
●	1	tb_mcdecoder.vhd	xil_defaultlib	/home/rbshi/workspace/elec3342/hw

testbench, do not modify this file

Add Files Add Directories Create File

☐ Scan and add RTL include files into project
☐ Copy sources into project
☒ Add sources from subdirectories
☒ Include all design sources for simulation

STEP9: Run a hardware behavioral simulation to verify the design function.

Flow Navigator **PROJECT MANAGER - mcdecoder**

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

Run behavioral simulation

Sources

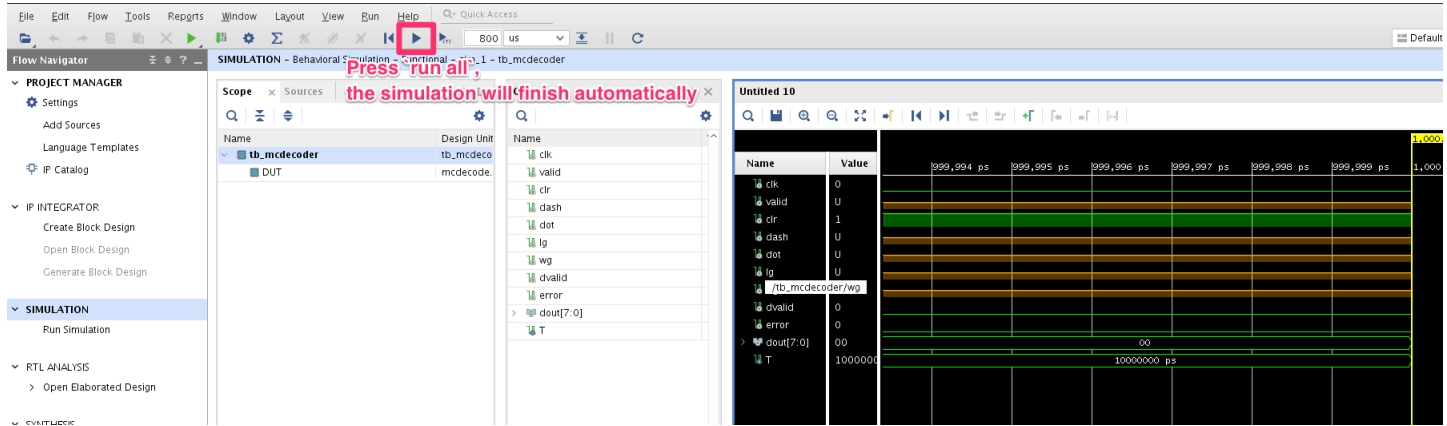
- Design Sources (1)
 - mcdecoder(behavioral) (mcdecoder.vhd)
- Constraints
 - constrs_1
- Simulation Sources (1)
 - sim_1 (1)
 - tb_mcdecoder(tb_behavior) (tb_mcdecoder.vhd)

Properties

- Run Behavioral Simulation
- Run Post-Synthesis Functional Simulation
- Run Post-Synthesis Timing Simulation
- Run Post-Implementation Functional Simulation
- Run Post-Implementation Timing Simulation

STEP10: Press the *run all* button to start the simulation. During the simulation, the testbench produces a sample Morse code signal to your hardware and collects the decoded results. It takes a few seconds and will finish automatically. The *wave window* can be used for tracing the bugs during design iterations.

Once you have changed your code (in mcdecoder.vhd), you can run the simulation by closing the simulation window and repeat **STEP9** again.



STEP11: To help verify the behavior, the decoded results (*dout*) indicated by high-value of *dvalid* signal are printed out in sequential, as the following figure. For this experiment, there are four ASCII codes are printed corresponding to (A,T,spcae,M) respectively. Note that the ASCII codes are in decimal format.

