Design Automation of Transferable Analog Circuit Using Deep Reinforcement Learning

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Abstract & Introduction

Moore's Law drives transistor counts to double every two years, prompting designers to migrate designs to smaller technology nodes. Analog circuit design traditionally demands extensive analysis and parameter tuning. To streamline this, we propose employing Deep Reinforcement Learning (DRL) for automatic transistor sizing. While existing research mainly adapts DRL for individual circuit adjustments, little attention has been given to knowledge transfer across different topologies or technology nodes. Our strategy involves training simplified circuit architectures on established processes and applying transfer learning to extend these capabilities to new processes or more complex designs.

Methodology

To implement the transfer learning in analog circuit design, we divide the process into two steps:

First step: We use Soft Actor-Critic as our main approach to train our agent, aiming to learn the policy for tuning small circuit structures. The circuit performance is evaluated as equation (1).

Second step: We use Qavatar framework as our method to transfer the trained policy for small structures from the first step as our source policy to the larger circuit structures to accelerate the target policy learning as shown in Figure 1.

$$Reward = \frac{Gain \cdot Bandwidth \cdot PMF}{Power} \qquad (1)$$

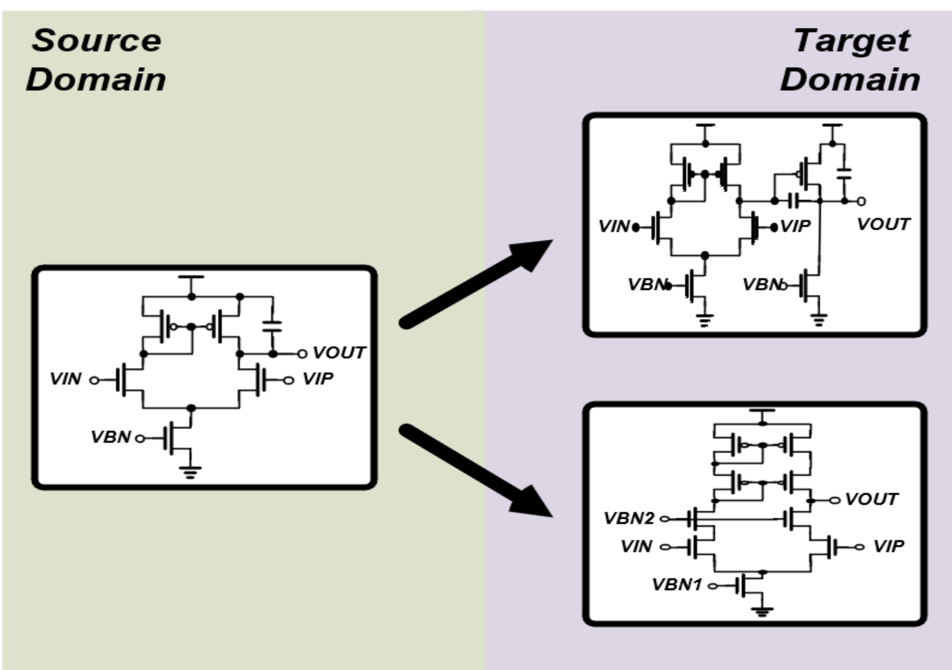

Figure 1: Transfer Learning

Experiments

For the experimental setup, we selected operational amplifiers (OPA), which are the most typical and widely used circuits in analog electronics. We conducted our simulations using the UMC 180nm process. To ensure the trained circuits meet basic requirements, we added a gain specification to the reward function. Due to time constraints, we chose the simplest circuit architecture, a single-stage amplifier, shown in Fig. 2.a, as the source domain for our first step, with simulation results depicted in Fig. 3.a.

During the second step of the transfer process, we conducted multiple tests based on the source policy trained in the first step:

Experiment 1: The experiment was adapted to a larger but similar circuit by implementing a OPA, shown in Fig. 2.b,with simulation results depicted in Fig. 3.b.

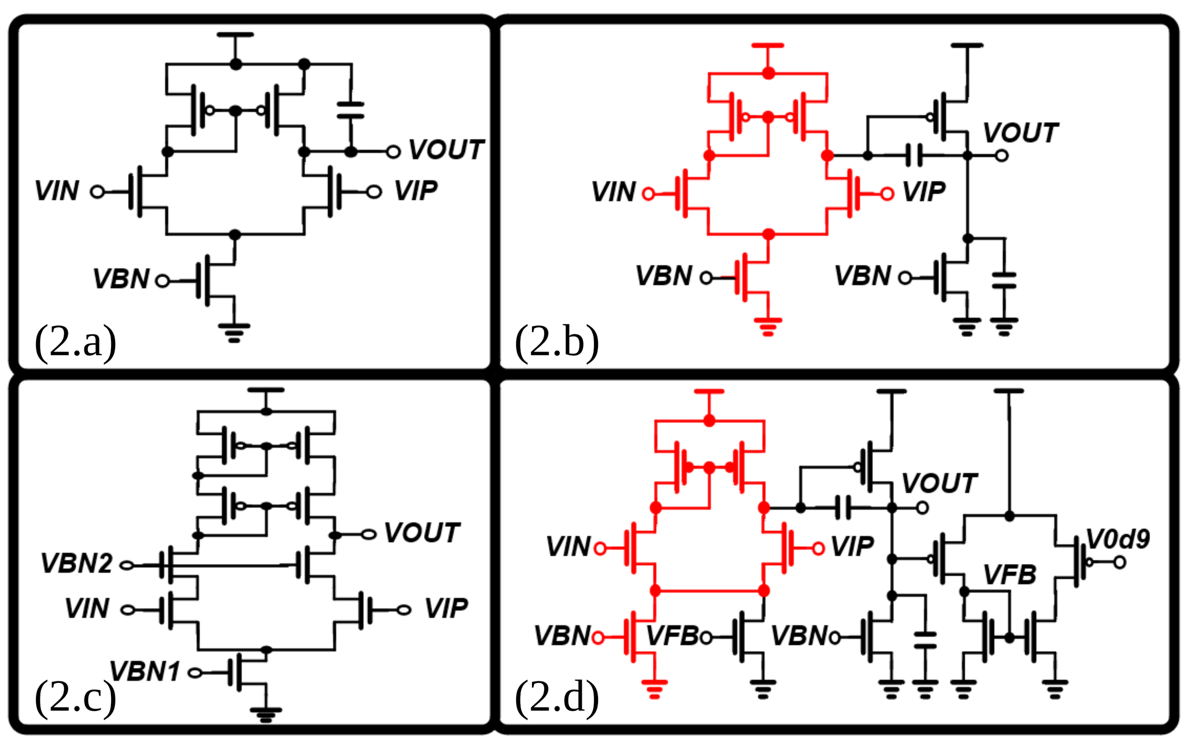

Figure 2: a) basic one stage OPA; b) two stage OPA; c) telescopic OPA; d) two stage OPA with CMFB

Experiment 2: the experiment was adjusted to a larger but significantly different architecture, employing a telescopic amplifier design illustrated in Fig. 2.c, with simulation results shown in Fig. 3.c.

Experiment 3: the investigation transitioned to a larger but similar circuit architecture, integrating a designed CMFB into the two-stage OPA, depicted in Fig. 2.d, with simulation results shown in Fig. 3.d.

Experiment 4: the experiment moved to a different process node, specifically transitioning from UMC 180nm to TSMC 28nm, with simulation results depicted in Fig. 3.e.

Experiment 5: the experiment shifted to a different reward function, with simulation results shown in Fig. 3.f.

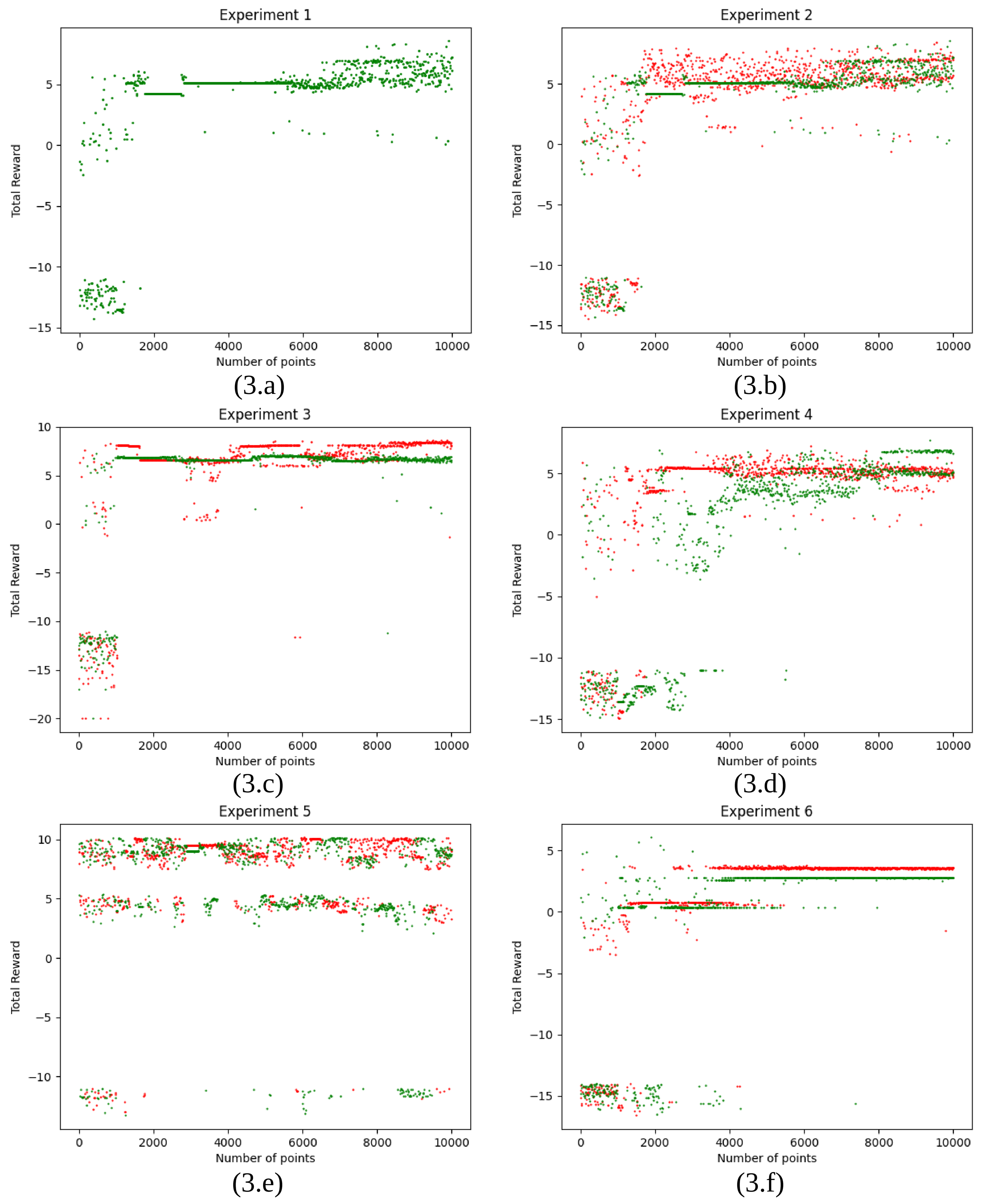

Figure 3: Simulation Results; Green dots: W/O Transfer; Red dots: W/ Transfer

Max Reward	Experiment 1	Experiment 2	Experiment 3	Experiment 4	Experiment 5	Experiment 6
W/	**-**	8.48	**8.60**	7.27	**10.17**	3.79
W/O	8.58	**8.58**	7.37	**7.69**	10.16	**6.07**

Table1: Maximum Total Reward

Conclusions & Future work

We introduce an RL agent as a circuit designer capable of automatically optimizing circuit sizing of the small architecture to outperform human designers in performance. Leveraging RL's transferability, we can transfer knowledge across different technology nodes and even diverse circuit topologies, a feat challenging for other methodologies. Consequently, the RL Circuit Designer enables more effective and efficient design portability.

We believe that even for the very large scale of analog circuit, we still can achieve a good result better than human designers using transfer learning in reinforcement learning.

References

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