EENGM6030_2022_TB-2: Analogue Integrated Circuit Design 2022

Coursework: Voltage reference circuit design

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The project GitHub link:

https://github.com/alfredzhang98/Bristol_ACID_lab.git

Catalogue

1. Introduction

In this project, we used the Cadence Design Suite and the 180nm GPDK to design a voltage reference circuit. In addition, this report would describe the topology operation and state the components' dimensions. This report would be divided into the following sections: design principles, schematic design analysis, single operation and direct current (DC) sweep analysis, circuit stability analysis, and system analysis with system temperature and process variations. Additionally, in this project, the load circuit is purely resistive and ranges from 2k to 10k ohms. With five MOSFET processes and temperatures between -40 and 125°C, the entire system is stable and could output 1 volt with an accuracy under 0.17% compared to the reference voltage.

2. Design Principals

2.1 Voltage Reference Circuit

The purpose of the voltage reference circuit (VRC) is to provide a stable and accurate output voltage to a load circuit with a certain range of pure resistive impedance. Its main applications are in voltage-controlled oscillators [1] and power management systems [2]. Figure 2.1 shows the schematic of an NMOS-based VRC, including a voltage-controlled voltage source (VCVS), a 1-volt voltage reference source called Vref, a load circuit, an NMOS, and a 2.5-volt power source. The VCVS is a high-gain differential amplifier, and it could output the difference between the two input signals and amplify them by a factor of K, as the following equation shows [3]:

$$V_{gs} = K\left(V_{C_+} - V_{C\_}\right) \tag{2.1}$$

In this circuit, Vref is the positive input of the VCVS, and a feedback network feeds the output voltage to the negative input of the VCVS. It appears that negative feedback is employed as the feedback path, but this is not the case as the NMOS performs an inverting function in signal terms. This means that the output voltage would increase as the Vgs rose. Therefore, if there is a difference between the output voltage and Vref, the NMOS could increase the output voltage so that the output voltage is close to Vref. This means that if the resistance of the load circuit changes, the current in the NMOS is adjusted so that the output voltage remains at Vref.

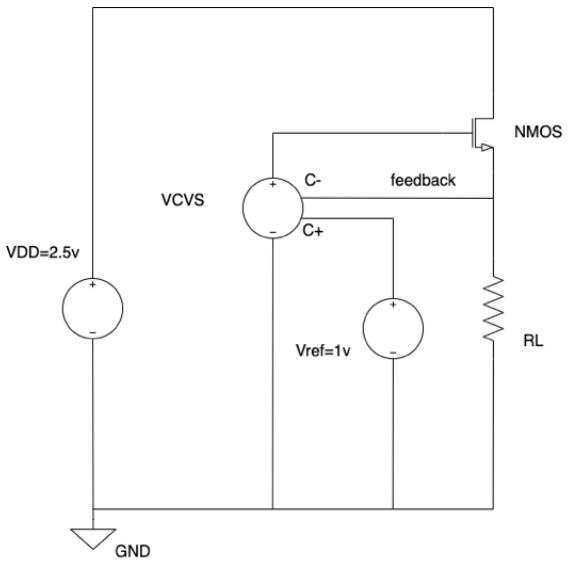


Figure.2.1 The schematic of the NMOS VRC.

2.2 Two-stage CMOS Amplifier

The design of the VCVS is very important. The differential amplifier circuit is the basic amplifier circuit for VCVS. It could be divided into two types, the NFET input operational amplifier and the PFET input differential amplifier. However, the PFET is more common than the NFET, because the PFET could provide a greater slew rate, have greater high-frequency gain, and have less input stage noise. Therefore, in this project, we would like to choose the PFET input differential amplifier to implement the differential amplification. Although a differential amplifier could provide gain, it cannot catch up with the high positive gain from a two-stage CMOS amplifier, which could achieve more sensitive feedback. Therefore, in this report, a two-stage CMOS amplifier would be designed to achieve the high-gain VCVS design requirement, as Figure 2.2 shows [3].

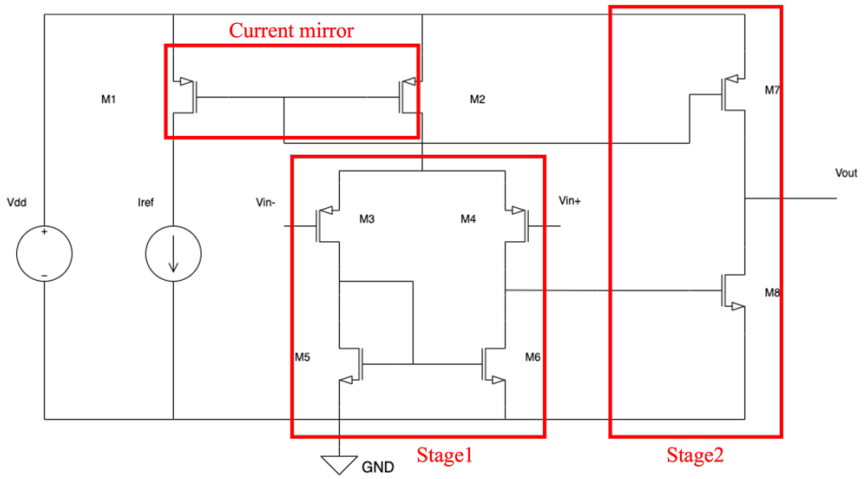


Figure.2.2 The schematic of the two-stage CMOS amplifier.

In this two-stage CMOS amplifier, there is a current mirror to provide the stable reference (bias) current, which is a 50 μA DC source in this project. In this circuit, the power supply is 2.5 volts, and all the bulk and source of PMOS are connected to it. As motioned before, stage one is the differential amplifier that could provide a small negative gain, whereas stage two has a common source amplifier with a current source load, which could provide a significantly high positive voltage gain with a high output resistance, as shown in the red box in Figure 2.3.

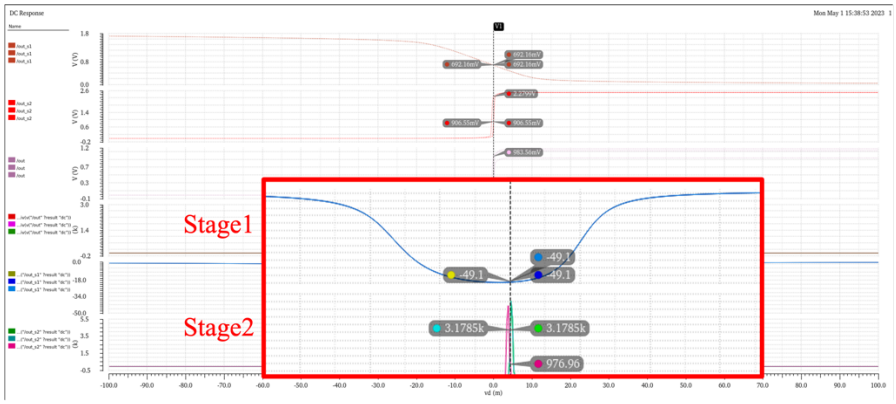


Figure.2.3 The gain analysis of the two-stage CMOS amplifier.

If we want the two-stage CMOS amplifier to be stable, a Miller capacitor could be put between the output stage 1 and the output stage 2. The capacitor could move the two frequency response poles closer in order to increase the phase margin and delay the attenuation of the phase. Additionally, a series resistor could move the frequency response zero to infinite, which could further slow the phase attenuation, thus increasing the phase

margin. The equations below show the above-mentioned corresponding relationship [3].

$$\begin{cases} f_{p1} \cong \dfrac{1}{2\pi R_1 G_{m2} R_2 C_c} \\ f_{p2} \cong \dfrac{G_{m2}}{2\pi C_2} \\ f_z \cong \dfrac{G_{m2}}{2\pi C_c} \end{cases} \tag{2.2}$$

Specifically analysing the values of these two stabilising elements, for the Miller capacitors their values, should comply with the following equation [3]:

$$C_{Miller} > 0.22 C_{stage2} \tag{2.3}$$

Where C_{stage2} is all the parasitic capacitors and the load capacitor in stage two. However, in this circuit, there is no load capacitor. Therefore, Cstage2 is at the fF level. This means that if we choose a 1pF Miller capacitor, it would always meet the stability design requirements. As for the series resistor, it could also be calculated using the following equation [3]:

$$R_c = \frac{1}{GM6} \tag{2.4}$$

Where GM6 is the transconductance of the M6 that is shown in Figure 2.2, Rc is the series resistor. Therefore, after those calculations, the two-stage CMOS amplifier becomes stable.

2.2 Improvement of the Performance of the Voltage Reference.

Above we have used an NMOS-based VRC circuit. The internal resistance is relatively high when the width of the NMOS is small, which means that the NMOS has more voltage dividing and weaker current conduction. Weaker current conduction means weaker voltage regulation, which prevents the output voltage from being very close to the Vref. Therefore, we would expand the width of the NMOS to reduce the voltage dividing of the NMOS and increase the regulation of the NMOS to achieve a voltage reference circuit with a more accurate output. By analysing the above two-stage CMOS amplifier, if we increase the width of the two PMOS of the differential amplifier, its input noise would be reduced. Therefore, reducing the noise by increasing the width of the two PMOS could also be a promising solution for optimising the VRC circuit. With these theories, I have carried out the corresponding verification, as shown in Figure 2.4.

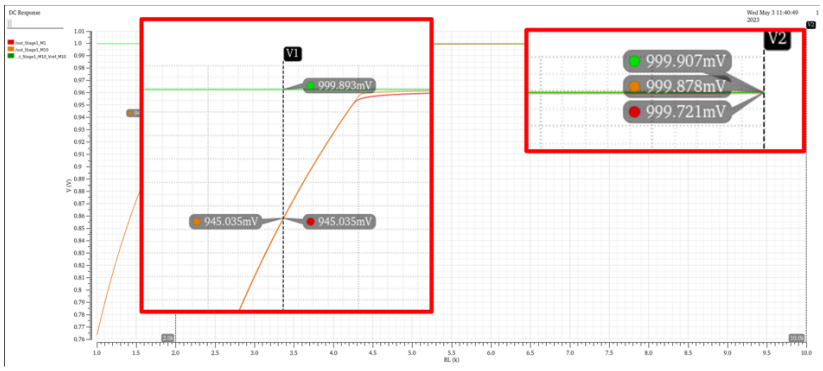


Figure.2.4 The verification of scaling the PMOS and the NMOS mention above.

In this figure, the red line is the original output voltage with the RL sweep from 1k to 10k ohms. The orange line is 10 times the original PMOS. The green line is 10 times the original NMOS based on the orange line. It is clearly verified that increasing the width of the input PMOS for differential amplification and the width of

the NMOS in the VRC circuit improves the voltage tracking accuracy. However, I do not believe that the improvements to the PMOS width have made a significant improvement to the accuracy of the output voltage. Therefore, I would keep the two-stage CMOS amplifier as the minimum size design and explore only that NMOS width design.

3. Schematic Design Analysis

The overall schematic of the VRC design is shown in Figure 3.1. I have also experimented with other designs of the circuit, such as adding a cascade current mirror to the reference current and designing the associated symbol, to make the circuit simpler. These designs are shown in Appendix 1.

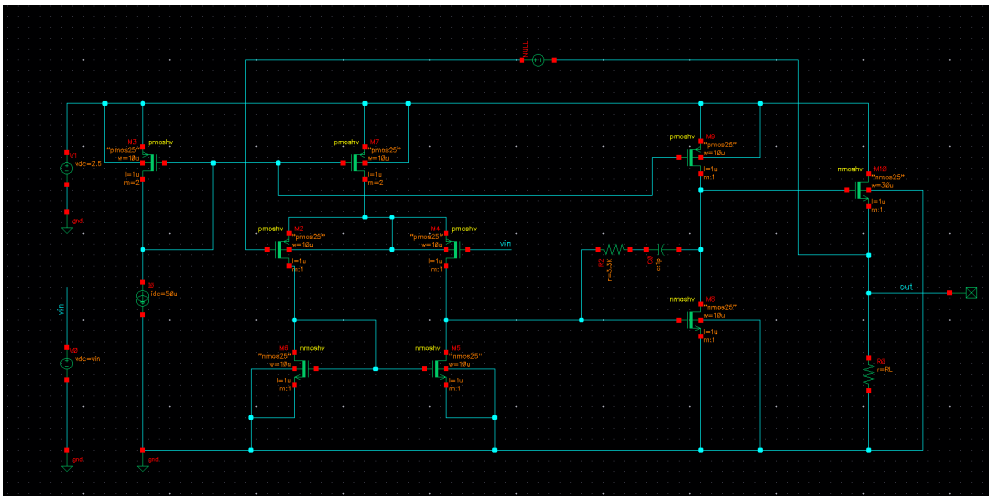


Figure.3.1 The overall schematic of VRC.

The components' parameters are shown in Table 3.1.

Table.3.1The schematic components parameters.

Components	Parameters
Vdc (V1)	2.5 V
Vdc (Vin)	1 V
idc	50 µA
Rc	3.3 k ohms
Cc	1 pF
M3/ M7 (PMOS)	length:1u, width: 10u M: 2
M2/M4/M9 (PMOS)	length:1u, width: 10u M: 1
M5/M6/M8 (NMOS)	length:1u, width: 10u M: 1
M10 (NMOS)	length:1u, width: 30u M: 1
RL	2k to 10k ohms

This circuit has been changed from the original voltage reference circuit by changing the width of M10 and adding Cc and Rc to stabilise the circuit. The design principle of Cc shows that 1pF is sufficient to compensate for this circuit. Therefore, we could use 1pF Cc directly. The Rc was analysed at 27°C in the NN process, and the transconductance of GM6, i.e., M8, was found to be approximately 304.88 µA/V by DC sweep analysis.

Therefore, we could estimate the Rc, which is approximately 3.28k ohms. In practical applications, we often use nominal resistance values for circuit design. Therefore, I would use a nominal resistance of 3.3k ohms here. As for M10 width, M10 is the NMOS mentioned in chapter 2 that requires a change of area in the VRC circuit. Its width is set to 30u. This width is designed to meet the design requirement of an output voltage error of less than 0.17%. The following is a detailed analysis of how to choose this width.

We need to find a width that meets the error accuracy requirements of the output voltage in all cases, so we need to find the worst possible temperature and process conditions, as shown in Figure 3.2.

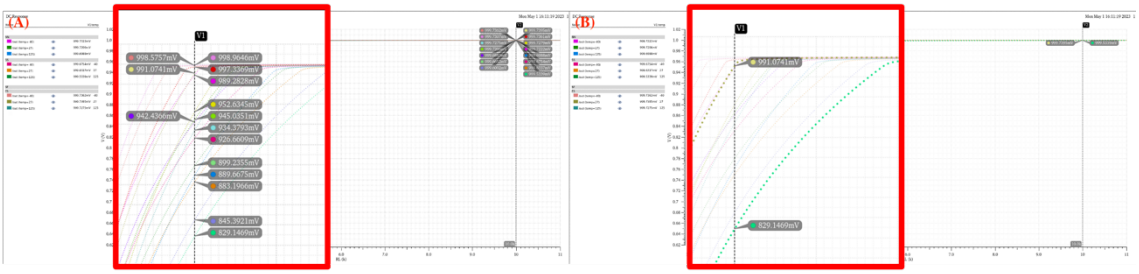


Figure.3.2 The worst temperature and process analysis. (A) is a graph of the output voltage vs. load resistance waveforms for five different processes: NN, SS, SF, FS and SS. (B) is a graph of the output voltage vs. load resistance waveforms for five different temperatures: -40°C, 27°C, 125°C.

As shown above, the worst conditions we find are the SS process and the 125°C case. The next step will be to traverse the width of the corresponding NMOS in this case to find a suitable width to meet the design error requirements, as shown in Figure 3.3.

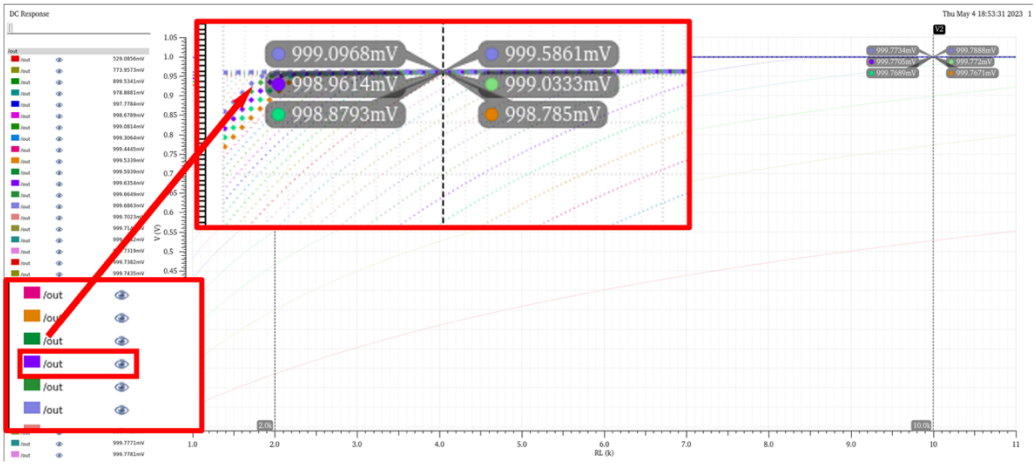


Figure.3.3 The sweep of the NMOS width at the SS process and the 125°C.

In this figure, we could see that the 30u is a good choice, and tracking accuracy error (TAE) could be calculated by the following equation:

$$TAE = \left(\frac{V_{ref} - V_{out}}{V_{ref}}\right) \times 100\% = \left(\frac{1 - 998.9614\text{mv}}{1}\right) \times 100\% = 0.1039\% \qquad (3.1)$$

The result of TAE is below 0.17%, which means that this width meets design needs. However, if we keep increasing the width of the NMOS to 50u, we could get a more accurate TAE, as shown in the following equation:

$$TAE = \left(\frac{1 - 999.0968\text{mv}}{1}\right) \times 100\% = 0.0903\% \quad (3.2)$$

If we keep increasing the width of the NMOS, the result will also be better. This means that I found the method to get a smaller TAE. Although in some applications a more precise design and a larger PMOS design are required, in this experiment I designed a circuit that wanted to guarantee a certain size and power consumption. Therefore, I chose an NMOS width that is an integer multiple of ten and has a low TAE as a schematic for the next chapter's analysis.

4. Single DC Operation and DC Sweep Analysis

4.1 Single DC Operation

From the above preliminary analysis of the output voltage of the RL, the output of the RL at 2k tends to be the worst-case, so set the RL to a constant value of 2k ohms. Figure 4.1 shows the single DC operating point and annotated node voltages. When RL is 2k ohms, the temperature at 27°C, the process at NN. The DC operating point and node voltages in this figure show that the voltage at the output point is 999.64mv, which meets the TA requirement. In addition, it is obvious that the GM6 used for the analysis in chapter 2 could also be obtained from this figure.

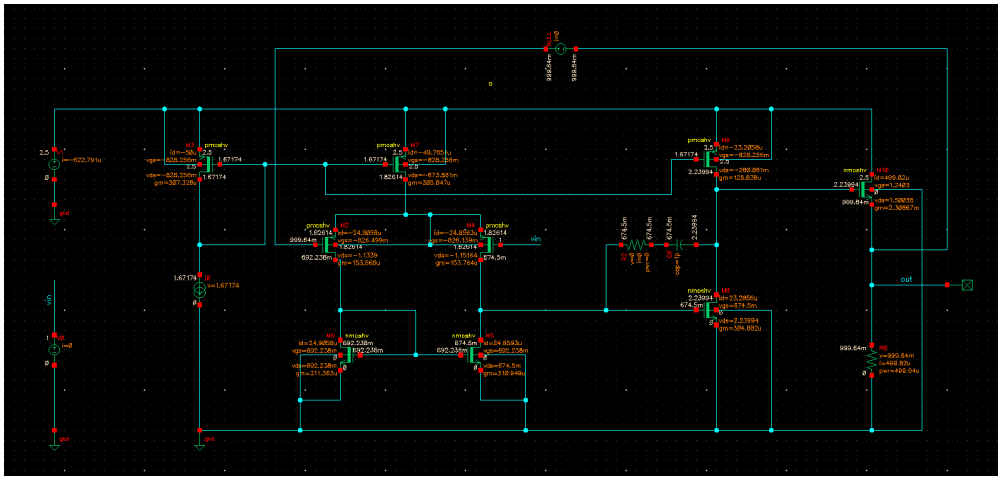


Figure.4.1 Single DC operating point and annotated node voltages on the schematic.

4.2 DC Sweep Analysis

Afterwards, based on this circuit, DC sweep analysis could be performed to analyse the output voltage waveform and the waveform of the current flow into the RL at the NN process and at 27°C. Those waveforms are shown in Figure 4.2.

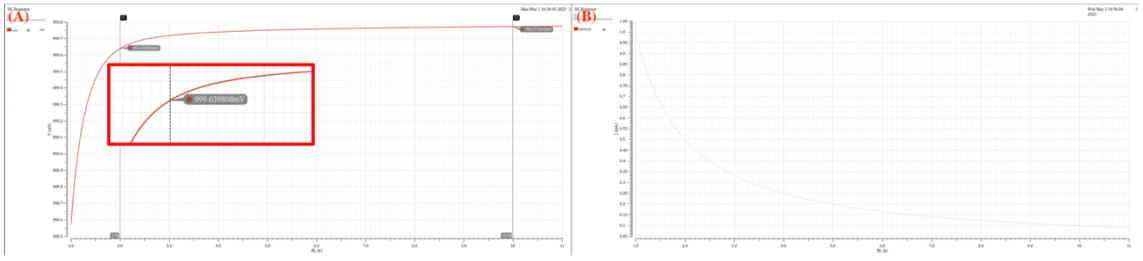


Figure.4.2 The RL voltage and current waveform at the NN process and the 27°C. (A) is the output voltage waveform that sweeps with the RL. (B) is the current flow into the RL waveform that sweeps with the RL

This figure shows the RL sweeps from 1k ohms to 11k ohms. As above, 2k ohms is the worst case. The output voltage is 999.6398mv when the RL is 2k ohms. The maximum TAE could be calculated as follows:

$$TAE = \left(\frac{1 - 999.6398\text{mv}}{1}\right) \times 100\% = 0.0360\% \tag{4.1}$$

Therefore, at the NN process and the 27°C case, the TAE is small enough to meet the design accuracy requirements. Additionally, the relationship between the output current of RL and the value of RL could be easily inferred from Ohm's law.

5. Circuit Stability Analysis

In the design principles section, I have calculated the Miller capacitor through theoretical analysis and found a suitable value for the nominal resistance in series with the Miller capacitor to significantly improve the stability of the system. This chapter will focus on the stability simulation of this circuit. We begin by analysing the original circuit without any stability optimisation, as shown in Figure 5.1.

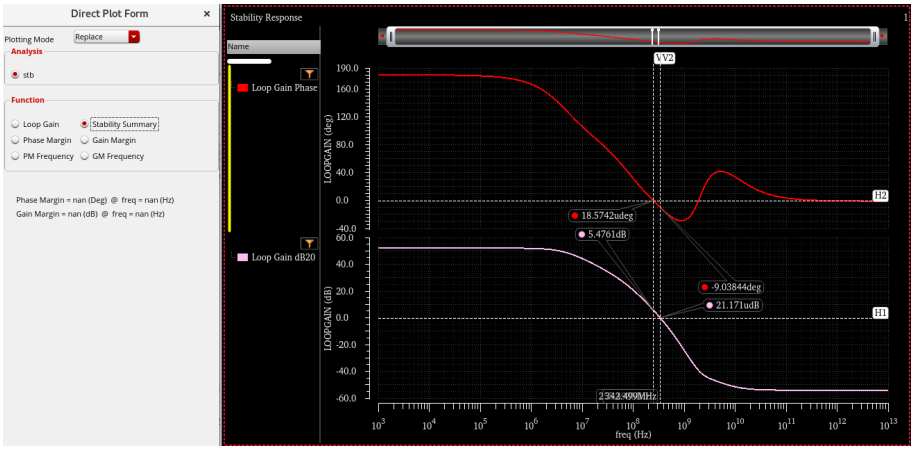


Figure.5.1 The phase margin and the loop gain (in 20 dB) waveform without stability circuit.

It is clear to see that the circuit is not stable because of the positive gain margin at 0 degree of phase margin, and the small and negative phase margin at 0 dB of gain margin. This could also be verified by the stability summary, where the NAN is shown in the stability results. Subsequently, a Miller capacitor is added to the circuit, and the stability waveform is shown in Figure 5.2.

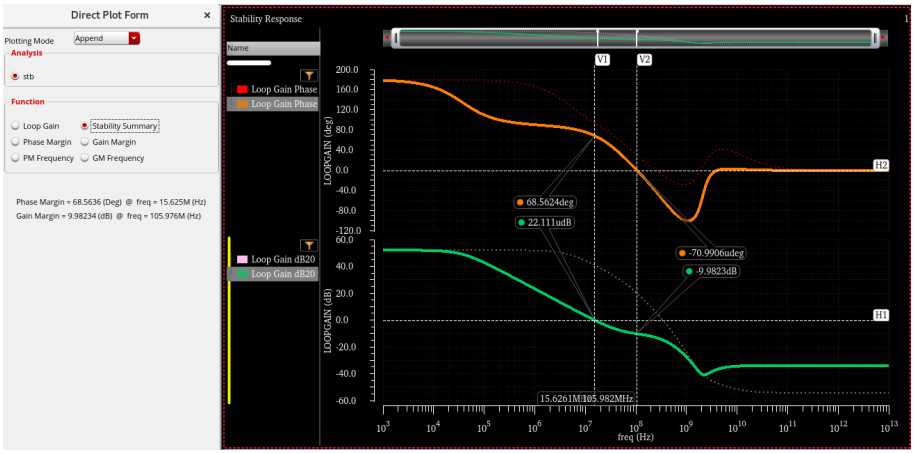


Figure.5.2 The phase margin and the loop gain (in 20 dB) waveform with a Miller capacitor.

In this circuit, the Miller capacitor helps a lot to improve the stability of the circuit. There is a 68.5624 degrees phase margin when the loop gain comes to zero. This phase margin is really great. It is not too high to make the system slow, and it is not too low that, although there are noise, disturbances, or non-linearity situations, the system could maintain the expected performance. In most cases, circuits are designed to have a phase margin between 80 degrees and 90 degrees. Therefore, we need to add a resistor to move the frequency response zero to infinity, thus increasing the phase margin even further. For the selection of this resistor, we could sweep the resistor values to select the desired resistance range, as shown in Figure 5.3 and Figure 5.4.

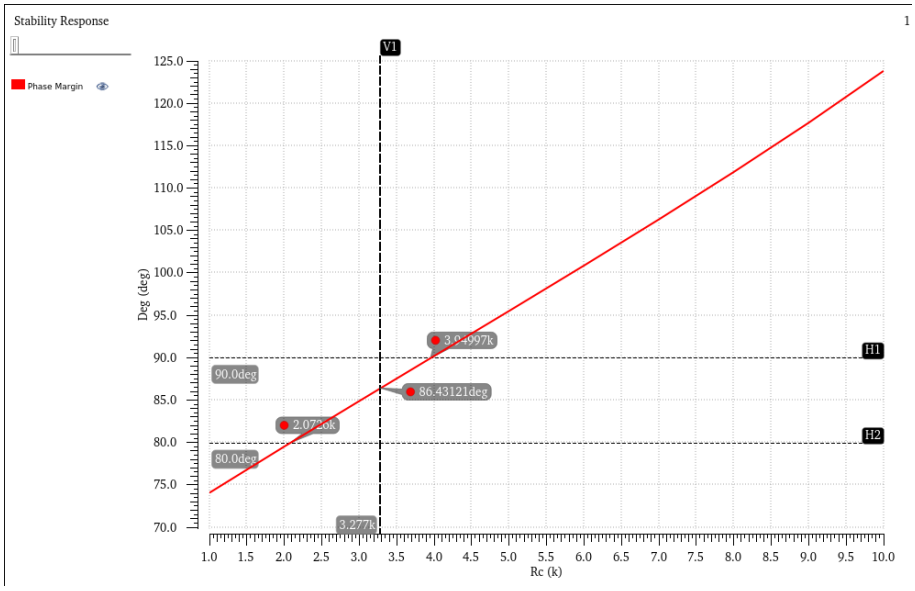


Figure.5.3 The Rc and phase margin waveforms.

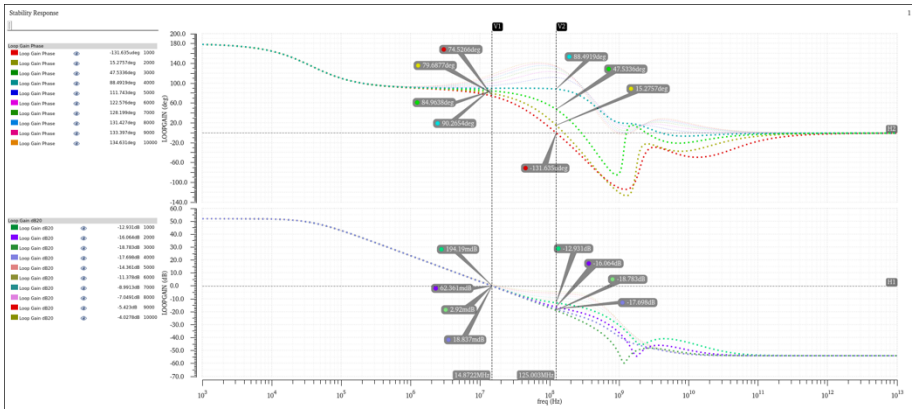


Figure.5.4. The stability analysis waveform of phase margin and loop gain.

In this figure, when the Rc value is between 2.0726k ohms to 3.9500k ohms, the phase margin could reach between 80 degrees and 90 degrees. Through the above simulations, the correctness of the previous theoretical analysis is verified again. It is further shown that the use of a 3.3k ohms series resistor leads to the desired phase margin range. Therefore, Figure 5.5 below shows the Miller capacitance stabilisation analysis waveform with the addition of a series resistor.

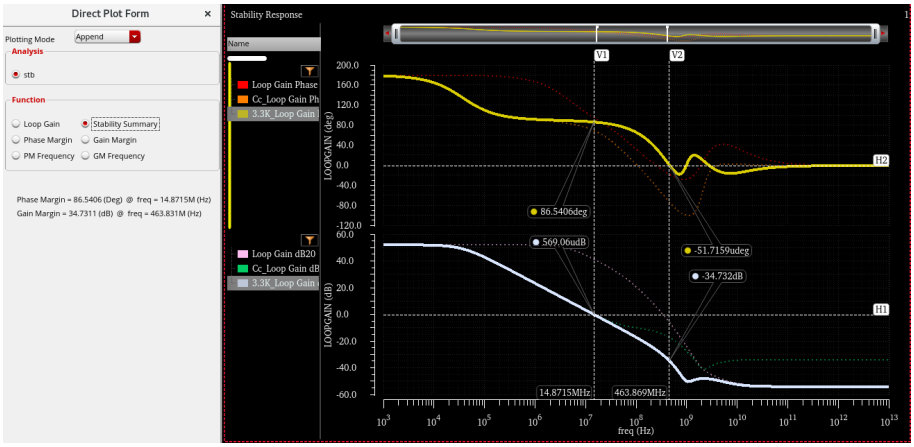


Figure.5.5 The phase margin and the loop gain (in 20 dB) waveform with a Miller capacitor and a series resistor.

In Figure 5.5, the phase margin has increased to 86.5406 degrees. Meanwhile, the gain margin has increased to 34.7311 dB. These margins provide significant stability for the whole system instead of an unstable or slowing system.

6. System Analysis with System Temperature and Process Variations

The tracking voltage accuracy and robustness of all size and component parameters of the system for the NN process and 27°C have been analysed. However, in this chapter, some more detailed simulations and analysis would be carried out. Analogue circuit design requires a trade-off where we need to balance the stability of the system with the performance of the system. This means that if we use a larger size MOSFET, it will not only affect the tracking accuracy but also have a significant impact on the stability. The related influence is shown in Figure 6.1.

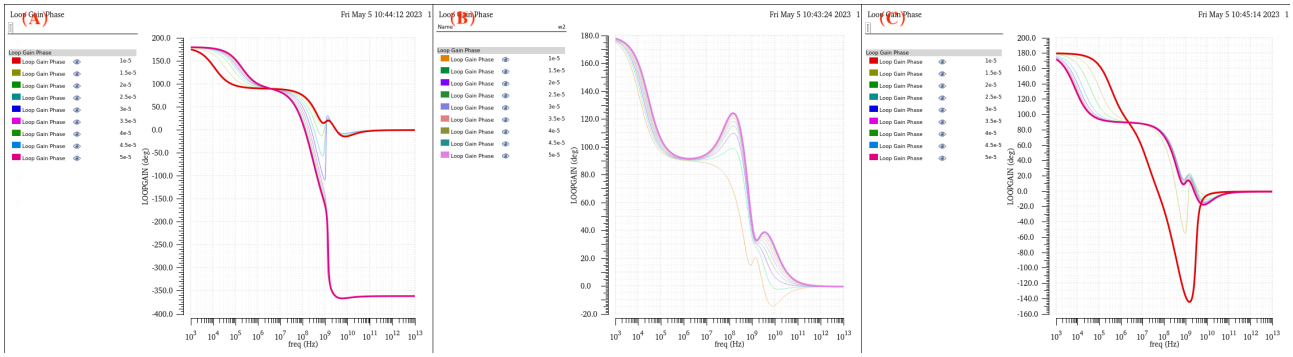


Figure.6.1 The phase margin waveform with different width sweeping. (A) sweep with the differential amplifier PMOS width. (B) sweep with the stage 2 PMOS width. (C) sweep with the VRC NMOS width.

This figure shows that if we increase the differential amplifier PMOS width, the performance would decrease very quickly, which would influence the performance and response speed of the whole system. Therefore, if I kept the width at 10 u, this would not happen. If we increase the stage 2 PMOS width, the phase margin does not have too much variation. Therefore, 10u is also a good choice because it has low power consumption. It is

the same when sweeping the VRC NMOS width. If the width is very large at a certain frequency, the performance and response speed would be very poor. Therefore, the use of the smallest possible NMOS width will give the system excellent response over a wide range of frequencies while still meeting the voltage reference accuracy. This phase margin analysis further validates the correctness of our choice of parameters. Thus, I will then make a final statement on the accuracy and stability of the output of the whole system based on the five process levels of NN, SS, SF, FS, and FF, and the characteristic temperatures of -40°C, 27°C, and 125°C. As a result, we got 15 cases of this simulation [3]. Firstly, I did a DC sweep of the temperature at the NN process, as shown in Figure 6.2.

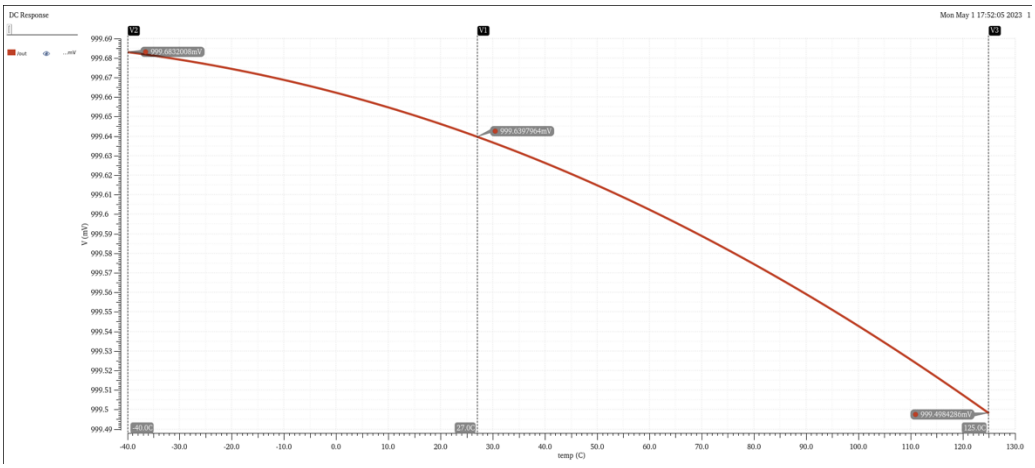


Figure.6.2 The output voltage sweeps with the temperature from -40°C to 125°C.

This figure shows that, the output voltage is accurate enough when the temperature variation from -40°C to 125°C, which is the full-range industrial testing criteria. Subsequently, I analysed whether the TAE of the output voltages meet design requirement is these 15 cases, as is shown in Figure 6.3.

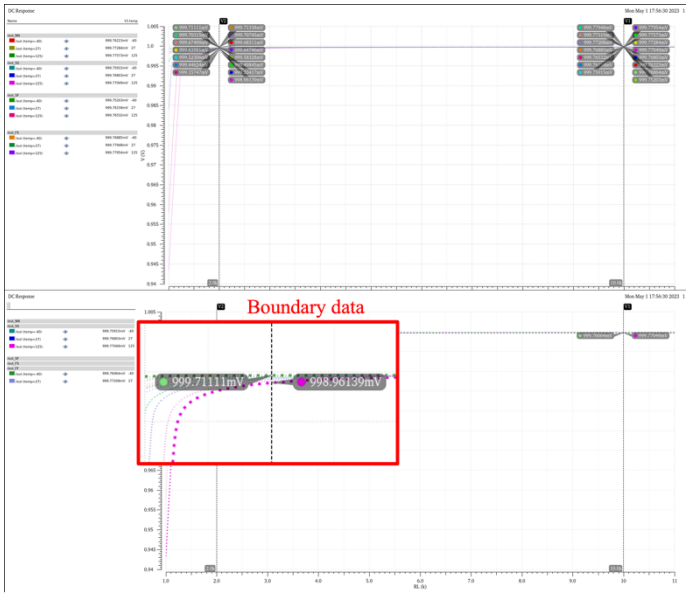


Figure.6.3 The DC sweeps with the RL value from 1k to 11k at 15 cases.

In this figure, if the worst-case boundary data is accurate enough, then we could assume that the system meets the design requirements under any operating condition and manufacturing regulations. In this system, the worst-case is the process at SS and the temperature at 125°C. This TAE value is the same as 0.1039% that was calculated in chapter 2. In addition, this means that the previous analysis is entirely correct. The final step of this analysis is to analyse the loop gain margin (in 20 dB) and phase margin for these 15 cases to analyse the stability of the system. Again, the system is analysed for stability at the worst-case boundary, where there are two boundaries, one for the SS process, 125 °C., and one for the FF process, -40 °C, as is shown in Figure 6.4 and Figure 6.5.

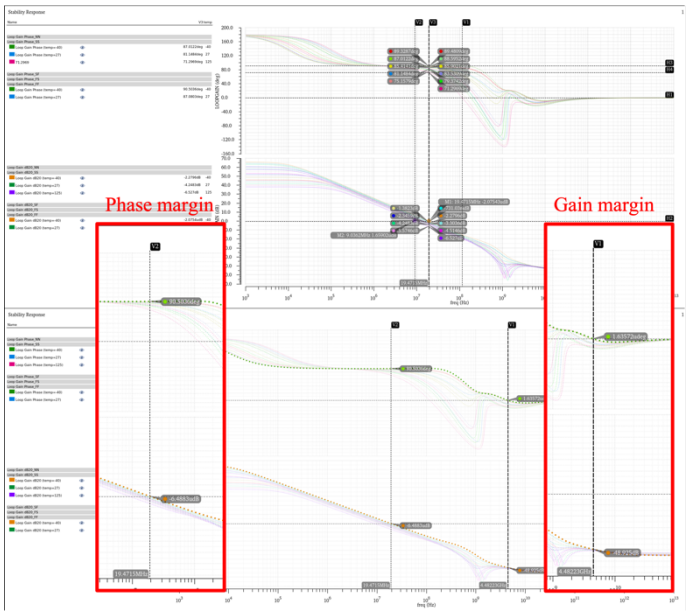


Figure.6.4 The phase margin and the loop gain (in 20 dB) waveform of boundary one.

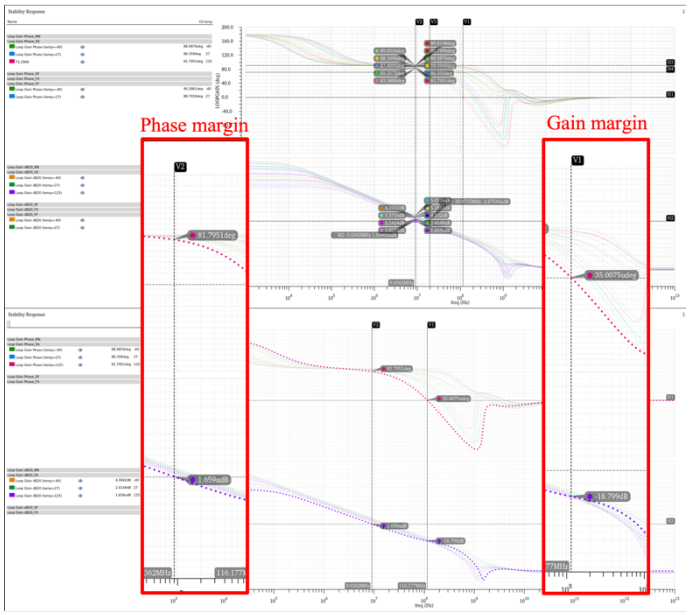


Figure.6.5 The phase margin and the loop gain (in 20 dB) waveform of boundary two.

In those figures, there is an excellent phase margin and gain margin, which could promise a stable system for this circuit. The above analysis shows very well that the system is stable under all operating conditions and manufacturing regulations. The stability summary table could also infer this conclusion to be verified again, but it is not placed here because there is too much data in the table.

7. Conclusion

This coursework has designed a VRC that could achieve a maximum voltage tracking accuracy of 0.0289% and a minimum voltage tracking accuracy of 0.1039%, which fully meets the design target of 0.17% for voltage tracking. The system is also very well analysed for stability, making it possible to meet the requirements for tracking accuracy and stability in all operating conditions and manufacturing regulations. In summary, this coursework was a success.

8. Project Repository

I have written a shell file, called "auto_aicd.sh," for the quick launch of Cadence, so that other students could quickly launch the corresponding libraries and applications. All the source files are on GitHub. Here is the link:

https://github.com/alfredzhang98/Bristol_ACID_lab.git

Reference

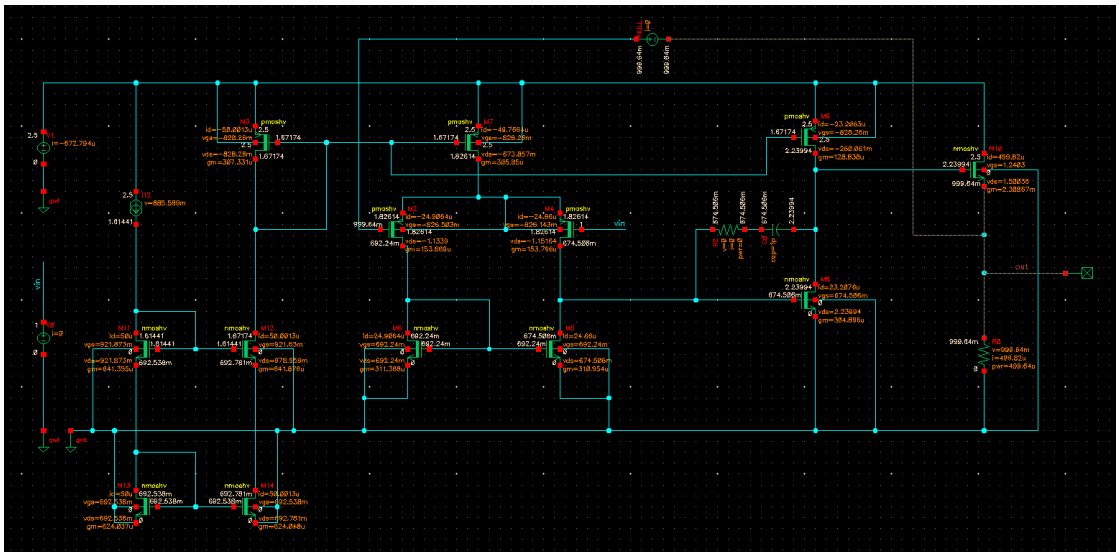
[1] M.-C. Lee and S.-Q. Hong, 'Design and implementation of a voltage-controlled oscillator with bandgap voltage reference source and temperature sensing', in *2017 International Conference on Green Energy and Applications (ICGEA)*, Mar. 2017, pp. 39–45. doi: 10.1109/ICGEA.2017.7925452.

[2] 'A programmable voltage reference optimized for power management applications | Proceedings of the 20th annual conference on Integrated circuits and systems design'. https://dl.acm.org/doi/abs/10.1145/1284480.1284498 (accessed May 05, 2023).

[3] P. E. Allen, R. Dobkin, and D. R. Holberg, *CMOS Analog Circuit Design*. Elsevier, 2011.

Appendix 1 - Topology Circuits

This topology circuit, which adds a cascade current mirror to the reference current.



This topology circuit implements the VCVS circuit by using symbols, which perform the same functions as those described in the main text.