File: f:/project345/src/alu.vhd (/file_io_tb/UUT/u3)

```
1
2     library ieee;
3     use ieee.std_logic_1164.all;
4     use ieee.numeric_std.all;
5     --use ieee.std_logic_arith.all;
6
7     entity alu is
8         port(
9         r1: in std_logic_vector(127 downto 0);
10        r2: in std_logic_vector(127 downto 0);
11        r3: in std_logic_vector(127 downto 0);
12        ins: in std_logic_vector(24 downto 0);
13        clk : in std_logic;
14        ins_out: out std_logic_vector(24 downto 0);
15        alu_out: out std_logic_vector(127 downto 0)
16        );
17    end alu;
18
19    architecture behavioral of alu is
20    begin
21        process(r1, r2, r3, ins,clk)
22            variable temp1, temp2: std_logic_vector(31 downto 0);
23            variable temp3, temp4: std_logic_vector(63 downto 0);
24            variable zero count : integer;
25            variable one_count : integer;
26            variable bits_of_shift : integer;
27        begin
28            if rising_edge(clk) then
29
30            ins_out<=ins;
31
32            ------------------4.1 load imm instruction-------------------------
33            if ins(24) = '0' then
34                if ins(23 downto 21) = "000" then
35                alu out <= r1;
36                alu out(15 downto 0) <= ins(20 downto 5);
37                elsif ins(23 downto 21) = "001" then
38                alu_out <= r1;
39                alu_out(31 downto 16) <= ins(20 downto 5);
40                elsif ins(23 downto 21) = "010" then
41                alu_out <= r1;
42                alu_out(47 downto 32) <= ins(20 downto 5);
43                elsif ins(23 downto 21) = "011" then
44                alu out <= r1;
45                alu out(63 downto 48) <= ins(20 downto 5);
46                elsif ins(23 downto 21) = "100" then
47                alu out <= r1;
48                alu out(79 downto 64) <= ins(20 downto 5);
49                elsif ins(23 downto 21) = "101" then
50                alu_out <= r1;
51                alu_out(95 downto 80) <= ins(20 downto 5);
52                elsif ins(23 downto 21) = "110" then
53                alu_out <= r1;
54                alu_out(111 downto 96) <= ins(20 downto 5);
55                elsif ins(23 downto 21) = "111" then
56                alu out <= r1;
57                alu out(127 downto 112) <= ins(20 downto 5);
58                end if;
59
60            ------------------4.2 R4 instruction--------------------------
61            -----------saturation??
62                elsif ins(24 downto 23) = "10" then
63
64                    case ins(22 downto 20) is
65                        -----Signed Integer Multiply-Add Low with
      Saturation------------------
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```
66                          when "000" =>
67                          temp1:=std_logic_vector(signed(r2(111 downto 96))* signed(r3(111
    downto 96)));
68                          temp2:=std_logic_vector(signed(temp1) + signed(r1(127 downto 96)));
69                          if temp2(31)='1' and temp1(31)='0' and r1(127)='0' then
70                              alu_out(127 downto 96)<=(others=>'1');
71                              alu_out(127)<='0';
72                          elsif temp2(31)='0' and temp1(31)='1' and r1(127)='1' then
73                              alu_out(127 downto 96)<=(others=>'0');
74                              alu_out(127)<='1';
75                          else
76                              alu_out(127 downto 96)<=temp2;
77                          end if;
78
79                          temp1:=std_logic_vector(signed(r2(79 downto 64))* signed(r3(79
    downto 64)));
80                          temp2:=std_logic_vector(signed(temp1) + signed(r1(95 downto 64)));
81                          if temp2(31)='1' and temp1(31)='0' and r1(95)='0' then
82                              alu_out(95 downto 64)<=(others=>'1');
83                              alu_out(95)<='0';
84                          elsif temp2(31)='0' and temp1(31)='1' and r1(95)='1' then
85                              alu_out(95 downto 64)<=(others=>'0');
86                              alu_out(95)<='1';
87                          else
88                              alu_out(95 downto 64)<=temp2;
89                          end if;
90
91                          temp1:=std_logic_vector(signed(r2(47 downto 32))* signed(r3(47
    downto 32)));
92                          temp2:=std_logic_vector(signed(temp1) + signed(r1(63 downto 32)));
93                          if temp2(31)='1' and temp1(31)='0' and r1(63)='0' then
94                              alu_out(63 downto 32)<=(others=>'1');
95                              alu_out(63)<='0';
96                          elsif temp2(31)='0' and temp1(31)='1' and r1(63)='1' then
97                              alu_out(63 downto 32)<=(others=>'0');
98                              alu_out(63)<='1';
99                          else
100                             alu_out(63 downto 32)<=temp2;
101                         end if;
102
103                         temp1:=std_logic_vector(signed(r2(15 downto 0))* signed(r3(15 downto
    0)));
104                         temp2:=std_logic_vector(signed(temp1) + signed(r1(31 downto 0)));
105                         if temp2(31)='1' and temp1(31)='0' and r1(31)='0' then
106                             alu_out(31 downto 0)<=(others=>'1');
107                             alu_out(31)<='0';
108                         elsif temp2(31)='0' and temp1(31)='1' and r1(31)='1' then
109                             alu_out(31 downto 0)<=(others=>'0');
110                             alu_out(31)<='1';
111                         else
112                             alu_out(31 downto 0)<=temp2;
113                         end if;
114                         --------Signed Integer Multiply-Add High with
    Saturation----------------
115                         when "001" =>
116                         temp1:=std_logic_vector(signed(r2(127 downto 112))* signed(r3(127
    downto 112)));
117                         temp2:=std_logic_vector(signed(temp1) + signed(r1(127 downto 96)));
118                         if temp2(31)='1' and temp1(31)='0' and r1(127)='0' then
119                             alu_out(127 downto 96)<=(others=>'1');
120                             alu_out(127)<='0';
121                         elsif temp2(31)='0' and temp1(31)='1' and r1(127)='1' then
122                             alu_out(127 downto 96)<=(others=>'0');
123                             alu_out(127)<='1';
124                         else
125                             alu_out(127 downto 96)<=temp2;
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126                         end if;
127
128                         temp1:=std_logic_vector(signed(r2(95 downto 80))* signed(r3(95
    downto 80)));
129                         temp2:=std_logic_vector(signed(temp1) + signed(r1(95 downto 64)));
130                         if temp2(31)='1' and temp1(31)='0' and r1(95)='0' then
131                             alu_out(95 downto 64)<=(others=>'1');
132                             alu_out(95)<='0';
133                         elsif temp2(31)='0' and temp1(31)='1' and r1(95)='1' then
134                             alu_out(95 downto 64)<=(others=>'0');
135                             alu_out(95)<='1';
136                         else
137                             alu_out(95 downto 64)<=temp2;
138                         end if;
139
140                         temp1:=std_logic_vector(signed(r2(63 downto 48))* signed(r3(63
    downto 48)));
141                         temp2:=std_logic_vector(signed(temp1) + signed(r1(63 downto 32)));
142                         if temp2(31)='1' and temp1(31)='0' and r1(63)='0' then
143                             alu_out(63 downto 32)<=(others=>'1');
144                             alu_out(63)<='0';
145                         elsif temp2(31)='0' and temp1(31)='1' and r1(63)='1' then
146                             alu_out(63 downto 32)<=(others=>'0');
147                             alu_out(63)<='1';
148                         else
149                             alu_out(63 downto 32)<=temp2;
150                         end if;
151
152                         temp1:=std_logic_vector(signed(r2(31 downto 16))* signed(r3(31
    downto 16)));
153                         temp2:=std_logic_vector(signed(temp1) + signed(r1(31 downto 0)));
154                         if temp2(31)='1' and temp1(31)='0' and r1(31)='0' then
155                             alu_out(31 downto 0)<=(others=>'1');
156                             alu_out(31)<='0';
157                         elsif temp2(31)='0' and temp1(31)='1' and r1(31)='1' then
158                             alu_out(31 downto 0)<=(others=>'0');
159                             alu_out(31)<='1';
160                         else
161                             alu_out(31 downto 0)<=temp2;
162                         end if;
163                         ----------Signed Integer Multiply-Subtract Low with
    Saturation-------------
164                         when "010" =>
165                         temp1:=std_logic_vector(signed(r2(111 downto 96))*signed(r3(111
    downto 96)));
166                         temp2:=std_logic_vector(signed(r1(127 downto 96))-signed(temp1));
167                         if temp2(31)='1' and temp1(31)='1' and r1(127)='0' then
168                             alu_out(127 downto 96)<=(others=>'1');
169                             alu_out(127)<='0';
170                         elsif temp2(31)='0' and temp1(31)='0' and r1(127)='1' then
171                             alu_out(127 downto 96)<=(others=>'0');
172                             alu_out(127)<='1';
173                         else
174                             alu_out(127 downto 96)<=temp2;
175                         end if;
176
177                         temp1:=std_logic_vector(signed(r2(79 downto 64))* signed(r3(79
    downto 64)));
178                         temp2:=std_logic_vector(signed(r1(95 downto 64)) - signed(temp1));
179                         if temp2(31)='1' and temp1(31)='1' and r1(95)='0' then
180                             alu_out(95 downto 64)<=(others=>'1');
181                             alu_out(95)<='0';
182                         elsif temp2(31)='0' and temp1(31)='0' and r1(95)='1' then
183                             alu_out(95 downto 64)<=(others=>'0');
184                             alu_out(95)<='1';
185                         else
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186                         alu_out(95 downto 64)<=temp2;
187                     end if;
188
189                     temp1:=std_logic_vector(signed(r2(47 downto 32))* signed(r3(47
    downto 32)));
190                     temp2:=std_logic_vector(signed(r1(63 downto 32)) - signed(temp1));
191                     if temp2(31)='1' and temp1(31)='1' and r1(63)='0' then
192                         alu_out(63 downto 32)<=(others=>'1');
193                         alu_out(63)<='0';
194                     elsif temp2(31)='0' and temp1(31)='0' and r1(63)='1' then
195                         alu_out(63 downto 32)<=(others=>'0');
196                         alu_out(63)<='1';
197                     else
198                         alu_out(63 downto 32)<=temp2;
199                     end if;
200
201                     temp1:=std_logic_vector(signed(r2(15 downto 0))* signed(r3(15 downto
    0)));
202                     temp2:=std_logic_vector(signed(r1(31 downto 0)) - signed(temp1));
203                     if temp2(31)='1' and temp1(31)='1' and r1(31)='0' then
204                         alu_out(31 downto 0)<=(others=>'1');
205                         alu_out(31)<='0';
206                     elsif temp2(31)='0' and temp1(31)='0' and r1(31)='1' then
207                         alu_out(31 downto 0)<=(others=>'0');
208                         alu_out(31)<='1';
209                     else
210                         alu_out(31 downto 0)<=temp2;
211                     end if;
212
213                     ----------Signed Integer Multiply-Subtract High with
    Saturation-------------
214                     when "011" =>
215                     temp1:=std_logic_vector(signed(r2(127 downto 112))* signed(r3(127
    downto 112)));
216                     temp2:=std_logic_vector(signed(r1(127 downto 96)) - signed(temp1));
217                     if temp2(31)='1' and temp1(31)='1' and r1(127)='0' then
218                         alu_out(127 downto 96)<=(others=>'1');
219                         alu_out(127)<='0';
220                     elsif temp2(31)='0' and temp1(31)='0' and r1(127)='1' then
221                         alu_out(127 downto 96)<=(others=>'0');
222                         alu_out(127)<='1';
223                     else
224                         alu_out(127 downto 96)<=temp2;
225                     end if;
226
227                     temp1:=std_logic_vector(signed(r2(95 downto 80))* signed(r3(95
    downto 80)));
228                     temp2:=std_logic_vector(signed(r1(95 downto 64)) - signed(temp1));
229                     if temp2(31)='1' and temp1(31)='1' and r1(95)='0' then
230                         alu_out(95 downto 64)<=(others=>'1');
231                         alu_out(95)<='0';
232                     elsif temp2(31)='0' and temp1(31)='0' and r1(95)='1' then
233                         alu_out(95 downto 64)<=(others=>'0');
234                         alu_out(95)<='1';
235                     else
236                         alu_out(95 downto 64)<=temp2;
237                     end if;
238
239                     temp1:=std_logic_vector(signed(r2(63 downto 48))* signed(r3(63
    downto 48)));
240                     temp2:=std_logic_vector(signed(r1(63 downto 32)) - signed(temp1));
241                     if temp2(31)='1' and temp1(31)='1' and r1(63)='0' then
242                         alu_out(63 downto 32)<=(others=>'1');
243                         alu_out(63)<='0';
244                     elsif temp2(31)='0' and temp1(31)='0' and r1(63)='1' then
245                         alu_out(63 downto 32)<=(others=>'0');
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```
246                         alu_out(63)<='1';
247                     else
248                         alu_out(63 downto 32)<=temp2;
249                     end if;
250
251                     temp1:=std_logic_vector(signed(r2(31 downto 16))* signed(r3(31
    downto 16)));
252                     temp2:=std_logic_vector(signed(r1(31 downto 0)) - signed(temp1));
253                     if temp2(31)='1' and temp1(31)='1' and r1(31)='0' then
254                         alu_out(31 downto 0)<=(others=>'1');
255                         alu_out(31)<='0';
256                     elsif temp2(31)='0' and temp1(31)='0' and r1(31)='1' then
257                         alu_out(31 downto 0)<=(others=>'0');
258                         alu_out(31)<='1';
259                     else
260                         alu_out(31 downto 0)<=temp2;
261                     end if;
262
263                     ---------Signed Long Integer Multiply-Add Low with
    Saturation--------------
264                     when "100" =>
265                     temp3:=std_logic_vector(signed(r2(95 downto 64))* signed(r3(95
    downto 64)));
266                     temp4:=std_logic_vector(signed(temp3) + signed(r1(127 downto 64)));
267                     if temp4(63)='1' and temp3(63)='0' and r1(127)='0' then
268                         alu_out(127 downto 64)<=(others=>'1');
269                         alu_out(127)<='0';
270                     elsif temp4(63)='0' and temp3(63)='1' and r1(127)='1' then
271                         alu_out(127 downto 64)<=(others=>'0');
272                         alu_out(127)<='1';
273                     else
274                         alu_out(127 downto 64)<=temp4;
275                     end if;
276
277                     temp3:=std_logic_vector(signed(r2(31 downto 0))* signed(r3(31 downto
    0)));
278                     temp4:=std_logic_vector(signed(temp3) + signed(r1(63 downto 0)));
279                     if temp4(63)='1' and temp3(63)='0' and r1(63)='0' then
280                         alu_out(63 downto 0)<=(others=>'1');
281                         alu_out(63)<='0';
282                     elsif temp4(63)='0' and temp3(63)='1' and r1(63)='1' then
283                         alu_out(63 downto 0)<=(others=>'0');
284                         alu_out(63)<='1';
285                     else
286                         alu_out(63 downto 0)<=temp4;
287                     end if;
288                     ----------Signed Long Integer Multiply-Add High with
    Saturation-----------
289                     when "101" =>
290                         temp3:=std_logic_vector(signed(r2(127 downto 96))* signed(r3(127
    downto 96)));
291                     temp4:=std_logic_vector(signed(temp3) + signed(r1(127 downto 64)));
292                     if temp4(63)='1' and temp3(63)='0' and r1(127)='0' then
293                         alu_out(127 downto 64)<=(others=>'1');
294                         alu_out(127)<='0';
295                     elsif temp4(63)='0' and temp3(63)='1' and r1(127)='1' then
296                         alu_out(127 downto 64)<=(others=>'0');
297                         alu_out(127)<='1';
298                     else
299                         alu_out(127 downto 64)<=temp4;
300                     end if;
301
302                     temp3:=std_logic_vector(signed(r2(63 downto 32))* signed(r3(63
    downto 32)));
303                     temp4:=std_logic_vector(signed(temp3) + signed(r1(63 downto 0)));
304                     if temp4(63)='1' and temp3(63)='0' and r1(63)='0' then
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305                         alu_out(63 downto 0)<=(others=>'1');
306                         alu_out(63)<='0';
307                     elsif temp4(63)='0' and temp3(63)='1' and r1(63)='1' then
308                         alu_out(63 downto 0)<=(others=>'0');
309                         alu_out(63)<='1';
310                     else
311                         alu out(63 downto 0)<=temp4;
312                     end if;
313                     ----------Signed Long Integer Multiply-Subtract Low with
    Saturation----------
314                     when "110" =>
315                     temp3:=std_logic_vector(signed(r2(95 downto 64))* signed(r3(95
    downto 64)));
316                     temp4:=std_logic_vector(signed(r1(127 downto 64))- signed(temp3));
317                     if temp4(63)='1' and temp3(63)='1' and r1(127)='0' then
318                         alu_out(127 downto 64)<=(others=>'1');
319                         alu_out(127)<='0';
320                     elsif temp4(63)='0' and temp3(63)='0' and r1(127)='1' then
321                         alu out(127 downto 64)<=(others=>'0');
322                         alu out(127)<='1';
323                     else
324                         alu out(127 downto 64)<=temp4;
325                     end if;
326
327                     temp3:=std_logic_vector(signed(r2(31 downto 0))* signed(r3(31 downto
    0)));
328                     temp4:=std_logic_vector(signed(r1(63 downto 0))-signed(temp3));
329                     if temp4(63)='1' and temp3(63)='1' and r1(63)='0' then
330                         alu_out(63 downto 0)<=(others=>'1');
331                         alu_out(63)<='0';
332                     elsif temp4(63)='0' and temp3(63)='0' and r1(63)='1' then
333                         alu out(63 downto 0)<=(others=>'0');
334                         alu out(63)<='1';
335                     else
336                         alu out(63 downto 0)<=temp4;
337                     end if;
338                     ----------Signed Long Integer Multiply-Subtract High with
    Saturation----------
339                     when "111" =>
340                     temp3:=std_logic_vector(signed(r2(127 downto 96))* signed(r3(127
    downto 96)));
341                     temp4:=std_logic_vector(signed(r1(127 downto 64))- signed(temp3));
342                     if temp4(63)='1' and temp3(63)='1' and r1(127)='0' then
343                         alu out(127 downto 64)<=(others=>'1');
344                         alu out(127)<='0';
345                     elsif temp4(63)='0' and temp3(63)='0' and r1(127)='1' then
346                         alu out(127 downto 64)<=(others=>'0');
347                         alu out(127)<='1';
348                     else
349                         alu_out(127 downto 64)<=temp4;
350                     end if;
351
352                     temp3:=std_logic_vector(signed(r2(63 downto 32))* signed(r3(63
    downto 32)));
353                     temp4:=std_logic_vector(signed(r1(63 downto 0))-signed(temp3));
354                     if temp4(63)='1' and temp3(63)='0' and r1(63)='1' then
355                         alu out(63 downto 0)<=(others=>'1');
356                         alu out(63)<='0';
357                     elsif temp4(63)='0' and temp3(63)='1' and r1(63)='0' then
358                         alu out(63 downto 0)<=(others=>'0');
359                         alu out(63)<='1';
360                     else
361                         alu_out(63 downto 0)<=temp4;
362                     end if;
363                     when others  => null;
364
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```
365                 end case;
366
367
368         ----------------4.3 R3 instruction-----------------------------------
369             elsif ins(24 downto 23) = "11" then
370             case ins(19 downto 15) is
371                 ---------NOP---------
372                 when "00000" =>  null;
373                 --------A: add word---------
374                 when "00001" =>
375                     alu_out(127 downto 96)<=std_logic_vector(unsigned(r2(127 downto 96
    ))+unsigned(r1(127 downto 96)));
376                     alu_out(95 downto 64)<=std_logic_vector(unsigned(r2(95 downto 64))+
    unsigned(r1(95 downto 64)));
377                     alu_out(63 downto 32)<=std_logic_vector(unsigned(r2(63 downto 32))+
    unsigned(r1(63 downto 32)));
378                     alu_out(31 downto 0)<=std_logic_vector(unsigned(r2(31 downto 0))+
    unsigned(r1(31 downto 0)));
379                 ----AH: add halfword--
380                 when "00010" =>
381                     alu_out(127 downto 112)<=std_logic_vector(unsigned(r2(127 downto 112
    ))+unsigned(r1(127 downto 112)));
382                     alu_out(111 downto 96)<=std_logic_vector(unsigned(r2(111 downto 96
    ))+unsigned(r1(111 downto 96)));
383                     alu_out(95 downto 80)<=std_logic_vector(unsigned(r2(95 downto 80))+
    unsigned(r1(95 downto 80)));
384                     alu_out(79 downto 64)<=std_logic_vector(unsigned(r2(79 downto 64))+
    unsigned(r1(79 downto 64)));
385                     alu_out(63 downto 48)<=std_logic_vector(unsigned(r2(63 downto 48))+
    unsigned(r1(63 downto 48)));
386                     alu_out(47 downto 32)<=std_logic_vector(unsigned(r2(47 downto 32))+
    unsigned(r1(47 downto 32)));
387                     alu_out(31 downto 16)<=std_logic_vector(unsigned(r2(31 downto 16))+
    unsigned(r1(31 downto 16)));
388                     alu_out(15 downto 0)<=std_logic_vector(unsigned(r2(15 downto 0))+
    unsigned(r1(15 downto 0)));
389                 ----AHS: add halfword saturated
390                 when "00011" =>
391                 alu_out(127 downto 112)<=std_logic_vector(signed(r2(127 downto 112)) +
    signed(r1(127 downto 112)));
392                 if alu_out(127)='1' and r2(127) = '0' and r1(127) = '0' then

393                     alu_out(127 downto 112)<=(others=>'1');
394                     alu_out(127)<='0';
395                 elsif alu_out(127) ='0' and r2(127) ='1' and r1(127)='1' then
396                     alu_out(127 downto 112)<=(others=>'0');
397                     alu_out(127)<='1';
398                 end if;
399                 alu_out(111 downto 96)<=std_logic_vector(signed(r2(111 downto 96))+
    signed(r1(111 downto 96)));
400                 if alu_out(111)='1' and r2(111) = '0' and r1(111) = '0' then

401                     alu_out(111 downto 96)<=(others=>'1');
402                     alu_out(111)<='0';
403                 elsif alu_out(111) ='0' and r2(111) ='1' and r1(111)='1' then
404                     alu_out(111 downto 96)<=(others=>'0');
405                     alu_out(111)<='1';
406                 end if;
407                 alu_out(95 downto 80)<=std_logic_vector(signed(r2(95 downto 80))+signed(
    r1(95 downto 80)));
408                 if alu_out(95)='1' and r2(95) = '0' and r1(95) = '0' then

409                     alu_out(95 downto 80)<=(others=>'1');
410                     alu_out(95)<='0';
411                 elsif alu_out(95) ='0' and r2(95) ='1' and r1(95)='1' then
412                     alu_out(95 downto 80)<=(others=>'0');
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```
413                     alu_out(95)<='1';
414                 end if;
415                 alu_out(79 downto 64)<=std_logic_vector(signed(r2(79 downto 64))+signed(
    r1(79 downto 64)));
416                 if alu_out(79)='1' and r2(79) = '0' and r1(79) = '0' then

417                     alu out(79 downto 64)<=(others=>'1');
418                     alu out(79)<='0';
419                 elsif alu out(79) ='0' and r2(79) ='1' and r1(79)='1' then
420                     alu out(79 downto 64)<=(others=>'0');
421                     alu out(79)<='1';
422                 end if;
423                 alu_out(63 downto 48)<=std_logic_vector(signed(r2(63 downto 48))+signed(
    r1(63 downto 48)));
424                 if alu_out(63)='1' and r2(63) = '0' and r1(63) = '0' then

425                     alu_out(63 downto 48)<=(others=>'1');
426                     alu_out(63)<='0';
427                 elsif alu out(63) ='0' and r2(63) ='1' and r1(63)='1' then
428                     alu out(63 downto 48)<=(others=>'0');
429                     alu out(63)<='1';
430                 end if;
431                 alu out(47 downto 32)<=std_logic_vector(signed(r2(47 downto 32))+signed(
    r1(47 downto 32)));
432                 if alu_out(47)='1' and r2(47) = '0' and r1(32) = '0' then

433                     alu_out(47 downto 32)<=(others=>'1');
434                     alu_out(47)<='0';
435                 elsif alu_out(47) ='0' and r2(47) ='1' and r1(32)='1' then
436                     alu_out(47 downto 32)<=(others=>'0');
437                     alu out(47)<='1';
438                 end if;
439                 alu out(31 downto 16)<=std_logic_vector(signed(r2(31 downto 16))+signed(
    r1(31 downto 16)));
440                 if alu out(31)='1' and r2(31) = '0' and r1(31) = '0' then

441                     alu out(31 downto 16)<=(others=>'1');
442                     alu_out(31)<='0';
443                 elsif alu_out(31) ='0' and r2(31) ='1' and r1(31)='1' then
444                     alu_out(31 downto 16)<=(others=>'0');
445                     alu_out(31)<='1';
446                 end if;
447                 alu_out(15 downto 0)<=std_logic_vector(signed(r2(15 downto 0))+signed(r1
    (15 downto 0)));
448                 if alu out(15)='1' and r2(15) = '0' and r1(15) = '0' then

449                     alu out(15 downto 0)<=(others=>'1');
450                     alu out(15)<='0';
451                 elsif alu out(15) ='0' and r2(15) ='1' and r1(15)='1' then
452                     alu_out(15 downto 0)<=(others=>'0');
453                     alu_out(15)<='1';
454                 end if;
455                 --------AND: bitwise logical and
456                 when "00100" =>
457                 alu_out <= r1 and r2;
458                 --------BCW: broadcast word
459                 when "00101" =>
460                 alu out(127 downto 96)<=r1(31 downto 0);
461                 alu out(95 downto 64)<=r1(31 downto 0);
462                 alu out(63 downto 32)<=r1(31 downto 0);
463                 alu out(31 downto 0)<=r1(31 downto 0);
464
465                 -------CLZ: count leading zeros in words
466                 when "00110" =>
467                 zero_count := 0;
468                     for i in 127 downto 96 loop
```

```
469                         if r1(i) = '0' then
470                             zero_count := zero_count+1;
471                         else
472                             exit;
473                         end if;
474                     end loop;
475                     alu_out(127 downto 96) <= std_logic_vector(to_unsigned(zero_count,32
    ));
476                     zero_count :=0;
477
478                     for i in 95 downto 64 loop
479                         if r1(i) = '0' then
480                             zero_count := zero_count+1;
481                         else
482                             exit;
483                         end if;
484                     end loop;
485                     alu_out(95 downto 64) <= std_logic_vector(to_unsigned(zero_count,32
    ));
486                     zero_count :=0;
487
488                     for i in 63 downto 32 loop
489                         if r1(i) = '0' then
490                             zero_count := zero_count+1;
491                         else
492                             exit;
493                         end if;
494                     end loop;
495                     alu_out(63 downto 32) <= std_logic_vector(to_unsigned(zero_count,32
    ));
496                     zero_count :=0;
497
498                     for i in 31 downto 0 loop
499                         if r1(i) = '0' then
500                             zero_count := zero_count+1;
501                         else
502                             exit;
503                         end if;
504                     end loop;
505                     alu_out(31 downto 0) <= std_logic_vector(to_unsigned(zero_count,32
    ));
506                     zero_count :=0;
507                 ---------MAX: max signed word
508                 when "00111" =>
509                     if signed(r1(127 downto 96)) > signed(r2(127 downto 96)) then
510                         alu_out(127 downto 96)<= r1(127 downto 96);
511                         else
512                             alu_out(127 downto 96) <= r2(127 downto 96);
513                     end if;
514
515                     if(signed(r1(95 downto 64)) > signed(r2(95 downto 64))) then
516                         alu_out(95 downto 64)<= r1(95 downto 64);
517                         else
518                             alu_out(95 downto 64) <= r2(95 downto 64);
519                     end if;
520
521                     if(signed(r1(63 downto 32)) > signed(r2(63 downto 32))) then
522                         alu_out(63 downto 32)<= r1(63 downto 32);
523                         else
524                             alu_out(63 downto 32) <= r2(63 downto 32);
525                     end if;
526
527                     if(signed(r1(31 downto 0)) > signed(r2(31 downto 0))) then
528                         alu_out(31 downto 0)<= r1(31 downto 0);
529                         else
530                             alu_out(31 downto 0) <= r2(31 downto 0);
```

```
531                     end if;
532
533
534                 ----------MIN: min signed word
535                 when "01000" =>
536                     if (to integer(signed(r1(127 downto 96))) > to integer(signed(r2(127
    downto 96)))) then
537                         alu out(127 downto 96)<= r2(127 downto 96);
538                         else
539                             alu out(127 downto 96) <= r1(127 downto 96);
540                     end if;
541
542                     if signed(r1(95 downto 64)) > signed(r2(95 downto 64)) then
543                         alu_out(95 downto 64)<= r2(95 downto 64);
544                         else
545                             alu_out(95 downto 64) <= r1(95 downto 64);
546                     end if;
547
548                     if signed(r1(63 downto 32)) > signed(r2(63 downto 32)) then
549                         alu out(63 downto 32)<= r2(63 downto 32);
550                         else
551                             alu out(63 downto 32) <= r1(63 downto 32);
552                     end if;
553
554                     if signed(r1(31 downto 0)) > signed(r2(31 downto 0)) then
555                         alu_out(31 downto 0)<= r2(31 downto 0);
556                         else
557                             alu_out(31 downto 0) <= r1(31 downto 0);
558                     end if;
559
560
561                 ---------MSGN: multiply signed
562                 -----???
563                 when "01001" =>
564                 if to integer(signed(r1(127 downto 96)))= -2147483648 and r2(127)='1'
    then
565                     alu out(127 downto 96) <= (Others=>'1');
566                     alu_out(127)<='0';
567                 else
568                     if r2(127)='1' then
569                         --signed(r1(127 downto 96)*(-1)
570                         alu_out(127 downto 96)<=std_logic_vector(to_signed(to_integer(
    signed(r1(127 downto 96)))*(-1),32));
571
572                     elsif r2(127 downto 96)="00000000000000000000000000000000" then
573                         alu out(127 downto 96)<="00000000000000000000000000000000" ;
574                     else
575                         alu out(127 downto 96)<=r1(127 downto 96);
576                     end if;
577                 end if;
578
579
580                 if to_integer(signed(r1(95 downto 64)))= -2147483648 and (r2(127)='1')
    then
581                     alu_out(95 downto 64)<=(Others=>'1');
582                     alu out(95)<='0';
583                 else
584                     if(r2(95)='1') then
585                         alu out(95 downto 64)<=std_logic_vector(to signed(to integer(
    signed(r1(95 downto 64)))*(-1),32));
586                         elsif unsigned(r2(95 downto 64))=0 then
587                         alu out(95 downto 64)<="00000000000000000000000000000000" ;
588                         else
589                         alu_out(95 downto 64)<=r1(95 downto 64);
590                     end if;
591                 end if;
```

```
592
593                 if to_integer(signed(r1(63 downto 32)))= -2147483648 and (r2(127)='1')
    then
594                     alu_out(63 downto 32)<=(Others=>'1');
595                     alu_out(63)<='0';
596                 else
597                     if(r2(63)='1') then
598                         alu out(63 downto 32)<=std_logic_vector(to signed(to integer(
    signed(r1(63 downto 32)))*(-1),32));
599                         elsif unsigned(r2(63 downto 32))=0 then
600                         alu out(63 downto 32)<="00000000000000000000000000000000" ;
601                         else
602                         alu_out(63 downto 32)<=r1(63 downto 32);
603                     end if;
604                 end if;
605
606
607                 if to_integer(signed(r1(31 downto 0)))= -2147483648 and (r2(127)='1')
    then
608                     alu out(31 downto 0)<=(Others=>'1');
609                     alu out(31)<='0';
610                 else
611                     if(r2(31)='1') then
612                         alu out(31 downto 0)<=std_logic_vector(to signed(to integer(
    signed(r1(31 downto 0)))*(-1),32));
613                         elsif unsigned(r2(31 downto 0))=0 then
614                         alu_out(31 downto 0)<="00000000000000000000000000000000" ;
615                         else
616                         alu_out(31 downto 0)<=r1(31 downto 0);
617                     end if;
618                 end if;
619                 ---------MPYU: multiply unsigned
620                 when "01010" =>
621                 alu out(127 downto 96)<=std_logic_vector(to unsigned(to integer(unsigned
    (r1(111 downto 96)))*to integer( unsigned(r2(111 downto 96))),32));
622                 alu out(95 downto 64)<=std_logic_vector(to unsigned(to integer(unsigned(
    r1(79 downto 64)))*to integer( unsigned(r2(79 downto 64))),32));
623                 alu_out(63 downto 32)<=std_logic_vector(to_unsigned(to_integer(unsigned(
    r1(47 downto 32)))*to_integer( unsigned(r2(47 downto 32))),32));
624                 alu_out(31 downto 0)<=std_logic_vector(to_unsigned(to_integer(unsigned(
    r1(15 downto 0)))*to_integer( unsigned(r2(15 downto 0))),32));
625                 ---------OR: bitwise logical or
626                 when "01011" =>
627                     alu out <= r1 or r2;
628
629                 ---------POPCNTH: count ones in halfwords
630                 when "01100" =>
631                 one count := 0;
632                     for i in 127 downto 112 loop
633                         if r1(i)='1' then
634                             one_count := one_count+1;
635                         end if;
636                     end loop;
637                     alu_out(127 downto 112) <= std_logic_vector(to_unsigned(one_count,16
    ));
638                     one count:=0;
639
640                     for i in 111 downto 96 loop
641                         if r1(i)='1' then
642                             one count := one count +1;
643                         end if;
644                     end loop;
645                     alu_out(111 downto 96) <= std_logic_vector(to_unsigned(one_count,16
    ));
646                     one_count:=0;
647
```

```
648                     for i in 95 downto 80 loop
649                         if r1(i)='1' then
650                             one_count := one_count+1;
651                         end if;
652                     end loop;
653                     alu_out(95 downto 80) <= std_logic_vector(to_unsigned(one_count,16
    ));
654                     one_count:=0;
655
656                     for i in 79 downto 64 loop
657                         if r1(i)='1' then
658                             one_count := one_count +1;
659                         end if;
660                     end loop;
661                     alu_out(79 downto 64) <= std_logic_vector(to_unsigned(one_count,16
    ));
662                     one_count:=0;
663
664                     for i in 63 downto 48 loop
665                         if r1(i)='1' then
666                             one_count := one_count+1;
667                         end if;
668                     end loop;
669                     alu_out(63 downto 48) <= std_logic_vector(to_unsigned(one_count,16
    ));
670                     one_count:=0;
671
672                     for i in 47 downto 32 loop
673                         if r1(i)='1' then
674                             one_count := one_count +1;
675                         end if;
676                     end loop;
677                     alu_out(47 downto 32) <= std_logic_vector(to_unsigned(one_count,16
    ));
678                     one_count:=0;
679
680                     for i in 31 downto 16 loop
681                         if r1(i)='1' then
682                             one_count := one_count+1;
683                         end if;
684                     end loop;
685                     alu_out(31 downto 16) <= std_logic_vector(to_unsigned(one_count,16
    ));
686                     one_count:=0;
687
688                     for i in 15 downto 0 loop
689                         if r1(i)='1' then
690                             one_count := one_count +1;
691                         end if;
692                     end loop;
693                     alu_out(15 downto 0) <= std_logic_vector(to_unsigned(one_count,16));
694                     one_count:=0;
695
696                 ---------ROT: rotate bits right
697                 when "01101" =>
698                     bits_of_shift:=to_integer(unsigned(r2(6 downto 0)));
699                     alu_out<=r1 ror bits_of_shift;
700
701                 ---------ROTW: rotate bits in word
702                 when "01110" =>
703                     bits_of_shift:=to_integer(unsigned(r2(100 downto 96)));
704                     alu_out(127 downto 96)<=r1(127 downto 96) ror bits_of_shift;
705                     bits_of_shift:=to_integer(unsigned(r2(68 downto 64)));
706                     alu_out(95 downto 64)<=r1(95 downto 64) ror bits_of_shift;
707                     bits_of_shift:=to_integer(unsigned(r2(36 downto 32)));
708                     alu_out(63 downto 32)<=r1(63 downto 32) ror bits_of_shift;
```

```
709                     bits_of_shift:=to_integer(unsigned(r2(4 downto 0)));
710                     alu_out(31 downto 0)<=r1(31 downto 0) ror bits_of_shift;
711
712                 ---------SHLHI: shift left halfword immediate:
713                 ------???
714                 when "01111" =>
715                     bits of shift:=to integer(unsigned(r2(115 downto 112)));
716                     alu out(127 downto 112)<=r1(127 downto 112) SLL bits of shift;
717                     bits of shift:=to integer(unsigned(r2(99 downto 96)));
718                     alu out(111 downto 96)<=r1(111 downto 96) SLL bits of shift;
719                     bits of shift:=to integer(unsigned(r2(83 downto 80)));
720                     alu out(95 downto 80)<=r1(95 downto 80) SLL bits of shift;
721                     bits_of_shift:=to_integer(unsigned(r2(67 downto 64)));
722                     alu_out(79 downto 64)<=r1(79 downto 64) SLL bits_of_shift;
723                     bits_of_shift:=to_integer(unsigned(r2(51 downto 48)));
724                     alu_out(63 downto 48)<=r1(63 downto 48) SLL bits_of_shift;
725                     bits_of_shift:=to_integer(unsigned(r2(35 downto 32)));
726                     alu_out(47 downto 32)<=r1(47 downto 32) SLL bits_of_shift;
727                     bits of shift:=to integer(unsigned(r2(19 downto 16)));
728                     alu out(31 downto 16)<=r1(31 downto 16) SLL bits of shift;
729                     bits of shift:=to integer(unsigned(r2(3 downto 0)));
730                     alu out(15 downto 0)<=r1(15 downto 0) SLL bits of shift;
731
732                 ---------SFH: subtract from halfword immediate
733                 when "10000" =>
734                 alu_out(127 downto 112)<=std_logic_vector(to_unsigned(to_integer(
    unsigned(r2(127 downto 112)))-to_integer(unsigned(r2(127 downto 112))),16));
735                 alu_out(111 downto 96)<=std_logic_vector(to_unsigned(to_integer(unsigned
    (r2(111 downto 96)))-to_integer(unsigned(r2(111 downto 96))),16));
736                 alu_out(95 downto 80)<=std_logic_vector(to_unsigned(to_integer(unsigned(
    r2(95 downto 80)))-to integer(unsigned(r2(95 downto 80))),16));
737                 alu out(79 downto 64)<=std_logic_vector(to unsigned(to integer(unsigned(
    r2(79 downto 64)))-to integer(unsigned(r2(79 downto 64))),16));
738                 alu out(63 downto 48)<=std_logic_vector(to unsigned(to integer(unsigned(
    r2(63 downto 48)))-to integer(unsigned(r2(63 downto 48))),16));
739                 alu out(47 downto 32)<=std_logic_vector(to unsigned(to integer(unsigned(
    r2(47 downto 32)))-to integer(unsigned(r2(47 downto 32))),16));
740                 alu_out(31 downto 16)<=std_logic_vector(to_unsigned(to_integer(unsigned(
    r2(31 downto 16)))-to_integer(unsigned(r2(31 downto 16))),16));
741                 alu_out(15 downto 0)<=std_logic_vector(to_unsigned(to_integer(unsigned(
    r2(15 downto 0)))-to_integer(unsigned(r2(15 downto 0))),16));
742
743                 ---------SFW: subtract from word
744                 when "10001" =>
745                 alu out(127 downto 96)<=std_logic_vector(to unsigned(to integer(unsigned
    (r2(127 downto 96)))-to integer(unsigned(r2(127 downto 96))),32));
746                 alu out(95 downto 64)<=std_logic_vector(to unsigned(to integer(unsigned(
    r2(95 downto 64)))-to integer(unsigned(r2(95 downto 64))),32));
747                 alu out(63 downto 32)<=std_logic_vector(to unsigned(to integer(unsigned(
    r2(63 downto 32)))-to_integer(unsigned(r2(63 downto 32))),32));
748                 alu_out(31 downto 0)<=std_logic_vector(to_unsigned(to_integer(unsigned(
    r2(31 downto 0)))-to_integer(unsigned(r2(31 downto 0))),32));
749
750                 ---------SFHS: subtract from halfword saturated
751                 ---------saturation??
752                 when "10010" =>
753                 alu out(127 downto 112)<=std_logic_vector(signed(r2(127 downto 112)) -
    signed(r1(127 downto 112)));
754                 if alu out(127)='0' and r2(127)='1' and r1(127)='0'  then
755                     alu out(127 downto 112) <= (others=>'0');
756                     alu out(127)<='1';
757                 elsif alu out(127)='1' and r2(127)='0' and r2(127)='1' then
758                     alu_out(127 downto 112) <= (others=>'1');
759                     alu_out(127)<='0';
760                 end if;
761
```

```
762                     alu_out(111 downto 96)<=std_logic_vector(signed(r2(111 downto 96))-
    signed(r1(111 downto 96)));
763                     if alu_out(111)='0' and r2(111)='1' and r1(111)='0'  then
764                         alu_out(111 downto 96) <= (others=>'0');
765                         alu_out(111)<='1';
766                     elsif alu out(111)='1' and r2(111)='0' and r2(111)='1' then
767                         alu out(111 downto 96) <= (others=>'1');
768                         alu out(111)<='0';
769                     end if;
770
771                     alu out(95 downto 80)<=std_logic_vector(signed(r2(95 downto 80))-signed(
    r1(95 downto 80)));
772                     if alu_out(95)='0' and r2(95)='1' and r1(95)='0'  then
773                         alu_out(95 downto 80) <= (others=>'0');
774                         alu_out(95)<='1';
775                     elsif alu_out(95)='1' and r2(95)='0' and r2(95)='1' then
776                         alu_out(95 downto 80) <= (others=>'1');
777                         alu_out(95)<='0';
778                     end if;
779
780                     alu out(79 downto 64)<=std_logic_vector(signed(r2(79 downto 64))-signed(
    r1(79 downto 64)));
781                     if alu out(79)='0' and r2(79)='1' and r1(79)='0'  then
782                         alu out(79 downto 64) <= (others=>'0');
783                         alu_out(79)<='1';
784                     elsif alu_out(79)='1' and r2(79)='0' and r2(79)='1' then
785                         alu_out(79 downto 64) <= (others=>'1');
786                         alu_out(79)<='0';
787                     end if;
788
789                     alu out(63 downto 48)<=std_logic_vector(signed(r2(63 downto 48))-signed(
    r1(63 downto 48)));
790                     if alu out(63)='0' and r2(63)='1' and r1(63)='0'  then
791                         alu out(63 downto 48) <= (others=>'0');
792                         alu out(63)<='1';
793                     elsif alu out(63)='1' and r2(63)='0' and r2(63)='1' then
794                         alu out(63 downto 48) <= (others=>'1');
795                         alu_out(63)<='0';
796                     end if;
797
798                     alu_out(47 downto 32)<=std_logic_vector(signed(r2(47 downto 32))-signed(
    r1(47 downto 32)));
799                     if alu_out(47)='0' and r2(47)='1' and r1(47)='0'  then
800                         alu out(47 downto 32) <= (others=>'0');
801                         alu out(47)<='1';
802                     elsif alu out(47)='1' and r2(47)='0' and r2(47)='1' then
803                         alu out(47 downto 32) <= (others=>'1');
804                         alu out(47)<='0';
805                     end if;
806
807                     alu_out(31 downto 16)<=std_logic_vector(signed(r2(31 downto 16))-signed(
    r1(31 downto 16)));
808                     if alu_out(31)='0' and r2(31)='1' and r1(31)='0'  then
809                         alu_out(31 downto 16) <= (others=>'0');
810                         alu_out(31)<='1';
811                     elsif alu out(31)='1' and r2(31)='0' and r2(31)='1' then
812                         alu out(31 downto 16) <= (others=>'1');
813                         alu out(31)<='0';
814                     end if;
815
816                     alu out(15 downto 0)<=std_logic_vector(signed(r2(15 downto 0))-signed(r1
    (15 downto 0)));
817                     if alu_out(15)='0' and r2(15)='1' and r1(15)='0'  then
818                         alu_out(15 downto 0) <= (others=>'0');
819                         alu_out(15)<='1';
820                     elsif alu_out(15)='1' and r2(15)='0' and r2(15)='1' then
```

```
821                     alu_out(15 downto 0) <= (others=>'1');
822                     alu_out(15)<='0';
823                 end if;
824
825                 ---------XOR: bitwise logical exclusive-or
826                 when "10011" =>
827                 alu out <= r1 xor r2;
828                 when others => null;
829
830             end case;
831         end if;
832         end if;
833     end process;
834
835 end behavioral;
```