```
1     ----------------------------------------------------------------------------
2     --
3     -- Title       : forwarding_unit
4     -- Design      : processor
5     -- Author      :
6     -- Company     :
7     --
8     ----------------------------------------------------------------------------
9     --
10    -- File        :
      C:\Users\gavin\Desktop\Study\ESE345\project\processor\processor\src\forwarding_unit.vhd
11    -- Generated   : Sat Nov 30 17:16:23 2019
12    -- From        : interface description file
13    -- By          : Itf2Vhdl ver. 1.22
14    --
15    ----------------------------------------------------------------------------
16    --
17    -- Description :
18    --
19    ----------------------------------------------------------------------------
20
21    --{{ Section below this comment is automatically maintained
22    --   and may be overwritten
23    --{entity {forwarding_unit} architecture {\behavioral \}}
24
25    library ieee;
26    use ieee.std_logic_1164.all;
27    use ieee.numeric_std.all;
28
29    entity forwarding_unit is
30        port(
31        ALU_out : in std_logic_vector(127 downto 0);
32        r1_in : in std_logic_vector(127 downto 0);
33        r2_in : in std_logic_vector(127 downto 0);
34        r3_in : in std_logic_vector(127 downto 0);
35        ins : in std_logic_vector(24 downto 0);
36        old_ins : in std_logic_vector(24 downto 0);
37        r1_out : out std_logic_vector(127 downto 0);
38        r2_out : out std_logic_vector(127 downto 0);
39        r3_out : out std_logic_vector(127 downto 0)
40        );
41    end forwarding_unit;
42
43    --}} End of automatically maintained section
44
45    architecture behavioral of forwarding_unit is
46    signal older_ins : std_logic_vector(24 downto 0);
47    signal old_out : std_logic_vector(127 downto 0);
48    begin
49        process(ALU_out, r1_in, r2_in, r3_in, ins, old_ins)
50        begin
51            if ins(24) = '0' then
52                if old_ins(4 downto 0) = ins(4 downto 0) then
53                    r1_out <= ALU_out;
54                    r2_out <= r2_in;
55                    r3_out <= r3_in;
56                elsif older_ins(4 downto 0) = ins(4 downto 0) then
57                    r1_out <= old_out;
58                    r2_out <= r2_in;
59                    r3_out <= r3_in;
60                else
61                    r1_out <= r1_in;
62                    r2_out <= r2_in;
63                    r3_out <= r3_in;
64                end if;
65            elsif ins(24) = '1' then
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```
66              if ins(23) = '1' then
67                  if ins(19 downto 15) = "00000" then
68                      r1_out <= r1_in;
69                      r2_out <= r2_in;
70                      r3_out <= r3_in;
71                  else
72                      if old ins(4 downto 0) = ins(9 downto 5) then
73                          r1 out <= ALU out;
74                          r2 out <= r2 in;
75                          r3 out <= r3 in;
76                      elsif old ins(4 downto 0) = ins(14 downto 10) then
77                          r2 out <= ALU out;
78                          r1_out <= r1_in;
79                          r3_out <= r3_in;
80                      elsif older_ins(4 downto 0) = ins(9 downto 5) then
81                          r1_out <= old_out;
82                          r2_out <= r2_in;
83                          r3_out <= r3_in;
84                      elsif older ins(4 downto 0) = ins(14 downto 10) then
85                          r2 out <= old out;
86                          r1 out <= r1 in;
87                          r3 out <= r3 in;
88                      else
89                          r1 out <= r1 in;
90                          r2_out <= r2_in;
91                          r3_out <= r3_in;
92                      end if;
93                  end if;
94              elsif ins(23) = '0' then
95                  if old_ins(4 downto 0) = ins(9 downto 5) then
96                      r1 out <= ALU out;
97                      r2 out <= r2 in;
98                      r3 out <= r3 in;
99                  elsif old ins(4 downto 0) = ins(14 downto 10) then
100                     r2 out <= ALU out;
101                     r1 out <= r1 in;
102                     r3 out <= r3 in;
103                 elsif old_ins(4 downto 0) = ins(19 downto 15) then
104                     r3_out <= ALU_out;
105                     r1_out <= r1_in;
106                     r2_out <= r2_in;
107                 elsif older_ins(4 downto 0) = ins(9 downto 5) then
108                     r1_out <= old_out;
109                     r2 out <= r2 in;
110                     r3 out <= r3 in;
111                 elsif older ins(4 downto 0) = ins(14 downto 10) then
112                     r2 out <= old out;
113                     r1 out <= r1 in;
114                     r3 out <= r3 in;
115                 elsif older_ins(4 downto 0) = ins(19 downto 15) then
116                     r3_out <= old_out;
117                     r1_out <= r1_in;
118                     r2_out <= r2_in;
119                 else
120                     r1_out <= r1_in;
121                     r2 out <= r2 in;
122                     r3 out <= r3 in;
123                 end if;
124             end if;
125         end if;
126         older ins <= old ins;
127         old out <= ALU out;
128     end process;
129
130
131      -- enter your statements here --
```

File: f:/project345/src/forwarding_unit.vhd (/file_io_tb/UUT/u4)

```
132
133   end behavioral;
134
```