

ESE345 Project Report

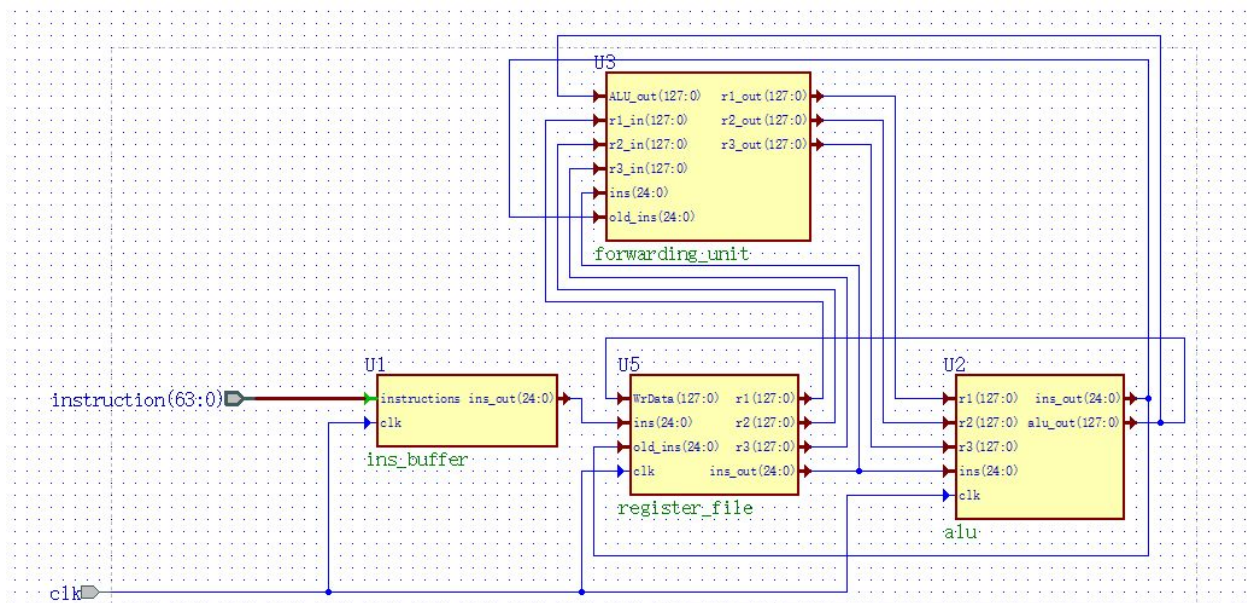
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1. Project Goal

This objective of the project is to learn the use of VHDL/Verilog hardware description language and modern CAD tools for the hierarchical gate-level and dataflow/RTL design of the 4-stage pipelined multimedia unit with a reduced set of multimedia instructions similar to those in the Sony Cell SPU and Intel SSE architectures.

2. Multimedia unit block diagram



3. Design procedure

3.1. ALU

In this module, there are five input which are 128 bit vector r1, r2, r3 and 25 bit instruction and clk, and two outputs 25 bit ins and calculated 128 bit alu_out. Case statement based on instruction's 25 to 15 bit is used to tell which instruction is in this

cycle. The reason why there is a `ins_out` is like transferring the control signal to register file to tell register which register have to write into.

For the load instruction, first give `r1`'s value to the `alu_out` and then load immediate to the `alu_out`.

For the R4 type instruction, `temp1` and `temp2` which are short 32 bit vector variable and `temp3` and `temp4` which are long 64 bit vector variable are used to get the temporary product of `rs2` and `rs3` and sum of product of `rs2` and `rs3` and `rs1`. There might be saturation when add and subtract. For the add saturation case, there are two cases, one is positive number plus positive number to get a positive saturation and negative number subtract negative numbers to get a negative saturation. For the subtract saturation case, there are still two cases which are positive number subtract negative numbers to get a positive saturation and negative number subtract positive number to get a negative saturation.

For the R3 type instruction, there are some or, xor, rotate, left shift and right shift instruction which can use pre-defined function or, xor, ror, sll and srl. Saturation cases are like the R4 type instruction, while in the MSGN instruction there is only one saturation case which is the for the same number of bit maximum negative number is bigger than the maximum positive number.

3.2. Instruction Buffer

Declare a 64 capacity array to store 64 instructions. Every PC count 1 more then fetch next instruction.

3.3. Register File

There are write enable control signal to determine should write into register. The `old_ins` is transferred from alu to determine in last cycle which register have to write into.

3.4. Forwarding Unit

All instructions takes 4 clock cycles to complete, which will cause data hazard if an instruction uses a register that is recently modified in the earlier 2 clock cycles. The forwarding unit will detect this situation and delivers the most recent data of that register to the input of ALU to avoid data hazard.

3.5. Pipeline Unit

Pipeline unit is a structural unit in the project. It works as a bridge between each unit. Signals or Variables will be declared to store the data and instructions output

from one unit and send them to the next unit's inputs. These signals can be seen as the pipeline registers, they have the same function.

4. Testbenches

Imported two new libraries `STD.textio.all` and `ieee.std_logic_textio.all` to use built-in function to read txt file generated by assembly to binary instruction converter program written in Java. And still write the `alu_out` 128 bit data into txt file.

5. Conclusions

The final design was tested and verified for various input data and different op-codes using different inputs in the testbench. All the instructions functions as expected and the results generated match the theoretical results. So it was determined that the final design is a success.

Test Instruction List:

li r1,0,0000000000000001

li r1,1,0000000000000010

li r1,2,0000000000000011

li r1,3,0000000000000100

li r1,4,0000000000000101

li r1,5,0000000000000110

li r1,6,0000000000000111

li r1,7,0000000000001000

li r2,0,0000000000000001

li r2,1,0000000000000010

li r2,2,0000000000000011

li r2,3,0000000000000100

li r2,4,0000000000000101

li r2,5,0000000000000110

li r2,6,0000000000000111

li r2,7,0000000000001000

li r3,0,0000000000000001

li r3,1,0000000000000010

li r3,2,0000000000000011

li r3,3,0000000000000100

li r3,4,0000000000000101

li r3,5,0000000000000110

li r3,6,0000000000000111

li r3,7,0000000000001000

IAL r4,r1,r2,r3

IAH r5,r1,r2,r3

ISL r6,r1,r2,r3

ISH r7,r1,r2,r3

LAL r8,r1,r2,r3

LAH r9,r1,r2,r3

LSL r10,r1,r2,r3

LSH r11,r1,r2,r3

A r12,r1,r2

AH r13,r1,r2

AHS r14,r1,r2

AND r15,r1,r2

BCW r16,r1,r2

CLZ r17,r1,r2

MAX r18,r1,r2

MIN r19,r1,r2

MSGN r20,r1,r2

MPYU r21,r1,r2

OR r22,r1,r2

POPCNTH r23,r1,r2

ROT r24,r1,r2

ROTW r25,r1,r2

SHLHI r26,r1,r2

SFH r27,r1,r2

SFW r28,r1,r2

SFHS r29,r1,r2

XOR r30,r1,r2

Opcode after transformed:

000000000000000000000000100001

00010000000000000001000001

00100000000000000001100001

00110000000000000010000001

010000000000000000010100001

0101000000000000011000001

0110000000000000011100001

011100000000000100000001

000000000000000000000100010

0001000000000000001000010

0010000000000000001100010

001100000000000010000010

0100000000000000010100010

0101000000000000011000010

0110000000000000011100010

011100000000000100000010

000000000000000000000000100011

0001000000000000001000011

0010000000000000001100011

001100000000000010000011

0100000000000000010100011

0101000000000000011000011

0110000000000000011100011

0111000000000000100000011
1000000011000100000100100
1000100011000100000100101
1001000011000100000100110
1001100011000100000100111
1010000011000100000101000
1010100011000100000101001
1011000011000100000101010
1011100011000100000101011
1100000001000100000101100
1100000010000100000101101
1100000011000100000101110
1100000100000100000101111
1100000101000100000110000
1100000110000100000110001
1100000111000100000110010
1100001000000100000110011
1100001001000100000110100
1100001010000100000110101
1100001011000100000110110
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1100001110000100000111001
1100001111000100000111010

1100010000000100000111011

1100010001000100000111100

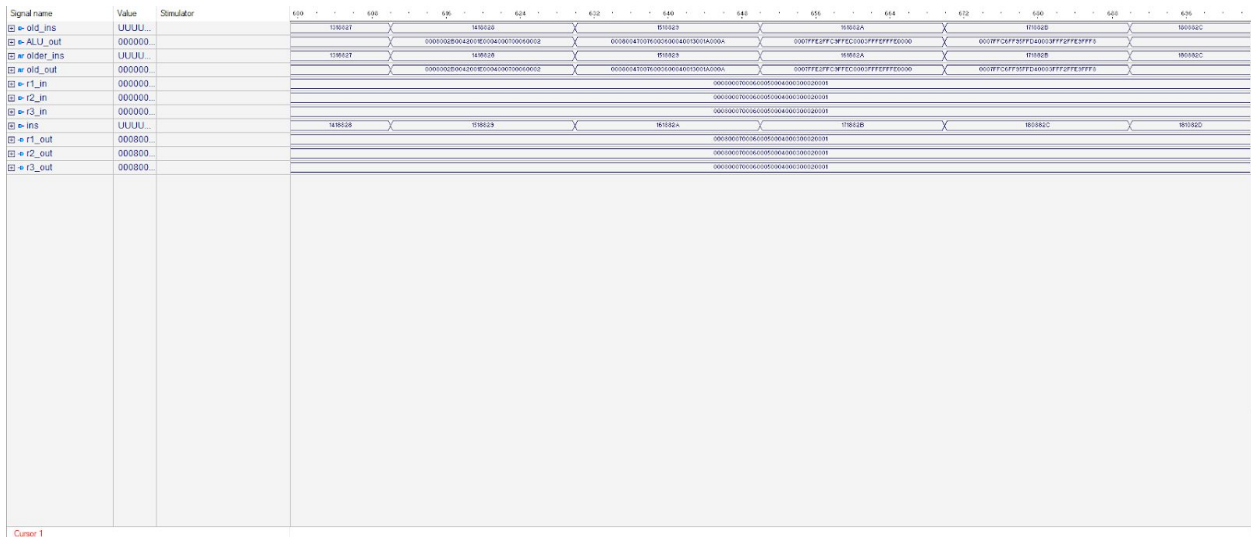
1100010010000100000111101

1100010011000100000111110

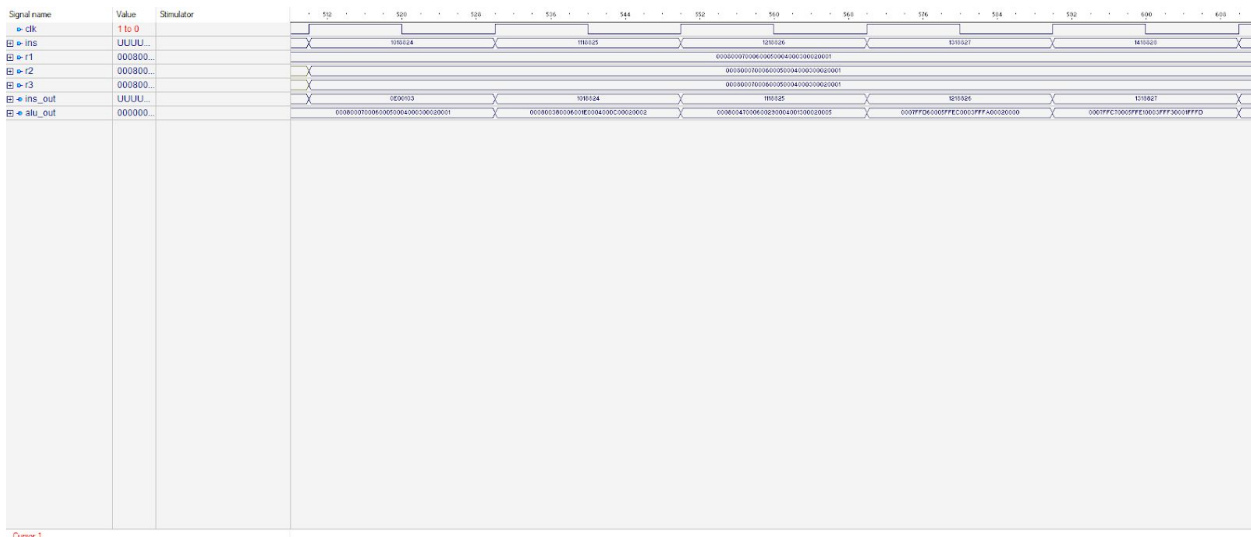
Signal name	Value	Simulator
clk	0	
ins_out	Q200042	
PC	0A	
instructions[83]	UUUU...	
instructions[82]	UUUU...	
instructions[81]	UUUU...	
instructions[80]	UUUU...	
instructions[59]	UUUU...	
instructions[58]	UUUU...	
instructions[57]	UUUU...	
instructions[56]	UUUU...	
instructions[55]	UUUU...	
instructions[54]	UUUU...	
instructions[53]	UUUU...	
instructions[52]	UUUU...	
instructions[51]	UUUU...	
instructions[50]	189883E	
instructions[49]	189883D	
instructions[48]	188883C	
instructions[47]	188883B	
instructions[46]	187883A	
instructions[45]	1870839	
instructions[44]	1868838	
instructions[43]	1860837	
instructions[42]	1858836	
instructions[41]	1850835	
instructions[40]	1848834	
instructions[39]	1840833	
instructions[38]	1838832	
instructions[37]	1830831	
instructions[36]	1828830	
instructions[35]	182082F	
instructions[34]	181882E	
instructions[33]	181082D	
instructions[32]	180882C	

[illegible]

Waveform of forwarding unit during working



Waveform of ALU during working



Waveform of final results in the registers

Signal name	Value	Simulator	reg0	reg1	reg2	reg3	reg4	reg5	reg6	reg7	reg8	reg9	reg10	reg11	reg12	reg13	reg14	reg15	reg16	reg17	reg18	reg19	reg20	reg21	reg22	reg23	reg24	reg25	reg26	reg27	reg28	reg29	reg30	reg31	reg32	reg33	reg34	reg35	reg36	reg37	reg38	reg39	reg40	reg41	reg42	reg43	reg44	reg45	reg46	reg47	reg48	reg49	reg50	reg51	reg52	reg53	reg54	reg55	reg56	reg57	reg58	reg59	reg60	reg61	reg62	reg63	reg64	reg65	reg66	reg67	reg68	reg69	reg70	reg71	reg72	reg73	reg74	reg75	reg76	reg77	reg78	reg79	reg80	reg81	reg82	reg83	reg84	reg85	reg86	reg87	reg88	reg89	reg90	reg91	reg92	reg93	reg94	reg95	reg96	reg97	reg98	reg99	reg100	reg101	reg102	reg103	reg104	reg105	reg106	reg107	reg108	reg109	reg110	reg111	reg112	reg113	reg114	reg115	reg116	reg117	reg118	reg119	reg120	reg121	reg122	reg123	reg124	reg125	reg126	reg127	reg128	reg129	reg130	reg131	reg132	reg133	reg134	reg135	reg136	reg137	reg138	reg139	reg140	reg141	reg142	reg143	reg144	reg145	reg146	reg147	reg148	reg149	reg150	reg151	reg152	reg153	reg154	reg155	reg156	reg157	reg158	reg159	reg160	reg161	reg162	reg163	reg164	reg165	reg166	reg167	reg168	reg169	reg170	reg171	reg172	reg173	reg174	reg175	reg176	reg177	reg178	reg179	reg180	reg181	reg182	reg183	reg184	reg185	reg186	reg187	reg188	reg189	reg190	reg191	reg192	reg193	reg194	reg195	reg196	reg197	reg198	reg199	reg200	reg201	reg202	reg203	reg204	reg205	reg206	reg207	reg208	reg209	reg210	reg211	reg212	reg213	reg214	reg215	reg216	reg217	reg218	reg219	reg220	reg221	reg222	reg223	reg224	reg225	reg226	reg227	reg228	reg229	reg230	reg231	reg232	reg233	reg234	reg235	reg236	reg237	reg238	reg239	reg240	reg241	reg242	reg243	reg244	reg245	reg246	reg247	reg248	reg249	reg250	reg251	reg252	reg253	reg254	reg255	reg256	reg257	reg258	reg259	reg260	reg261	reg262	reg263	reg264	reg265	reg266	reg267	reg268	reg269	reg270	reg271	reg272	reg273	reg274	reg275	reg276	reg277	reg278	reg279	reg280	reg281	reg282	reg283	reg284	reg285	reg286	reg287	reg288	reg289	reg290	reg291	reg292	reg293	reg294	reg295	reg296	reg297	reg298	reg299	reg300	reg301	reg302	reg303	reg304	reg305	reg306	reg307	reg308	reg309	reg310	reg311	reg312	reg313	reg314	reg315	reg316	reg317	reg318	reg319	reg320	reg321	reg322	reg323	reg324	reg325	reg326	reg327	reg328	reg329	reg330	reg331	reg332	reg333	reg334	reg335	reg336	reg337	reg338	reg339	reg340	reg341	reg342	reg343	reg344	reg345	reg346	reg347	reg348	reg349	reg350	reg351	reg352	reg353	reg354	reg355	reg356	reg357	reg358	reg359	reg360	reg361	reg362	reg363	reg364	reg365	reg366	reg367	reg368	reg369	reg370	reg371	reg372	reg373	reg374	reg375	reg376	reg377	reg378	reg379	reg380	reg381	reg382	reg383	reg384	reg385	reg386	reg387	reg388	reg389	reg390	reg391	reg392	reg393	reg394	reg395	reg396	reg397	reg398	reg399	reg400	reg401	reg402	reg403	reg404	reg405	reg406	reg407	reg408	reg409	reg410	reg411	reg412	reg413	reg414	reg415	reg416	reg417	reg418	reg419	reg420	reg421	reg422	reg423	reg424	reg425	reg426	reg427	reg428	reg429	reg430	reg431	reg432	reg433	reg434	reg435	reg436	reg437	reg438	reg439	reg440	reg441	reg442	reg443	reg444	reg445	reg446	reg447	reg448	reg449	reg450	reg451	reg452	reg453	reg454	reg455	reg456	reg457	reg458	reg459	reg460	reg461	reg462	reg463	reg464	reg465	reg466	reg467	reg468	reg469	reg470	reg471	reg472	reg473	reg474	reg475	reg476	reg477	reg478	reg479	reg480	reg481	reg482	reg483	reg484	reg485	reg486	reg487	reg488	reg489	reg490	reg491	reg492	reg493	reg494	reg495	reg496	reg497	reg498	reg499	reg500	reg501	reg502	reg503	reg504	reg505	reg506	reg507	reg508	reg509	reg510	reg511	reg512	reg513	reg514	reg515	reg516	reg517	reg518	reg519	reg520	reg521	reg522	reg523	reg524	reg525	reg526	reg527	reg528	reg529	reg530	reg531	reg532	reg533	reg534	reg535	reg536	reg537	reg538	reg539	reg540	reg541	reg542	reg543	reg544	reg545	reg546	reg547	reg548	reg549	reg550	reg551	reg552	reg553	reg554	reg555	reg556	reg557	reg558	reg559	reg560	reg561	reg562	reg563	reg564	reg565	reg566	reg567	reg568	reg569	reg570	reg571	reg572	reg573	reg574	reg575	reg576	reg577	reg578	reg579	reg580	reg581	reg582	reg583	reg584	reg585	reg586	reg587	reg588	reg589	reg590	reg591	reg592	reg593	reg594	reg595	reg596	reg597	reg598	reg599	reg600	reg601	reg602	reg603	reg604	reg605	reg606	reg607	reg608	reg609	reg610	reg611	reg612	reg613	reg614	reg615	reg616	reg617	reg618	reg619	reg620	reg621	reg622	reg623	reg624	reg625	reg626	reg627	reg628	reg629	reg630	reg631	reg632	reg633	reg634	reg635	reg636	reg637	reg638	reg639	reg640	reg641	reg642	reg643	reg644	reg645	reg646	reg647	reg648	reg649	reg650	reg651	reg652	reg653	reg654	reg655	reg656	reg657	reg658	reg659	reg660	reg661	reg662	reg663	reg664	reg665	reg666	reg667	reg668	reg669	reg670	reg671	reg672	reg673	reg674	reg675	reg676	reg677	reg678	reg679	reg680	reg681	reg682	reg683	reg684	reg685	reg686	reg687	reg688	reg689	reg690	reg691	reg692	reg693	reg694	reg695	reg696	reg697	reg698	reg699	reg700	reg701	reg702	reg703	reg704	reg705	reg706	reg707	reg708	reg709	reg710	reg711	reg712	reg713	reg714	reg715	reg716	reg717	reg718	reg719	reg720	reg721	reg722	reg723	reg724	reg725	reg726	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Final result in register:

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Expected Results:

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