



User Manual

FPGA Explorer

2025/03/31

v.1.2

A step-by-step user guide to getting started

Developed by the Team 1

from ALGOSUP

SUMMARY

| | |
|----|--------------------------------|
| 2 | The website |
| 3 | What can you do? |
| | The main page |
| | The animation page |
| | The help page |
| 5 | Launch the website |
| 6 | Main page |
| | open it |
| | Interaction |
| 7 | Load a file |
| | Drag & Drop |
| | Replace the current file |
| 9 | Play animation |
| | Start |
| | Stop |
| 11 | Modify the view |
| | Zoom |
| | Unzoom |
| | Fit to the view |
| 13 | Modify the view |
| 14 | Help tab |
| 15 | Definitions |
| 16 | Q&A |
| 17 | Ressources |
| 18 | Copyrights |
| 19 | Credits |

The website

This website is focused on helping you teach or learn how the FPGA board system works. It combine a realistic 2D representation with a dynamic signal propagation over time. The aim is to create an interactive and intuitive platform that allow you to observe and analyze signal propagation.

For simplicity, we will represent the FPGA system with different view to understand the FPGA system through animations that symbolize signals transfers.

This includes integrating the layout resulting from the synthesis and P&R processes with timing simulation data. You can analyze using a test bench and a timing netlist, both written in Verilog.

What can you do?

Main page

The main page serves as a gateway to essential insights on CNES, FPGA, and Verilog, providing a detailed overview of the FPGA ecosystem. It aims to enhance your understanding of how FPGA technology works, its advantages, and why CNES integrates it into its projects. Through clear explanations and key resources, this page helps you grasp the role of FPGA in space applications and beyond.

Animation page

The animation page provides an interactive and visual representation of how an FPGA board operates based on your programmed instructions. It allows you to explore the internal functioning of the FPGA, helping you understand how different configurations influence its behavior and execution.

Help page

The help page is designed to assist you in navigating the website with ease, ensuring that you can quickly find the information you need. Whether you're looking for specific content or general guidance on FPGA, Verilog, or CNES-related topics, this section provides clear instructions and support to enhance your browsing experience.

In addition to navigation assistance, the help page also serves as a resource hub where you can access important documents. This includes the ability to view and download relevant materials directly, ensuring you have the necessary information at your fingertips. Whether you're a beginner exploring FPGA technology or an experienced user seeking in-depth details, this page is structured to provide comprehensive support.

Launch the website

To launch the website, you have to:

1. Open your control terminal
2. Write the following commands:

```
# move on the backend folder  
cd src/backend
```

```
# install all dependencies  
npm install
```

```
# launch the server  
node app
```

3. Launch your preferred navigator
4. Type the following link:

```
localhost
```

5. Select the "Main Page" one

Main Page

Open it

If you have just arrived on the site, you are automatically there.

If you have already browsed the site, to return to the main page, you have to :

- Click on “FPGA Explorer” tab in the navigation bar

Interaction

You can interact with the FPGA board to learn information of each components of the board.



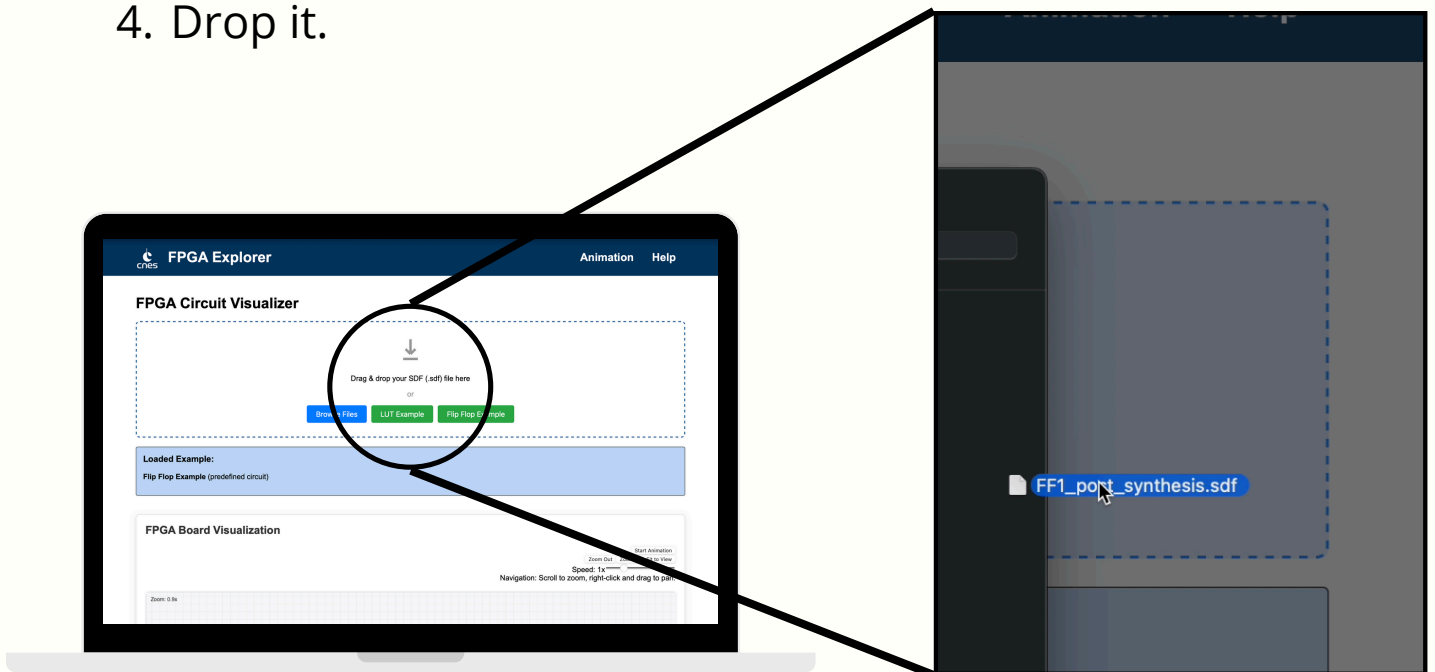
Load a file

Drag & Drop

You are on the “Animation” page.

To load files using the drag and drop, you have to:

1. Click on the “Browse Files” button.
2. Maintain the click on the file with the SDF (.sdf) extension.
3. Drag the file into the defined area in the background.
4. Drop it.



Replace the current file

To replace the current files, you have to load other files.



If you can't use the drag & drop, you can also click on the file and upload it.

You can see the file you have uploaded in the “Loaded Files” box.



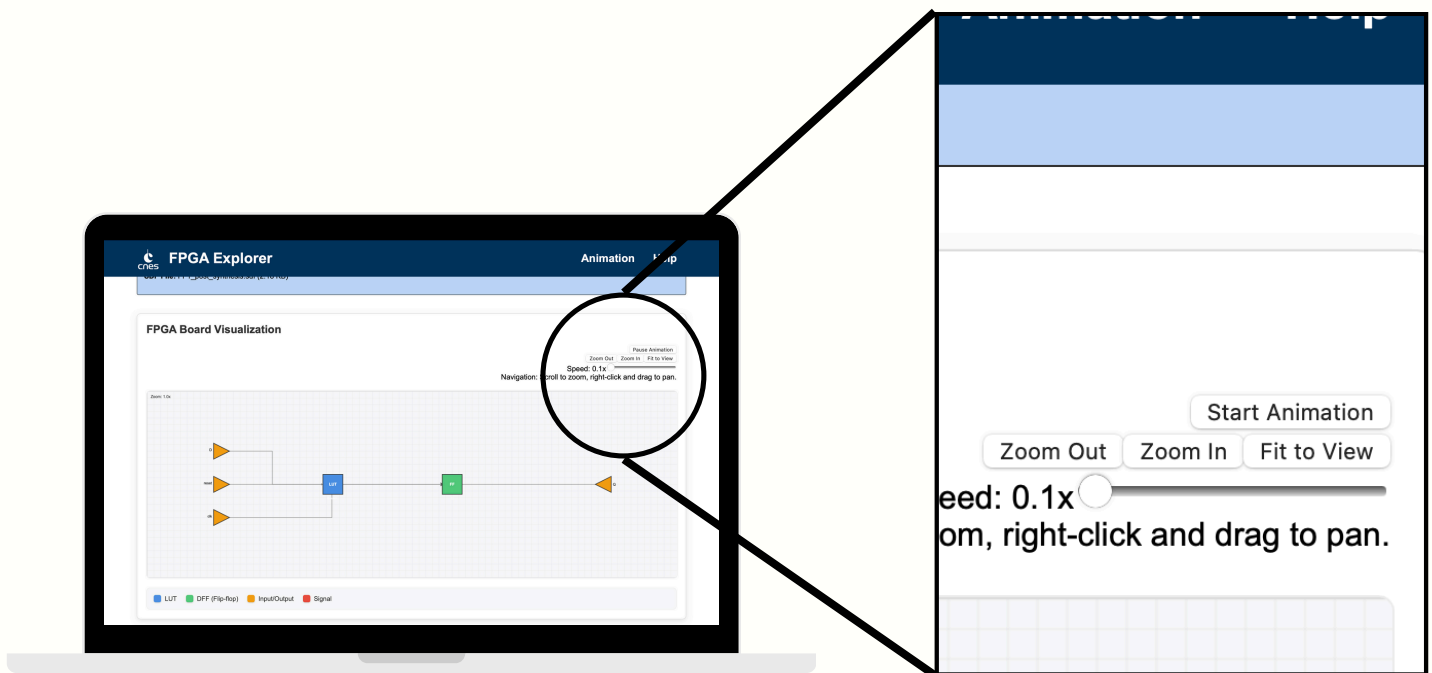
The two green buttons are some example some see before utilization.

Play animation

Start

To start the animation, you have to:

- Click on the “Start Animation” button.



You can only start the animation when the file is load.

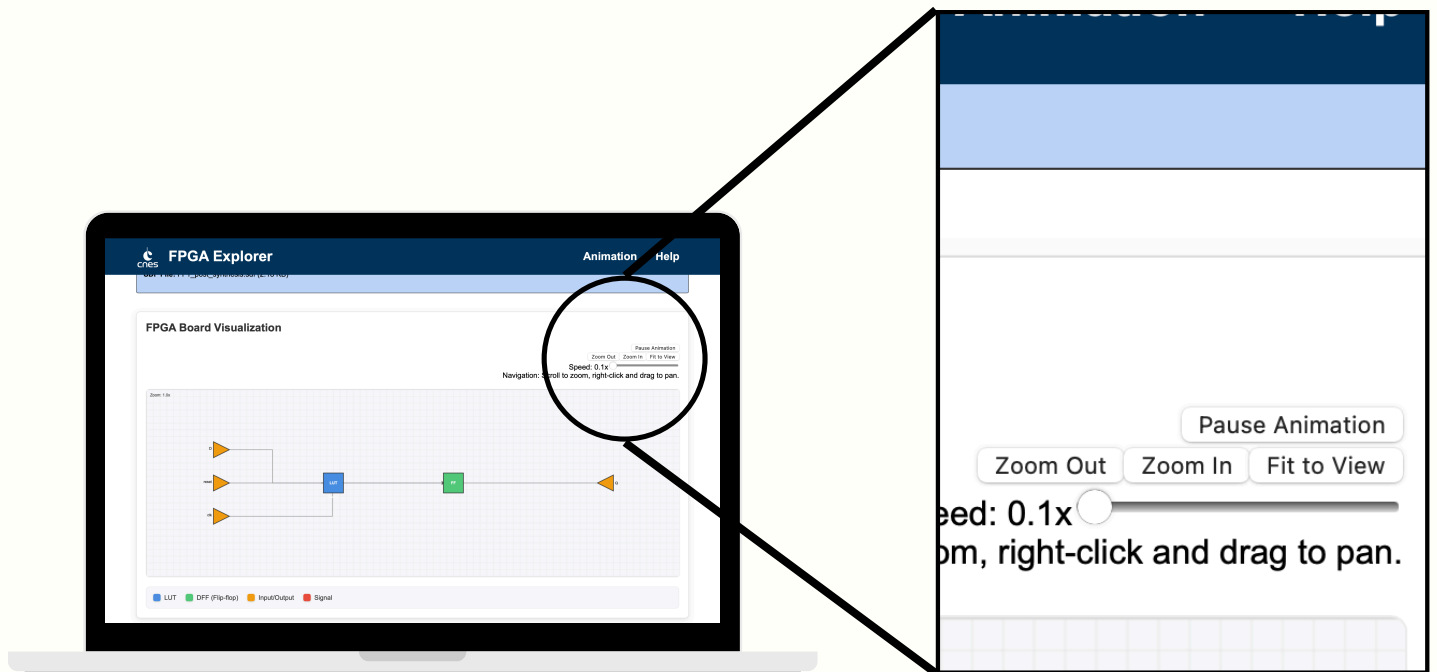


You can find the color index of the schema a the bottom of the “FPGA Board Visualization.

Stop

To start the animation, you have to:

- Click on the “Pause Animation” button.

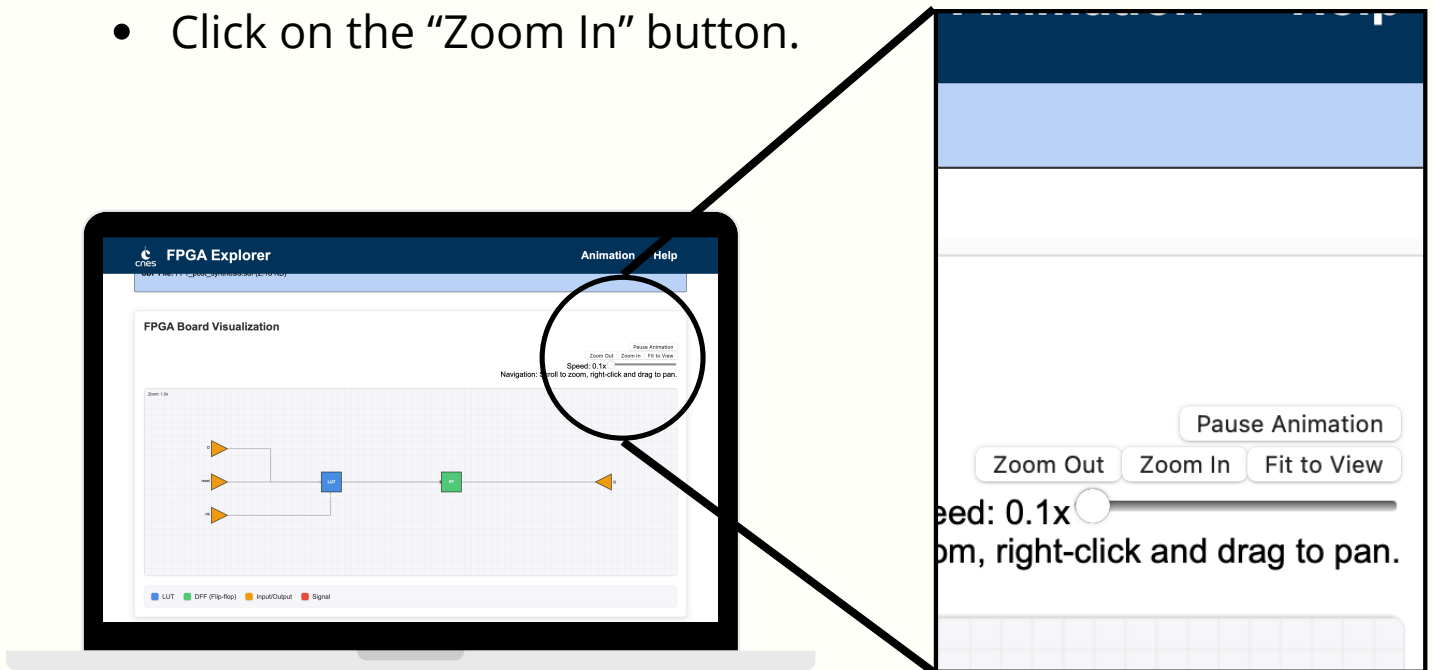


Modify the view

Zoom

To zoom, you have to:

- Click on the “Zoom In” button.

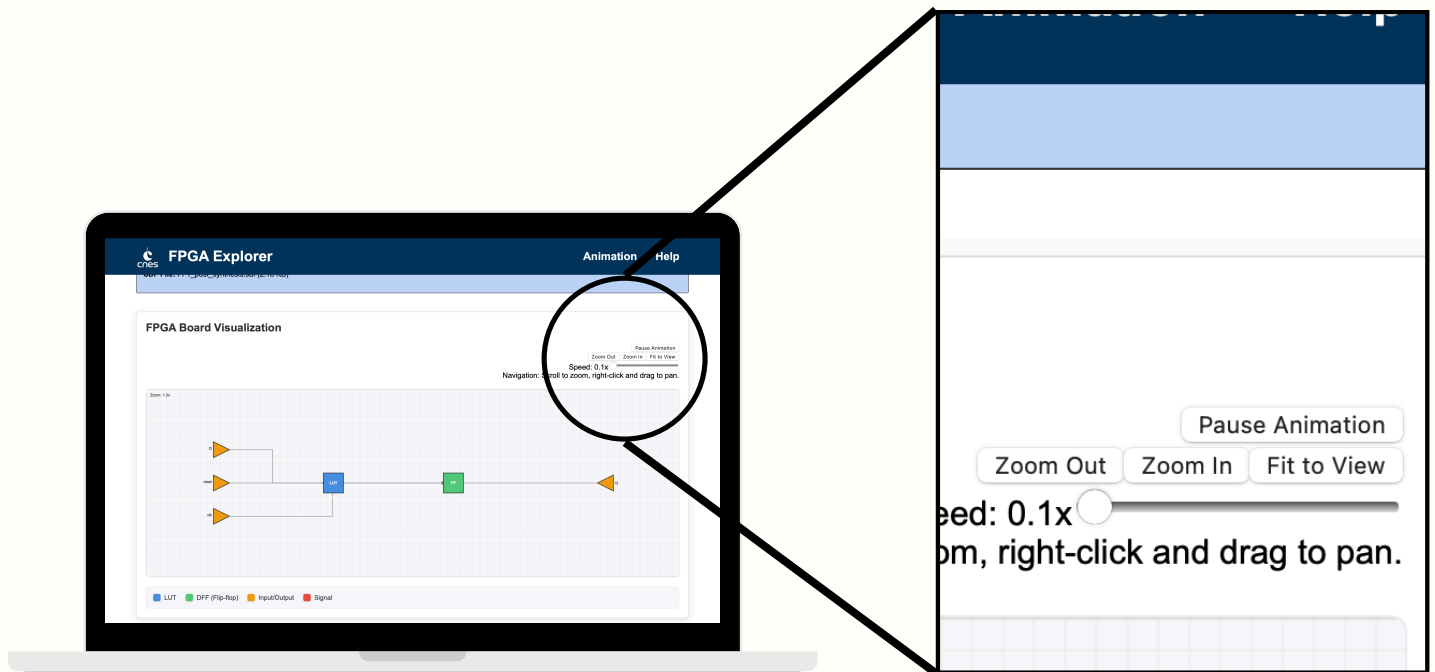


You can only zoom on the animation when there is at least one file uploaded.

Unzoom

To unzoom, you have to:

- Click on the “Zoom Out” button.



Fit to the view

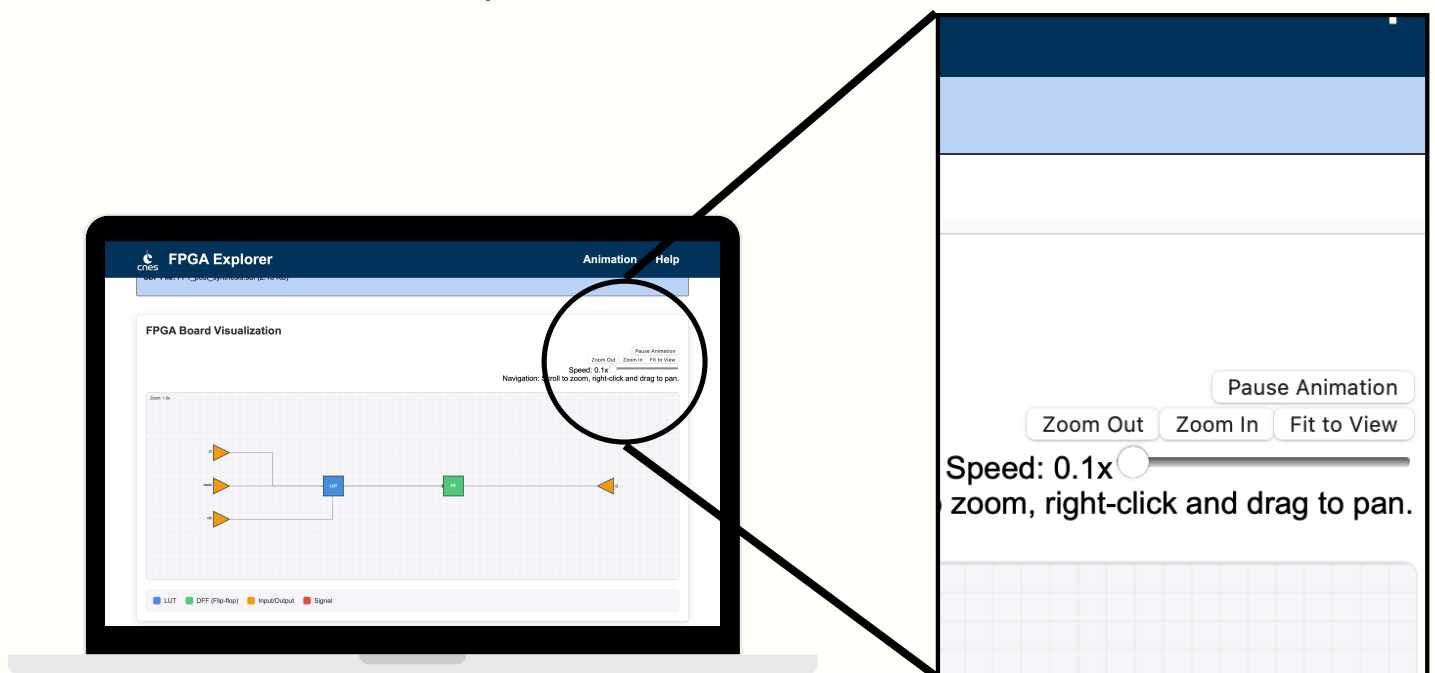
To fit to the view, you have to:

- Click on the “Fit to View” button.

Modify the speed

To modify the speed of the animation, you have to:

- Move the cursor to the left to decrease or to the right to increase the speed.

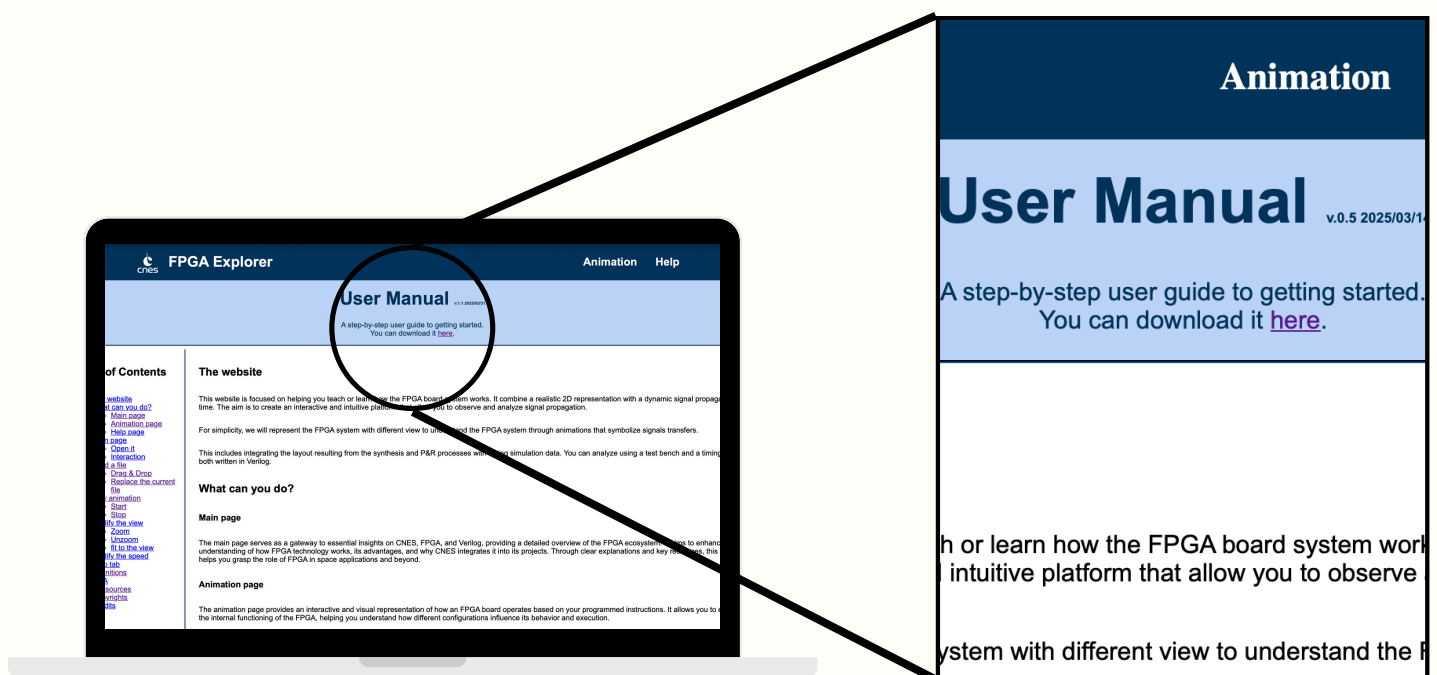


Help tab

Download the Guide

To download the user guide, you have to click on the link “here”.

The file is now on the download folder of your computer. You can print it and read it whenever you want.



Definitions

Here are the definitions of words whose meaning is important to know:

| Word | Definition |
|------------|---|
| FPGA | A Field-Programmable Gate Array is an integrated circuit with basic elements and preconfigured electrical signal routes between them. |
| netlist | A netlist is like a recipe for building an electronic circuit. It tells you what components you need and how to connect them together to create a functioning circuit. |
| P&R | Place and Route is the packing of the netlist component in the FPGA available BEL (Place). Then a route for signals between each BEL is selected (Route). A timing netlist is created and can be exported in Verilog. |
| test bench | A test bench is a crucial tool in the design and verification process, helping to ensure that digital circuits and systems function correctly before they are manufactured. |
| Verilog | Verilog is a language used to program a system using the FPGA layout. It use to writting instruction to the system. |

Q&A

Here are the most frequently asked questions:

| Questions | Answers |
|---|--|
| How can we navigate on the website? | You can navigate the website using the navigation bar at the top. |
| Do we need a real FPGA board to work? | The website is a tool to allow you to work, train, and learn about FPGA without a FPGA board. |
| What is the difference between an FPGA and a microcontroller? | A microcontroller executes a program sequentially, whereas an FPGA can be used to implement configurable digital hardware that operates in parallel, offering better performance for certain applications. |
| What is the difference between VHDL and Verilog? | VHDL is more structured and used in Europe and in aerospace, whereas Verilog is closer to C and more popular in American industry. |
| Can artificial intelligence be used on FPGAs? | Yes, neural network models can be accelerated on FPGAs using optimised architectures and libraries such as Xilinx's Vitis AI. |

Ressources

How to code in Verilog?

To have more documentation about Verilog, you can search on the following site: www.nandland.com or buy "Getting Started FPGAs" from Russell Merrick

What is FPGA?

To have more information about FPGA, you can search on the following site: www.wikipedia.org/wiki/FPGA

Copyrights

Unless explicit mention is made of intellectual property held by third parties, the content of this site is offered under the following conditions Licence Etalab-2.0 that allows public information to be re-used free of charge. It grants users a non-exclusive and unlimited right, for commercial or non-commercial purposes, provided they mention the source and the date of update.

Users may :

- ✓ Copy, modify, adapt and create derived information
- ✓ Distribute, redistribute and commercially exploit the data.

They must simply cite the source and not mislead as to the origin or official status of the information.

The licence is compatible with other free licences (CC-BY, OGL, ODC-BY). It is governed by French law and does not guarantee the accuracy or continuity of the data.



The icons used for Tips, Warnings, and Informations were created by Freepik - Flaticon

Credits

Project Owner



Project development Team

from ALGOSUP's team 1

| | |
|--------------------------|------------------|
| Project Manager | Loic Nogues |
| Program Manager | Alexis Santos |
| Technical Leader | Yann-Mael Bouton |
| Software Engineer | Lucas Megnan |
| Quality Assurance | Mathis Lebel |
| Technical Writer | Gregory Pagnoux |