



USER MANUAL

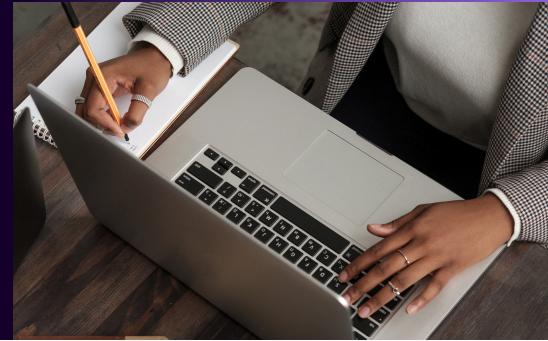


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Introduction

Purpose

This manual provides comprehensive guidance for using SPIN (Signal Propagation Inspector), our web-based FPGA simulation tool. SPIN is designed to simulate and visually display signal propagation within an FPGA board, making it easier for users to understand the inner workings of FPGA architectures. This document covers everything you need to launch the project, access the web interface, navigate its features, and initiate simulations effectively.

Scope

SPIN offers an intuitive visualization of real-time signal behavior on an FPGA board, serving as an educational tool for individuals who may not be familiar with FPGA technology. The primary objectives of SPIN are to:

- **Educate:** Introduce and clarify how signals propagate through an FPGA board.
- **Demonstrate:** Provide hands-on examples of FPGA functionality through simulation.

Getting Started

In the part below is presented how you can access our website.

1. Minimum Hardware Configuration

- **Processor:** 1 core x86_64 or ARM64.
- **RAM:** 1 GB
- **Storage:** 20 GB SSD

2. Compatible Operating Systems

- **Linux**
- **Windows 10/11**
- **MacOS (mojave minimum)**

3. Required Software

Languages & Runtimes:

- Node.js

4. Installation Guide

In your terminal:

1.Clone the repository

```
git clone  
https://github.com/algosup/2024-2025-  
project-4-web-fpga-team-5
```

2.Navigate to the directory

```
cd  
2024-2025-project-4-web-fpga-team-5
```

3.Install dependencies

```
npm i
```

4.Run the application

```
npm run main
```

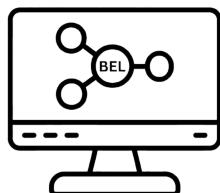
5. Accessing The Application

The application is now available at the following address:

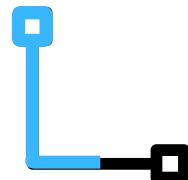
```
https://localhost:5173
```

Overview Of The FPGA Simulator

Key Features And Functionalities



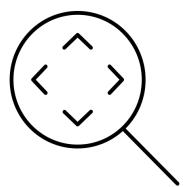
2D floorplan visualization



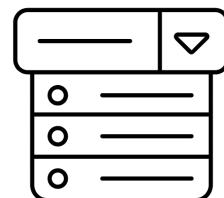
Real-time signal propagation



Interactive simulation controls



Zoom and pan



Preloaded examples

Visualize Or Create

This dual-mode approach allows all users whether learners or advanced designers to either explore existing examples or craft custom simulations based on their own designs.

Get Started

Visualize

Create

Visualize existing FPGA designs or create your own from scratch

- **Visualize:** Select from preloaded examples to explore how signals propagate in different FPGA setups.
- **Create:** Upload your own Verilog and testbench files to generate new examples. Once created, these examples appear in the list alongside any preloaded ones.

User Interface Overview

Main Dashboard

Upon launching the application and choosing your mode you'll have access to different features :

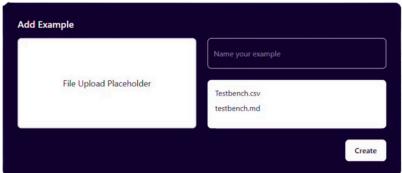
Visualize mode

| | |
|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|
|  | Example Selection: Choose from a list of existing preloaded examples. |
|  | Simulation Controls: Use the reset, play, pause, step, and speed-adjustment buttons to view how signals propagate across the FPGA. |
|  | Zoom & Pan: Focus on specific regions of the FPGA floorplan to observe timing and routing details. |



Once in the visualization screen, use your mouse or touch gestures to zoom and pan across the FPGA. This helps in closely examining signal paths and delays.

Creation mode

| | |
|-----------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------|
|  | File Upload: Select a Verilog file and a corresponding testbench file. |
|  | Naming Your Example: Assign a name to your newly created example for easy identification. |
|  | Example Management: Once created, your custom example appears in a table where you can edit or delete it. |
|  | Visualization: Switch to the visualization interface, where you can see your newly created example along with any preloaded ones. |



At any time, you can return to the main dashboard to select a different example or create another one.

Visualize Preloaded Examples

Selecting Preloaded Examples

The Visualize section allows you to explore preloaded FPGA simulations with a 2D floorplan and signal propagation.

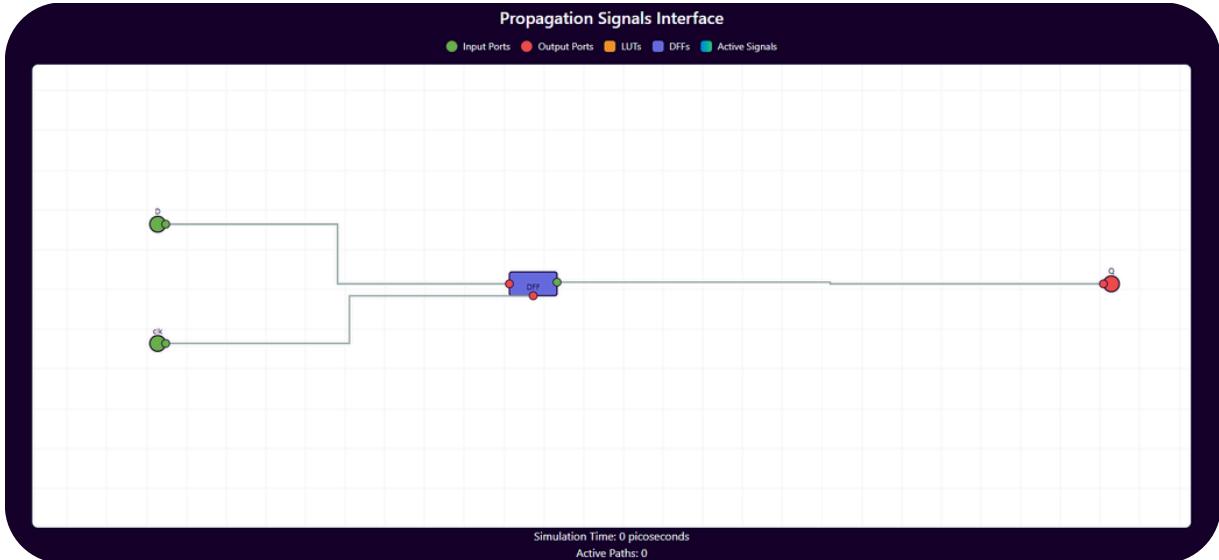
To select an example :

1. Open the dropdown menu at the top of the page.
2. Choose from the available examples (e.g., "1ff_VTR," "2ffs_VTR," etc.).

If you have created your own simulations, they will also appear in this menu for easy access.

2D Floorplan View

This interface provides a graphical representation of the FPGA's internal components (BELs) and the signal paths connecting them. The image below illustrates how signals propagate through various elements in real time:



Color-Coded Elements

- **Input Ports** (green labels) are entry points where external signals enter the FPGA.
- **Output Ports** (red labels) are endpoints where processed signals exit the FPGA.
- **LUTs** (orange blocks) represent Look-Up Tables, which perform combinational logic.
- **DFFs** (blue blocks) are Flip-Flops, which store and synchronize data on clock edges.
- **Active Signals** (highlighted lines) indicate the paths currently propagating signals.

Signal Tracing

Each line connecting the blocks shows a **route** that signals take when traveling between **components**. It reflects the simulated real-time propagation timing based on the time a **BEL** takes to reach each other matching their distance in the FPGA board.

Simulation Time & Active Paths

Below the floorplan, you'll see information like **Simulation Time** and **Active Paths**. These metrics help you track how long the simulation has been running and how many distinct signal routes are currently active.

Simulation Controls

After selecting an example, you'll have access to a panel of tools within the simulation interface, below is a description of the main buttons :

▶ **Play:** Starts the simulation for the selected preloaded example, initiating the real time display of signal propagation.

⏸ **Pause:** Temporarily stop the simulation and then resume it from the same point.

▶ **Step:** One click advances the simulation, enabling you to observe the transition of each electrical signal (represented by a line). You can also move back to review previous steps (the number of steps represent the number of clock cycle).

1 × Speed: click on it to adjusts the simulation speed to 0.001*, 0.01*, or 0.1* or 1*.

⟳ **Reset:** Erase the current state of the propagation signal of the simulation and restart it from the beginning.

⤢ **Full page:** Increase the size of the simulation to fill the size of your screen.

I/O Hide I/O labels: Remove or show the name of the inputs and outputs

Interactive Features

The simulation interface is navigable, and the following features can be used to drive inside it :

🔍 **Zoom:** Click on the magnifying glass icons to adjust the zoom level, allowing you to focus on specific areas or view the entire FPGA layout.

🖱️ **Pan:** Click and drag within the simulation area to move across different regions of the FPGA.

Create Simulation

Uploading New Applications

If you want to create your own simulation, the "Create" section allows you to upload and manage custom examples.

To upload a new example :

1. Select "Create" on the homepage.
2. Provide the testbench and Verilog application files.
3. Enter a name for your example.
4. Click "create" to upload your simulation.

Right File Format

Before creating a new simulation, ensure that your files meet the following requirements:

- **Verilog application :** Must be a netlist schematic in a Verilog (.v) format.
- **Testbench :** Must be a Standard Delay (SDF) file with a .sdf format.

Supported FPGA Models

Our simulator is designed to be flexible, supporting at least two primary FPGA architectures:

- **NanoXplore NGultra:**

This is our main target FPGA model. The netlist and timing files generated for NGultra devices can be visualized in the simulator, showing how signals propagate within the specific architecture.

- **Xilinx Series 7 (via VTR Flow):**

When using the VTR (Verilog-to-Routing) flow, the simulator can also interpret netlists for a basic Xilinx Series 7 FPGA model. This provides an alternative viewpoint on how signals traverse different hardware layouts.

Troubleshooting

Common Issues

Simulation not starting

- **Potential causes:**
 - Missing or incorrectly formatted input files (Verilog netlist or SDF delay file), or incompatible FPGA model.
- **Solutions:**
 - Verify that your files follow the correct format and naming conventions.
 - Ensure the files are compatible with the selected FPGA model (e.g., NanoXplore NGultra or Xilinx Series 7).

Display errors

- **Potential causes:**
 - Incorrect file content or missing graphical elements.
- **Solutions:**
 - Check the netlist schematic to ensure all BELs are correctly represented.
 - Confirm that the SDF file accurately reflects timing delays.

Control buttons not responding

- **Potential causes:**
 - Browser compatibility issues or incomplete file uploads.
- **Solutions:**
 - Try refreshing the page or using a different browser.
 - Ensure that the simulation example is fully loaded before interacting with controls.

FAQs

Q: What should I do if my created simulation doesn't start?

A: Verify that your Verilog and SDF files adhere to the required formats, and check the compatibility with the FPGA model.

Q: How can I adjust the simulation speed?

A: Use the Speed control options (e.g., 1x, 2x, or 3x) provided in the simulation interface.

Q: Can I edit my created examples?

A: Yes, examples you create can be managed (edited or deleted) via the table at the bottom of the page.

Q: What browsers are supported?

A: The application works best on modern browsers. For the best experience, ensure your browser is up-to-date.