FPGA VISION

FPGA Visualization Platform

User Manual

Version 1.0.0

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1. Introduction

1.1 About the Platform

The FPGA Visualization Platform is an educational web application designed to help students learn about FPGA (Field-Programmable Gate Array) operations through interactive visualization. This platform provides a simulated environment for exploring digital designs without requiring physical FPGA hardware.

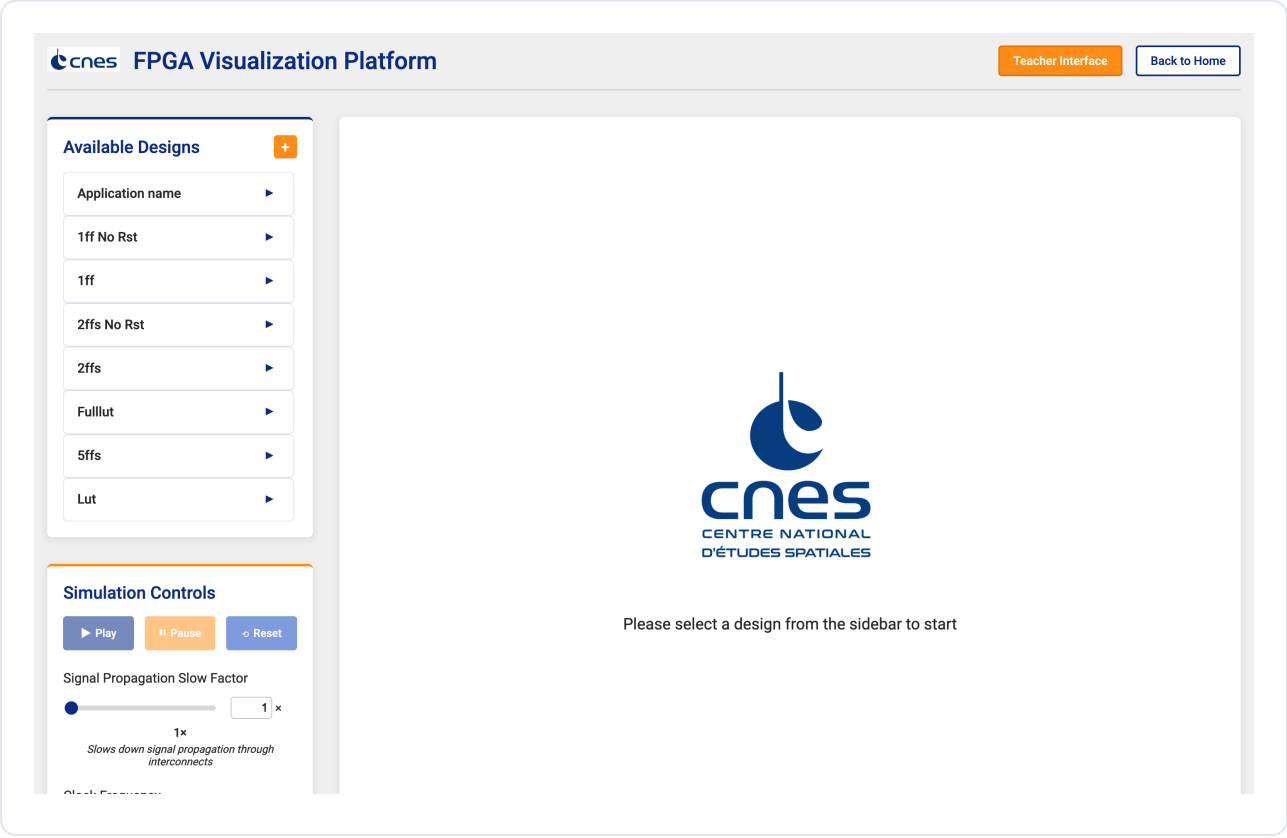


Figure 1.1: Main Platform Screen

What's an FPGA?

An FPGA is a programmable integrated circuit that contains an array of configurable logic blocks (CLBs) connected through programmable interconnects. FPGAs can be reprogrammed to implement different digital circuits, making them flexible platforms for hardware design education and prototyping.

1.2 Main Features

Interactive Design Visualization

See 2D visualization of BELs (Basic Elements of Logic) inside the FPGA

Run Simulations

Test designs with adjustable clock frequency and signal propagation speeds

Track Signal Flow

Observe how signals propagate through the circuit with visual indicators

Multiple Layout Views

Toggle between grid, hierarchical, or force-directed layouts

Dual Interface Design

The platform provides separate interfaces for students (focused on visualization and learning) and teachers (providing design upload and management tools).

1.3 System Requirements

To use the FPGA Visualization Platform effectively, ensure your system meets the following requirements:

Item	Minimum	Recommended
Browser	Recent Chrome, Firefox, or Safari	Latest Chrome or Firefox
Screen Size	1280 × 720	1920 × 1080 or larger
Internet	1 Mbps	5+ Mbps
RAM	4 GB	8+ GB
Processor	Dual-core 2 GHz	Quad-core 2.5+ GHz

Mobile Device Compatibility

While the platform is responsive, a desktop or laptop computer is strongly recommended for the best experience due to the complexity of the visualizations and the detailed interface controls.

2. Getting Started

2.1 Accessing the Platform

The FPGA Visualization Platform is a web application that runs directly in your browser without requiring installation or login.

1 Open the Platform

Navigate to the platform's URL in a modern web browser like Chrome, Firefox, or Safari.

2 View the Home Screen

The home screen presents two main options: Student Interface and Teacher Interface.

3 Choose Your Interface

Select either "Enter Student Interface" or "Enter Teacher Interface" based on your role.

No Installation or Registration Required

The platform operates entirely in your web browser - no downloads, installations, or account creation is needed to get started.

2.2 User Interface Overview

The platform features a clean, intuitive interface designed to help you focus on learning FPGA concepts.

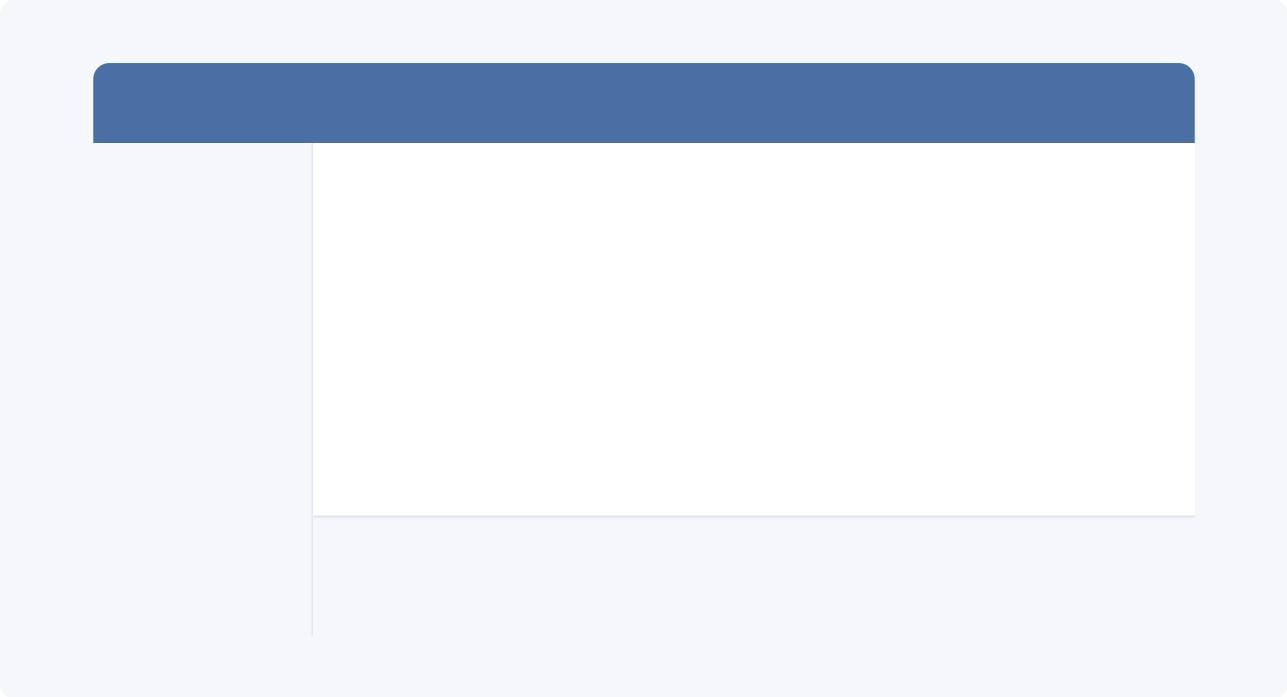


Figure 2.1: Main Interface Layout

Main Interface Components

Component	Function
Header Bar	Contains the application logo, title, and navigation links between interfaces
Sidebar Panel	Lists available designs and provides simulation controls
Main Visualization Area	Displays the active FPGA design with interactive components
Controls Panel	Provides tools for simulation speed, layout options, and other settings

2.3 Navigating Between Interfaces

The platform provides two specialized interfaces, each designed for different user needs.

Student Interface

- Browse available FPGA designs
- View interactive circuit visualizations
- Run simulations with adjustable speeds
- Switch between different circuit layouts

Learn More

Teacher Interface

- Upload Verilog (.v) and SDF (.sdf) files
- Add descriptions with Markdown suppo
- Export and import designs as package
- Manage the design library

Learn More

Switching Between Interfaces

You can easily switch between the Student and Teacher interfaces at any time using the navigation buttons in the header bar.

3. Student Interface

3.1 Overview and Layout

The Student Interface provides a simplified environment focused on visualization and simulation of FPGA designs. This interface is optimized for learning and exploring existing designs.

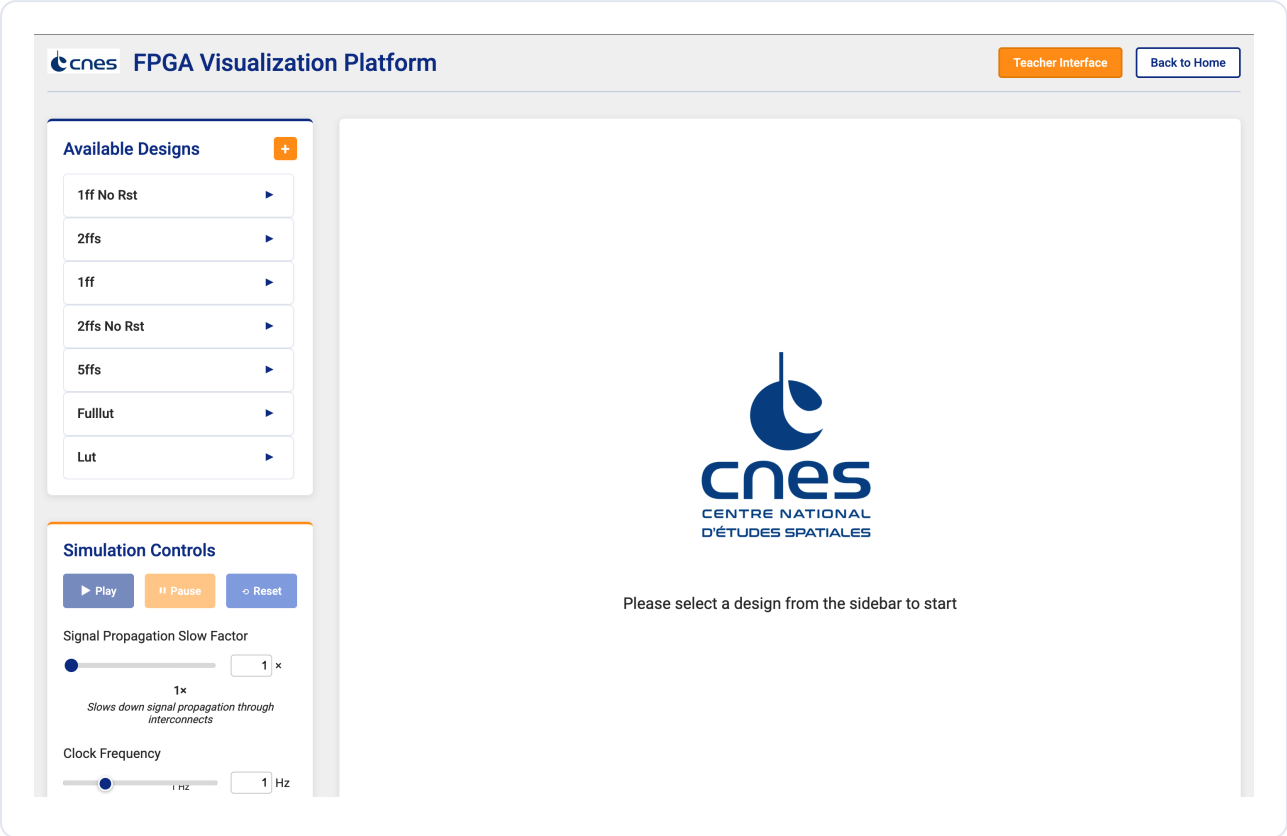


Figure 3.1: Student Interface Main View

The Student Interface is divided into three main areas:

Area	Description
Design Selection Panel	Browse and select available FPGA designs from the library
Visualization Canvas	Interactive area displaying the FPGA components and connections
Control Panel	Tools for simulation control, speed adjustment, and clock frequency settings

3.2 Selecting a Design

The platform allows you to explore FPGA designs that have been added to the design library. Follow these steps to select and load a design:

1 Browse Available Designs

Review the list of designs in the left sidebar. Each entry shows a name and can be expanded to view its description.

2 View Design Details

Click the arrow icon next to a design to expand and read its description.

3 Select a Design

Click on the design name to load it into the visualization canvas.

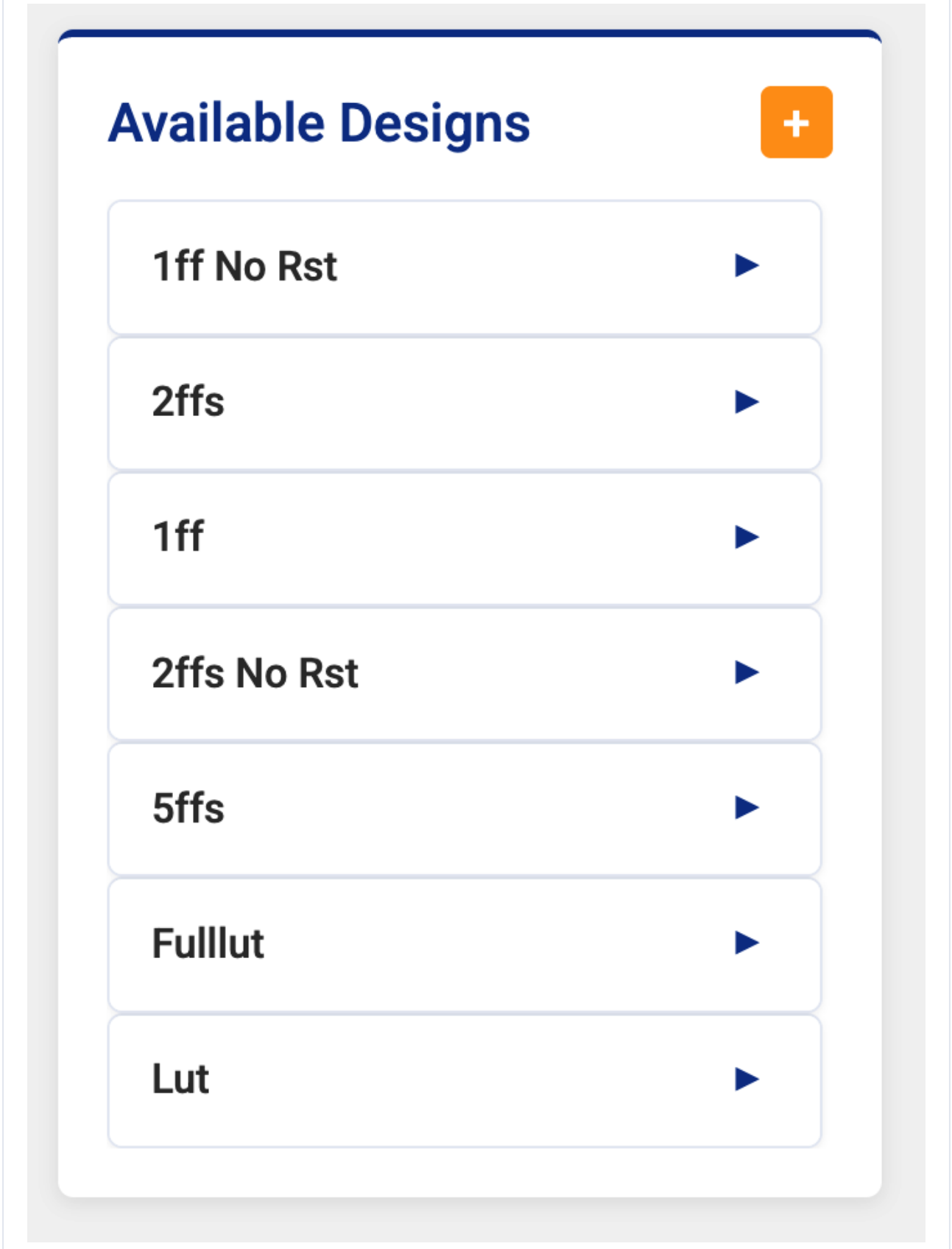


Figure 3.2: Design Selection Panel with Available Designs

Design Information

Each design includes a description that helps you understand its purpose and functionality. These descriptions may contain markdown-formatted text with educational objectives and explanations.

3.3 Visualization Controls

The platform provides various controls to navigate and interact with the FPGA visualization.

Zooming and Panning

Action	Mouse Control	Touch Control
Zoom In/ Out	Mouse wheel scroll	Pinch gesture
Pan View	Click and drag empty space	Touch and drag with one finger

Component Inspection

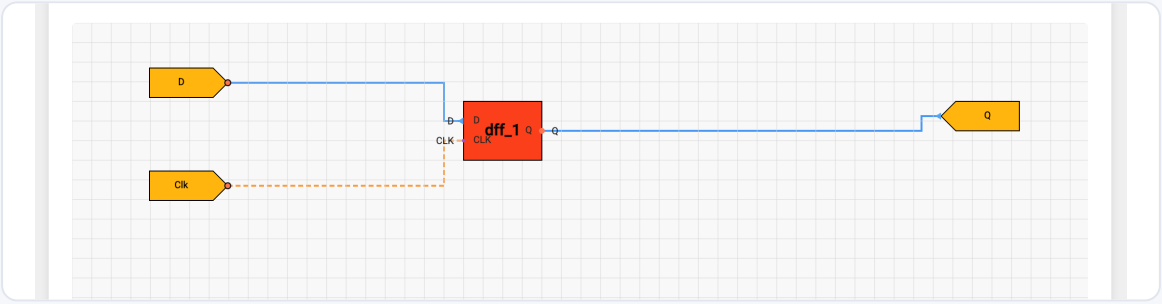
To inspect individual components in the visualization:

- Hover over components to see tooltips with component details
- Click on a component to focus on it
- Observe signals as they flow through the design during simulation

Layout Options

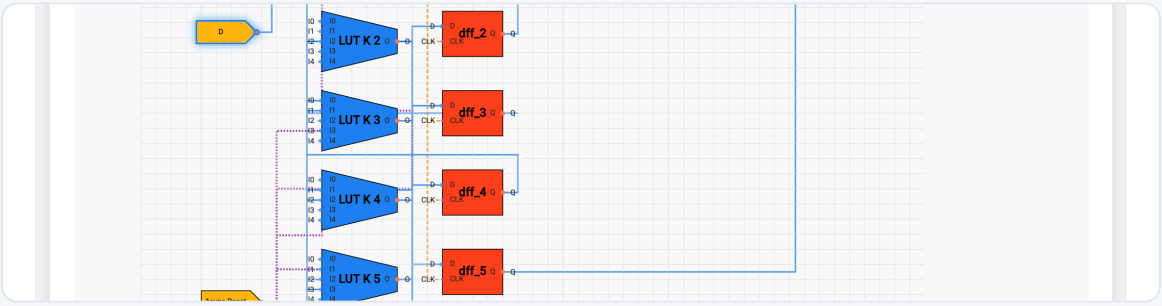
The visualization offers multiple layout options to help you understand the design from different perspectives. You can select different layouts from the visualization controls:

Grid Layout



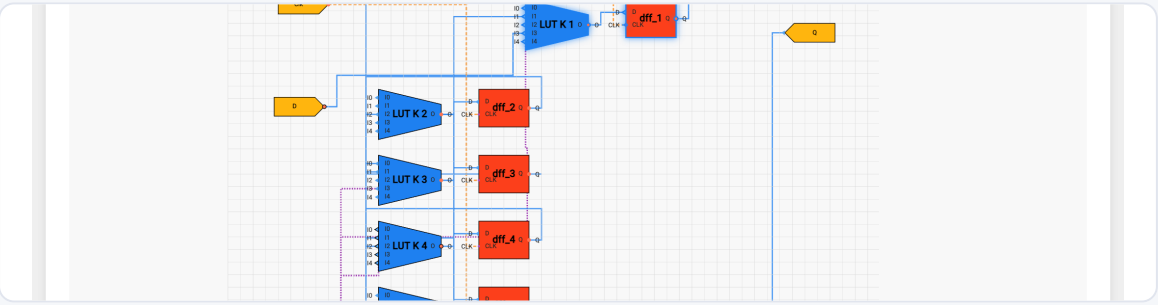
Organizes components in a neat grid pattern. Best for getting an overview of all components.

Force-Directed Layout



Positions components based on their connections, bringing related components closer together.

Hierarchical Layout



Displays components in a top-down hierarchy based on signal flow, with control signals like clock and reset specially positioned.

3.4 Simulation Controls

The simulation controls allow you to observe the behavior of the FPGA design over time as signals propagate through the components.

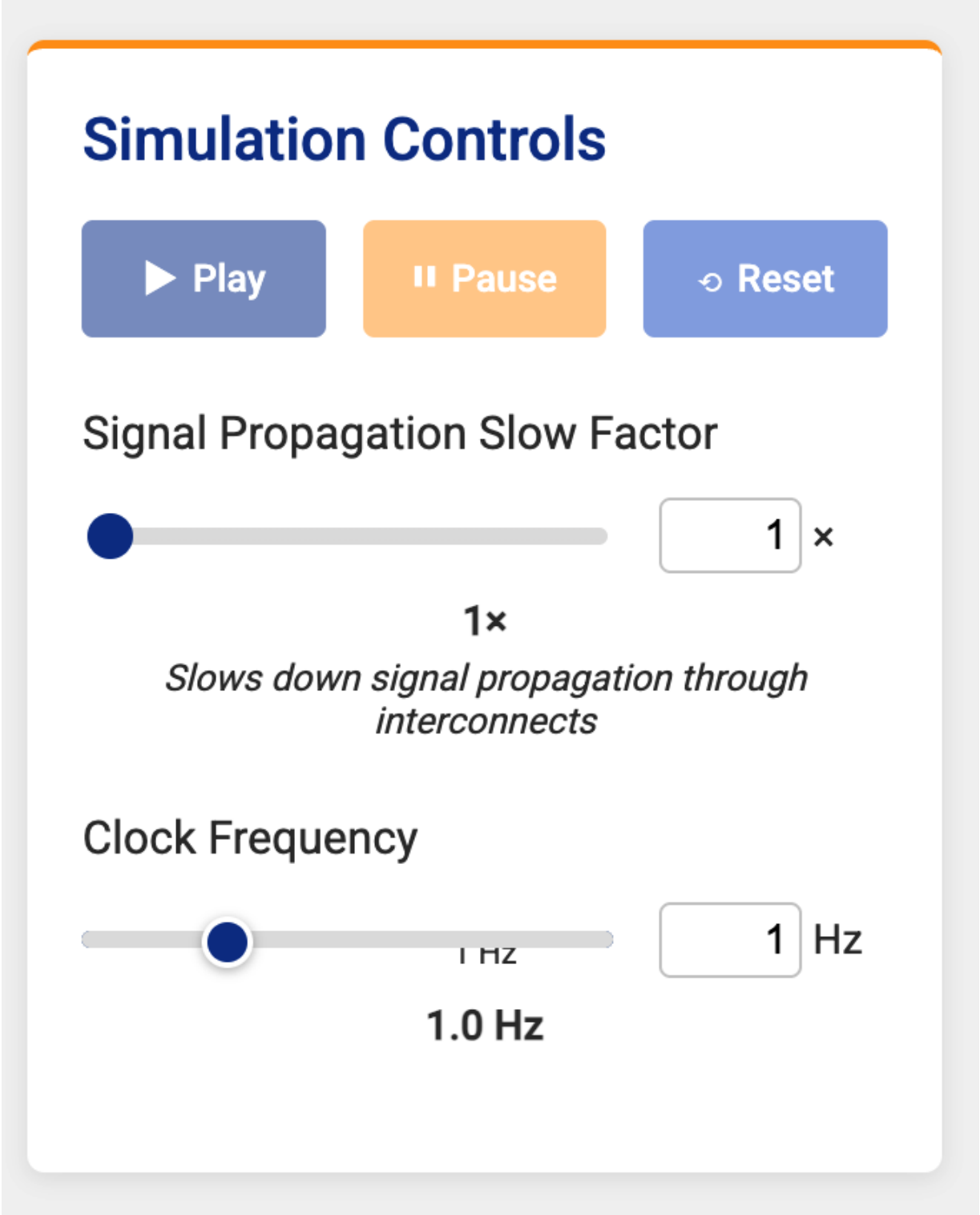


Figure 3.3: Simulation Control Panel

Basic Simulation Controls

Control	Function
Play	Start the simulation
Pause	Pause the running simulation
Resume	Continue a paused simulation
Reset	Reset the simulation to its initial state

Simulation Speed Controls

The platform offers two main controls for adjusting simulation speed:

- **Signal Propagation Slow Factor**: Controls how much to slow down signal propagation through interconnects (higher values mean slower simulation)
- **Clock Frequency**: Sets the clock frequency for the simulation (in Hz)

Understanding Simulation Controls

For learning purposes, the simulation intentionally slows down signal propagation so you can observe how signals move through the design. The propagation slow factor adjusts this behavior, while the clock frequency controls how fast clock signals are generated.

4. Teacher Interface

4.1 Overview and Layout

The Teacher Interface provides tools for creating and managing FPGA design libraries that students can access. Through this interface, educators can upload Verilog designs, add educational descriptions, and organize teaching materials.

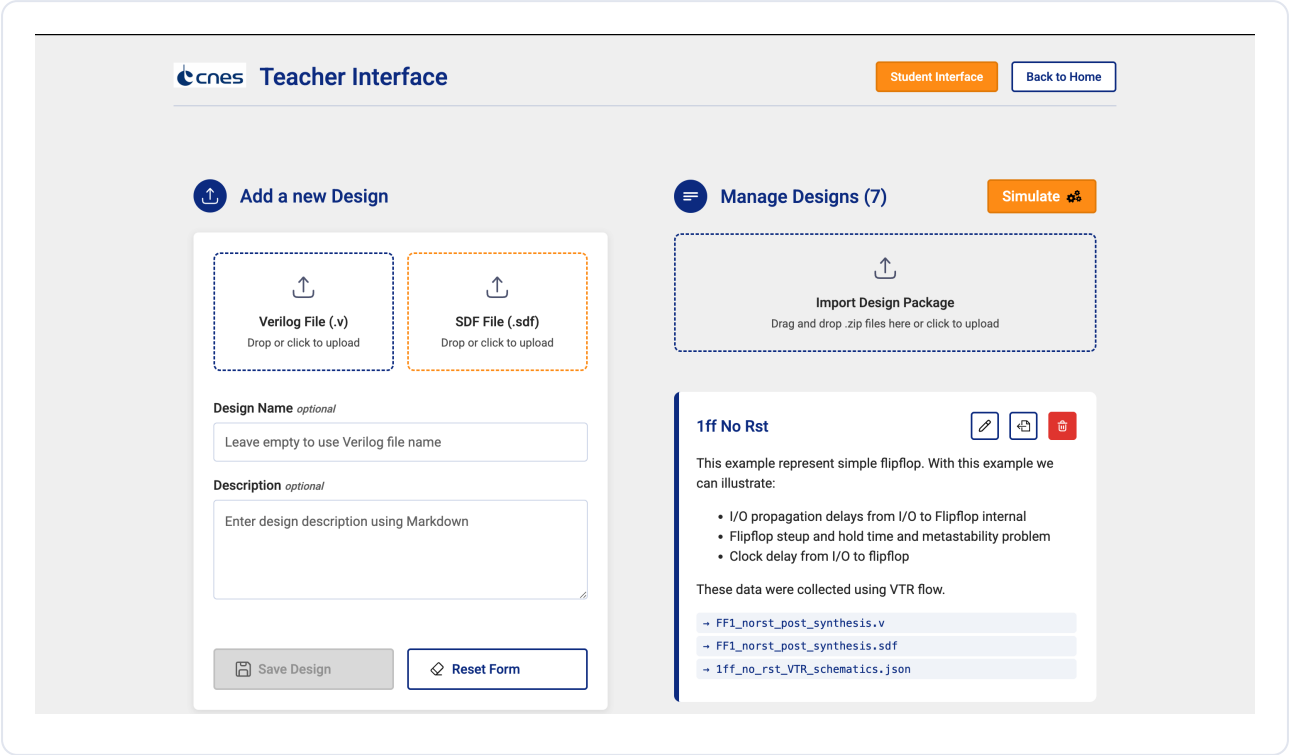


Figure 4.1: Teacher Interface Dashboard

Key Features of Teacher Interface

Feature Category	Available Tools	Purpose
Design Management	File Upload Interface Design Description Editor Design Preview	Create and maintain FPGA design collections
File Handling	Verilog (.v) Uploader SDF (.sdf) Uploader Drag-and-drop Support	Upload necessary design files
Import/Export	Design Package Exporter ZIP Import Functionality	Share designs between installations

4.2 Adding New Designs

Teachers can add new FPGA designs to the platform for students to explore and simulate. Follow these steps to add a new design:

1 Upload Design Files

In the "Add a new Design" section, upload both required files:

- Verilog File (.v): Contains the circuit design code
- SDF File (.sdf): Contains timing information for the design

2 Enter Design Details

Add a custom name (optional) and description for the design. The description supports Markdown formatting for rich text.

3 Save the Design

Click the "Save Design" button to process the files and make the design available to students.

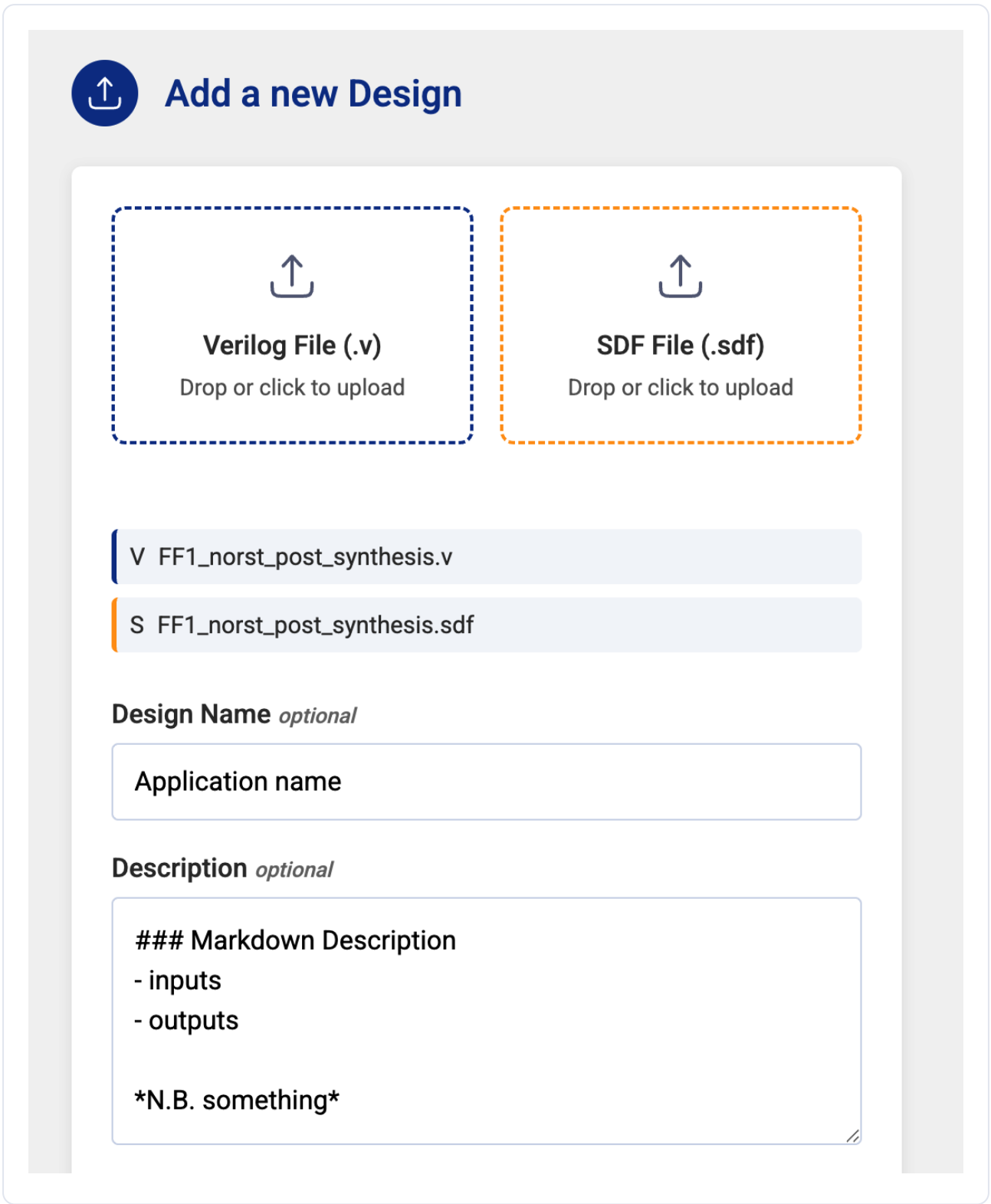


Figure 4.2: Form for Adding New Designs

File Requirements

Both Verilog (.v) and SDF (.sdf) files are required to create a complete design. The platform automatically processes these files to generate the visualization data.

Markdown Support

The description field supports Markdown formatting for rich text, including headings, lists, code blocks, and more. A preview is shown as you type.

4.3 Managing Existing Designs

The Teacher Interface includes tools for managing existing FPGA designs. Teachers can view, edit, and delete designs as needed.

Viewing Design Details

All designs are displayed in cards in the "Manage Designs" section. Each card shows:

- Design Name
- Description (in HTML format)
- List of associated files

Design Actions

For each design, you can perform the following actions:

- **Edit**: Update the design name and description
- **Export**: Create a portable design package
- **Delete**: Remove the design from the platform
- **View Files**: See the uploaded files associated with the design

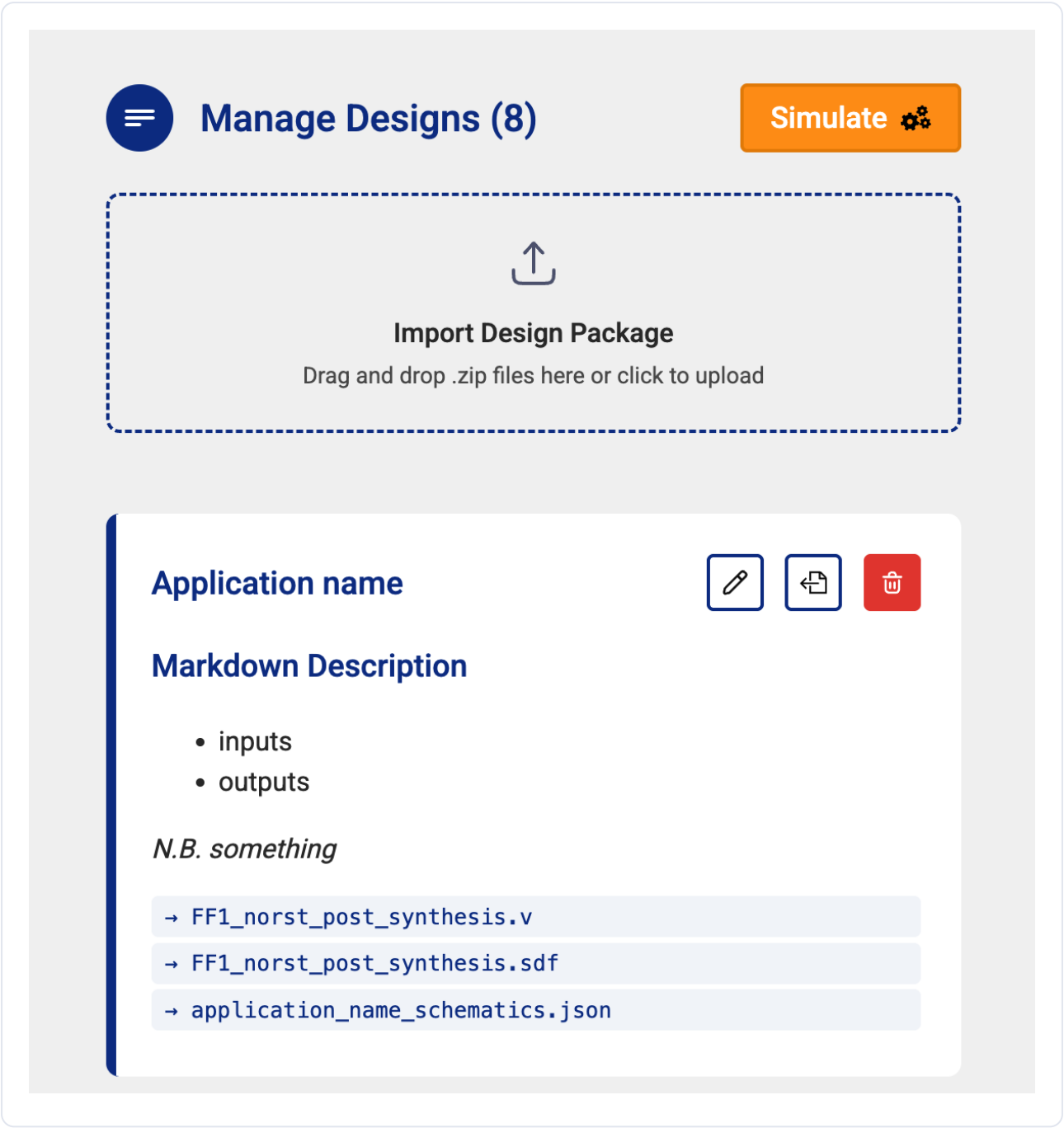


Figure 4.3: Interface for Managing Existing Designs

Editing Designs

When editing a design, you can update the name and description, but to change the Verilog or SDF files, you'll need to create a new design.

4.4 Importing Packaged Designs

The Teacher Interface supports importing and exporting designs, allowing for easy sharing between colleagues or different installations of the platform.

1 Exporting Designs

Click the "Export" button on any design card to download it as a ZIP package that includes all necessary files.

2 Importing Designs

In the "Import Design" section, click "Choose File" and select the ZIP package you wish to import.

3 Confirm Import

Review the details of the imported design and click "Import" to add it to your design library.

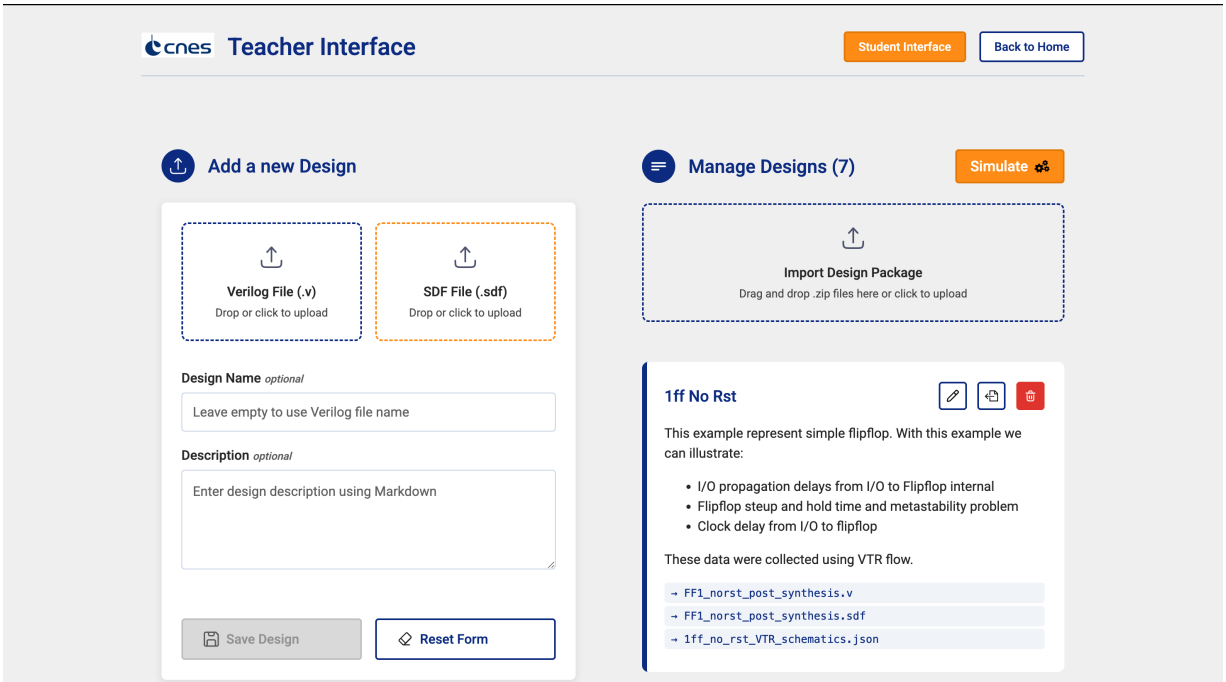


Figure 4.4: Interface for Importing and Exporting Designs

Package Format

Exported design packages are ZIP files containing the Verilog (.v) and SDF (.sdf) files, along with a manifest file that stores the design name and description. These packages can be easily shared with colleagues or transferred between different installations.

5. Understanding the Visualization

5.1 Components Representation

The FPGA Visualization Platform represents circuit components as simple geometric shapes with distinct colors to help you quickly identify different component types.

Component	Visual Representation	Description
Basic Logic Element (BEL)		Rectangular shape representing the fundamental processing units in the FPGA
Input Pin		Triangle pointing inward, representing entry points for signals into the design
Output Pin		Triangle pointing outward, representing exit points for signals from the design
Clock Generation		Special component that generates timing signals for synchronous operations

Tooltips for Details

Hover your mouse over any component in the visualization to see a tooltip with additional information, including the component name, type, and current state.

5.2 Signal Flow and Propagation

The platform visually represents how signals travel through your FPGA design, helping you understand the behavior of your circuit over time.

Understanding Signal Paths

Signals flow along the connections (lines) between components. The direction of signal flow is indicated by the design layout and simulation animation:

- Signals generally flow from inputs toward outputs
- During simulation, active signals are highlighted with animation effects
- Signal states (0 or 1) may be indicated by different colors

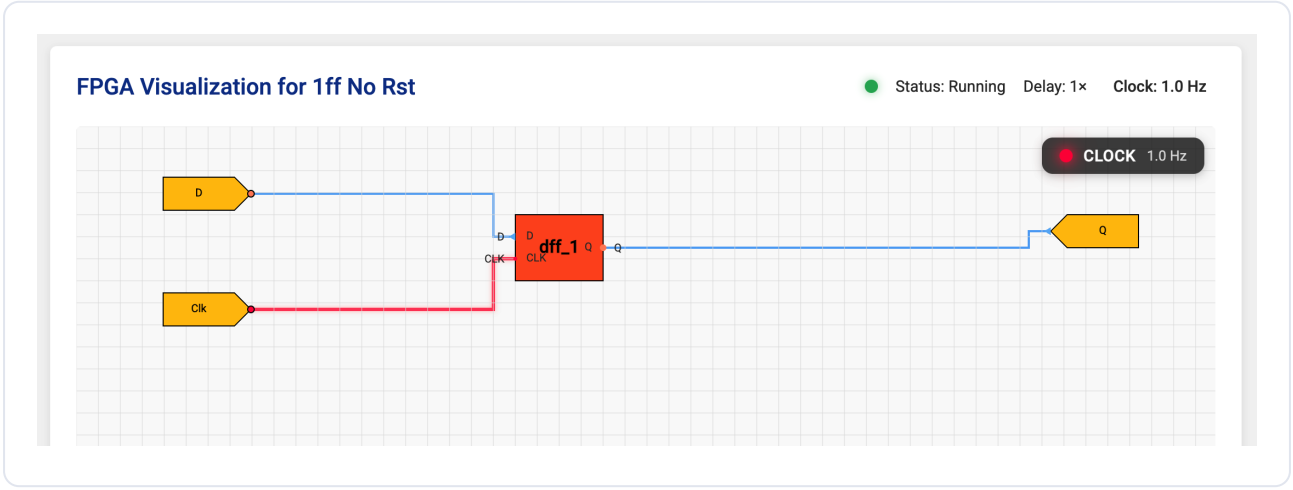


Figure 5.1: Animation showing signal propagation through components

Signal Propagation Timing

The simulation intentionally slows down signal propagation to make it visually traceable:

- Propagation delay is visualized through animated movement along connections
- Signals take time to travel from one component to another
- The propagation speed can be adjusted using the slow factor control

Educational Focus

Real FPGA signals propagate nearly instantaneously (nanoseconds). The platform's slower visualization is designed specifically for educational purposes to help you see and understand signal flow.

5.3 Connection Types

The visualization uses different line styles to represent various types of connections between components.

Connection Type	Visual Style	Description
Standard Connection		Solid line representing a normal signal path between components
Clock Network		Distinctively colored line showing clock signal distribution paths
Multi-bit Bus		Thicker line indicating multiple signals grouped together

Connection Direction

Even though connection lines may not always show arrows in the visualization, signal flow typically follows the design hierarchy from inputs to outputs.

5.4 Status Indicators

During simulation, various visual cues help you understand the current state of components and signals.

Indicator	Appearance	Meaning
Active Component		Highlighted component currently processing signals
Active Signal		Animated line showing signal propagation in progress
Logic High (1)		Indicates a connection carrying a logical "1" value
Logic Low (0)		Indicates a connection carrying a logical "0" value

The combination of these visual indicators allows you to trace signal flow and understand the behavior of your design during simulation.

Performance Considerations

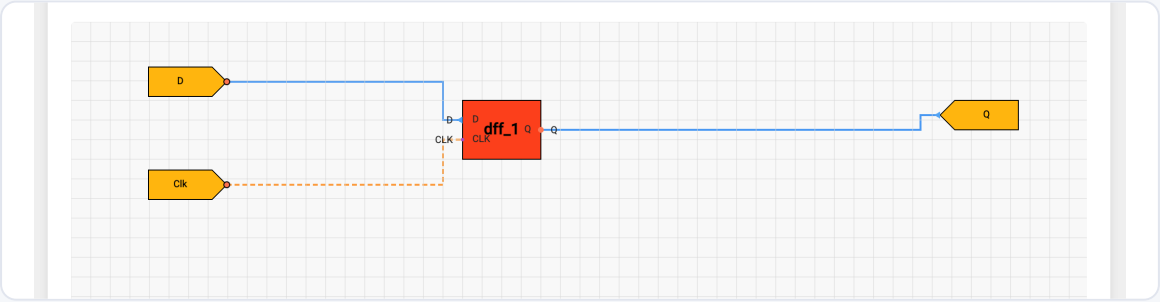
For complex designs with many components, the visualization may simplify some elements to maintain smooth performance. You can adjust the "Signal Propagation Slow Factor" to balance between visual detail and performance.

6. Advanced Features

6.1 Layout Options

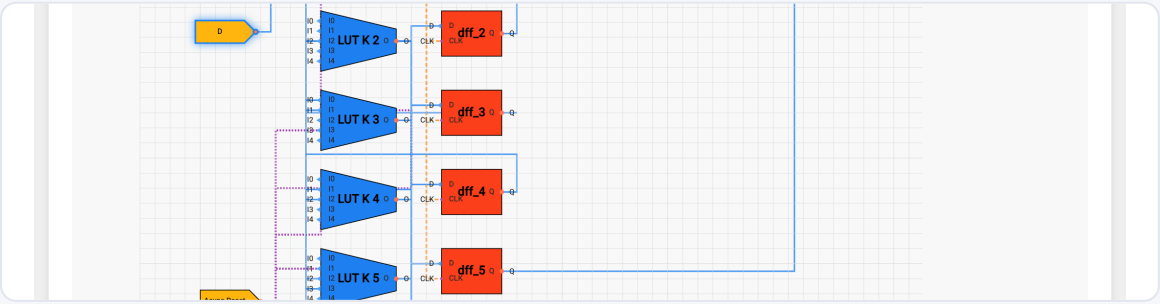
The visualization platform offers multiple layout options to help you understand circuit designs from different perspectives.

Grid Layout



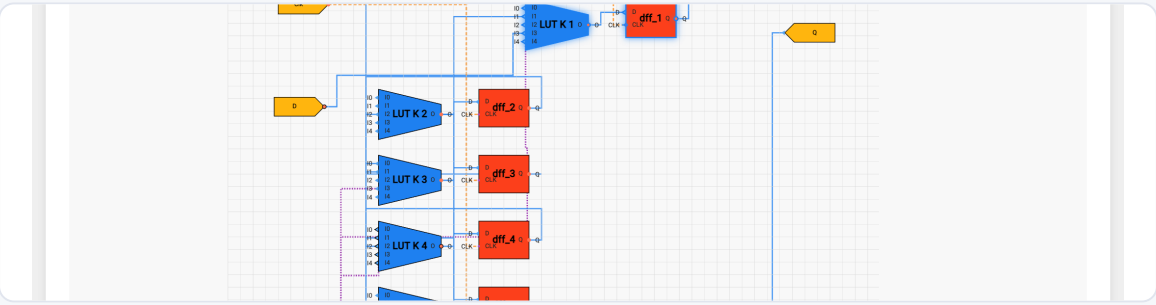
Arranges components in an organized grid pattern. This layout provides a clean, structured view that makes it easy to see all components.

Force-Directed Layout



Positions components based on their connections, creating organic clusters of related components. Connected elements are pulled closer together.

Hierarchical Layout



Organizes components in a top-down flow based on signal path directions, clearly showing the logical progression of signals through the design.

To change the layout:

1. Select a design in the Visualization Interface
2. Locate the layout selection controls in the settings panel
3. Choose your preferred layout type from the available options

Layout Performance

For complex designs with many components, the hierarchical and force-directed layouts may take longer to render. The grid layout generally offers the best performance.

6.2 Dark Mode

The platform provides a dark mode option that can reduce eye strain during extended use, especially in low-light environments.

Dark Mode Interface

Figure 6.1: Visualization Interface in Dark Mode

When dark mode is enabled:

- The background changes to a darker color
- Component and connection colors are adjusted for better contrast
- Text and UI elements adapt to be visible against the darker background
The dark mode setting applies across the entire visualization interface, enhancing readability while reducing the brightness of the display.

> **Visualization in Dark Mode**
>
> In dark mode, signal colors and component highlighting are automatically adjusted to maintain clear visibility and differentiation.

6.3 Keyboard Shortcuts

The platform includes several keyboard shortcuts to enhance efficiency when working with FPGA designs.

Action	Shortcut
Undo Last Component Movement	Ctrl + Z (or Cmd + Z on Mac)
Clear Component Selection	Esc
Multi-select Components	Shift + Click

> **Browser Integration**
>
> Some keyboard shortcuts may be intercepted by your web browser. If a shortcut doesn't work as expected, check if your browser has a conflicting shortcut assigned.

6.4 Multi-component Selection

The platform supports selecting multiple components simultaneously, allowing you to manipulate groups of components at once.

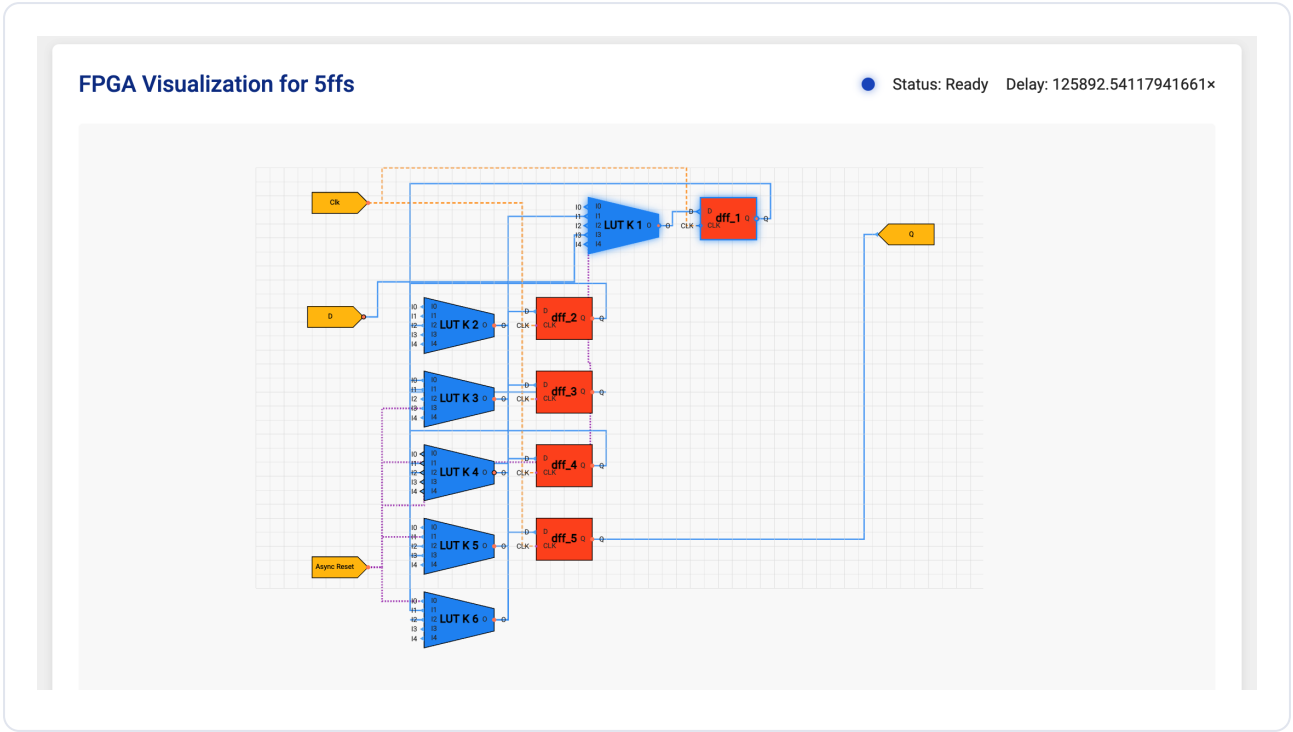


Figure 6.2: Multiple Components Selected in the Visualization

Selection Methods

There are several ways to select multiple components:

1 Rectangle Selection

Click and drag in an empty area of the visualization to create a selection rectangle. All components within or intersecting this rectangle will be selected.

2 Shift + Click Selection

Hold the Shift key while clicking on individual components to add them to the current selection. Click a selected component while holding Shift to remove it from the selection.

3 Working with Selected Components

Once multiple components are selected, you can move them as a group by dragging any of the selected components. The entire selection will move together, maintaining their relative positions.

Selection Visual Feedback

Selected components are visually highlighted with a blue border and drop shadow effect. This makes it easy to identify which components are currently selected.

Group Operations

When multiple components are selected, the following operations apply to all selected components:

- **Moving**: Drag any selected component to move the entire group
- **Deselection**: Click on an empty area or press Escape to deselect all components

Selection during Simulation

Component selection and movement are disabled during active simulations. You need to stop the simulation before you can select and manipulate components.

6.5 Connection Visualization

The platform provides enhanced visualization for different types of connections between components, helping you understand signal flow.

Connection Types

Connection Type	Visual Style	Description
Data Connection		Blue solid line representing standard data signal paths
Clock Connection		Orange dashed line showing clock signal distribution
Control Connection		Purple dotted line indicating control signals like reset

Connection State Visualization

During simulation, connections change their appearance based on signal state:

- **Inactive Connections**: Normal opacity and thickness
- **Active Connections**: Increased opacity, brightness, and glow effect
- **Animated Flow**: Active connections show signal propagation with pulse animations

Smart Connection Routing

The visualization uses an intelligent algorithm to route connections between components, avoiding overlaps with other components whenever possible. This creates a cleaner, more readable visualization.

7. Troubleshooting

7.1 Common Issues

This section covers specific issues you might encounter while using the FPGA Visualization Platform and provides practical solutions.

Issue	Possible Cause	Solution
Visualization not loading	Large design file or browser resource limitations	Try refreshing the page, closing other tabs, or switching to a different browser with better performance.
Simulation running too fast/slow	Clock frequency or propagation slow factor not set appropriately	Adjust the clock frequency (Hz) or signal propagation slow factor in the controls panel. Lower frequencies and higher slow factors will make signal propagation more visible.
Components don't respond to selection	Simulation is currently running	Stop the simulation before attempting to select or move components. Component selection is disabled during active simulations.
File upload errors on teacher interface	Missing required file or incorrect file format	Ensure you are uploading both a Verilog (.v) and SDF (.sdf) file. Check that the files are valid and properly formatted.
Connection lines not showing	Design missing proper connection definitions	Verify that your design files correctly define the interconnects between components. The platform needs proper connection data to visualize signal paths.

Browser Performance

The visualization uses advanced web technologies that can be resource-intensive. For the best experience, use a modern browser like Chrome or Firefox on a computer with sufficient RAM (at least 8GB recommended for complex designs).

7.2 Error Messages

Here are explanations and solutions for specific error messages you might see when using the platform:

Error Message	Meaning	Solution
"Error processing files"	The platform was unable to parse the uploaded Verilog or SDF files.	Check that your files follow the correct syntax and format. Try validating them with an external tool before uploading.
"Please select both Verilog and SDF files"	One or both required files are missing during design upload.	Make sure you've selected both a Verilog (.v) file and an SDF (.sdf) file before attempting to save a design.
"No data to visualize"	No design is currently selected or the design contains no visualizable data.	Select a design from the design list, or if the issue persists, check that the design contains proper component and connection definitions.
Connection-related errors in console	The platform is having trouble finding connection points between components.	This is likely due to issues in the design file. Ensure that interconnects are properly defined in your source files.

Checking Browser Console

If you encounter issues, checking the browser's developer console (press F12 or right-click and select "Inspect") can provide additional error information that may help diagnose problems.

7.3 Getting Support

If you can't resolve an issue using the troubleshooting guidance above, there are several ways to get additional help:

1 Check Documentation

Review this manual thoroughly, as many common issues and their solutions are covered in various sections.

2 Gather Information

Before contacting support, collect relevant details about your issue, including:

- Browser type and version
- Exact steps to reproduce the issue
- Any error messages displayed
- Screenshots if applicable

3 Contact Support

Reach out to the support team with your collected information. Technical support can be provided by your instructor or the platform administrators at your institution.

Browser Compatibility

The platform is optimized for Chrome and Firefox browsers. If you're experiencing issues, try switching browsers before contacting support.

8. Appendix

8.1 File Format Specifications

The FPGA Visualization Platform works with specific file formats. Understanding these formats is important for creating and managing designs.

File Type	Extension	Required	Description
Verilog	.v	Yes	Contains the hardware description of the digital circuit in Verilog HDL format. Defines modules, ports, and logic.
Standard Delay Format	.sdf	Yes	Contains timing information for the digital design, including propagation delays between components.
JSON Schematic	.json	Auto-generated	Generated automatically when you upload Verilog and SDF files. Contains the visualization data used by the platform.

Verilog (.v) File Requirements

For best compatibility with the platform, your Verilog files should:

- Define clear module boundaries with proper port declarations
- Use standard Verilog syntax (IEEE 1364-2001 or later)
- Include explicit connection definitions
- Avoid overly complex hierarchical structures

SDF (.sdf) File Requirements

Your SDF files should:

- Correspond directly to the components in the Verilog file
- Include proper timing specifications for all relevant paths
- Use the standard SDF format

Generated JSON Format

The platform automatically generates a JSON schematic from your Verilog and SDF files. This contains component position data, connection information, and state representation details needed for visualization.

8.2 Glossary of Terms

This section explains key terms and concepts used throughout the FPGA Visualization Platform.

Term	Definition
BEL	Basic Element of Logic - the fundamental building blocks in an FPGA, such as look-up tables (LUTs) or flip-flops.
Clock Frequency	The rate at which clock signals cycle in the simulation, measured in Hertz (Hz). Controls the timing of synchronous elements.
Component	A visual representation of an FPGA element like a LUT, flip-flop, or I/O buffer in the visualization interface.
Connection	A visual representation of signal paths between components, showing how data flows through the design.
DFF/FF	D Flip-Flop - A storage element that holds state information in digital circuits and captures data on clock edges.
Grid Layout	A visualization arrangement that places components in an organized grid pattern for clarity.
Hierarchical Layout	A visualization arrangement that organizes components based on signal flow hierarchy, typically from inputs through logic to outputs.
Interconnect	The routing resources that connect different components in an FPGA design.
LUT	Look-Up Table - A configurable component that implements combinational logic functions in FPGAs.
Propagation Delay	The time taken for a signal to travel from one component to another through an interconnect.
Propagation Slow Factor	A simulation parameter that deliberately slows down signal propagation for educational visualization purposes.

Term	Definition
SDF	Standard Delay Format - A file format that specifies timing information for digital designs.
Signal State	The logical value (high/1 or low/0) of a connection in the circuit.
Visualization	The interactive graphical representation of an FPGA design showing components and connections.

8.3 Additional Resources

Explore these resources to deepen your understanding of FPGAs and digital design concepts.

Learning Materials

FPGA Fundamentals

- Introduction to Digital Logic
- FPGA Architecture Basics
- Combinational vs. Sequential Logic

Verilog HDL

- Verilog Language Reference
- Common Verilog Patterns
- Writing Testbenches

Digital Design

- State Machine Design
- Clock Domain Crossing
- Timing Analysis Fundamentals

Circuit Types and Concepts

As you work with the FPGA Visualization Platform, you may encounter various types of digital circuits. Understanding these common circuit concepts will help you get more from your learning experience:

- **Counters** - Sequential circuits that count through a series of states and store values
- **Shift Registers** - Circuits that move data through a series of flip-flops
- **Combinational Logic** - Circuits where outputs depend only on current inputs
- **State Machines** - Circuits that transition between defined states based on inputs and current state

Keeping Up to Date

The platform is regularly updated with new features and capabilities. Check with your instructor or system administrator for information about new platform releases and additional learning materials.

8.4 Acknowledgments

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- The development team for their dedication to creating an intuitive visualization experience
- Academic partners who provided valuable feedback during the platform's development

- Students who participated in testing and helped refine the user experience