	Week 1 (24/03/2025 - 28/03/2025)		Week 2 (03/03/2025 - 07/03/2025)		Week 3 (10/03/2025 - 14/03/2025)		Week 4 (17/04/2025 - 21/04/2025)		Week 5 (24/04/2025 - 28/04/2025)		Week 6 (31/04/2025 - 04/05/2025)		Total (if needed)
Name	**Expected**	**Actual**	**Expected**	**Actual**	**Expected**	**Actual**	**Expected**	**Actual**	**Expected**	**Actual**	**Expected**	**Actual**	
Functional Specifications	25%	15%	75%	70%	100%	100%	100%	100%	100%	100%	100%	100%	
Technical Specifications	10%	0%	25%	10%	50%	30%	75%	80%	100%	100%	100%	100%	
Test Plan	0%	0%	50%	50%	75%	90%	100%	100%	100%	100%	100%	100%	
Management (Planning, KPIs, Risks, Documents...)	30%	25%	60%	50%	80%	75%	80%	75%	95%	95%	100%	100%	
FPGA Grid Layout Rendering (SVG + D3.js)	25%	30%	60%	40%	80%	60%	90%	100%	100%	100%	100%	100%	
Signal Playback Engine (play, pause, step)	0%	0%	10%	10%	40%	30%	70%	50%	90%	75%	100%	100%	
Verilog Parser Functionality	50%	50%	70%	65%	90%	80%	100%	100%	100%	100%	100%	100%	
SDF Parser & Timing Data Extraction	0%	0%	0%	0%	20%	10%	50%	30%	80%	60%	100%	100%	
Pivot JSON Data Merge & Validation	0%	0%	0%	0%	30%	10%	60%	50%	90%	80%	100%	100%	
Frontend–Backend Integration via API	0%	0%	20%	10%	60%	60%	80%	75%	90%	90%	100%	100%	
Simulation Timeline Visualization (Frontend)	0%	0%	0%	0%	0%	0%	20%	20%	60%	40%	100%	100%	
File Selector + UI Integration	25%	40%	60%	50%	80%	80%	90%	90%	100%	100%	100%	100%	
Final Product Completion	15%	16%	28%	23%	52%	38%	74%	66%	92%	83%	100%	100%	
Total Project Completion	**14%**	**13%**	**36%**	**30%**	**59%**	**52%**	**76%**	**73%**	**92%**	**87%**	**100%**	**100%**	
Members Absence Time - Justified (hours)	14h		0h		3h 15m		3h 15m		3h 15m		0h		23h 45m
Total Project Hours	9h 45m		6h 30m		16h 15m		3h 15m		16h 15m		13h		65h