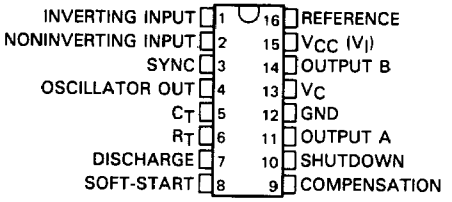
TYPES SG1525A, SG1527A, SG2525A, SG2527A, SG3525A, SG3527A PULSE-WIDTH MODULATION CONTROLLERS

D2806, SEPTEMBER 1983

- **Complete PWM Power Control Circuitry**
- **8-Volt to 35-Volt Operation**
- **5.1-Volt Reference Trimmed to ±1%**
- **Frequency Range . . . 100 Hz to 500 Hz**
- **Adjustable Deadtime Control**
- **Under-Voltage Lockout for Low V_{CC} Conditions**
- **Latched PWM Prevents Multiple Pulses**
- **Dual Sink or Source Output Drivers**
- **Direct Replacements for Silicon General SG1525A/SG1527A Series**

SG1525A, SG1527A . . . J
SG2525A, SG2527A . . . J OR N
SG3525A, SG3527A . . . J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



output logic

SG1525A, SG2525A, SG3525A . . . NOR
SG1527A, SG2572A, SG3527A . . . OR

description

The SG1525A/SG1527A series of pulse-width modulation integrated circuits are designed to offer improved performance and lower external parts count when used to implement various types of switching power supplies. Each device includes an on-chip 5.1-volt reference, error amplifier, programmable oscillator, pulse-steering flip-flop, a latched comparator under-voltage lockout, shutdown circuitry, and complementary source or sink outputs. The on-chip 5.1-volt reference is trimmed to ±1% initial accuracy, serves as a reference output, and supplies the internal regulator control circuitry. The input common-mode range of the error amplifier includes the reference voltage, which eliminates the need for external divider resistors.

The oscillator operates at a fixed frequency determined by one timing resistor R_T and one timing capacitor C_T. The timing resistor establishes the constant charging current for C_T, resulting in a linear voltage ramp at C_T, which is fed to the PWM comparator providing linear control of the output pulse duration by the error amplifier. A Sync input to the oscillator allows for external synchronization or for multiple units to be slaved together. A single external resistor between the C_T pin and the Discharge pin provides a wide range of dead-time adjustment. These devices also feature built-in soft-start circuitry that requires only an external timing capacitor. The Shutdown pin controls both the soft-start and the output drivers, and provides instantaneous turn-off with soft-start recycle for slow turn-on. The soft-start and output driver circuitry are also controlled by the under-voltage lockout circuit, which, during low-input supply voltage of less than that required for normal operation, keeps the soft-start capacitor discharged and the output drivers off.

Another unique feature is the S-R latch following the PWM comparator. This feature enables the output drivers to be turned off any time the PWM pulse is terminated. The latch is reset with each clock pulse. However, the PWM outputs will remain turned off for the duration of the period if the PWM comparator output is in a low-level state. The SG1525A, SG2525A, and SG3525A output stages feature NOR logic, resulting in a low output for an off-state. The SG1527A, SG2527A, and SG3527A output stages feature OR logic, resulting in a high-level output for an off-state. The output stages are totem-pole designs capable of sourcing or sinking 200 milliamperes of output current.

The SG1525A and SG1527A are characterized for operation over the full military temperature range of −55°C to 125°C. The SG2525A and SG2527A are characterized for operation from −25°C to 85°C. The SG3525A and SG3527A are characterized for operation for 0°C to 70°C.

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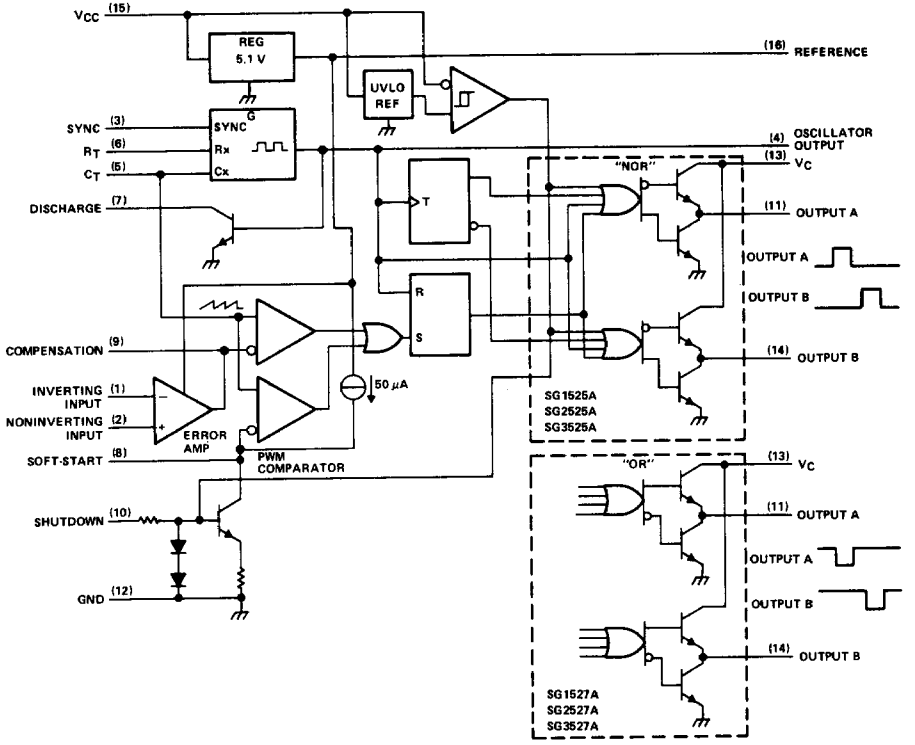
functional block diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	40 V
Collector voltage, V_C	40 V
Logic input voltage range sync and shutdown	−0.3 V to 5.5 V
Analog input voltage range error amplifier inputs	−0.3 V to V_{CC}
Output current, I_O	500 mA
Reference output current, I_{REF}	50 mA
Current through C_T terminal	−5 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1000 mW
Operating free-air temperature range: SG1525A, SG1527A	−55°C to 125°C
SG2525A, SG2527A	−25°C to 85°C
SG3525A, SG3527A	0°C to 70°C
Operating virtual junction temperature range	0°C to 150°C
Storage temperature range	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: J Package	300°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N Package	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operating above 25°C free-air temperature, see Dissipation Derating Curves, Figures 1 and 2. In the J package, SG1525A and SG1527A chips are alloy-mounted; SG2525A, SG2527A, SG3525A, and SG3527A chips are epoxy mounted.

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J PACKAGE FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

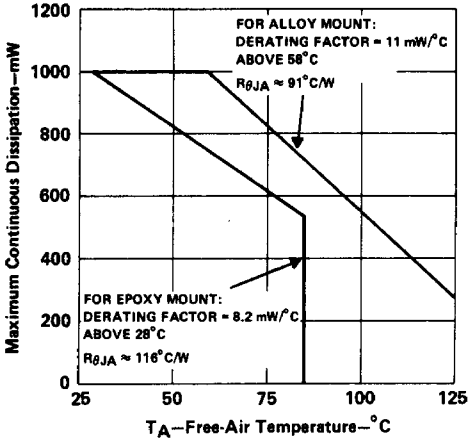

FIGURE 1

N PACKAGE FREE-AIR TEMPERATURE
DISSIPATION DERATING CURVE

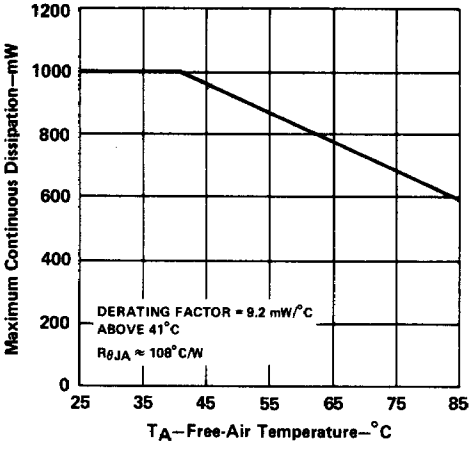

FIGURE 2

recommended operating conditions

PARAMETER		SG1525A, SG1527A		SG2525A, SG2527A		SG3525A, SG3527A		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Supply voltage, V_{CC}		8	35	8	35	8	35	V
Collector voltage, V_C		4.5	35	4.5	35	4.5	35	V
Output current, I_O	Steady state	0	±100	0	±100	0	±100	mA
	Peak	0	±400	0	±400	0	±400	
Reference output current, I_{REF}		0	20	0	20	0	20	mA
Oscillator frequency range		100	500	100	500	100	500	kHz
Timing resistor, R_T		2	150	2	150	2	150	kΩ
Timing capacitor, C_T		0.001	0.1	0.001	0.1	0.001	0.1	μF
Dead-time resistor, R_D		0	500	0	500	0	500	Ω
Operating free-air temperature range, T_A		−55	125	−25	85	0	70	°C

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	SG1525A, SG1527A SG2525A, SG2527A			SG3525A, SG3527A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Output voltage	T_J = 25°C	5.05	5.1	5.15	5	5.1	5.2	V
	V_{CC} = 8 V to 35 V, I_O = 0 to 20 mA	5		5.2	4.95		5.25	
Input regulation	V_{CC} = 8 V to 35 V		14	20		14	20	mV
Output regulation	I_O = 0 to 20 mA		5	50		5	50	mV
Output voltage change with temperature			24	50		24	50	mV
Output voltage long-term drift (see Note 3)	After 1000 h at T_J = 125°C		25	50		25	50	mV
Output noise voltage (RMS)	f = 10 Hz to 10 kHz, T_J = 25°C		40	200		40	200	μV
Short-circuit output current	V_O = 0 V, T_J = 25°C		80	100		80	100	mA

oscillator section

PARAMETER	TEST CONDITIONS	SG1525A, SG1527A SG2525A, SG2527A			SG3525A, SG3527A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Maximum frequency	R_T = 2 kΩ, C_T = 1 nF	400			400			kHz
Minimum frequency	R_T = 150 kΩ, C_T = 0.1 μF			100			100	Hz
Initial frequency error	R_T = 3.6 kΩ, R_D = 0 Ω, C_T = 0.1 μF, f = 40 kHz, T_A = 25°C		±2%	±6%		±2%	±6%	
Frequency change with supply voltage	V_{CC} = 8 V to 35 V		±0.3%	±1%		±1%	±2%	
Frequency change with temperature	T_A = MIN to MAX		±3%	±6%		±3%	±6%	
Output amplitude at Pin 4	R_T = 3.6 kΩ, R_D = 0 Ω, C_T = 0.1 μF, f = 40 kHz	3	3.5		3	3.5		V
Output pulse duration at Pin 4	R_T = 3.5 kΩ, R_D = 0 Ω, C_T = 0.1 μF, f = 40 kHz, T_J = 25°C	0.3	0.5	1	0.3	0.6	1	μs
Input threshold voltage at Pin 3		1.2	2	2.8	1.2	2	2.8	V
Input current at Pin 3	$V_{I(Pin3)}$ = 3.5 V		1.6	2.5		1.6	2.5	mA
Current through Pin 5 due to internal current mirror	Current through Pin 6 = 6 mA	1.7	2	2.2	1.7	2	2.2	mA

NOTE 3: Since long-term drift cannot be measured on the individual devices prior to shipment, this specification is not intended to be a guarantee or warranty. It is an engineering estimate of the average drift to be expected from lot to lot.

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 20 V (unless otherwise noted)

error amplifier section

PARAMETER	TEST CONDITIONS	SG1525A, SG1527A SG2525A, SG2527A			SG3525A, SG3527A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
High-level output voltage		3.8	5.6		3.8	5.6		V
Low-level output voltage			0.2	0.5		0.2	0.5	V
Input offset voltage			0.5	5		2	10	mV
Input bias current			1	10		1	10	μA
Input offset current				1			1	μA
Open-loop voltage amplification	$R_L \geq 10$ M	60	75		60	75		dB
Common-mode rejection ratio	V_{IC} = 1.5 V to 5.2 V	60	75		60	75		dB
Supply voltage rejection ratio	V_{CC} = 8 V to 35 V	50	60		50	60		dB
Gain-bandwidth product	A_V = 0 dB, T_J = 25°C	1	2		1	2		MHz

comparator section

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input threshold voltage	R_T = 3.6 kΩ, R_D = 0 Ω, C_T = 10 nF, f = 40 kHz	Duty cycle = 0%	0.6	0.9		V
		Duty cycle = MAX		3.3	3.6	
Input bias current				0.5	1	μA

soft-start section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Soft-start voltage	V_I at Pin 10 = 2 V		0.4	0.6	V
Soft-start current	V_I at Pin 10 = 0 V	25	50	80	μA
Input current, Shutdown	V_I at Pin 10 = 2.5 V		0.4	1	mA

output section

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level output voltage	I_{OH} = −20 mA	18	19		V
	I_{OH} = −100 mA	17	18		
Low-level output voltage	I_{OL} = 20 mA		0.2	0.4	V
	I_{OL} = 100 mA		1	2	
Under-voltage lockout voltage	V_I at Pins 8 and 9 = high	6	7	8	V
Collector cutoff current (see Note 4)	V_C = 35 V, I_O = 100 mA			200	μA
Output pulse rise time	C_L = 1 nF, T_J = 25°C		100	600	ns
Output pulse fall time	C_L = 1 nF, T_J = 25°C		50	300	ns
Shutdown delay time	V_I at Pin 10 = 3 V, capacitance at pin 8 = 0, T_J = 25°C		0.2	0.5	μs

NOTE 4: Collector cutoff current specifications apply only for the SG1525A, SG2525A, and SG3525A devices.

total device

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Minimum duty cycle				0%	
Maximum duty cycle		45%	49%		
Standby current	V_{CC} = 35 V		14	20	mA

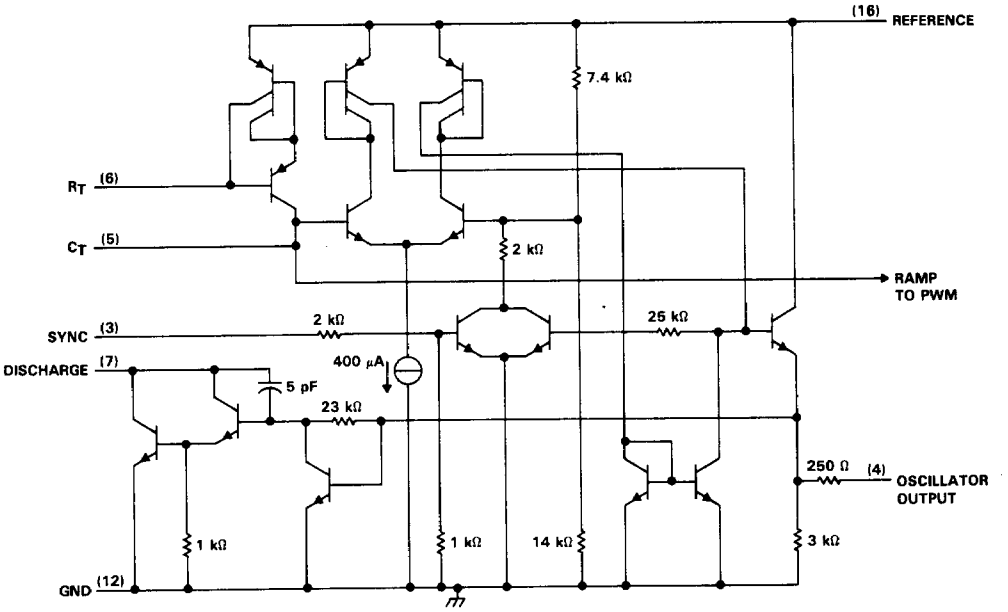

FIGURE 3 – OSCILLATOR SCHEMATIC DIAGRAM

TYPICAL CHARACTERISTICS

CHARGING TIME vs TIMING RESISTOR

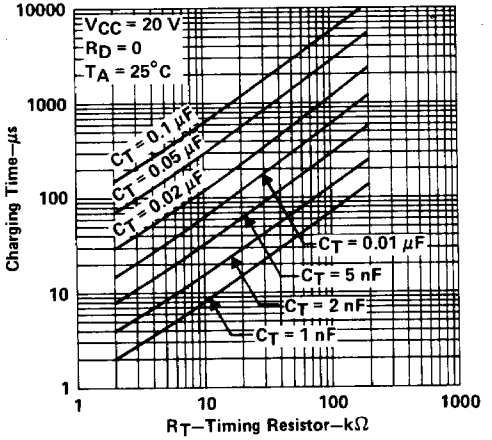

FIGURE 4

DISCHARGE TIME vs DEAD TIME RESISTOR

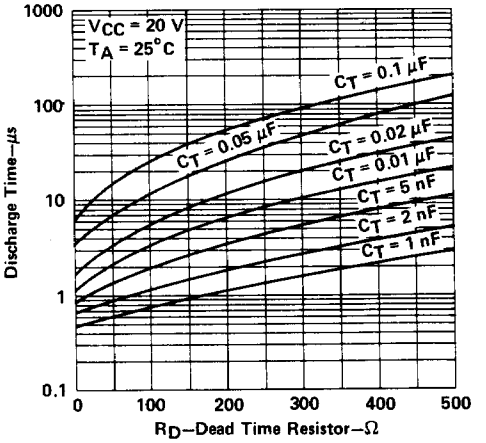

FIGURE 5

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TYPICAL CHARACTERISTICS

ERROR AMPLIFIER OPEN-LOOP
FREQUENCY RESPONSE

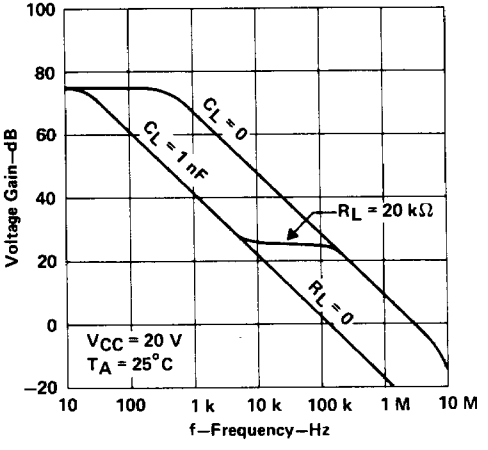

FIGURE 6

SG1525A OUTPUT SATURATION VOLTAGE
vs
OUTPUT CURRENT

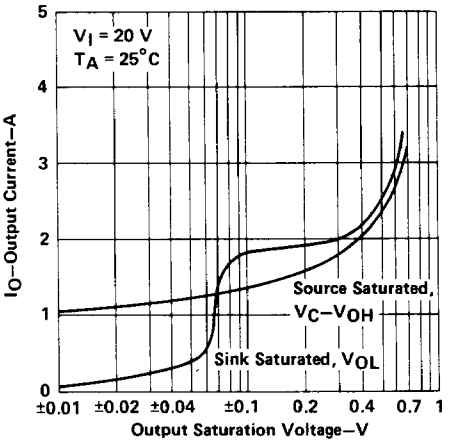

FIGURE 7

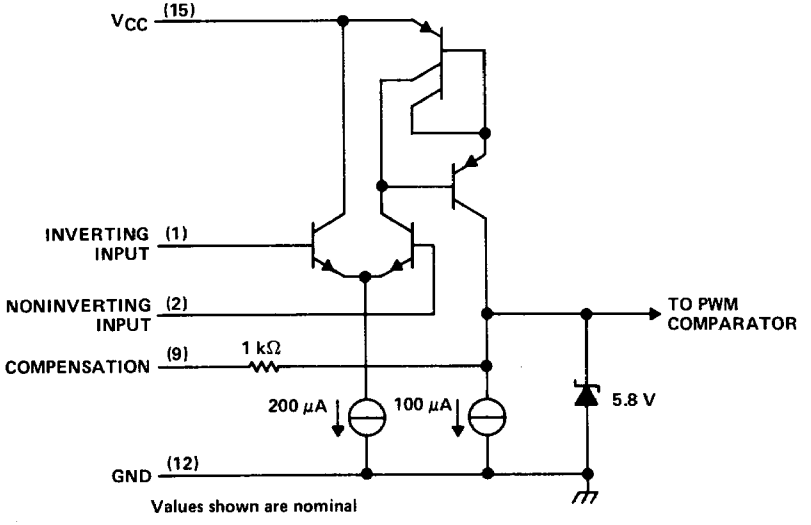

FIGURE 8 – ERROR AMPLIFIER SCHEMATIC DIAGRAM

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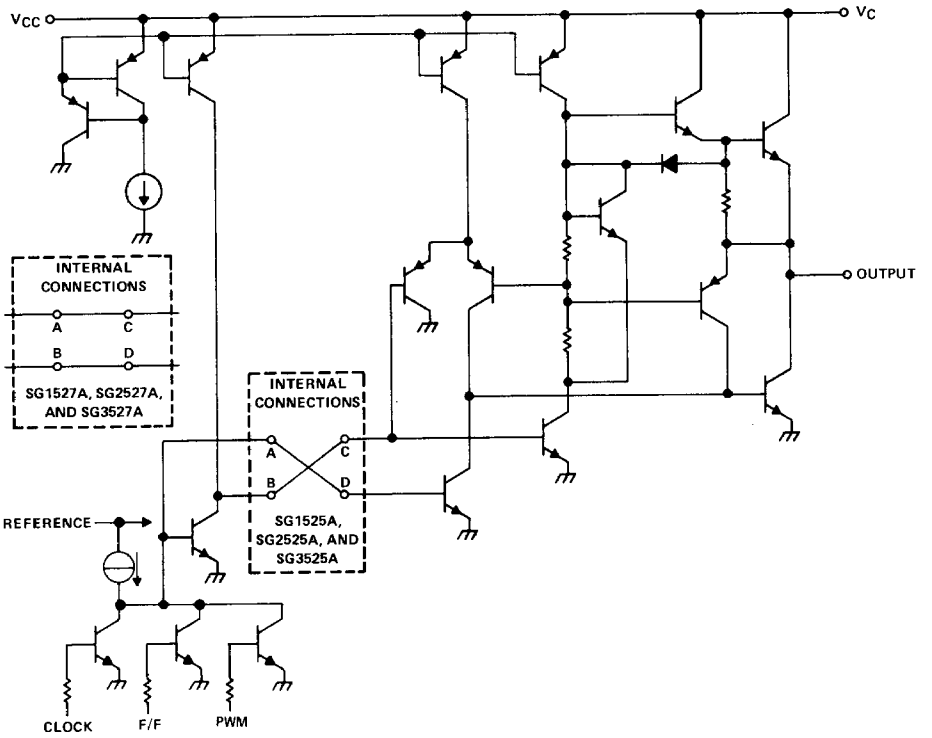

FIGURE 9 — OUTPUT CIRCUIT SCHEMATIC DIAGRAM

TYPICAL APPLICATION DATA

shutdown options

1. Use an external transistor or open-collector comparator to pull down on the Compensation terminal (Pin 9). This will set the PWM latch and turn off both driver outputs. If the shutdown signal is momentary, pulse-by-pulse protection will be accomplished as the PWM latch is reset with each clock pulse.
2. The same results may be accomplished by pulling down on the Soft-Start terminal (Pin 8) with the only difference being that on this pin shutdown will not affect the amplifier compensation network, but must discharge any soft-start capacitance.
3. Application of a positive-going signal to the Shutdown terminal (Pin 10) will provide the most rapid shutdown of the driver outputs but will not immediately set the PWM latch if there is a capacitor at the Soft-Start terminal. The capacitor will discharge but at a current twice the charging current. The PWM latch can be set on a pulse-by-pulse basis by the shutdown terminal if there is no external capacitance on the Soft-start terminal (Pin 8). Slow turn-on may still be accomplished by connecting an external capacitor, blocking diode, and charging resistor to the Compensation terminal (Pin 9).

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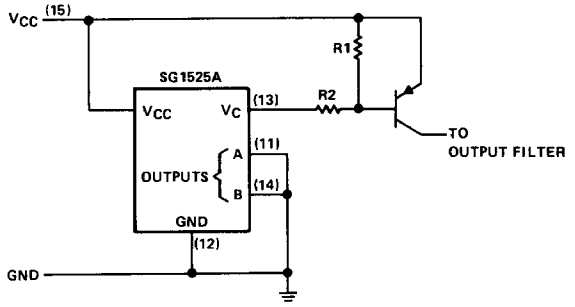
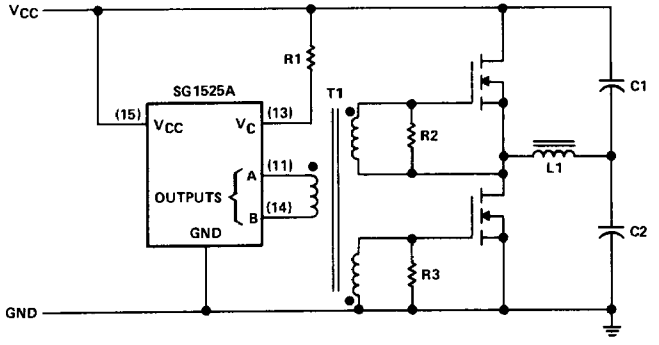
TYPICAL APPLICATION DATA



For single-ended supplies, the driver outputs are grounded. The V_C terminal is switched to ground by the totem-pole source transistors on the alternate oscillator cycles.

FIGURE 10 – SINGLE-ENDED CIRCUIT



Low-power transformers can be directly driven by the SG1525A. Automatic reset occurs during deadtime when both ends of the primary winding are switched to ground.

FIGURE 11 – TRANSFORMER-COUPLED CIRCUIT

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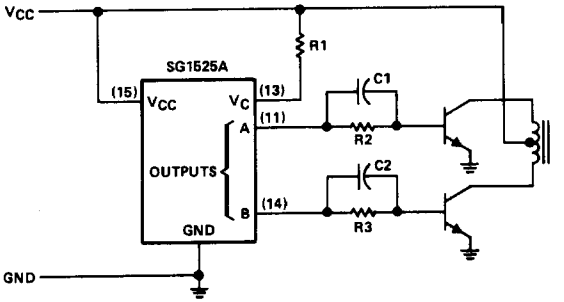
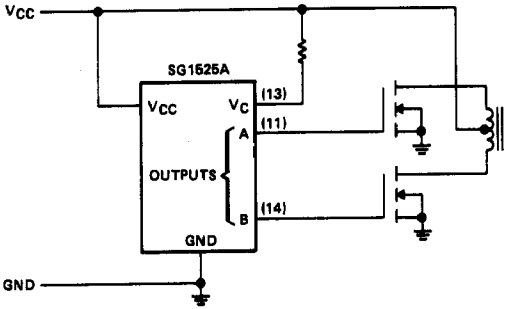
TYPICAL APPLICATION DATA



In conventional push-pull bipolar designs, forward base drive is controlled by R_1—R_3. Rapid turn-off times for the power devices are achieved with speed-up capacitors C_1 and C_2.

FIGURE 12 – BIPOLAR PUSH-PULL CIRCUIT



The low source impedance of the output drivers provides rapid charging of power FET input capacitance while minimizing external components.

FIGURE 13 – LOW-IMPEDANCE BIPOLAR-DRIVE PUSH-PULL CIRCUIT

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