

**本科实验报告**

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| 课程名称： | 计算机组成 |
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**浙江大学实验报告**

课程名称： 计算机组成 实验类型： 综合

实验项目名称： Lab 3: Design of CPU and setting up SOC test environment

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实验地点： 东4-510 实验日期：2019 年 03月29 日

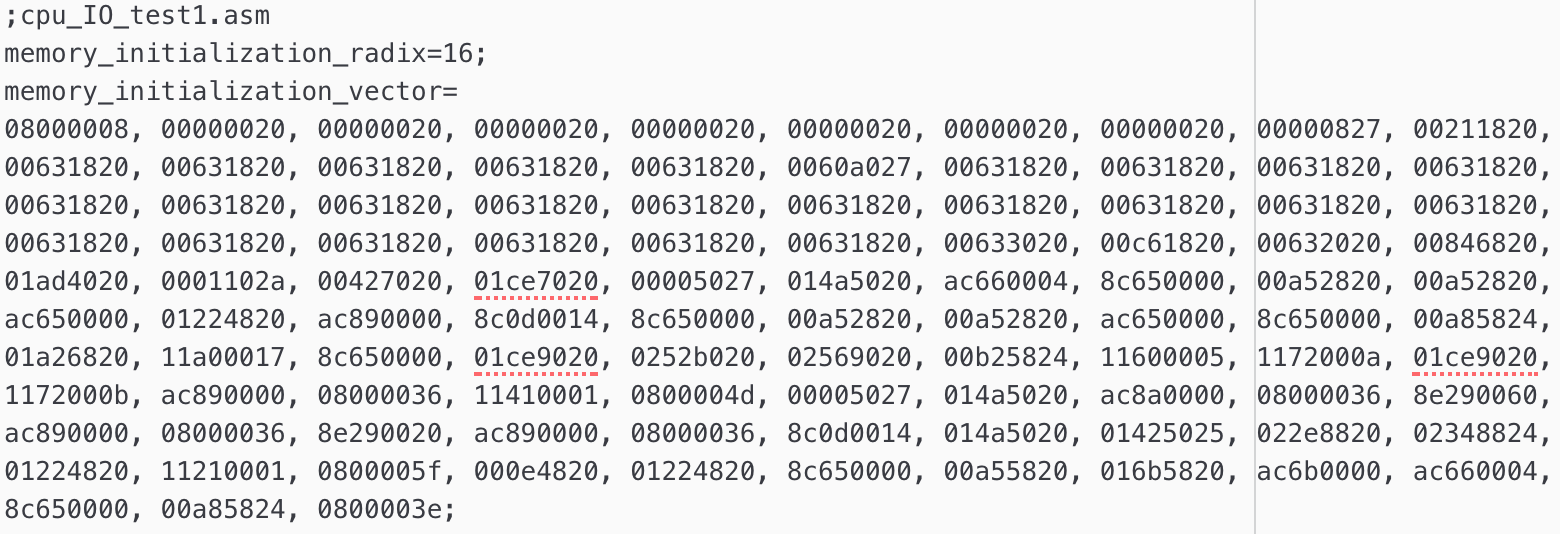
**1 – Purpose of the Experiments and Tasks**

1. Implement and design a SOC based on the given components
2. Design and implement the ROM and RAM
3. Understand the usage of each component and the circuitry the SOC

**2 – Instructions and Experiment Contents**

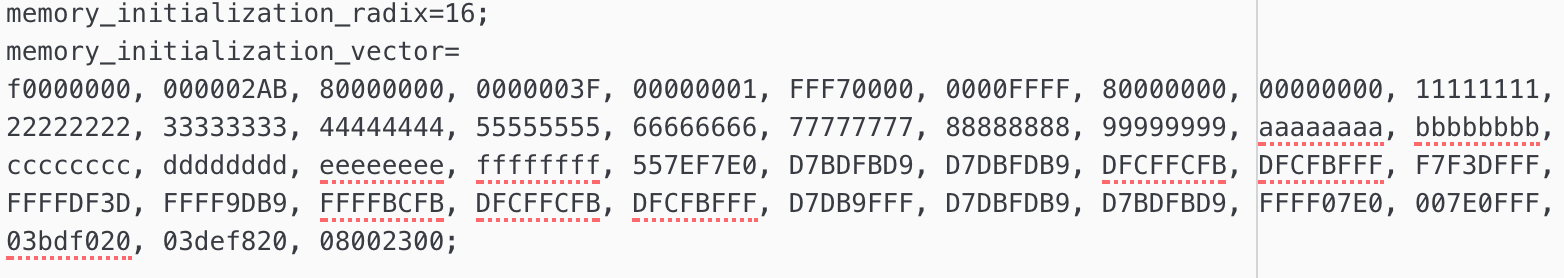
This experiment is built on top of the previous experiment where we had a ROM and a RAM and different modes defined, which we could control them by Switches 5 to 7. This experiment is a step closer to designing a proper CPU and SoC. This experiment has 3 new components, MIO\_BUS, Counter and SCPU and different contents for the RAM and ROM. The purpose of existing are not explained since they were explained in the previous lab report but rather the purpose of each new module is explained.

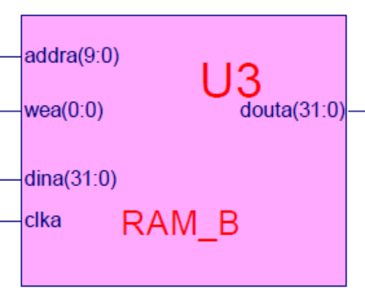
Let’s start off with the ROM and RAM. They both have the same sizes, 1024x32bits. But for this experiment they are initialized differently. For the rom we have the following initializer:

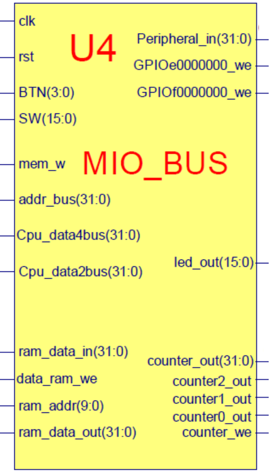


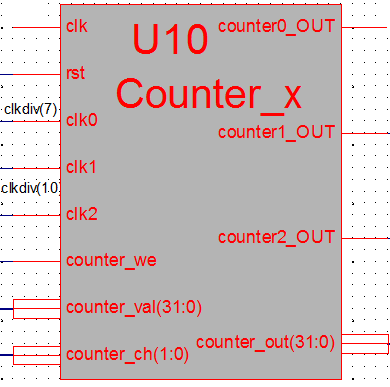
The first line is just a comment indicating that this file is going to be used by CPU\_IO assembly module(?) and the second line indicates that vector is going to be in hexadecimal form, and the third line is just an array which is going to be written in the ROM. As mentioned, this block is 1024x32 bits meaning that there are 1024 fields with each having the size of 32 bits. Given an address we can output its corresponding memory content. We don’t necessary need 1024 field, in this case 128 fields are sufficient enough, meaning that we only need an output of 7 bits to access the contents of the ROM. Since we are generating a 1024x32bits ROM we need an input of 10bits and an output of 32bits, which is the content of the given memory address. The contents of the ROM correspond to the value to be displayed on each segment, hence the size of 8x4bits (8 hexadecimal values).

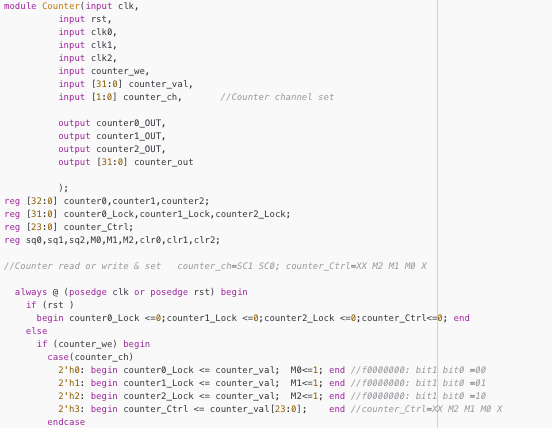
Similarly, we can initialize the RAM. The COE of RAM is also given and is as follow:

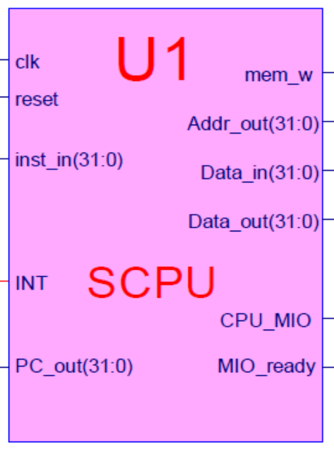


Unlike ROM, RAM requires a clock input, along that it requires an input which indicates whether we want to read or write data, and if we are going to write to the memory what is our data. The rest is similar to ROM. While generating the RAM we can specify whether it’s “write first” or “read first” this means if wea = 1 is whether it’s going to write to the memory or read from the memory. In this case, we have it set to write first.

Next, we have BUS\_MIO. It is a multiplexed I/O component which routes the inputs to their corresponding outputs based on the selector. MIO are usually used to redirect or route the I/O, peripherals and bus pins without them going to the processors or FPGA. In this case we are using this component to send our inputs to the RAM, ROM, GPIO, SCPU and the counter. The selectors are BTN and SW which are outputs of our AntiJitter module which takes the inputs from on-board switches and keypads as inputs and makes sure that there aren’t any noises. As can be seen from the MIO\_BUS\_IO module we have clk, rst, mem\_w, Cpu\_data2bus, addr\_bus, ram\_data\_out, led\_out, counter\_out, counter0\_out, counter1\_out and counter2\_out as inputs. Clk is the input clock of the module, rst is reset input of the module, mem\_w is an indication whether we want to write to memory or not, Cpu\_data2bus is the data received from CPU, addr\_bus is the address of the memory, ram\_data\_out is the data we get to from the ram, led\_out is the LEDs we want to turn on, counter\_out, counter1\_out, counter0\_out and counter2\_out are the inputs from the counter module. Then we have Cpu\_data4bus, ram\_data\_in, ram\_addr, data\_ram\_we, GPIOf000000\_we, GPIOe000000\_we, counter\_we and peripheral\_in as outputs. Cpu\_data4bus is our output data to CPU, ram\_data\_in is the data we want to write to ram, ram\_addr is the address of the memory we want to access/write to, data\_ram\_we is whether we want to write to ram or not, GPIOf000000\_we is the enabler switch for multiplexer and GPIOe000000\_we is the enabler switch for GPIO, counter\_we is a mode switch for the counter module, and peripheral\_in is our mode 0 for the displays and our LED controller.

Next, we have our counter module. This module is in charge of counting. There are different modes which are activated by the input signals. The input signals are clk, rst, clk0, counter\_we, counter\_val, counter\_ch. Clk is the clock of our module, rst is the reseter of the module, clk0 is used for the counting, counter\_we is our input from MIO\_BUS which is one of our mode selectors(or counter write mode?), counter\_val is the value of counter which is our input from MIO\_BUS which is the CPU’s output to the I/O and also our first mode on the multiplexer and counter\_ch is our channel counter controller. Our outputs are counter0\_out, counter1\_out, counter2\_out and counter\_out. As the name suggests our counter\_out is the output of our counter and counter0\_out, counter1\_out, counter2\_out are channel 0, channel 1 and channel 2 counter outputs respectfully.

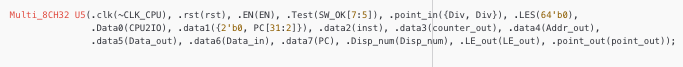
Finally, we have SCPU. This module is MIPS based which supports three types of instructions: R-Type, I-Type and J-Type. It’s the brain of this experiment. It has 6 inputs, clk, reset, inst\_in, Data\_in and INT. Clk is the input clock, reset is used to reset the module, inst\_in is the instruction set, Data\_in is the input data and INT is the interrupt input. As a result, we have the following outputs, PC\_out, Addr\_out, Data\_out, and mem\_w. PC\_out is program space access pointer which part of it goes to the ROM, Addr\_out is the ram address, Data\_out is the data to be written to the memory, mem\_w is whether we want to write to ram or not.

**3 – Implementation and results**

The top module should look like this:



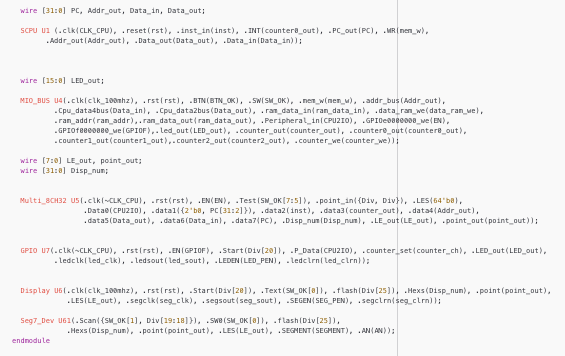
As discussed in chapter 1, this experiment shares a lot of similar components and connections to the previous lab. There are few new components in this experiment which were introduced and explained in chapter 2. Other components that exist in the previous serve the same purposes and used in a similar way. Similar to our previous lab we have a main multiplexer called Multi\_8CH32, which routes the inputs to our display module. The inputs though, differ compared to the previous experiment. Here we have CPU2IO as our first input which is the peripheral output from the MIO\_BUS or CPU’s output to the I/O, then we have PC as our second input which is the program space access pointer that comes from SCPU, next one is ROM’s output which is also the instructions, then we have the address of the memory which is coming from the SCPU, and Data\_out, Data\_in which are the output data and input data from SCPU. The outputs are stayed untouched. Here is the implementation of the multiplexer in the top module:



Another difference between this experiment and the previous is the input of the SPIO (GPIO) which in this case is replaced by the output of the MIO\_BUS (peripheral\_in) instead of switches. And as mentioned in chapter 2 the EN switch is now coming from GPIOf00000000\_we. This signal is produced by MIO\_BUS, similarly GPIOe00000000\_we is used for the enabler switch of Multiplexer (Multi\_8CH32). The other inputs and outputs are stayed intact. Here is the implementation of this module in the top module:



Once these changes are made, we can implement the top module by adding the new components and slightly modify the existing top module. Here is the final result of the top module:



Results:

A screen shot of a computer

Description automatically generated A picture containing building, electronics

Description automatically generated A screenshot of a computer

Description automatically generated

Mode 0: peripherals (~SW0) Mode 0: peripherals (SW0) Mode 1: PC(SW0)

A close up of a monitor

Description automatically generated A screen shot of a computer

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Description automatically generated

Mode 2: instructions Mode 3: Counter Mode 4: Address

A screen shot of a computer monitor

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Description automatically generated

Mode 5: Data out Mode 7: PC

There are more pictures in the images folder.

**4 – Discussion**

For debugging purposes, I used the Seg7\_Dev to see if what’s being displayed on the 8 segments matches the 4 segments one, and sure it did but the problem with that clock didn’t match so there was a blinking effect, and when SW[2] was turned off the display would be a bit unreadable and sometimes didn’t match the 8 segments one due to the clock syncing problem.

The second problem I encountered was that whenever SW[2] was turned on to slow down the counters, it state of the LEDs wouldn’t change until it was turned off.

The programming files and top files are all available in the Lab2 Content folder.