

**本科实验报告**

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| 课程名称： | 计算机组成 |
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2019年 04月 22日

**浙江大学实验报告**

课程名称： 计算机组成 实验类型： 综合

实验项目名称： Lab 3: Designing a single cycle mips cpu with datapath and controllers

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实验地点： 东4-510 实验日期：2019 年 04月22 日

**1 – Purpose of the Experiments and Tasks**

1. Design the controllers for each instruction set
2. Design an ALU
3. Design the cpu and datapath

**2 – Instructions and Experiment Contents**

Mips instruction sets has reserved 32 bits for each instruction. Instructions are divided into 3 different categories, I-Type, J-Type and R-Type. Each of these formats has a different structure when it comes to instructions.

R-Type or register format is used whenever we are dealing with variables that are stored in the registers. This type has the following format:

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Operation code | rs | rt | rd | shift | function |
| 6-bits | 5-bits | 5-bits | 5-bits | 5-bits | 6-bits |

i.e. let’s assume we want to add to registers together. We have the following instruction:

add $t0, $t1, $t2

In this case, add is the operation we want to perform. It has an operation code of 0 and function code of 20 in hex. Rs and rt are our source registers and rd is our destination register; rs and rt are t1 and t2 and rd is t0. Shift is used for sll and srl instructions which indicates how many bits we want to do the shifting.

I-Type: This instruction set is used when we are dealing with immediate values. It has a similar structure as R-type except we no longer need a secondary source register, instead we need an immediate. The structure of this type is as follows:

|  |  |  |  |
| --- | --- | --- | --- |
| Operation code | rs | rt | immediate |
| 6-bits | 5-bits | 5-bits | 16-bits |

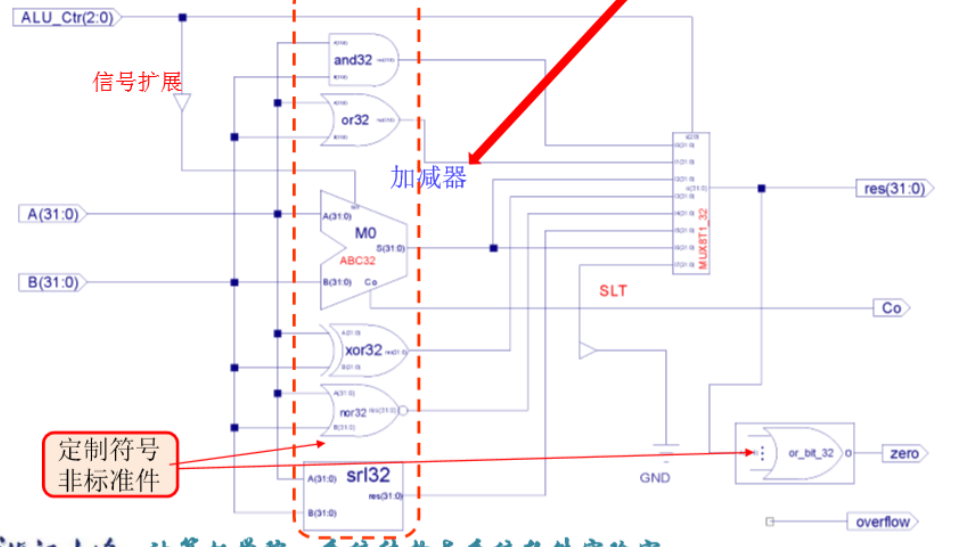
Rs is the source register and rt is the target register.

J-Type: This type is used when we are dealing with jump instructions. They take a operation code and an address. Its structure is as follows:

|  |  |
| --- | --- |
| Operation code | Address |
| 6-bits | 26-bits |

**3 – Implementations**

**ALU Setup:**

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**Alu is required to be able to perform the following operations: addition, subtraction, and, or, xor, nor, srl and slt. It is controlled by the signal coming from ALU\_ctrl which controls which signal is passed through to the results. Co is the carryout of the addition, and zero is used for SLT operation. Here is the implementation of the top module and its children modules.**

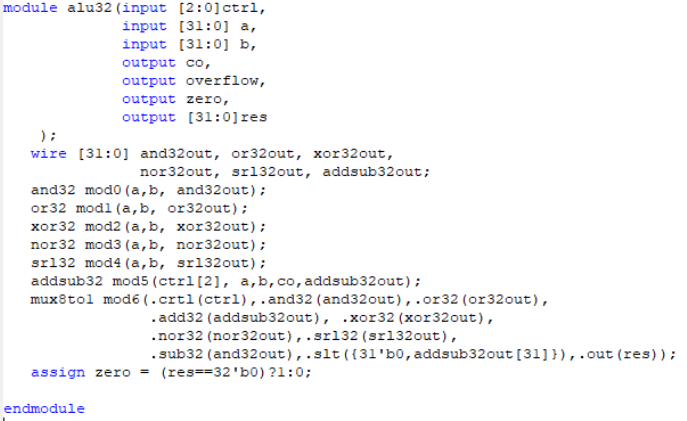
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Figure 1 32-bit ALU top module

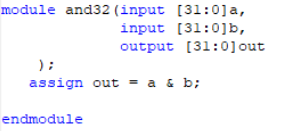


Figure 2 32-bit And module

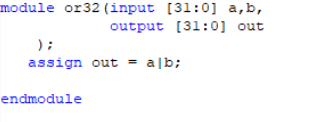


Figure 3 32-bit Or module

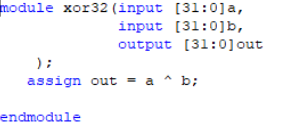


Figure 4 32-bit XOr module

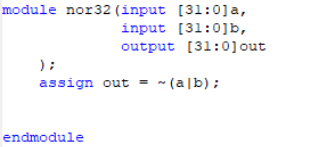


Figure 5 32-bit NOr module

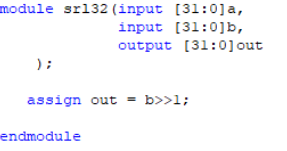


Figure 6 32-bit Srl module

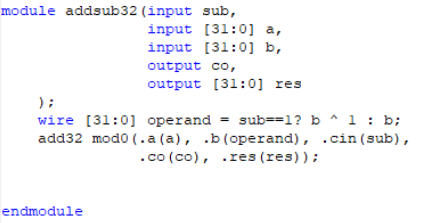


Figure 7 32-bit add/sub module

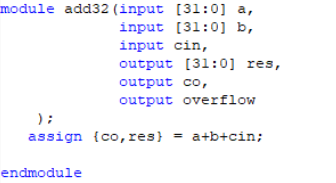


Figure 8 32-bit 2's complement addition module

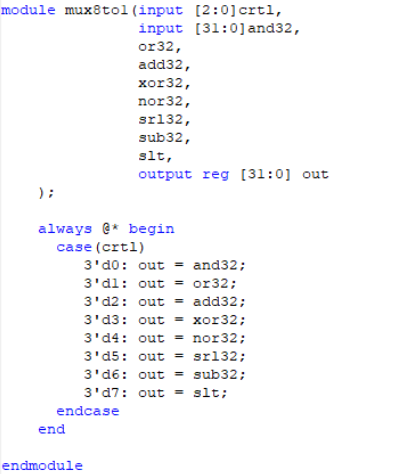


Figure 9 Multiplexer used for ALU

**Once we have all the components of the ALU designed we can focus on the other components of the DataPath. These components are program counter, Sign extension, and registers. Program counter keeps track of the current instruction, sign extension is used for I-Type instructions since our ALU only supports 32-bits operands. Registers module is a module that houses all the registers needed for our “CPU”. Here are the implementations of these modules:**

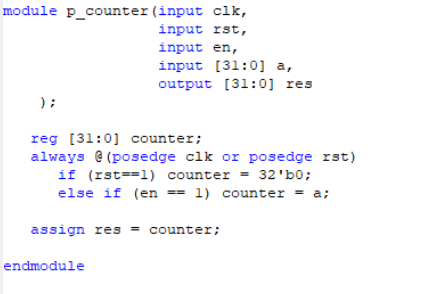
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Figure 10 Program counter module

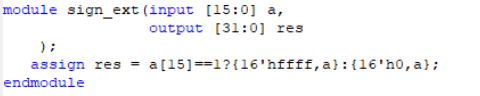


Figure 11 Sign Extension module

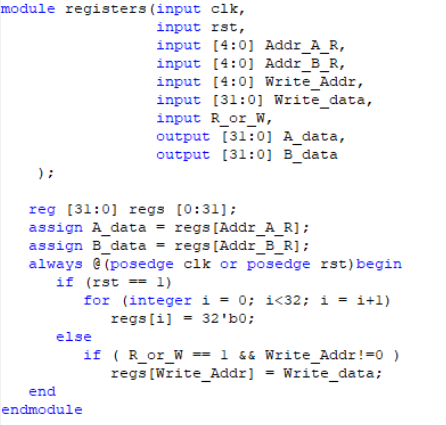


Figure 12 Registers module

**In registers modules, we have 32 registers with each having a length of 32-bits. Depending on the incoming signals we can either read from the registers or write to them, or reset all 32 registers.**

**Following the diagram below we can implement the datapath needed for our single cycle cpu:**

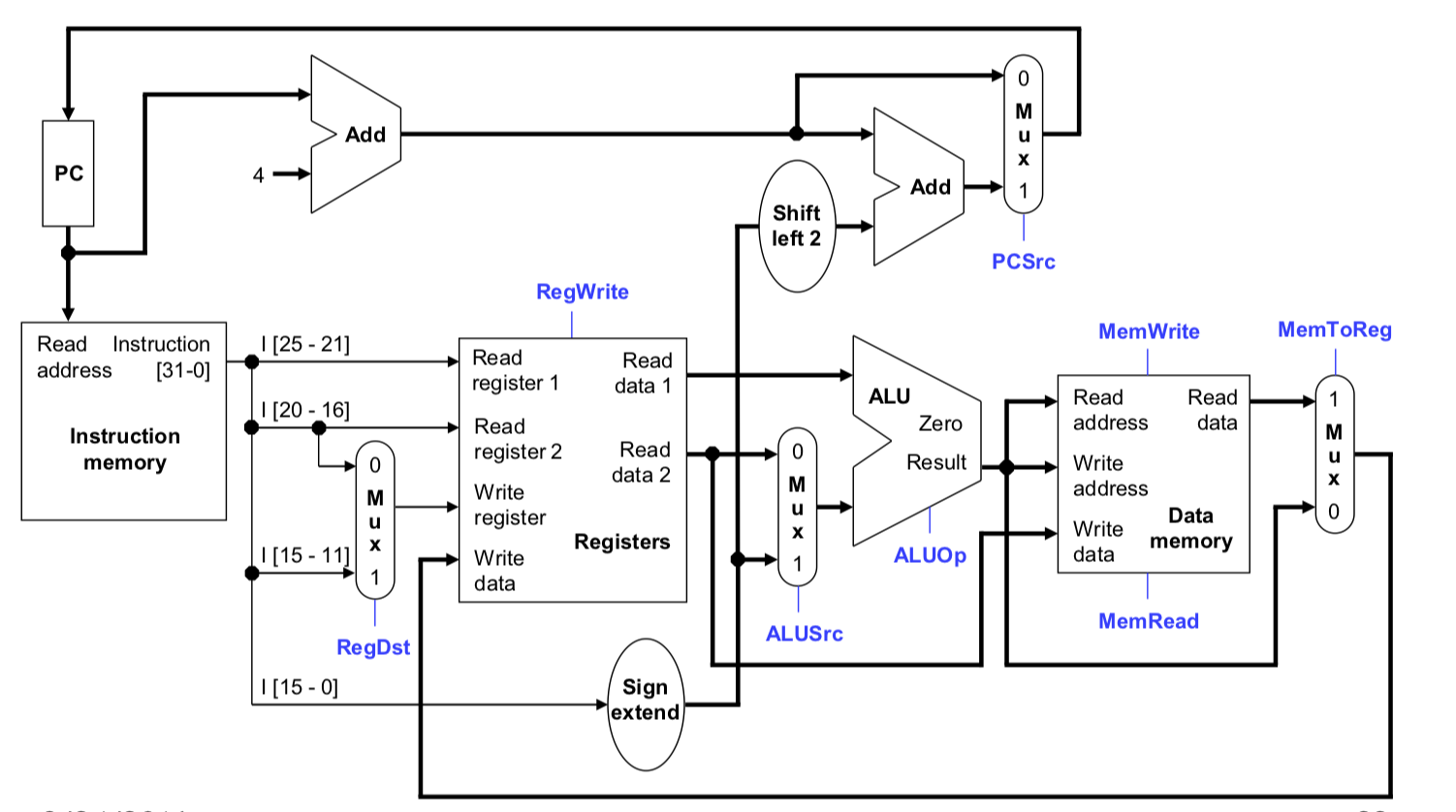
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Figure 13 Datapath diagram (University of Pittsburgh)

**Notice that in this diagram, we have a memory (RAM) module. We already have it implemented so there is no need to include it in our datapath, the output of our Read data 2 can be outputted as a bus called data\_out; similarly, we can output the output of ALU as alu\_out. The input of write is the output of a multiplexer with memtoreg as a switch and data\_in (output of RAM) and alu\_out. This diagram is missing J-Type instruction set. For that we are required to add two inputs: branch and jump. Branch is used for if statement-styled instructions and jump is used for J-Type instructions (Jr, Jl and etc.). We add a new multiplexer to this diagram that takes the jump address and if jump input is enabled then we set out pc to be the jump address otherwise it’d be pc+4 or address of branch. Here is the implementation of the Datapath:**

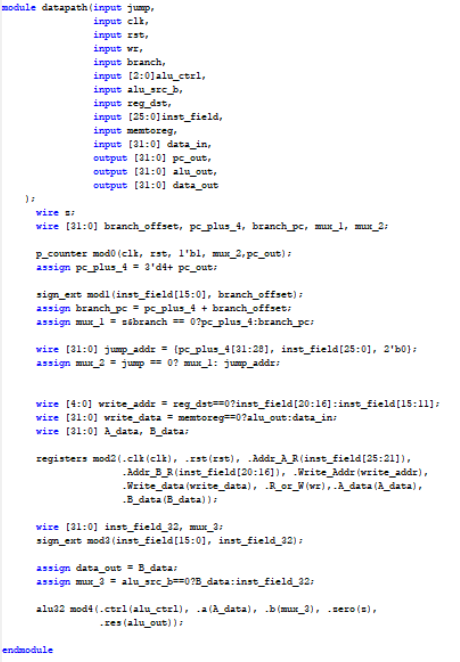
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Figure 14 implementation of datapath

According to this diagram, controller module is the module that creates the all the signals required for our datapath module.

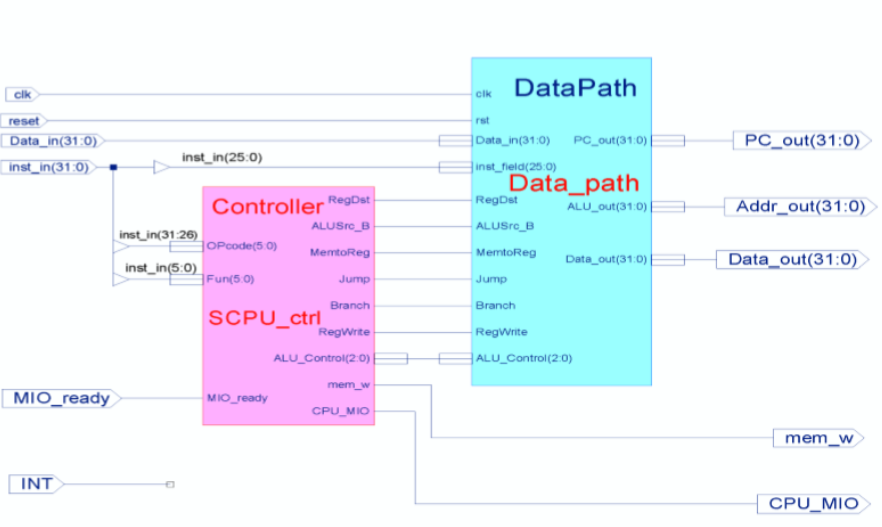


Figure 15 Schematics of the single cycle cpu

The implementation of controller module is pretty straight-forward. Branch is enabled if all 6 bits of the instructions except the second one are 0s. Regdst is the signal that chooses where data is written to and is enabled if all 6 bits are not enabled. For the rest, they can be seen in the controller module and are pretty easy to understand. Here is the implementation of this module:

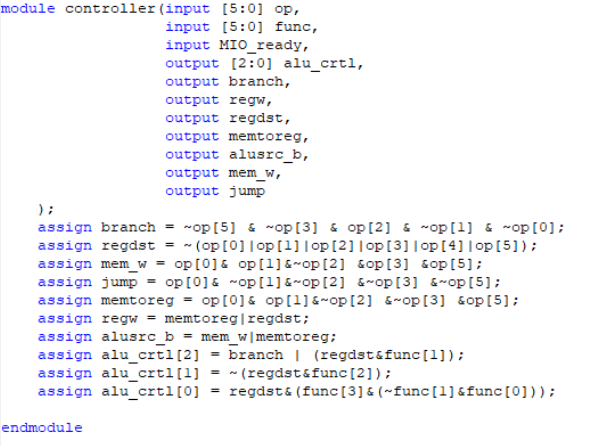


Figure 16 Controller module

**4 – Results**

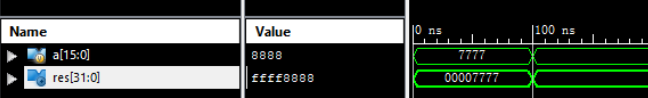
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Figure 17 results of sign extension

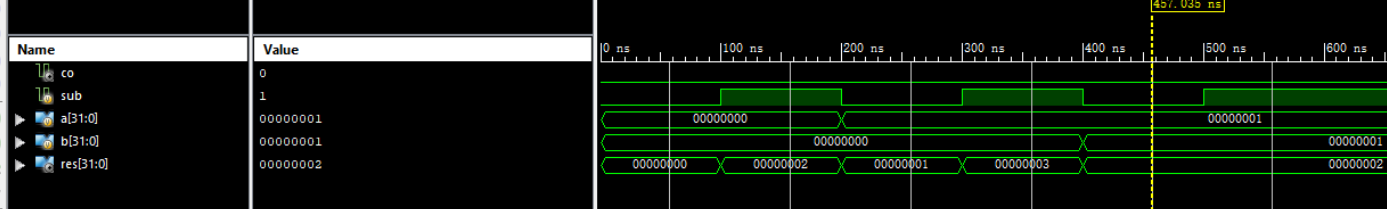


Figure 18 Adder and subtraction modules

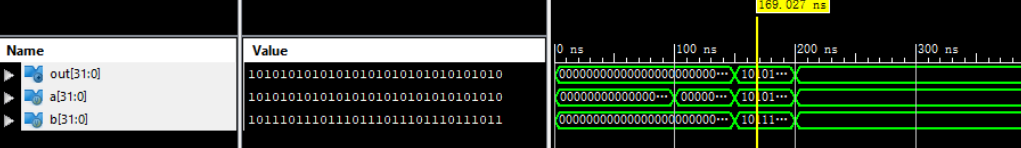


Figure 19 results of And module

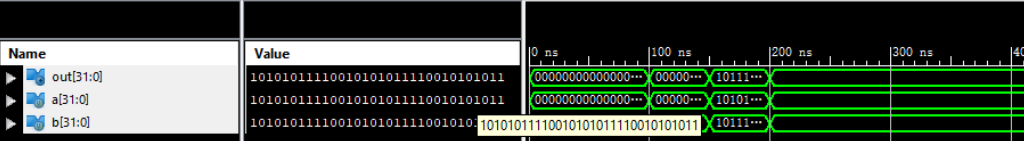


Figure 20 results of OR module

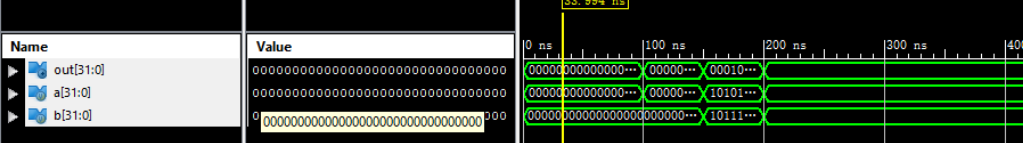


Figure 21 Results of XOR module

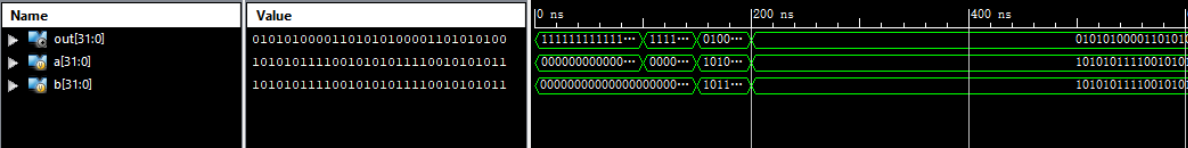


Figure 22 Results of Nor module

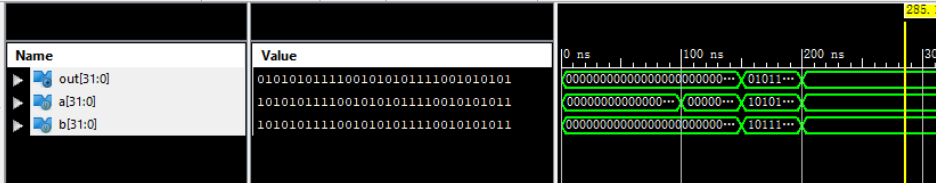


Figure 23 Results of SRL module