Information Technology Institute (ITI)

CMOS ANALOG IC DESIGN

LAB 1

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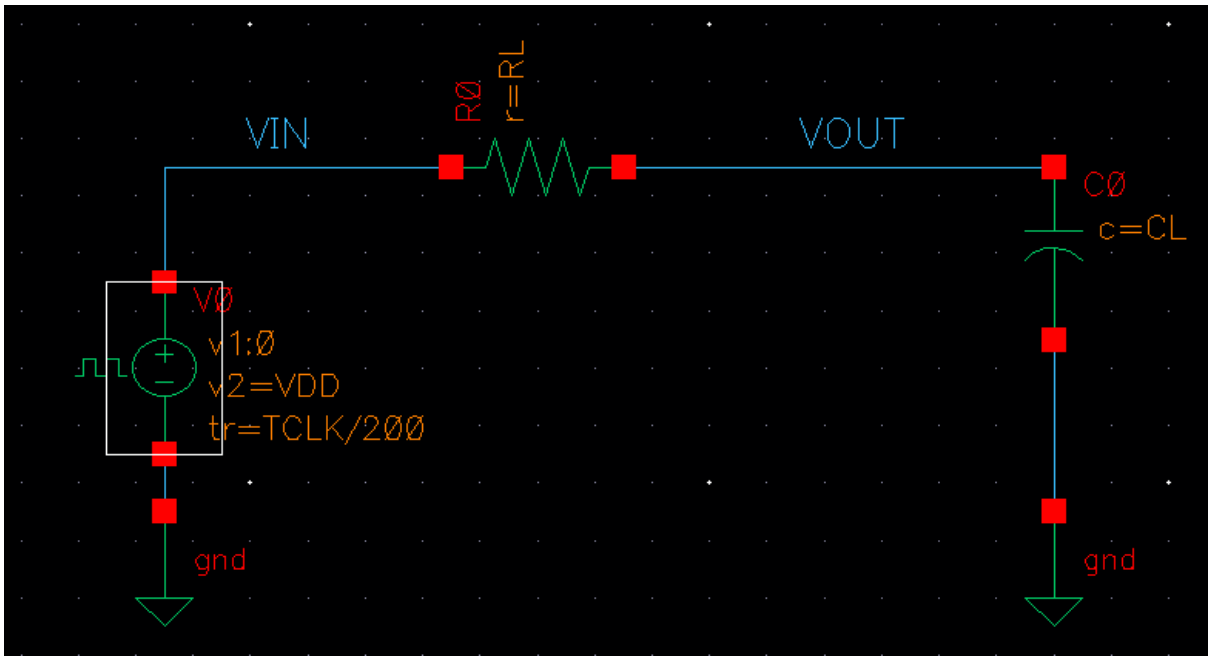
PART 1: LOW PASS FILTER SIMULATION (LPF)

1. Transient Analysis

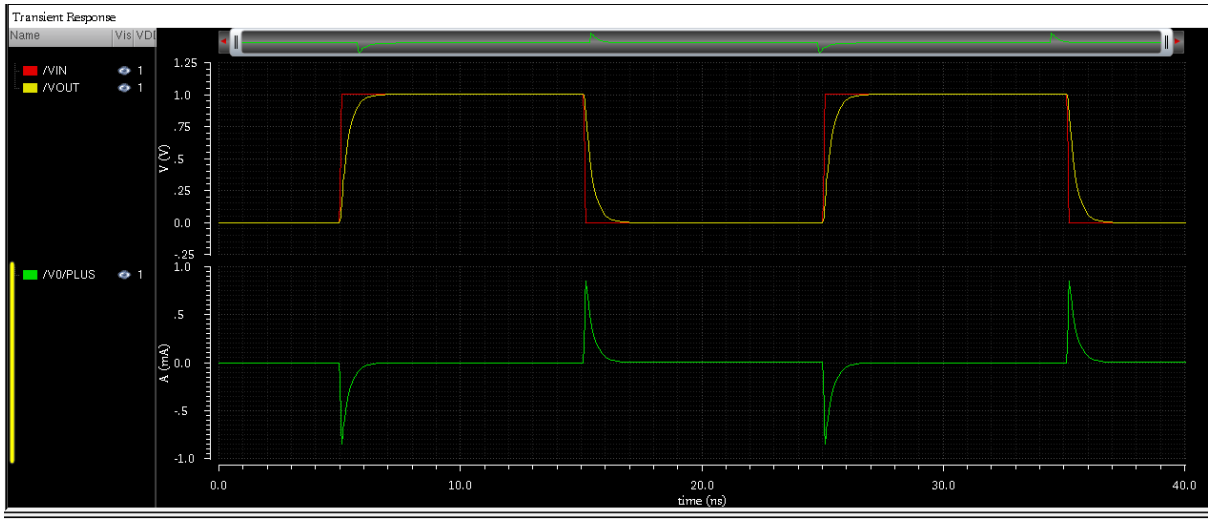
1) The circuit schematic is shown.



2) Parameters of the square pulse input signal are shown.

Voltage 1	0 V
Voltage 2	VDD V
Period	TCLK s
Delay time	TCLK/4 s
Rise time	TCLK/200 s
Fall time	TCLK/200 s
Pulse width	TCLK/2 s

3) Transient Analysis for two periods is shown



4)

Rise time

riseTime(VT("/VOUT") 0 nil 1 nil 10 90 nil "time") Calculator Expression

riseTime(VT("/VOUT") 0 nil 1 nil 10...

	VDD	riseTime..."time")
1	1.000	663.0E-12

Tabular Result

Fall Time

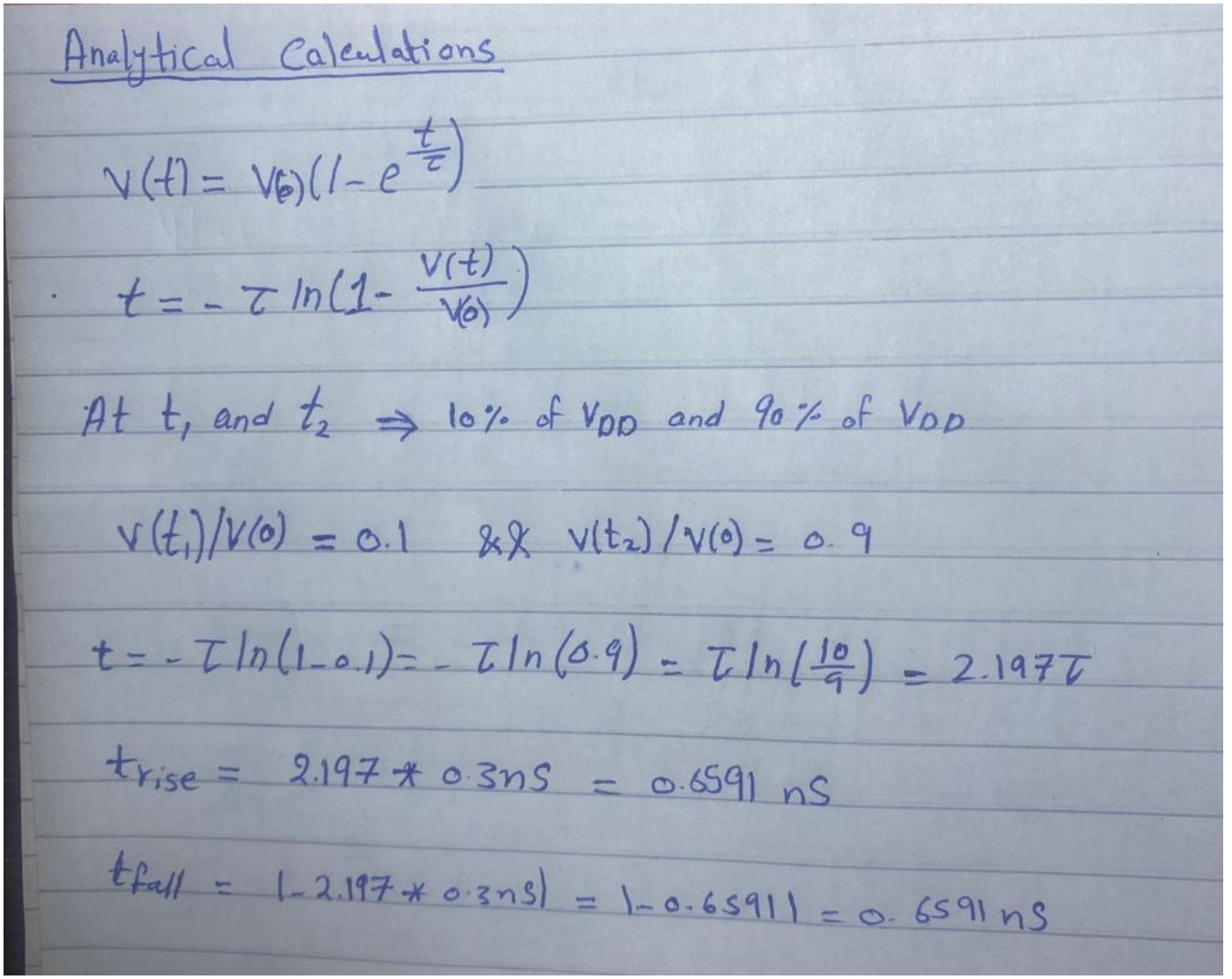
fallTime(VT("/VOUT") 1 nil 0 nil 90 10 nil "time") Calculator Expression

fallTime(VT("/VOUT") 1 nil 0 nil 90 ...

	VDD	fallTime..."time")
1	1.000	663.0E-12

Tabular Result

5) Comparison between the Results.



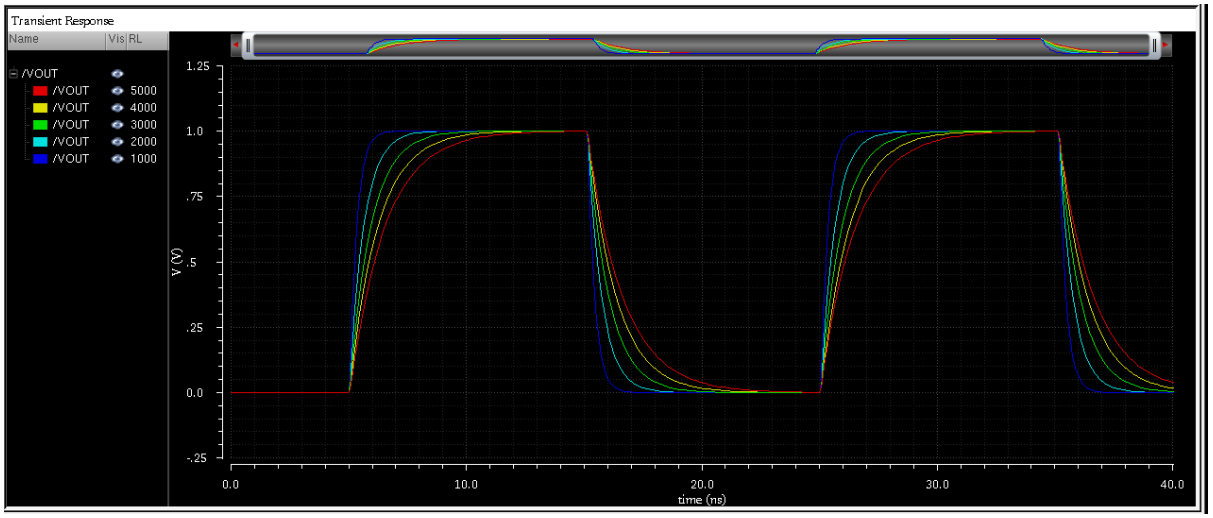
Analytical	Simulation
Rise time : 0.6591 ns	Rise Time : 0.6630 ns
Fall time : 0.6591 ns	Fall time : 0.6630 ns

6) Parametric Sweep for R = 1K : 1K : 5K

For different values of R, Results are shown below:

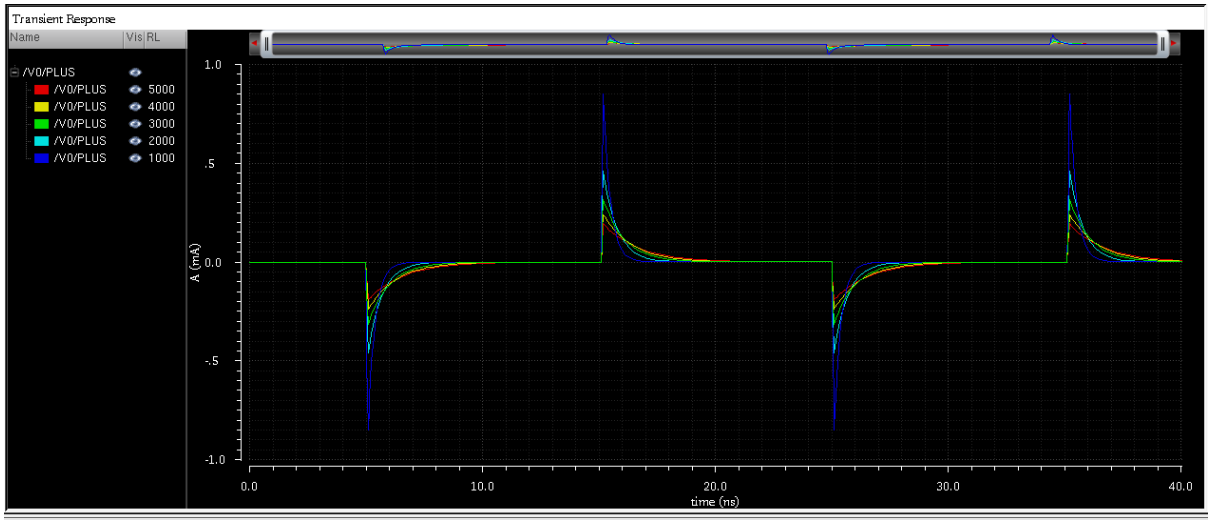
Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: RL=1k						
1	lab1:lpf:1	VIN				
1	lab1:lpf:1	VOUT				
1	lab1:lpf:1	I				
1	lab1:lpf:1	trise	663p			
1	lab1:lpf:1	tfall	663p			
Parameters: RL=2k						
2	lab1:lpf:1	VIN				
2	lab1:lpf:1	VOUT				
2	lab1:lpf:1	I				
2	lab1:lpf:1	trise	1.311n			
2	lab1:lpf:1	tfall	1.311n			
Parameters: RL=3k						
3	lab1:lpf:1	VIN				
3	lab1:lpf:1	VOUT				
3	lab1:lpf:1	I				
3	lab1:lpf:1	trise	1.974n			
3	lab1:lpf:1	tfall	1.974n			
Parameters: RL=4k						
4	lab1:lpf:1	VIN				
4	lab1:lpf:1	VOUT				
4	lab1:lpf:1	I				
4	lab1:lpf:1	trise	2.633n			
4	lab1:lpf:1	tfall	2.633n			
Parameters: RL=5k						
5	lab1:lpf:1	VIN				
5	lab1:lpf:1	VOUT				
5	lab1:lpf:1	I				
5	lab1:lpf:1	trise	3.293n			
5	lab1:lpf:1	tfall	3.293n			

Plot of Vout vs time (on using a parametric sweep on R)

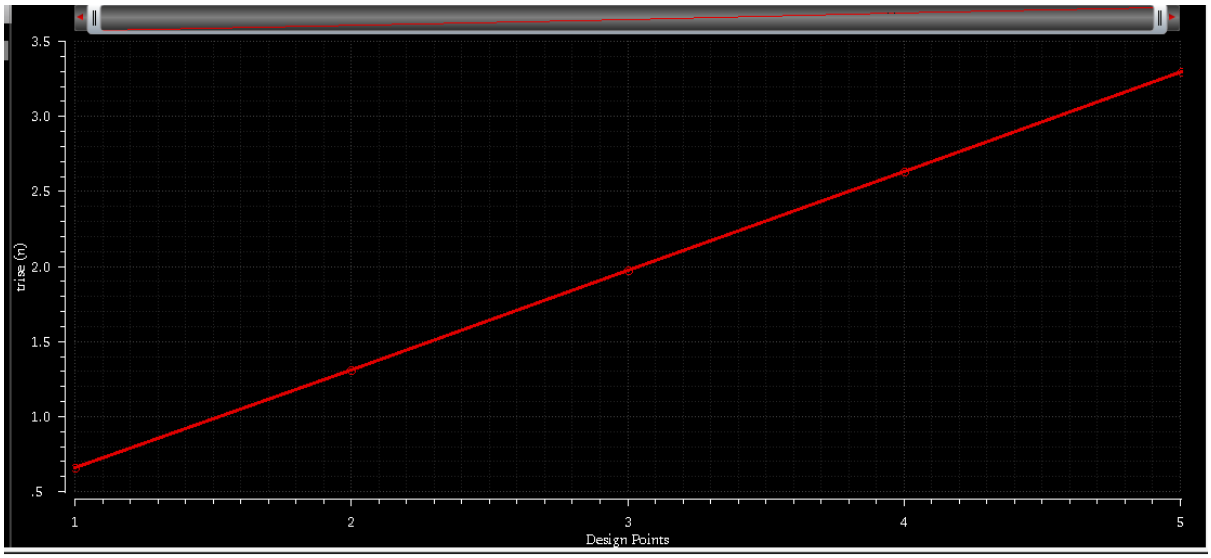


The graph affirms out knowledge that the higher the value of R, the more time it takes to charge the capacitor, and also the less time it takes for the capacitor to discharge. This is illustrated on the graph; As R increases, Vout graph gets less steep while charging (slower charging) and gets less steep while discharging (slower discharging).

Current vs time (on using a parametric sweep on R)



Rise and Fall times across the parametric sweep



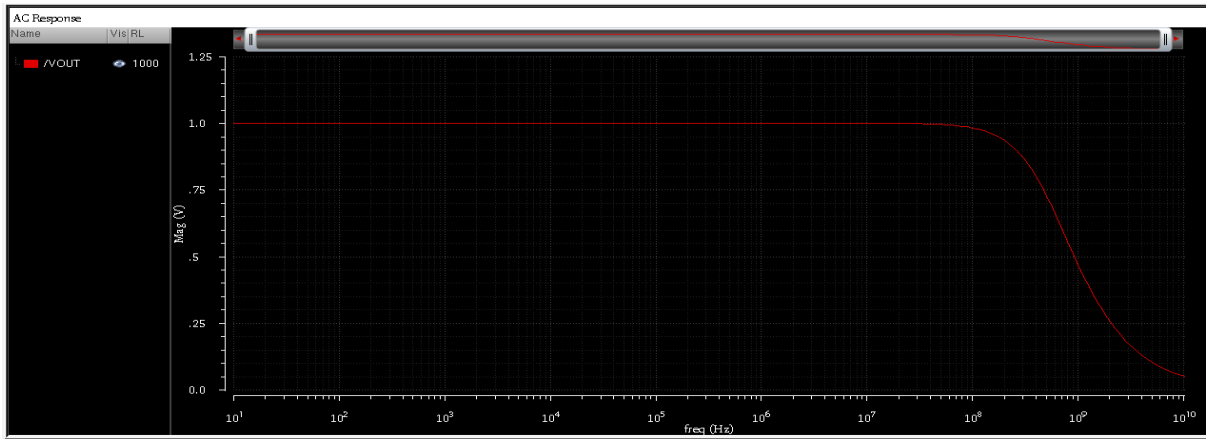
The rise and fall times are equal, as we expect for a first-order system.

The rise and fall times increase across design points; They increase as we increase R.

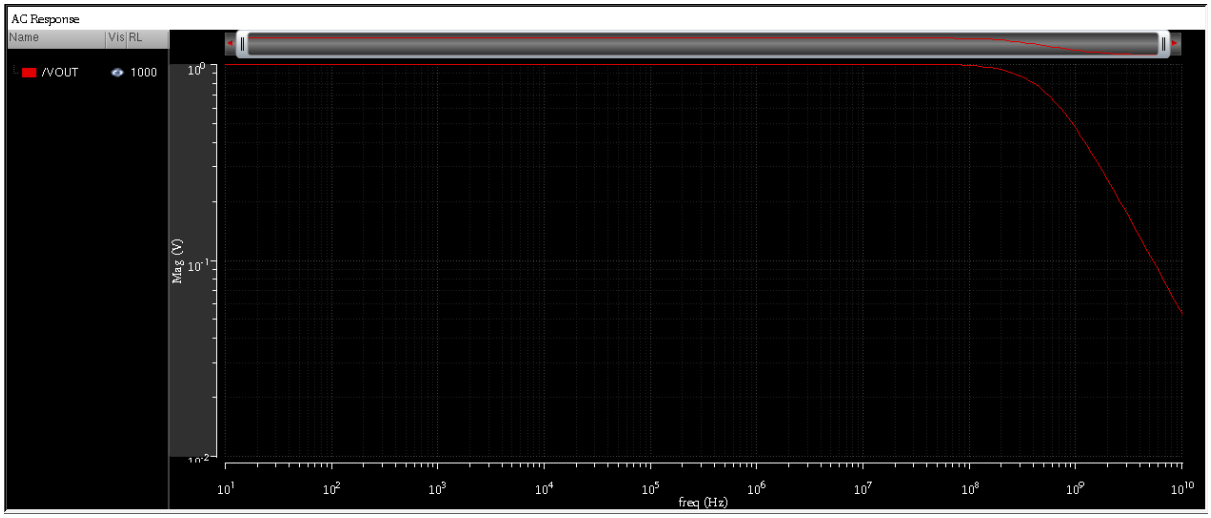
2. AC Analysis

1) Bode Plot Results

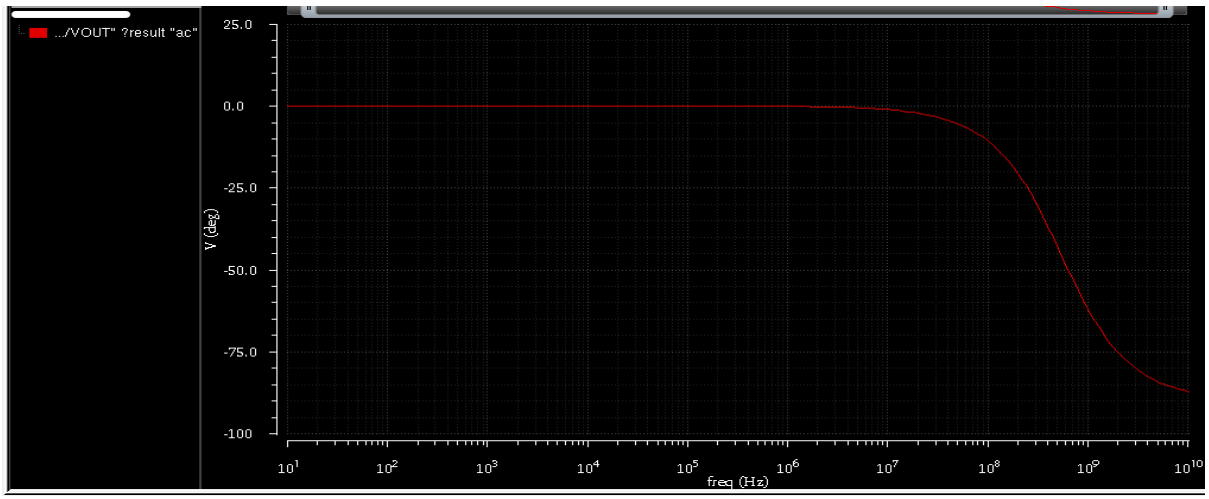
Magnitude



On log scale, we get the shown result for the magnitude of Vout



Phase



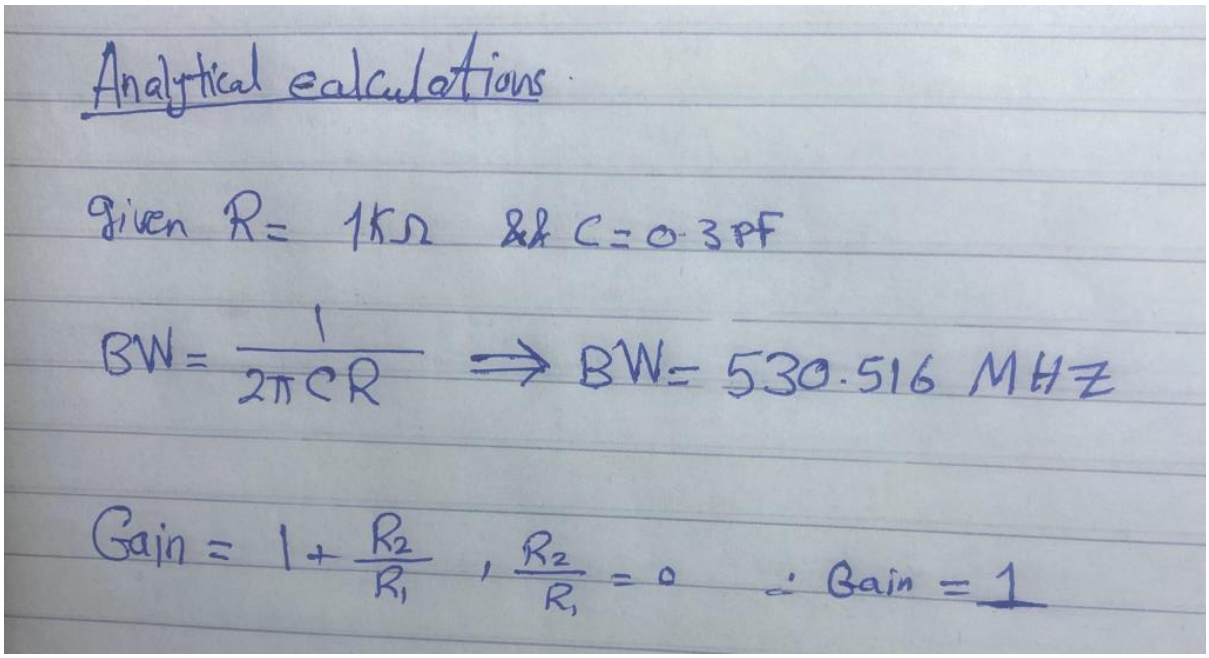
2) DC gain and Bandwidth

dB20 graph

DC gain and 3dB Bandwidth values are shown

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab1:lpf:1	VIN				
lab1:lpf:1	VOUT				
lab1:lpf:1	I				
lab1:lpf:1	3dB	529.7M			
lab1:lpf:1	DC gain	1			

3) Results Comparison



Analytical	Simulation
Bandwidth : 530.516477 MHZ	Bandwidth : 529.7 MHZ
Gain = 1	Gain = 1

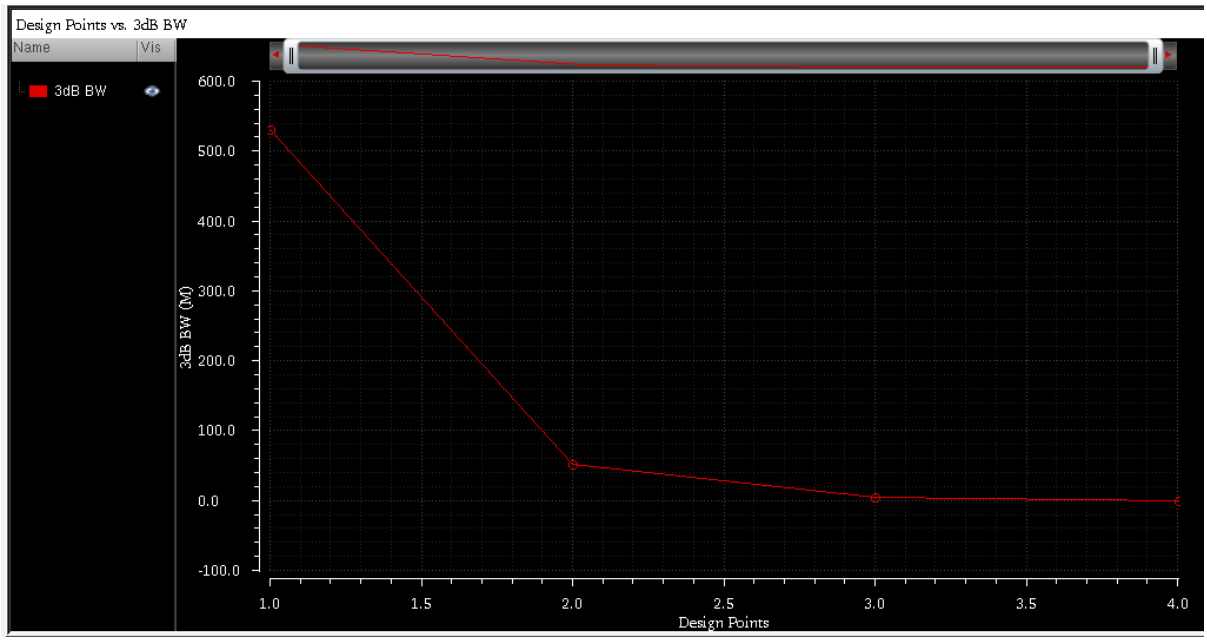
4) Results of simulation.

Point	Test	Output	Nominal	Spec	Weight	Pass/Fail
Parameters: RL=1k						
1	lab1:lpf:1	VIN				
1	lab1:lpf:1	VOUT				
1	lab1:lpf:1	I				
1	lab1:lpf:1	DC gain	1			
1	lab1:lpf:1	3dB BW	529.7M			
Parameters: RL=10k						
2	lab1:lpf:1	VIN				
2	lab1:lpf:1	VOUT				
2	lab1:lpf:1	I				
2	lab1:lpf:1	DC gain	1			
2	lab1:lpf:1	3dB BW	52.97M			
Parameters: RL=100k						
3	lab1:lpf:1	VIN				
3	lab1:lpf:1	VOUT				
3	lab1:lpf:1	I				
3	lab1:lpf:1	DC gain	1			
3	lab1:lpf:1	3dB BW	5.297M			
Parameters: RL=1M						
4	lab1:lpf:1	VIN				
4	lab1:lpf:1	VOUT				
4	lab1:lpf:1	I				
4	lab1:lpf:1	DC gain	1			
4	lab1:lpf:1	3dB BW	529.7k			

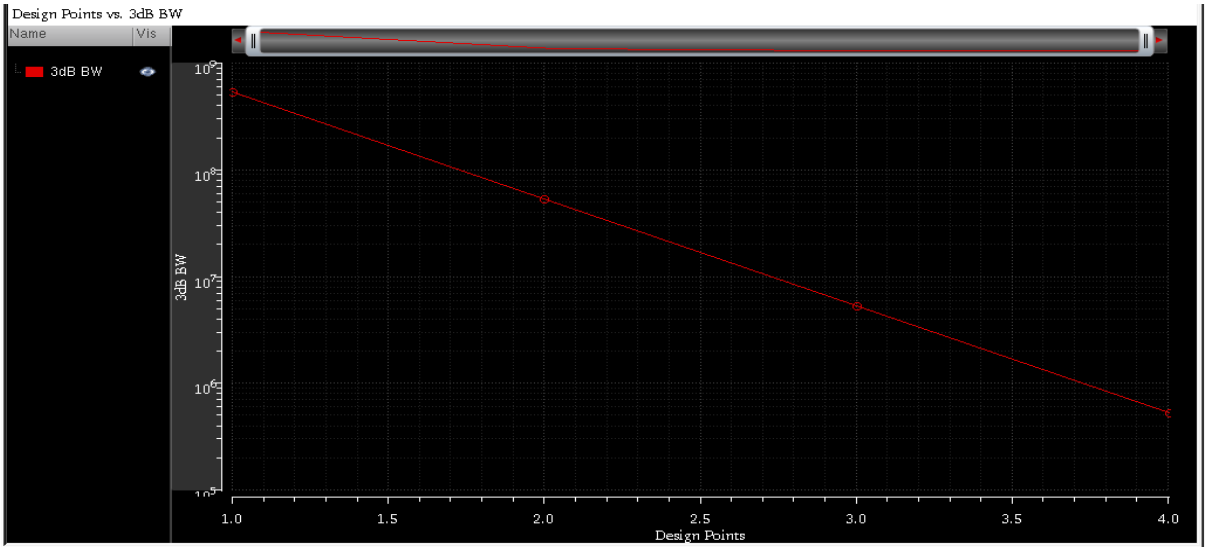
BW = 1/(2pi*R*C). That is BW is inversely proportional to R. As R increases by a factor of 10, BW decreases by a factor of 10, as can be observed.

Gain is independent of R, so it didn't change.

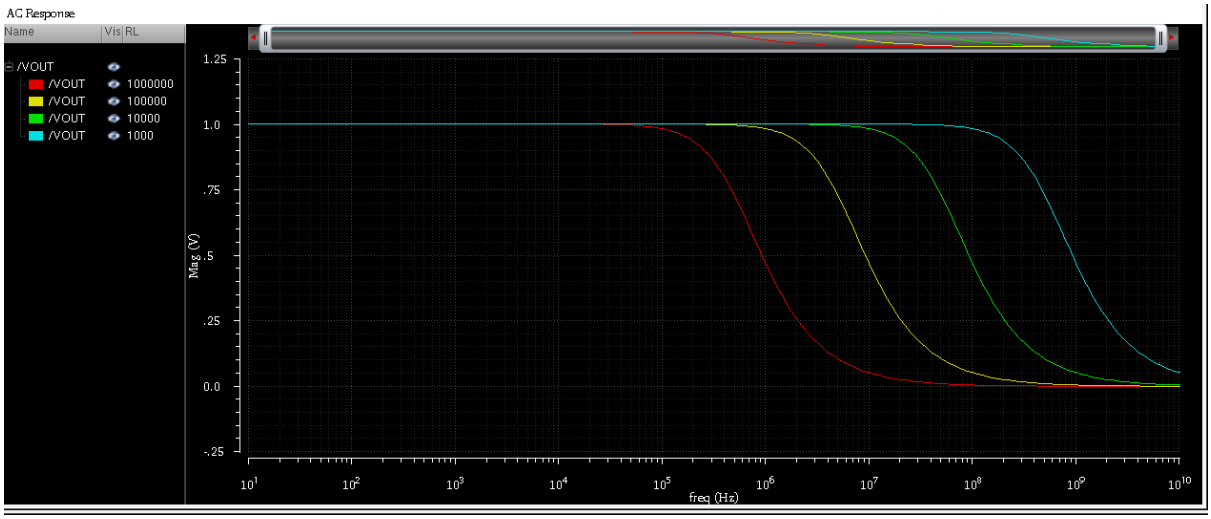
3dB bandwidth across design points (different R values) are shown below.



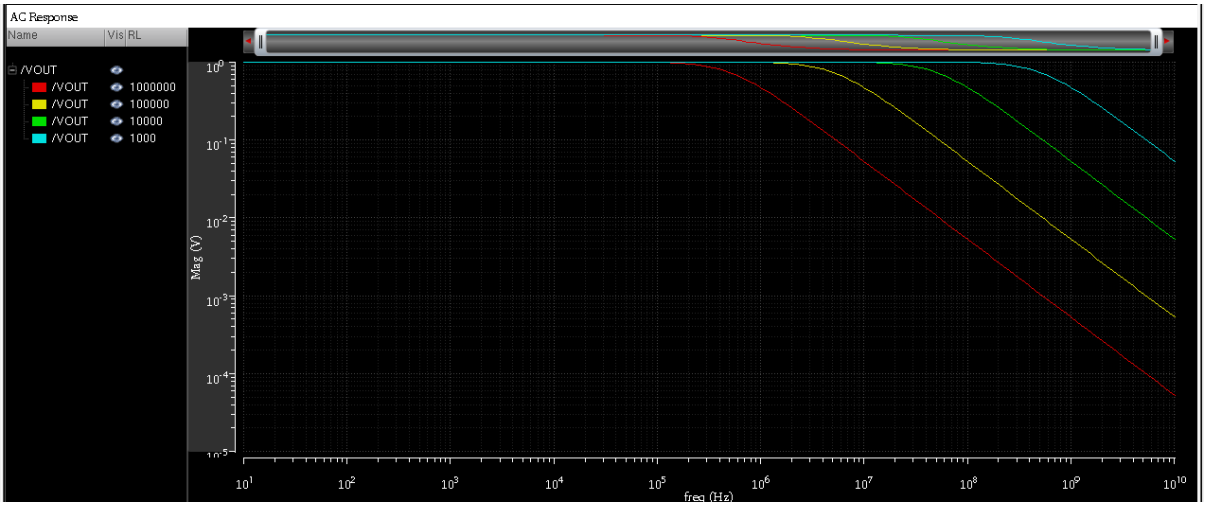
3dB bandwidth (on log scale) across design points



Vout across design points



Vout across design points on log scale



In the above graph, we can observe the bandwidth decreasing as R increases

3. Pole Zero Analysis

1) The PZ Analysis Results are reported for different values of RL.

RL = 1k

Poles (Hz)

	Real	Imaginary	Qfactor
1	-5.30516e+08	0.00000e+00	5.00000e-01

No zero is found

RL = 10k

Poles (Hz)

	Real	Imaginary	Qfactor
1	-5.30516e+07	0.00000e+00	5.00000e-01

No zero is found

RL = 100k

Poles (Hz)

	Real	Imaginary	Qfactor
1	-5.30516e+06	0.00000e+00	5.00000e-01

No zero is found

RL = 1M

Poles (Hz)

	Real	Imaginary	Qfactor
1	-5.30516e+05	0.00000e+00	5.00000e-01

No zero is found

As we expect, no zeros were found. A zero can be found at infinite frequency.

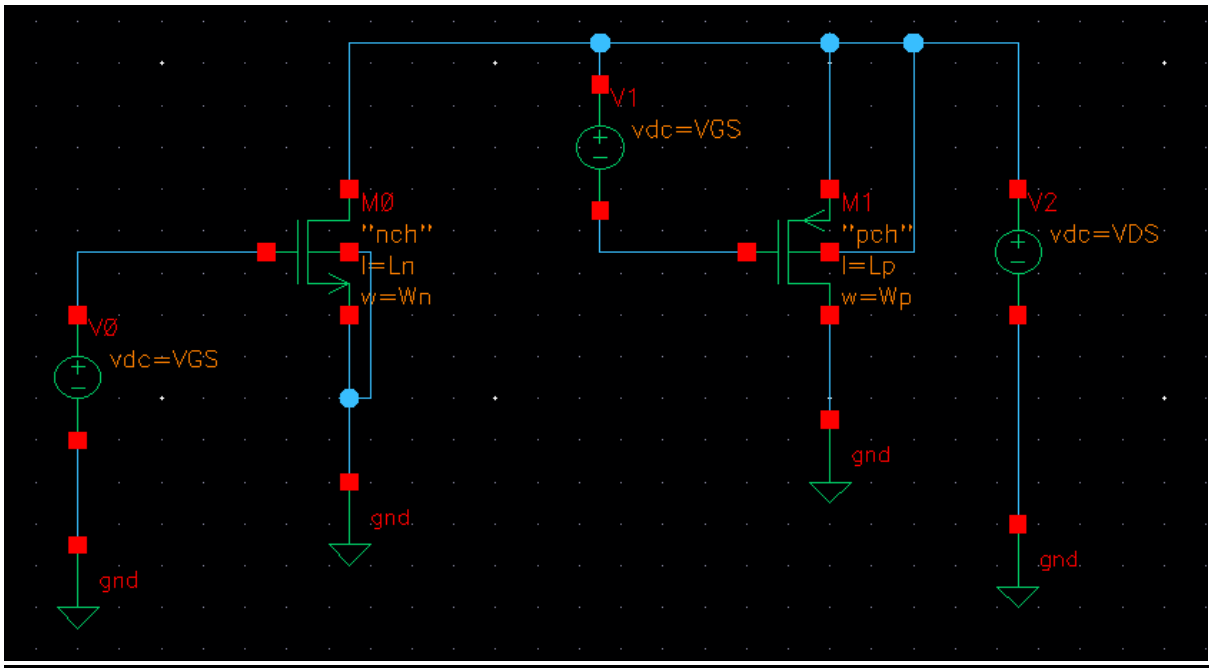
2) As the resistance gets higher, the frequency poles decrease.

Compared to the BW, the pole frequency is approximately equal to it.

Resistance	Frequency pole	BW
1K	530.5M	529.7M
10K	53.05M	52.97M
100k	5.305M	5.297M
1M	530.5k	529.7k

PART 2: MOSFET CHARACTERISTICS

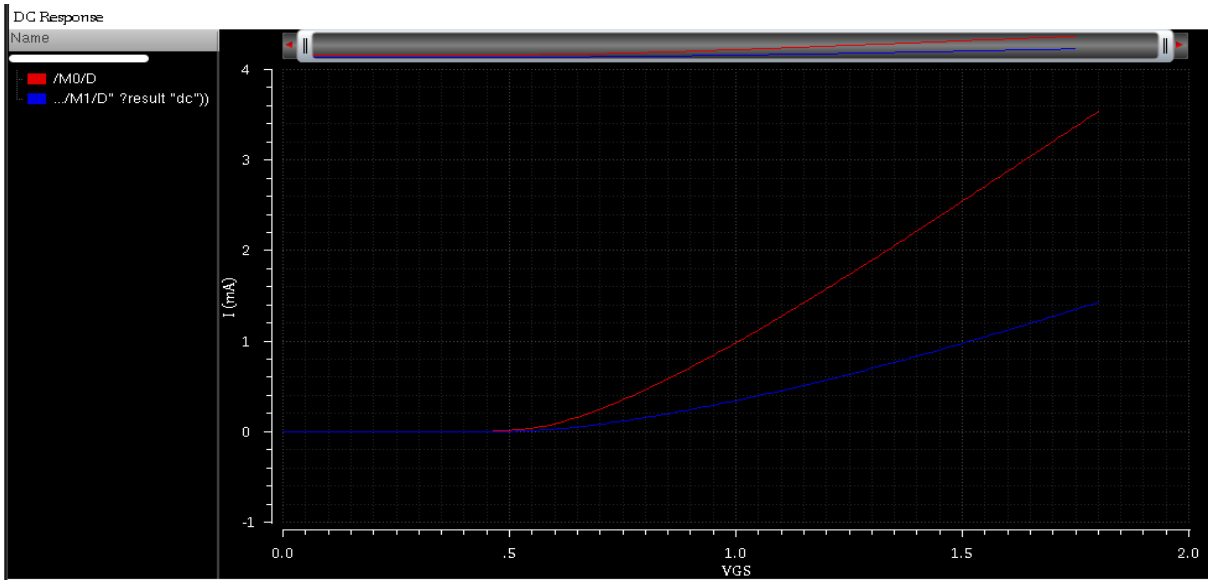
The circuit schematic is shown



1.ID vs VGS

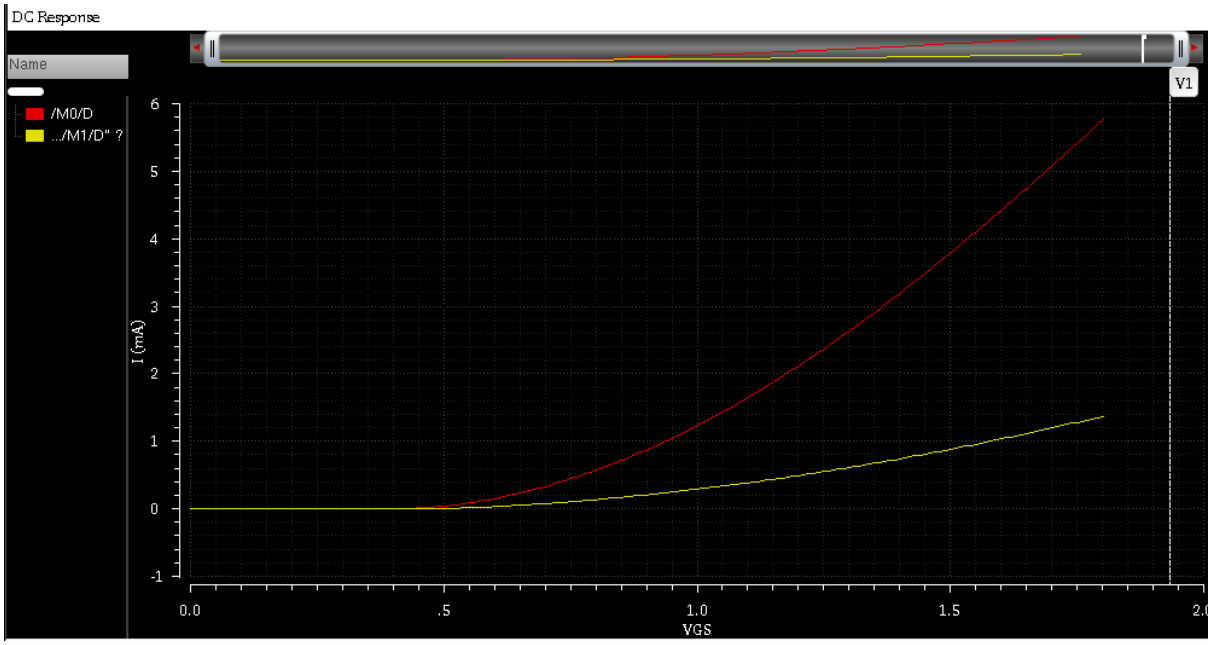
1) ***Short channel device***

ID(NMOS) is shown in red, and the absolute value of ID(PMOS) is shown in blue.



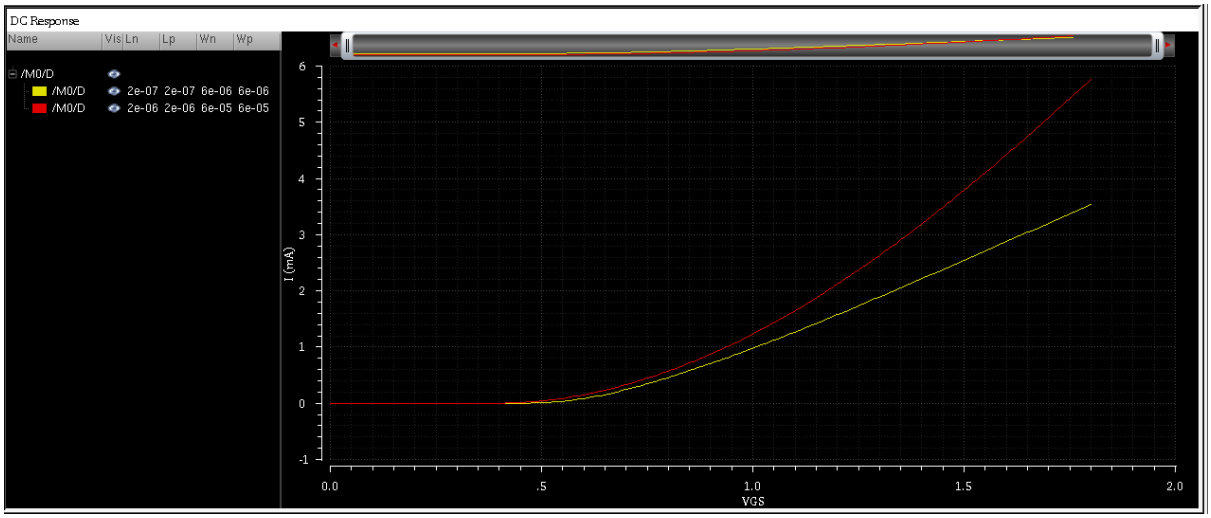
Long channel device

ID(NMOS) is shown in red, and the absolute value of ID(PMOS) is in blue.



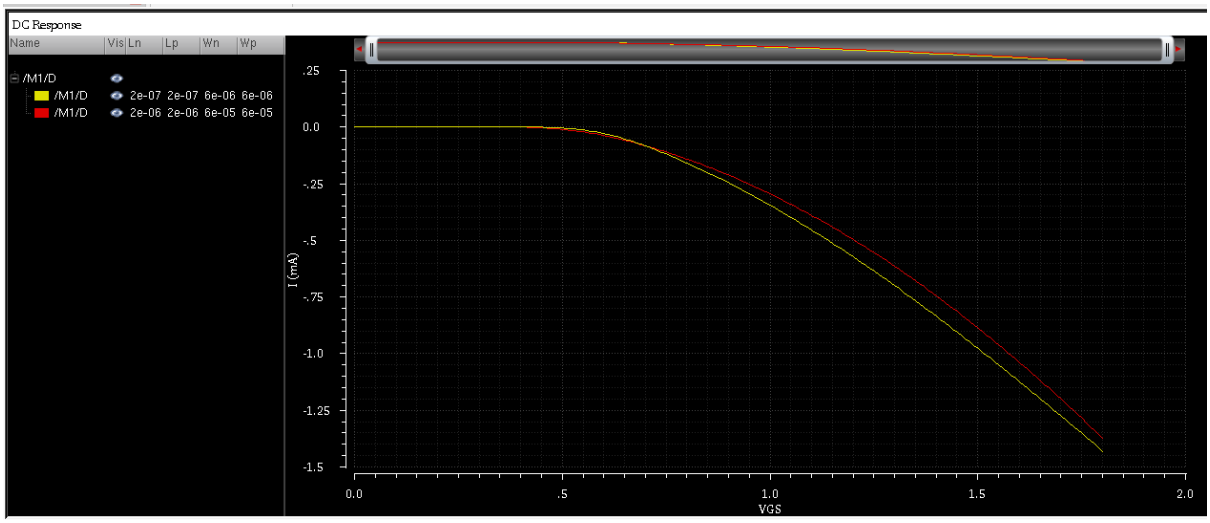
Ideally the two graphs should be the same, but actually there's a slight difference to be noticed if we look carefully.

2) **NMOS: Long Channel (red) vs Short Channel (yellow)**



We can observe that the current is higher for the long channel device. The current in the short channel device starts as a quadratic function, but follows a linear trend thereafter due to the short channel effect.

PMOS: Long Channel (red) vs Short Channel (yellow)



We can observe that the current is also higher for the long channel device. However, the difference is not as significant as was the case with the NMOS device since the PMOS device is less affected by velocity saturation since its carrier mobility, and therefore its speed, are already relatively low.

So, we conclude that:

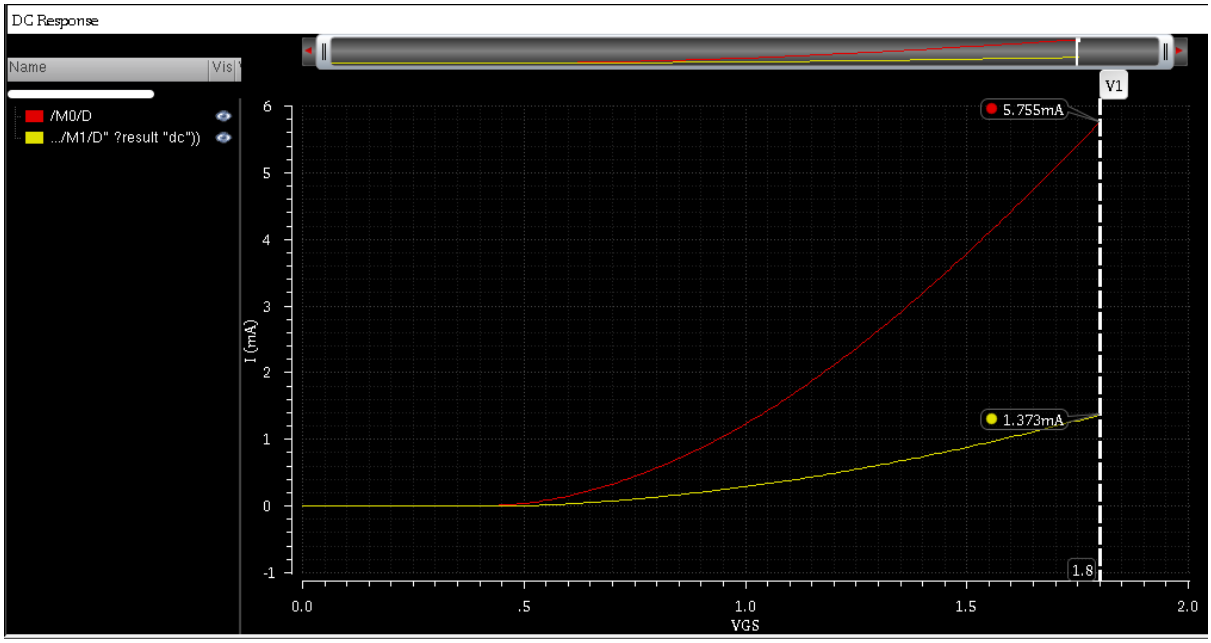
a) Long channel devices have higher currents than short channel devices.

b) The relation is quadratic for Long channel devices and almost linear for short channel devices

3) Differences between NMOS and PMOS

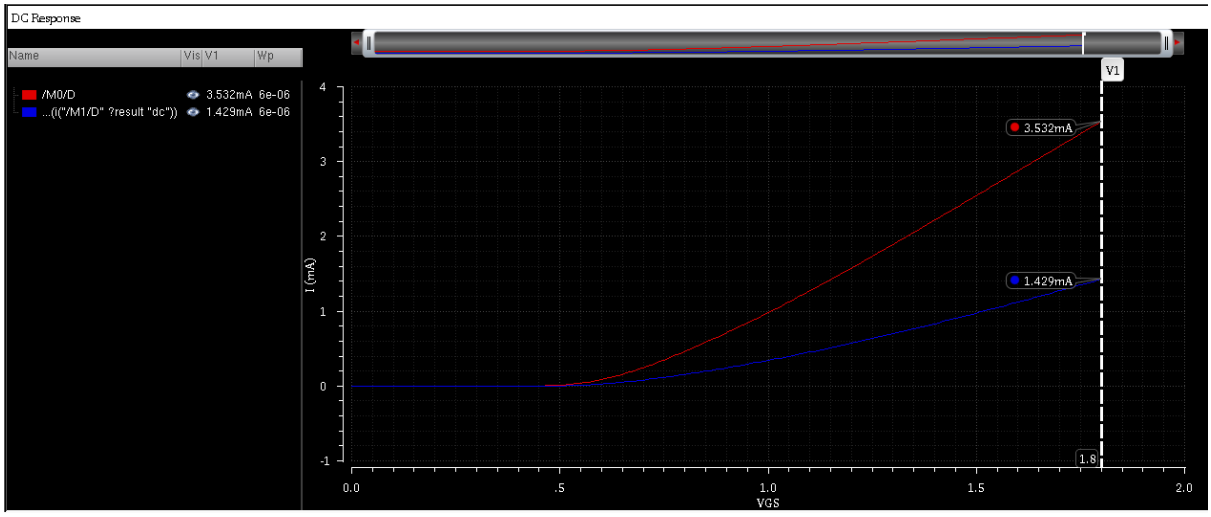
a) NMOS has higher current. Due to higher carrier mobility.

b) Ratios are calculated below



For long channel device, IDN = 5.755 mA, and IDP = 1.373 mA

so ratio = 5.755/1.373 = 4.19



For short channel device, IDN = 3.532 mA, and IDP = 1.429 mA

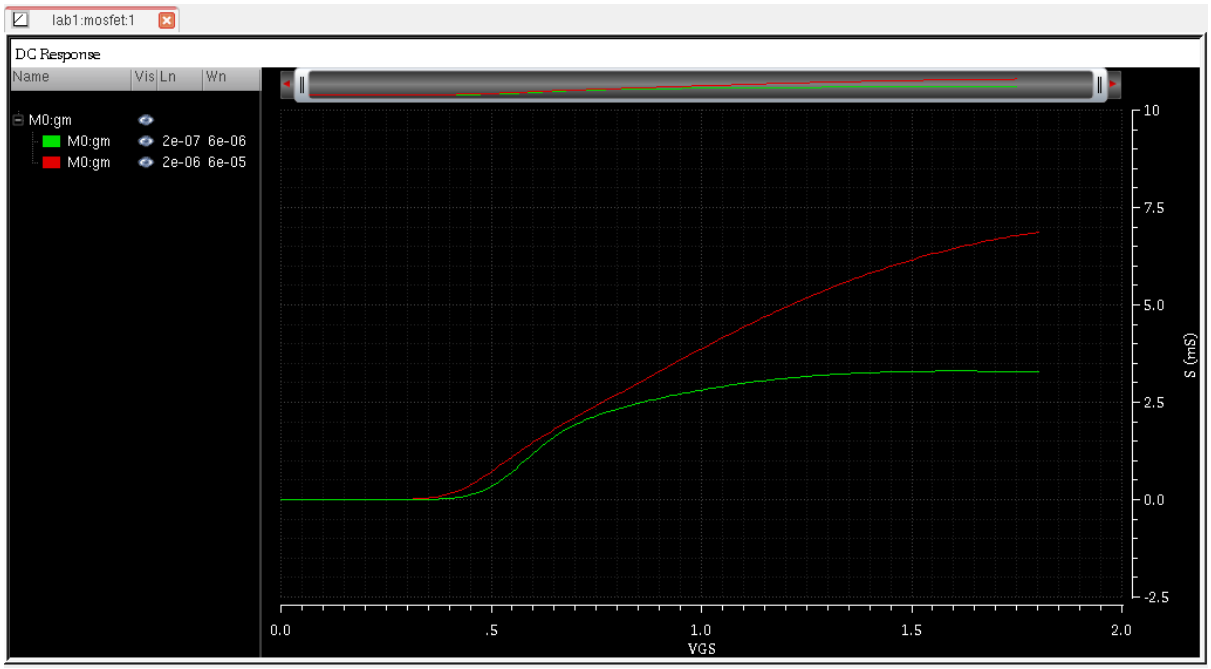
so ratio = 3.532/1.429 = 2.47

c) By comparing ratios and absolute values obtained,

NMOS is more affected by short channel effect due to its high carrier mobility and speed. PMOS already has low carrier mobility and speed so the effect of short channel is not as noticeable as with NMOS.

2.gm vs VGS

1)gm for short channel (green) and gm for long channel (red) are shown.



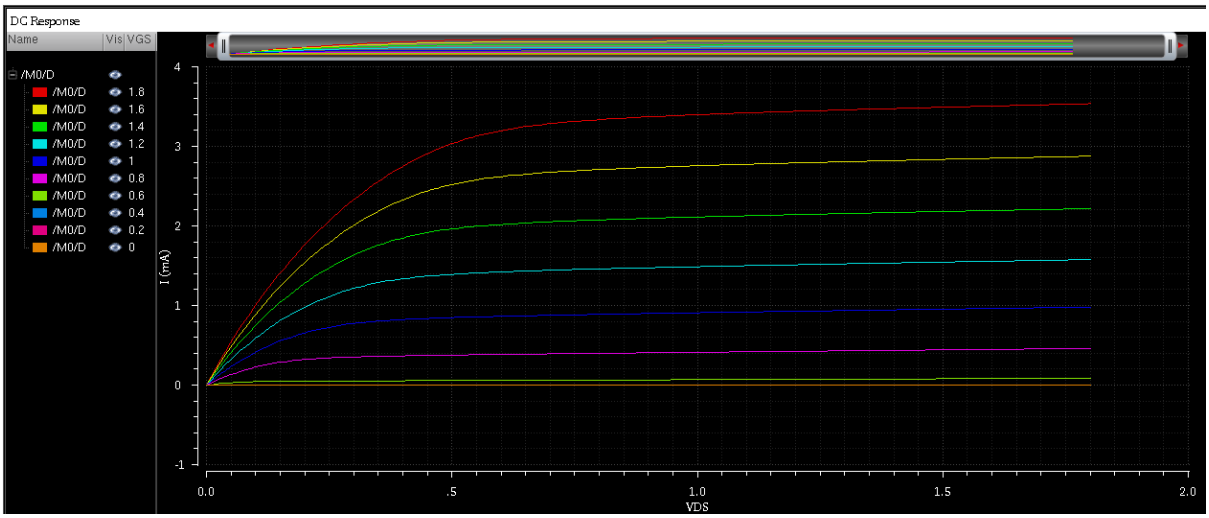
2) gm doesn't vary linearly with VGS. gm depends on the Q-point of the device, the device geometry (W/L), and the doping type. All these factors are non-linear and differ in different regions of operations, hence gm is not linearly related to VGS.

Does gm saturate?

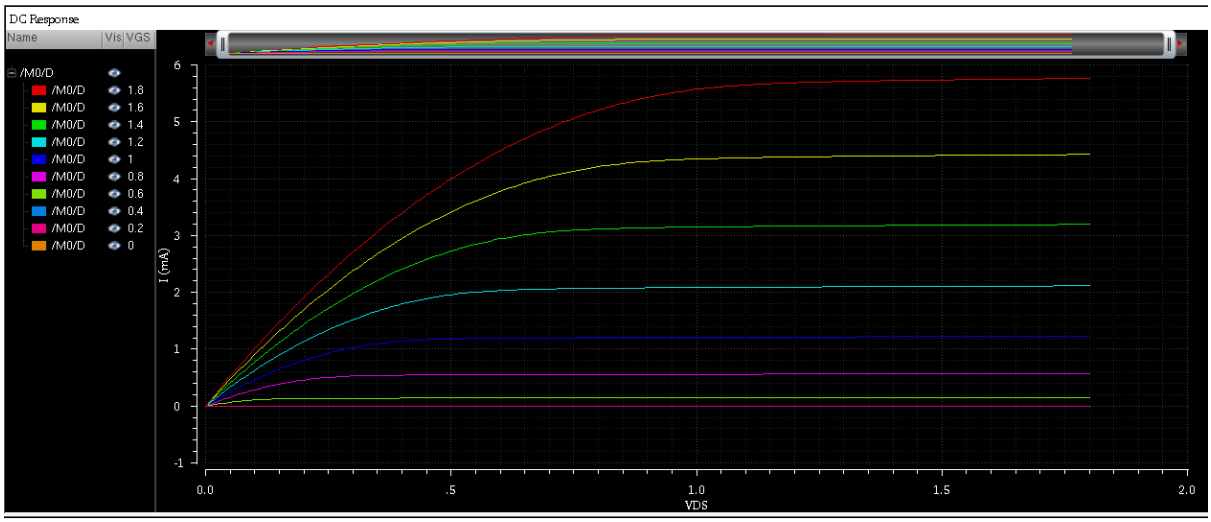
Yes, gm saturates. In the triode region, the transconductance gm is a function of VGS and hence increases with its increase. As VGS gets larger and the MOSFET enters the triode region, ID saturates, and gm is no longer a function of VGS, hence it saturates.

3.ID vs VDS

For short channel device



For long channel device

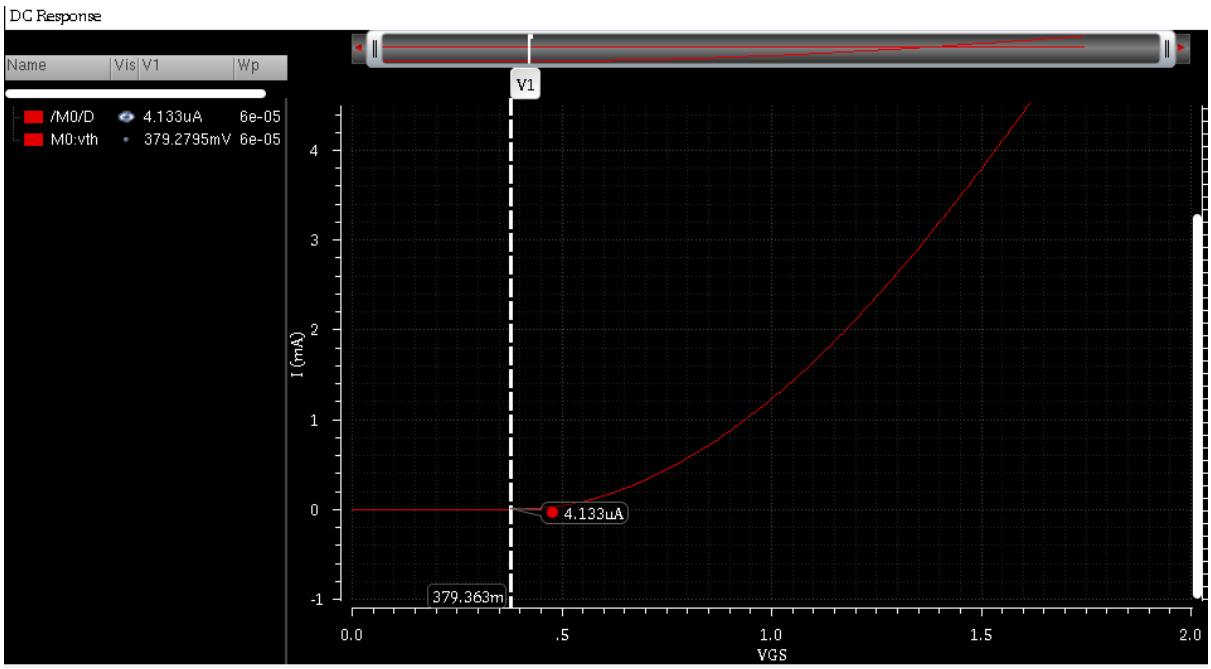


Long channel NMOS has a higher current than the short channel NMOS.

This is because the long-channel device has a longer channel length and a higher resistance.
Short-channel device has a higher slope in the saturation region, as according to CLM modulation we can't neglect the reduction from L to Leff in short-channel devices but we can neglect this effect in long-channel devices, also short-channel devices has DIBL effect

4. gm and ro in triode and saturation regions

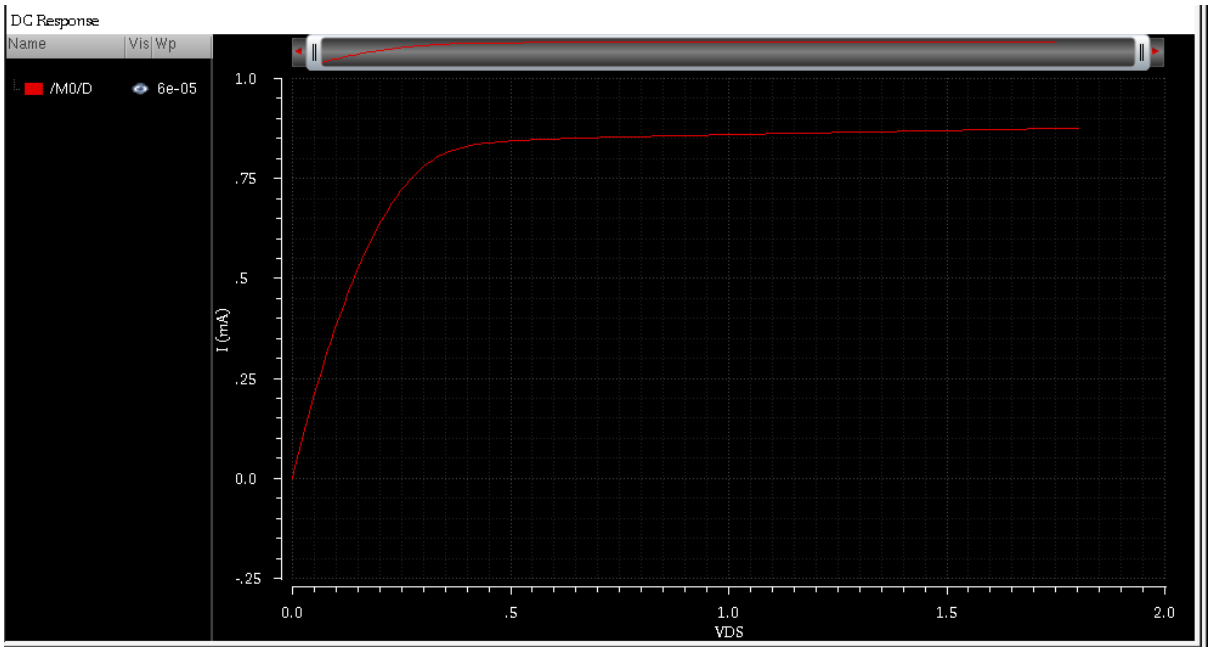
1) First, we will use the graph of ID vs VGS to obtain an estimate for VTH; At the point where ID starts to grow above zero, Transistor enters into the ON region and VGS = VTH.



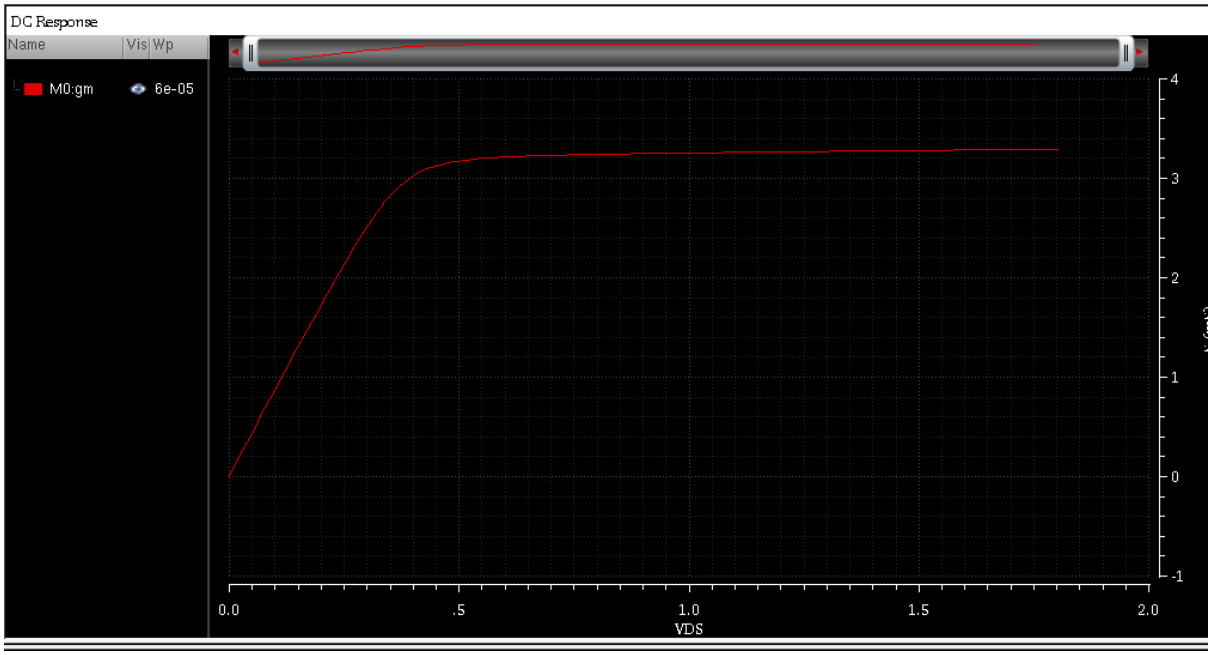
From the graph of ID vs VGS, VTH = 0.38, approximately.

Hence VGS = VTH + 0.5 = 0.88.

This is a plot for IDS vs VDS



This is the plot of gm vs VDS

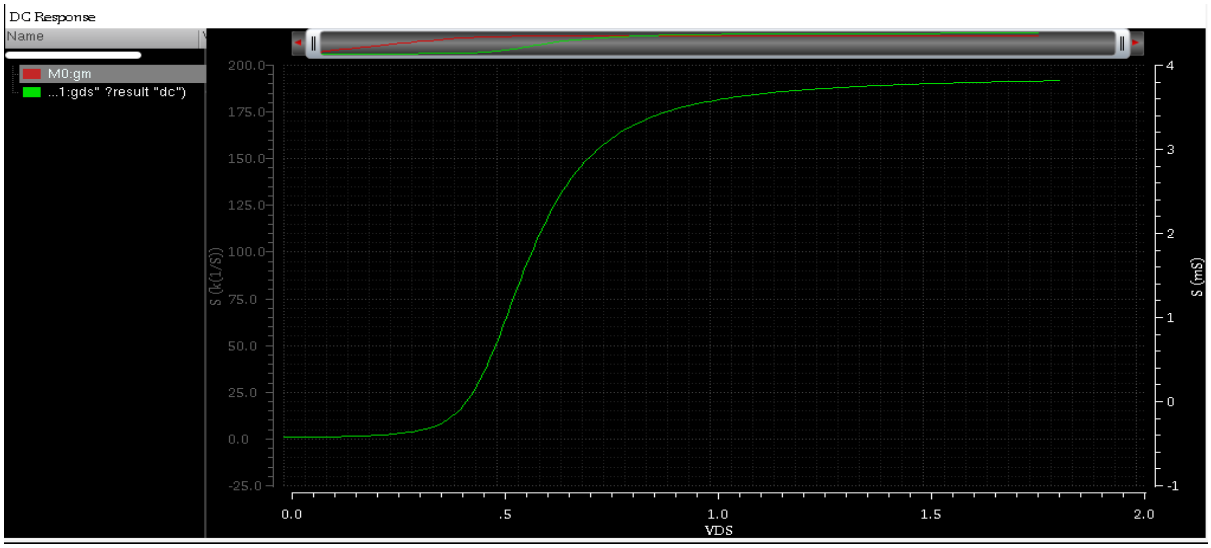


a) Yes, in the first part of the graph the relation is linear.

b) Yes, gm saturates since gm is proportional to ID and ID itself saturates beyond Vov.

c) For analog amplifier applications, it will be preferred to bias a transistor in the active region especially the saturation region because The biasing point can be chosen to provide a suitable operating point in the saturation region, where the transistor can provide linear amplification of the input signal without distortion or excessive power dissipation.

ro (1/gds) vs VDS



a) No. Since the change in ID becomes very small, and given that gds is the rate of change in ID wrt VDS and since ro = 1/gds, so ro increases. If we ignore channel length modulation, change in ID = 0, so gds = 0, and hence ro should be infinite.

b) Since ro is given by ro = 1/(λ * ID) and since ID can still increase in the saturation region, then ro will decrease. This happens when we take into effect channel length modulation.

c) No. It is recommended to bias the transistor in the saturation region, but not at the edge of saturation since it gives a minimal value of Rout, which lowers the gain. The biasing point should be chosen to provide a suitable operating point in the saturation region, where the transistor can provide linear amplification of the input signal without excessive power dissipation or distortion. The specific choice of biasing point depends on the specific requirements of the amplifier circuit and the characteristics of the NMOS transistor.

d) For analog amplifier applications, it will be preferred to bias a transistor in the active region especially the saturation region because The biasing point can be chosen to provide a suitable operating point in the saturation region, where the transistor can provide linear amplification of the input signal without distortion or excessive power dissipation.