ELCN201 – Electronics 2

Project-1 Report

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Code: 1200399

CCEE

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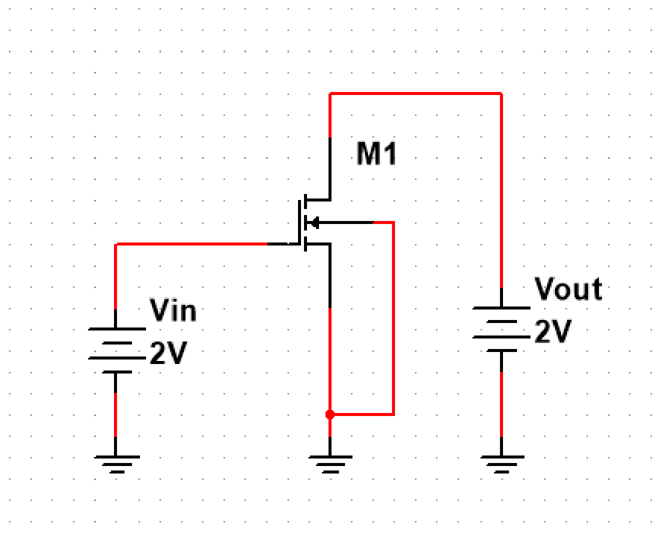
Problem (1): Transistor Characterization

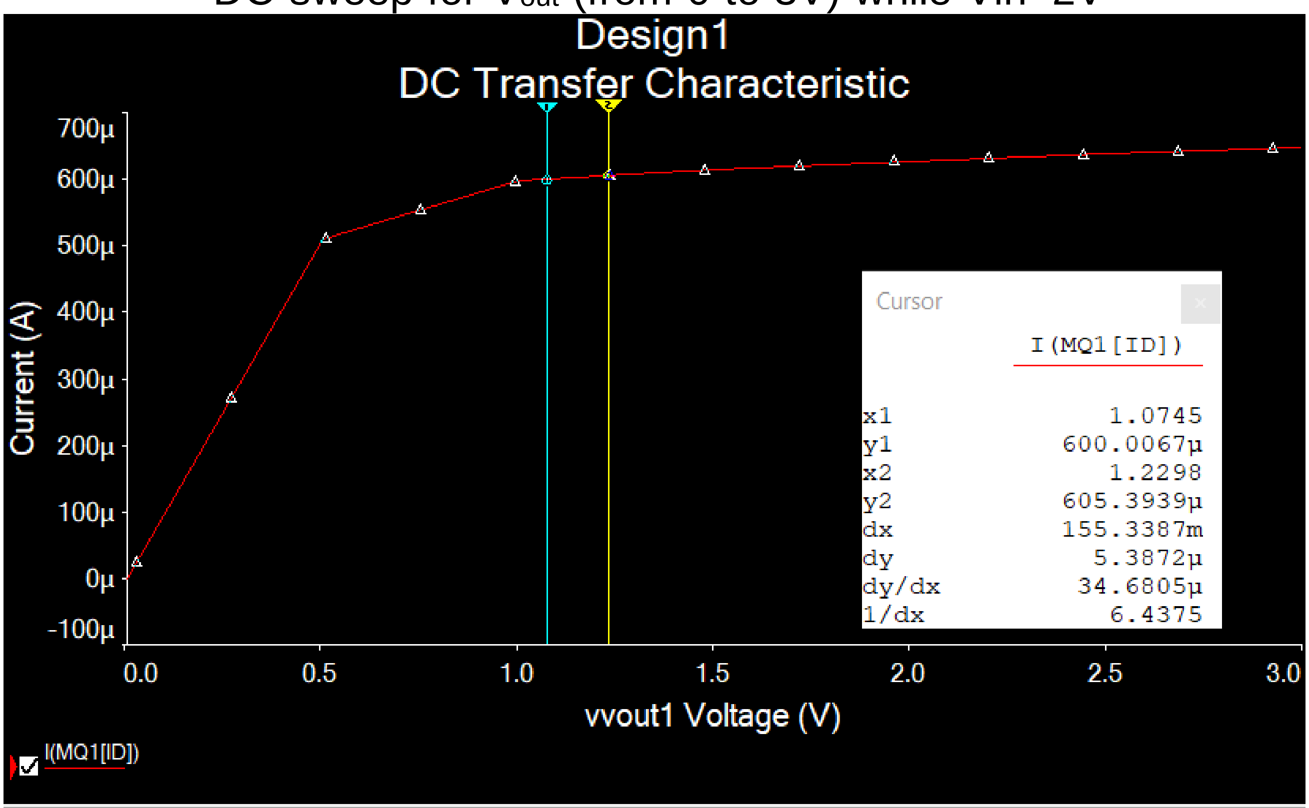
Using NMOS



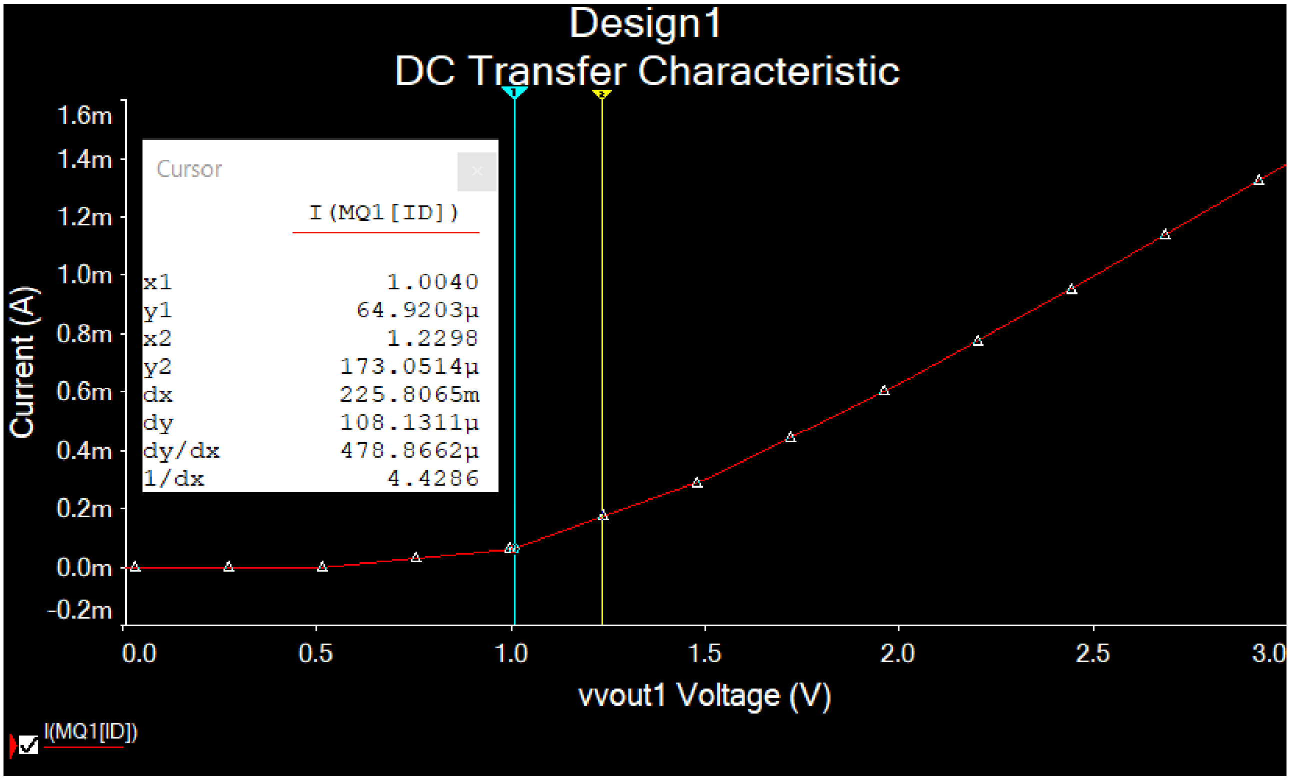
[A]

- **For W=10μm, L=1μm:**

DC sweep for V_{out} (from 0 to 3V) while Vin=2V



DC sweep for V_{in} (from 0 to 3V) while V_{out}=2V

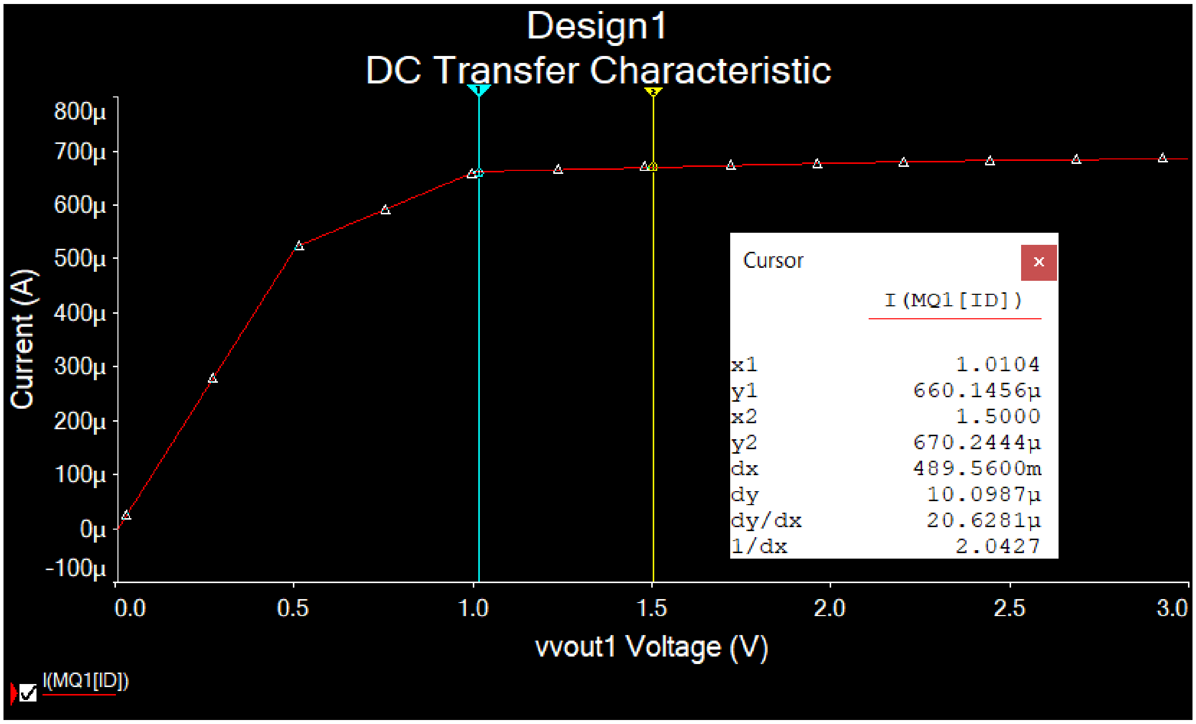


From graphs:

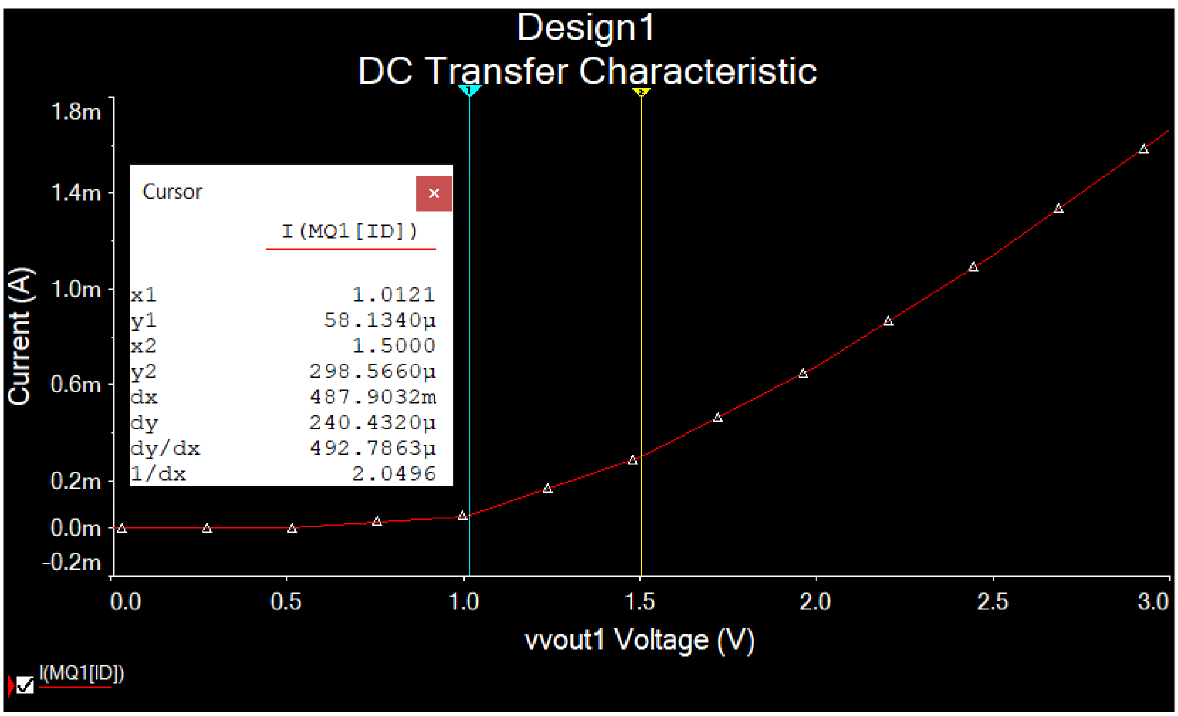
- **V_{ov}=** 1.0745 V
- **V_{th}=** 997.2618 mV
- **I_D=** 600.0060 µA
- **Slope=** 34.6805 $\mu\Omega^{-1}$
- **Slope=** $1/r_o = \lambda * I_D$
- **λ=** $\text{Slope}/I_D = 0.0578\ V^{-1}$
- **I_D =** $\frac{1}{2} * \mu nCox * (W/L) * V_{ov}^2 * (1+\lambda V_{DS})$
- **µnCox =** 103.427 $\mu A/V^2$

- **For W=20μm, L=2μm:**

DC sweep for V_{out} (from 0 to 3V) while V_{in}=2V



DC sweep for V_{in} (from 0 to 3V) while V_{out}=2V

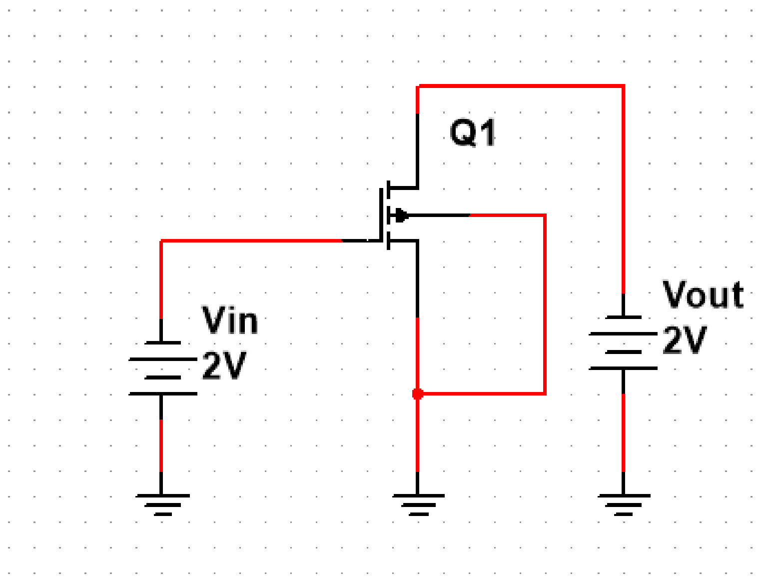


From graphs:

- **V_{ov}=** 1.0104 V
- **V_{th}=** 998.902 mV
- **I_D=** 660.145 µA
- **Slope=** 20.628 $\mu\Omega^{-1}$
- **Slope=** $1/r_o = \lambda * I_D$
- **λ=** $Slope/I_D = 0.0322\ V^{-1}$
- **I_D =** $\frac{1}{2} * \mu nCox * (W/L) * V_{ov}^2 * (1+\lambda V_{DS})$
- **$\mu_n C_{ox}$ =** 117.01 $\mu A/V^2$

❖ Doubling the width and the length of the NMOS will increase the current, and the slope will decrease, which leads to decrease in λ and a slight increase in ($\mu_n C_{ox}$).

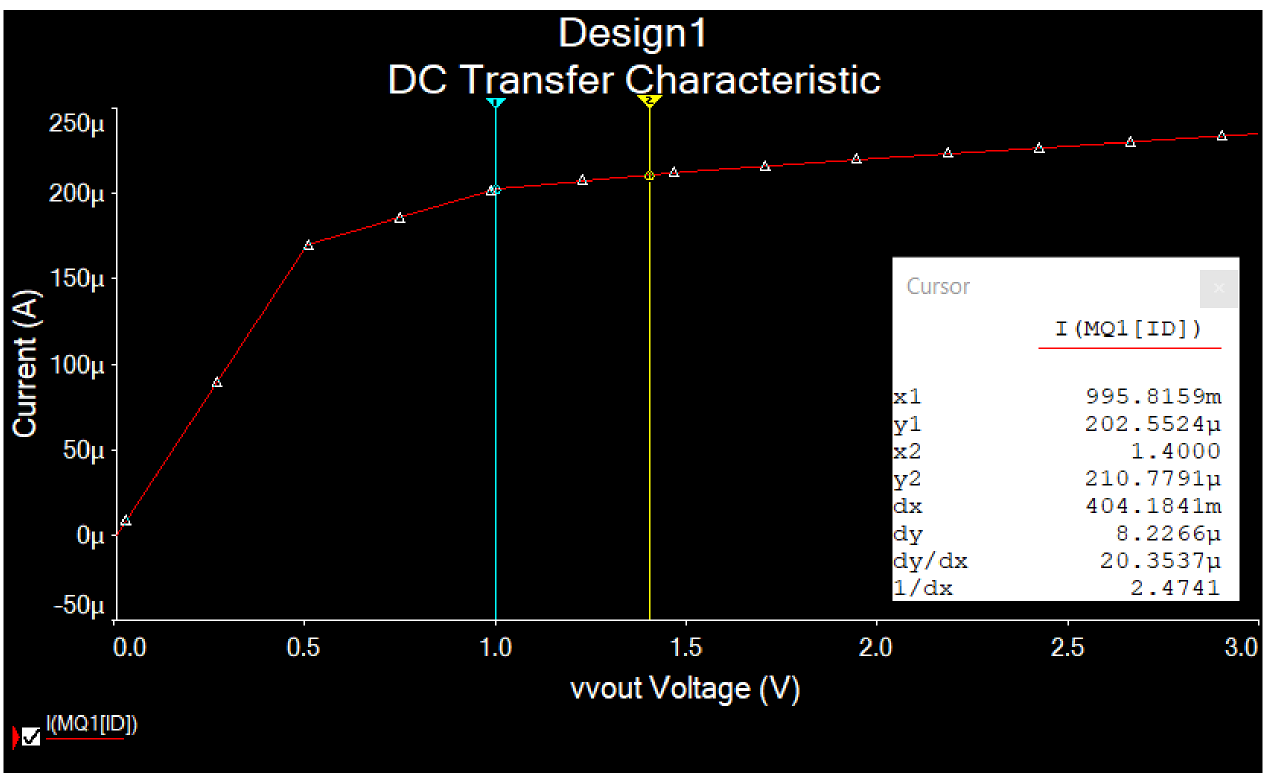
Using PMOS



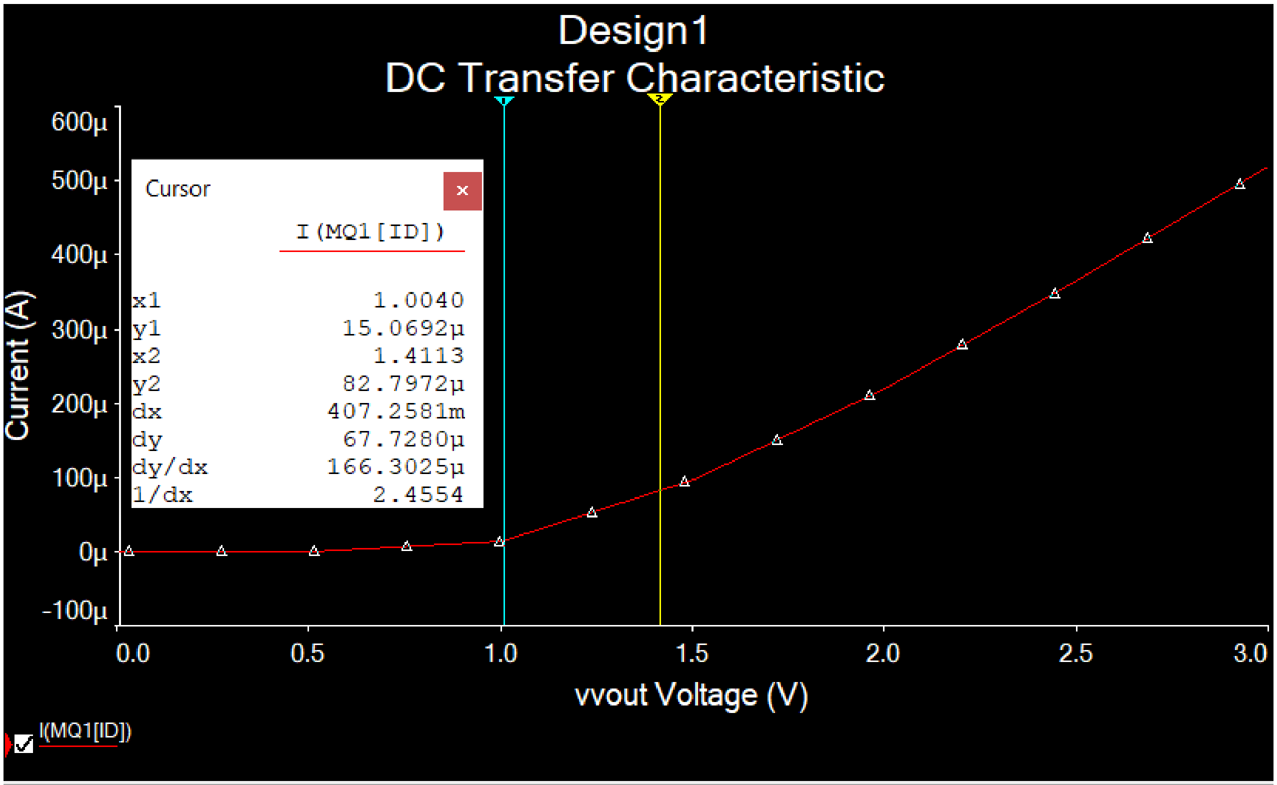
[B]

- **For W=10µm, L=1µm:**

DC sweep for V_{out} (from 0 to 3V) while V_{in}=2V



DC sweep for V_{in} (from 0 to 3V) while V_{out}=2V

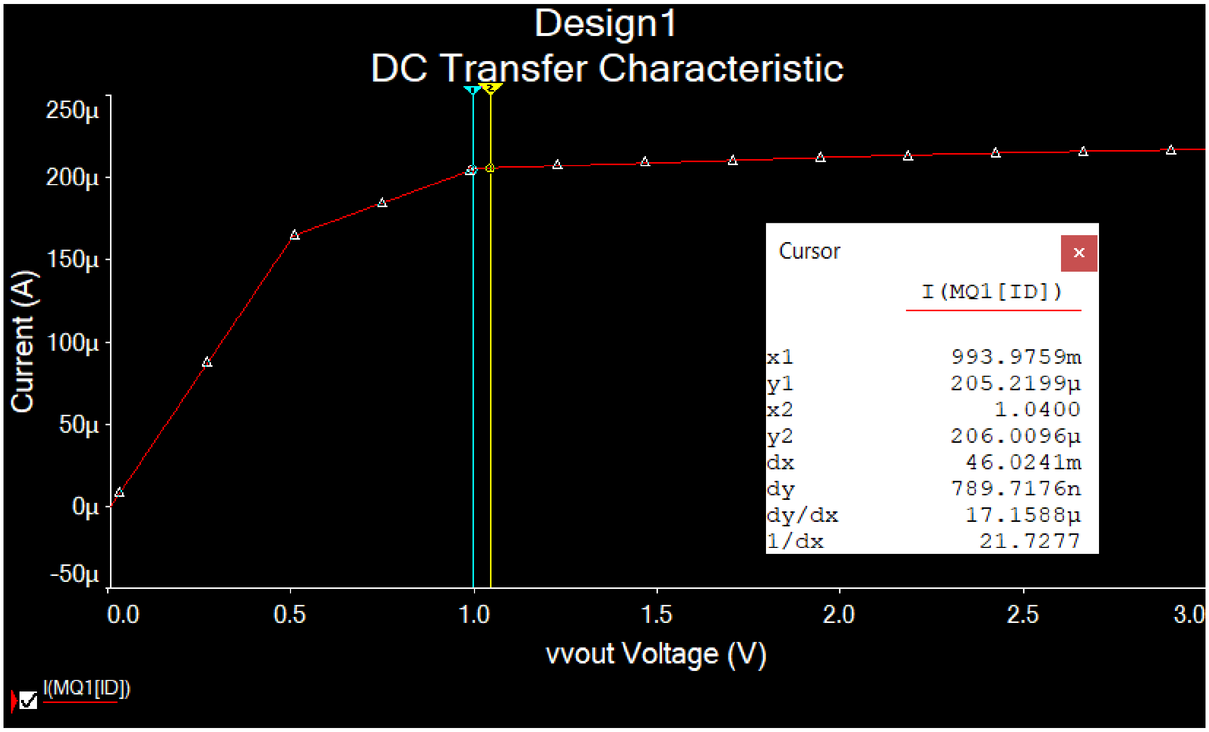


From graphs:

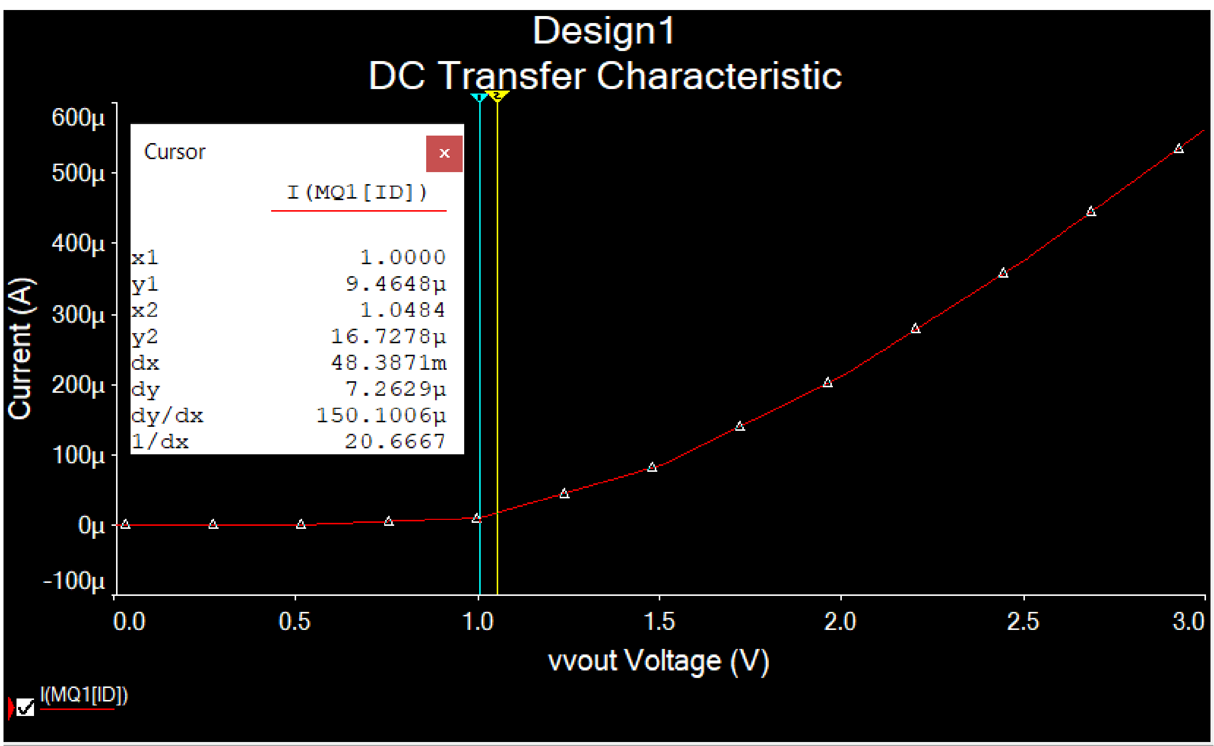
- V_{ov} = 995.8159 mV
- $|V_{th}|$ = 993.976mV
- I_D = 202.5524 µA
- Slope = 20.353 $\mu\Omega^{-1}$
- Slope = 1/Ro = λ*I_D
- λ = 0.1004 V^{-1}
- $I_D = \frac{1}{2} * \mu pCox * (W/L) * V_{ov}^2 * (1+\lambda * V_{DS})$
- µpCox = 34.02 µA/V^2

- **For W=20μm, L=2μm:**

DC sweep for V_{out} (from 0 to 3V) while V_{in}=2V



DC sweep for Vin (from 0 to 3V) while Vout=2V



From graphs:

- $V_{ov} = 993.9759$ mV
- $|V_{th}| = 992.3581$ mV
- $I_D = 205.0880\ \mu A$
- Slope = $17.1588\ \mu\Omega^{-1}$
- Slope = $1/R_o = \lambda * I_D$
- $\lambda = 0.08454\ V^{-1}$
- $I_D = ½ * \mu_P C_{ox} * (W/L) * V_{ov}^2 * (1 + \lambda * V_{DS})$
- $\mu_P C_{ox} = 35.62\ \mu A/V^2$

- Doubling the width and the length of the PMOS, will increase the current slightly, and the slope will decrease, which leads to a slight increase in ($\mu_p C_{ox}$).

[C] Comparison between NMOS and PMOS devices:

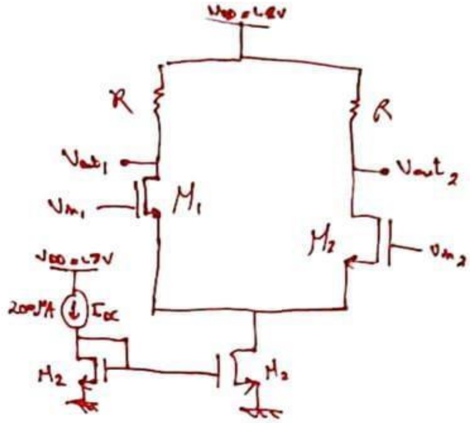
	NMOS	PMOS
For W/L=10	**V_{th}=** 997.2618 mV **λ=** 0.0578 V^{-1} **$\mu_n C_{ox}$=** 103.427 $\mu A/V^2$	**V_{th}=** 993.976 mV **λ=** 0.1004 V^{-1} **$\mu_p C_{ox}$=** 34.02 $\mu A/V^2$
For W/L= 20	**V_{th}=** 998.902 mV **λ=** 0.0322 V^{-1} **$\mu_n C_{ox}$=** 117.01 $\mu A/V^2$	**V_{th}=** 992.3581 mV **λ=** 0.08454 V^{-1} **$\mu_p C_{ox}$=** 35.62 $\mu A/V^2$

[D] Generally

Using the same dimensions for both the NMOS and PMOS (W=10 µm, L=1 µm) and applying the same changes to both MOSFETs which are ($W_2 = 2*W_1$ & $L_2 = 2*L_1$), it was observed that the changes in NMOS dimensions affects the current greatly, while in PMOS the change is negligible, and this is because of the difference between the mobility of the NMOS and the PMOS, where the mobility of NMOS (electrons) is larger than that of PMOS (holes). It is also noted that ro varies proportionally with the channel length L. Also due to the lower current-conducting ability of the PMOS devices, they offer a larger ro for the same dimensions.

Problem (2): Differential Amplifier

[A],[B]



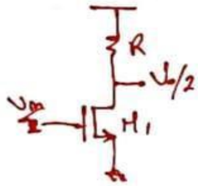
$I_{D1} = I_{D2} = \frac{I_{REF}}{2} = 100\,\mu A$

a] $A_{DM} \geq 5$

$I_{L}R \geq 0.2V$

Differential output swing $\geq 2.4\,V_{pp}$

→ Differential mode :



$A_V = -g_m(r_{o1} // R)$

$L_I R \geq 0.2\,V$

$0.9 V_{ov} \geq 0.2V$

$V_{ov} \geq 0.222$ Volts

Assume $V_{ov} = 0.42V$ & $\mu_n C_{ox} = 103.427\,\mu A/V^2$ "From M_1"

$I_{D1} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)(V_{ov})^2$

$\frac{W_1}{L_1} = 33.57$ "For 2 M1 mosfets"

$g_m = \frac{2I_D}{V_{ov}} = 8.33 \times 10^{-4}\,\Omega^{-1}$

$r_o = \frac{1}{\lambda I_D} = \frac{1}{0.578 \times 100 \times 10^{-6}} = 173.61\,K\Omega$

$A_{DM} \geq 5$, $g_{m1}\left(\frac{r_{o1} R}{r_{o1}+R}\right) \geq 5 \longrightarrow \frac{R(173.61)}{R+173.61} \geq 6002.4$

$R \geq 6215.59 \longrightarrow \boxed{R \simeq 6250\,\Omega}$

Diff. output Swing ≥ 2.4

$2(V_{DD} - V_{ov_1} - V_{ov_2}) \geq 2.4$

$1.8 - 0.24 - V_{ov_2} \geq 1.2$

$V_{ov_2} \leq 0.36$

$\boxed{V_{ov_2} \simeq 0.36}$

$$I_{D2} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W_2}{L_2}\right)(V_{ov_2})^2$$

$$\frac{W_2}{L_2} = 29.84$$ "for 2 M_2 mosfets"

* Check Saturation:

$$V_{ov_1} + V_{ov_2} < V_o$$
$$0.24 + 0.36 < 1.175$$
"Proven"

$$V_o = V_{DD} - I_{D1}R = 1.8 - 100\times10^{-6}\times 6250 = 1.175\ V$$

b]

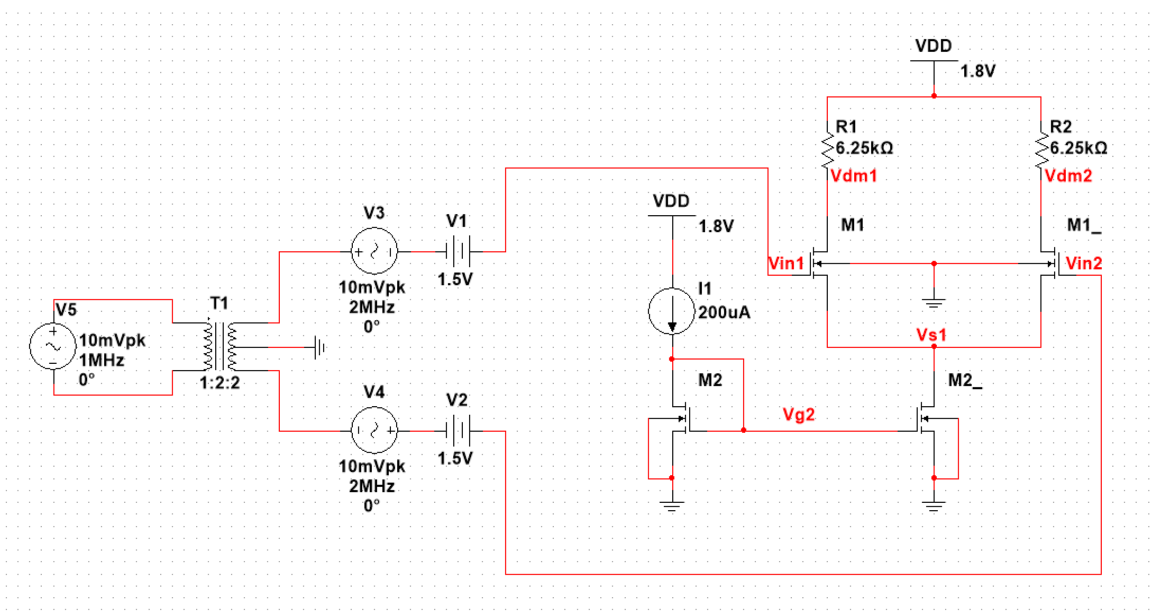
For saturation:

$$V_{DS} \geq V_{GS} - V_{th}$$
$$V_D \geq V_G - V_{th}$$
$$V_{DC} \leq V_D + V_{th}$$
$$V_{DC} \leq 1.175 + 0.997$$
$$\boxed{V_{DC_{max}} = 2.172\ V}$$

$$V_{GS_1} = V_{G_1} - V_{S_1}$$
$$V_{DC_{min}} = V_{GS} + V_S = V_{ov_1} + V_{ov_2} + V_T = 0.24 + 0.36 + 0.997$$
$$\boxed{V_{DC_{min}} = 1.597\ V}$$

[C]

➢ Differential circuit



DC analysis and the Q-point

For M1 & M1_ :

Design1
DC Operating Point Analysis

	Variable	Operating point value
1	V(vdm1)-V(vs1)	670.75510 m
2	V(vdm2)-V(vs1)	670.75510 m
3	V(vin1)-V(vs1)-0.7	279.49262 m
4	V(vin2)-V(vs1)-0.7	279.49262 m
5	I(M1[ID])	97.39800 u
6	I(M1_[ID])	97.39800 u

V_{ov1}= 0.279 V (for both M1 & M1_)

V_{DS}= 0.6707 V (for both M1 & M1_)

I_D= 97.398 µA (for both M1 & M1_)

For M2 & M2_ :

Design1
DC Operating Point Analysis

	Variable	Operating point value
1	V(vg2)-0.65	352.04549 m
2	V(vg2)	1.00205
3	I(M2[ID])	200.00000 u
4	V(vs1)	520.50738 m
5	I(M2_[ID])	194.79600 u

V_{ov2}= 0.352 V (for both M2 & M2_)

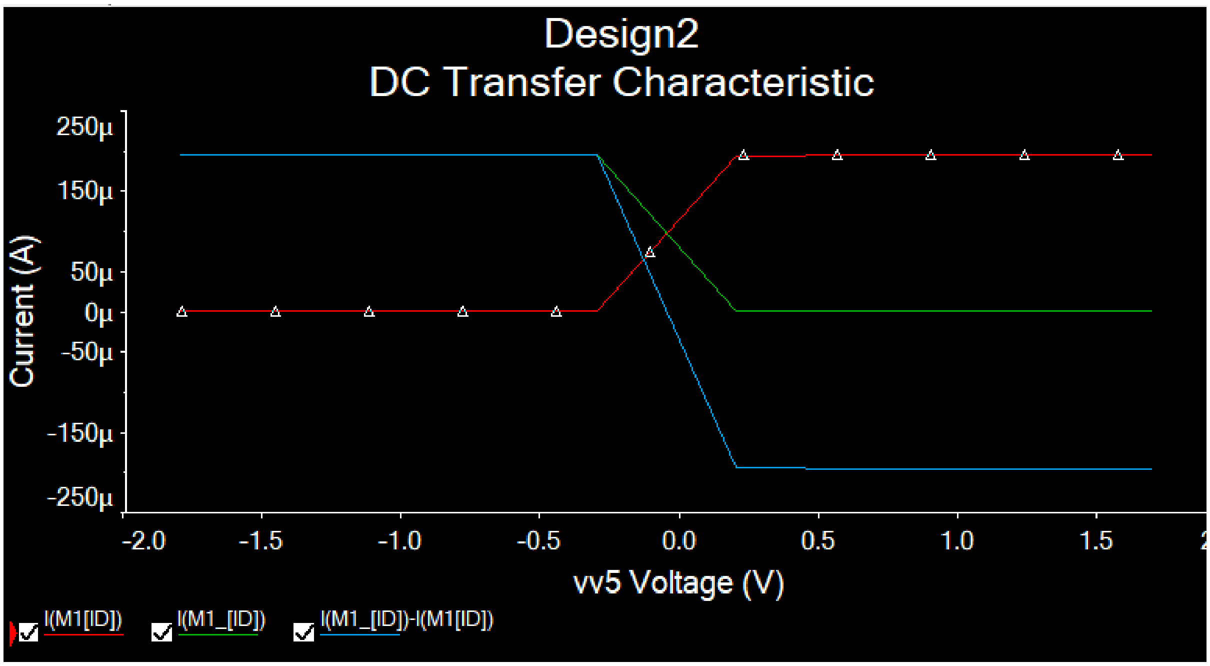
V_{DS}= 1.00205 V (for M2)

V_{DS}= 0.5205 V (for M2_)

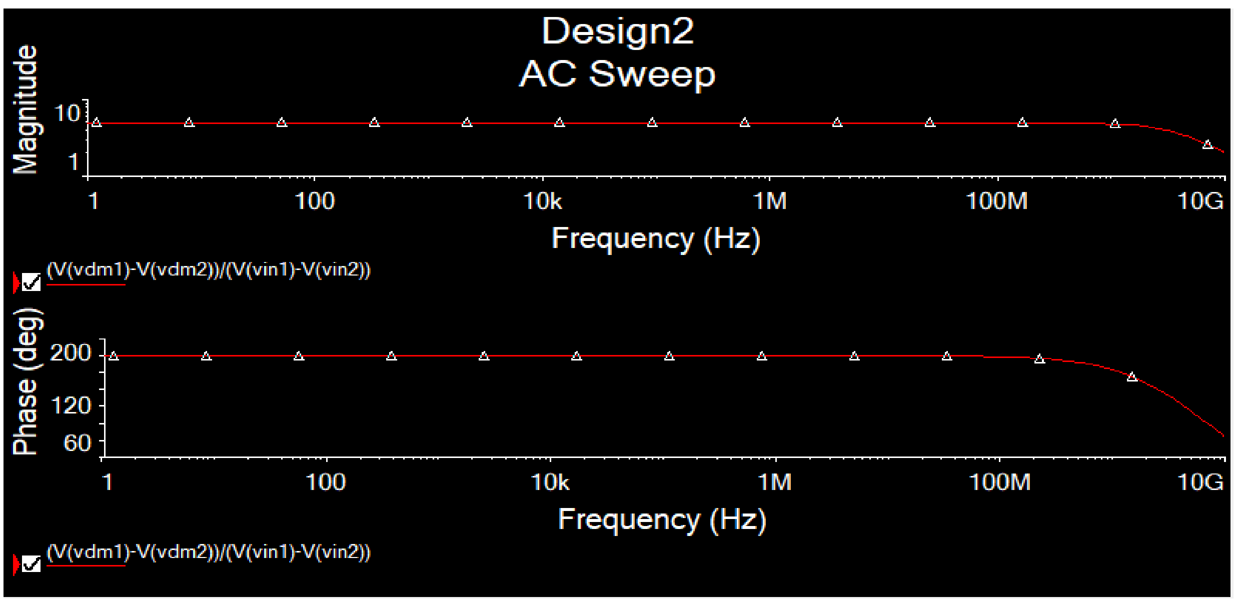
I_D= 200 µA (for M2)

I_D= 194.79 µA (for M2_)

DC sweep for V_{id} from -1.8V to 1.8V



AC analysis and the small-signal differential gain A_{DM}:



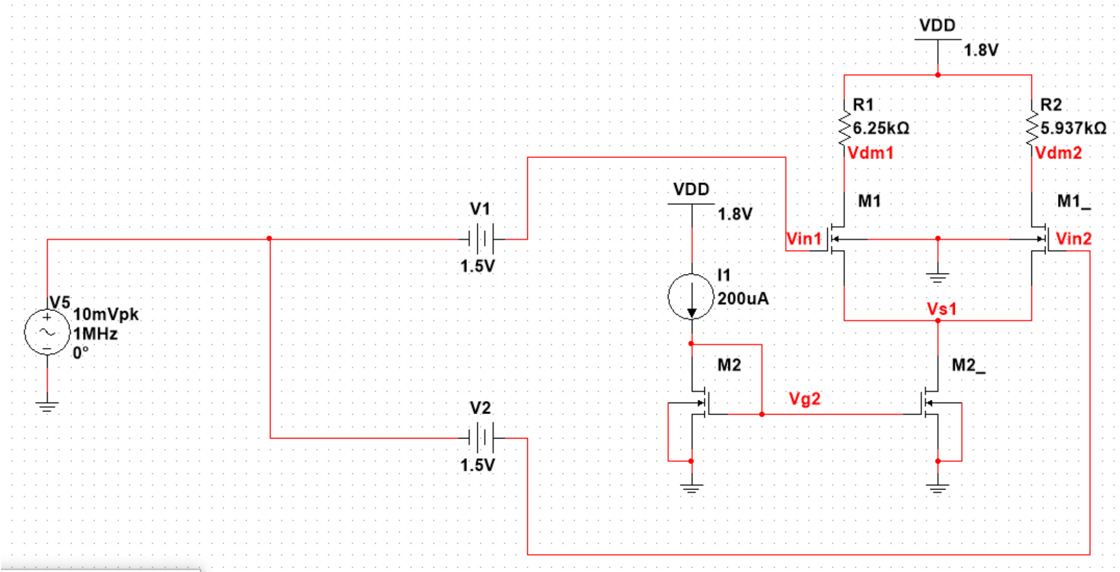
Sweep for $V_{out\ Diff}/ V_{in\ Diff}$, $A_{DM} \approx 5$

Cursor

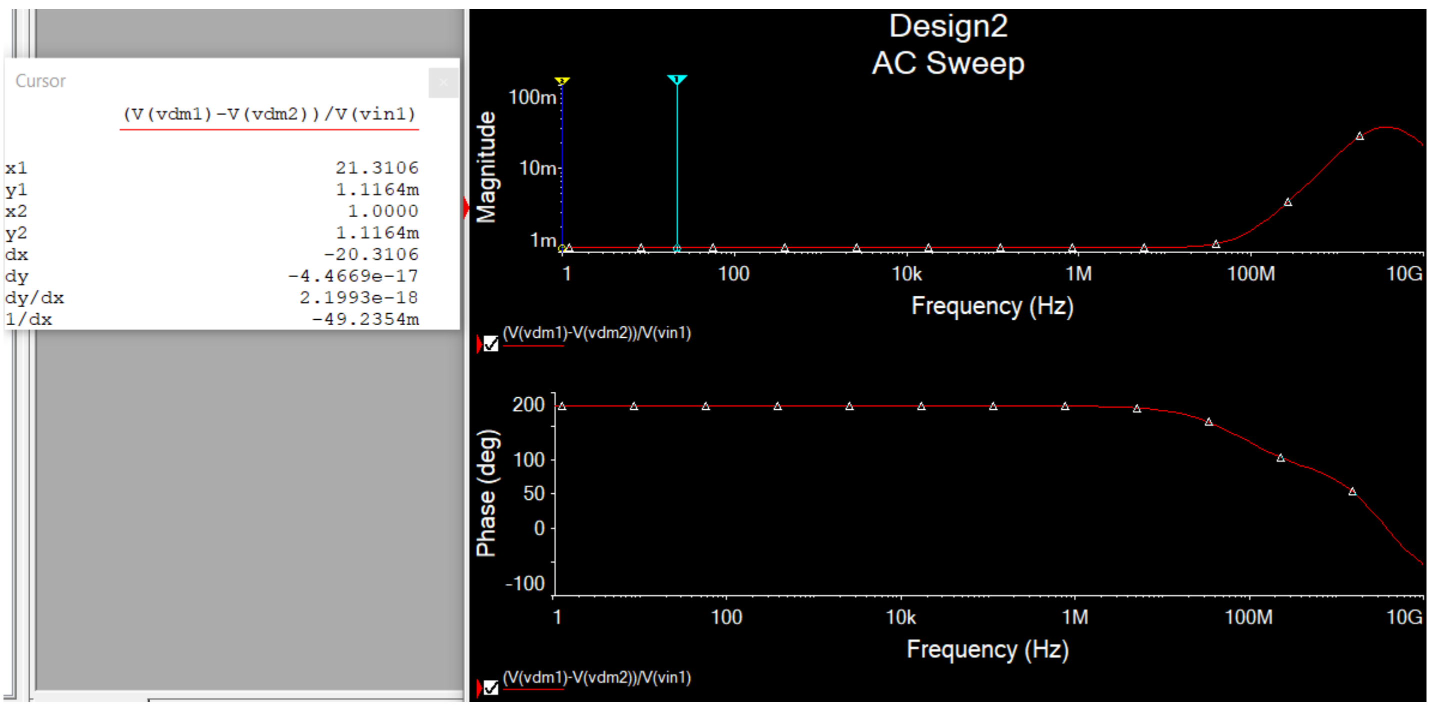
(V(vdm1)-V(vdm2))/(V(vin1)-V(vin2))

x1	1.9142k
y1	4.9148

➢ Common Mode Circuit: (5% mismatch in R)



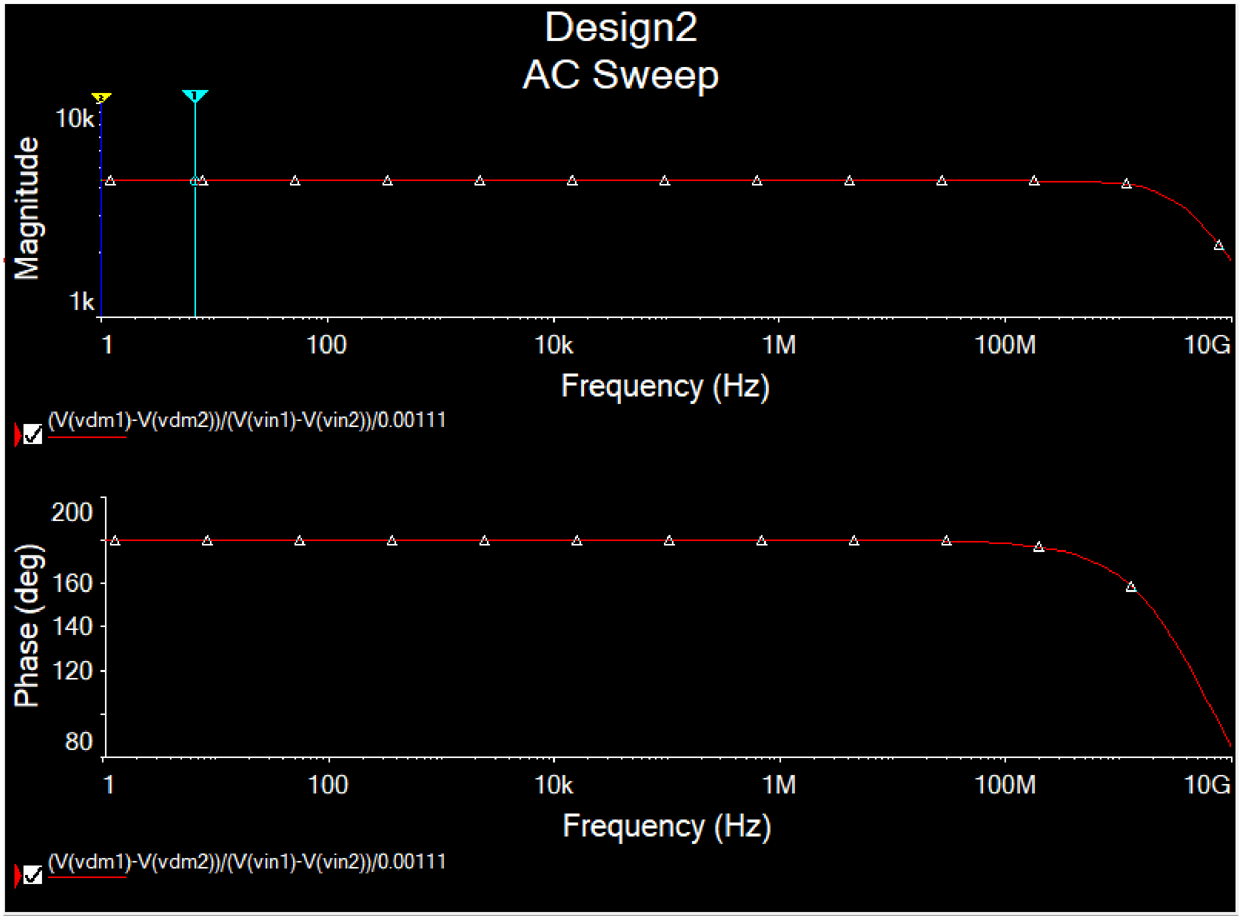
Conversion Gain:



From graph: $A_{CM\text{-}DM}$= 0.0011164

CMRR vs. Frequency:

CMRR=$A_{DM}/A_{CM\text{-}DM}$

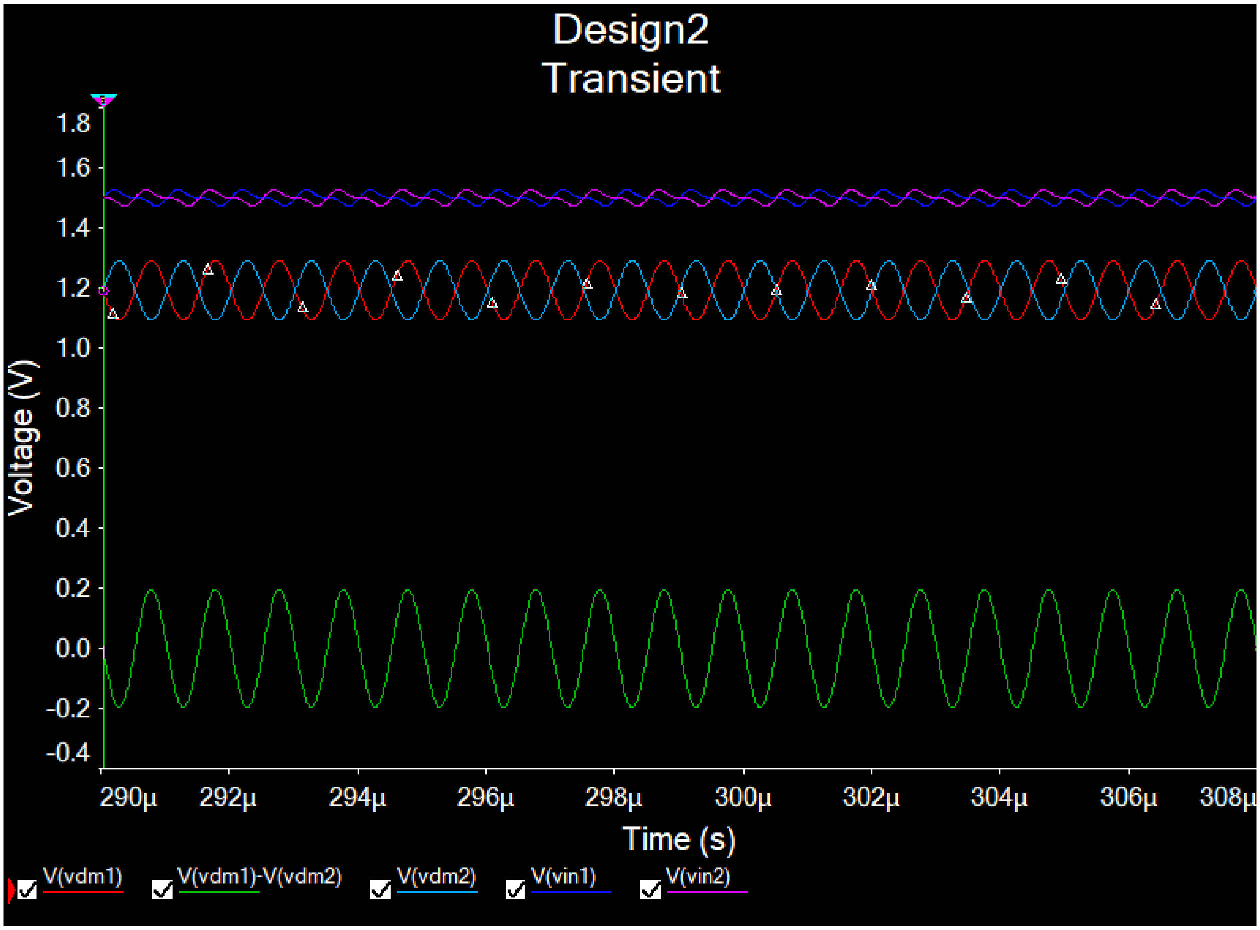


Cursor

	(V(vdm1)-V(vdm2))/(V(vin1)-V(vin2))/0.00111
x1	6.6970
y1	4.3239k
x2	1.0000
y2	4.3239k

CMRR ≈ 4.32K = 72.7 dB

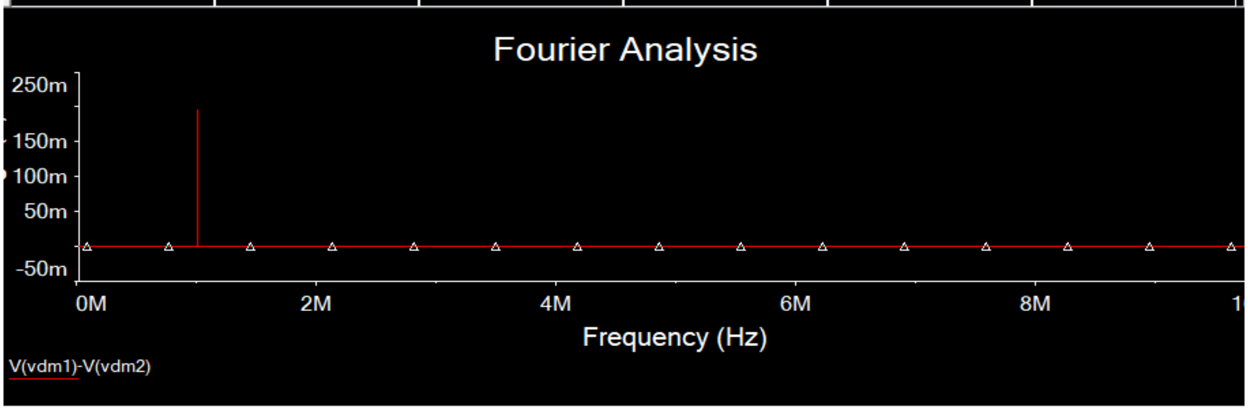
Transient Analysis:



Fourier analysis:

Design2

No. Harmonics:	9				
THD:	0.0737702 %				
Grid size:	256				
Interpolation Degree:	1				
Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
0	0	1.38541e-09	0	7.06517e-09	0
1	1e+06	0.19609	179.978	1	0
2	2e+06	2.77078e-09	92.8131	1.41302e-08	-87.165
3	3e+06	0.000144655	-173.8	0.000737701	-353.78
4	4e+06	2.77076e-09	95.6253	1.41301e-08	-84.353



THD=0.0737702 %

HD=Magnitude at n/Fundamental Magnitude

HD_2= 1.413 X 10^{-8}

HD_3=0.000737701

[D] Discussion

- ADM ≈ 5, ADM-CM ≈1m
- CMRR = 72.7 dB
- Differential output swing satisfied.
- There exists a slight, yet expected and acceptable, error in the mirrored current.

All the design specs are met. The large value of CMRR means our differential amplifier does its job of amplifying differential input and rejecting common mode input (i.e noise) well. Additionally, the value of the total harmonic distortion was quite small (THD=0.0737702 %) which means little distortion is added to the signal from undesired frequency components. Also, DC analysis results are very close to the hand analysis results