



Information Technology Institute (ITI)

CMOS ANALOG IC DESIGN

LAB 3

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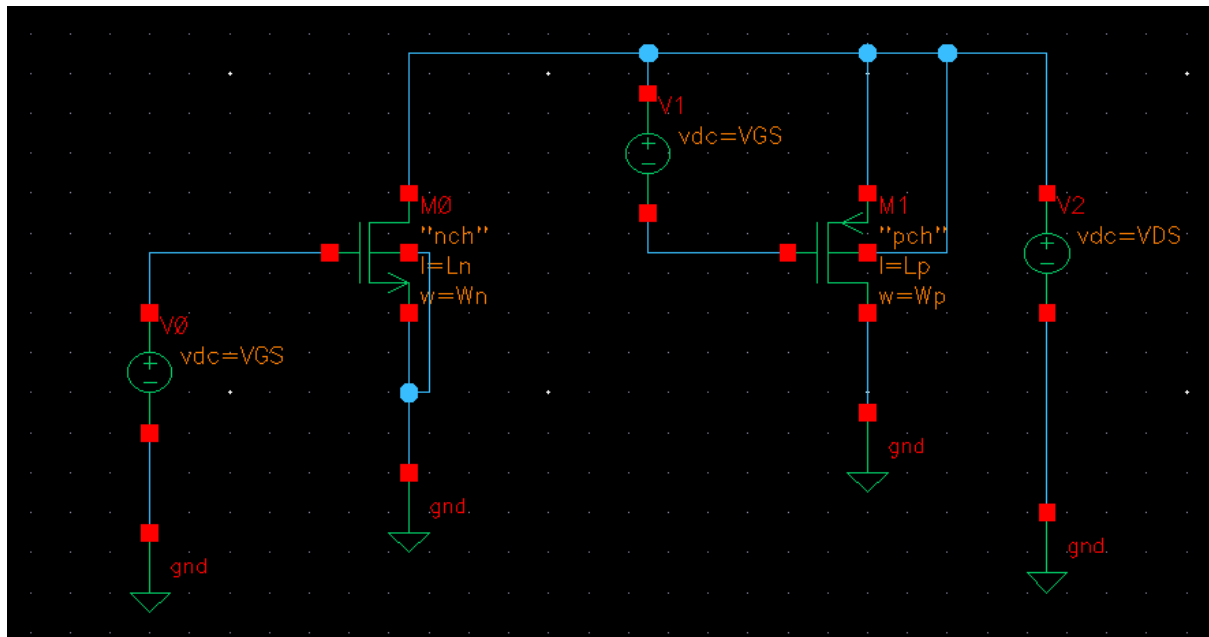
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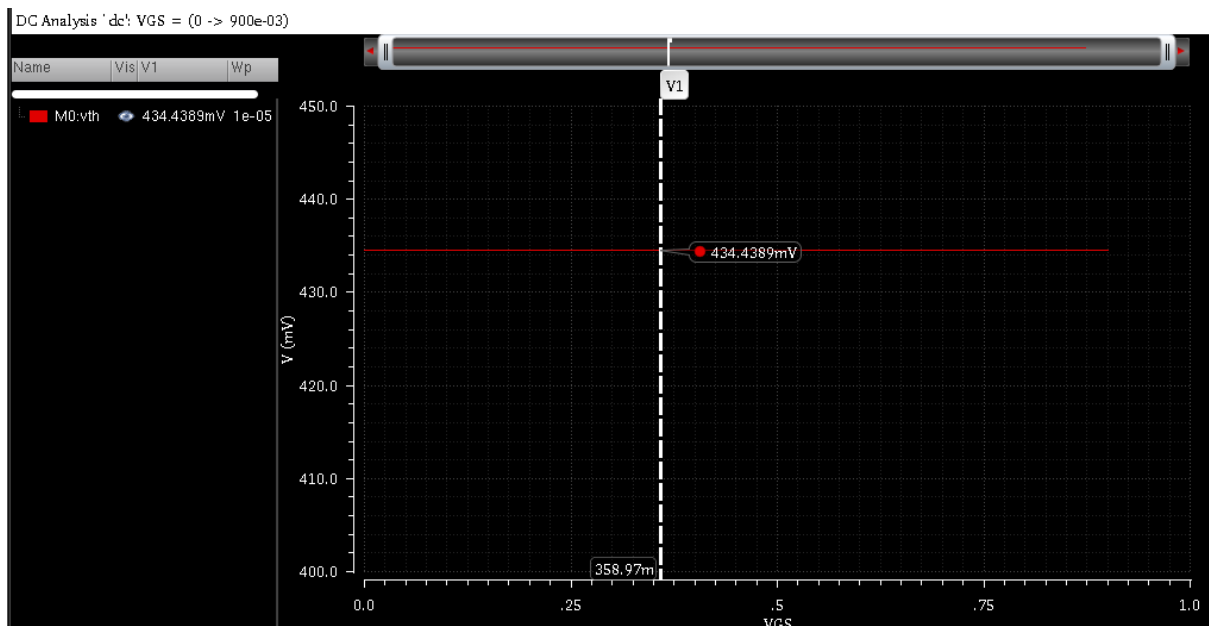
PART 1: Sizing Chart

The circuit schematic is shown



1), 2), 3) are satisfied

4) The value of V_{TH} is shown = 0.434 V.

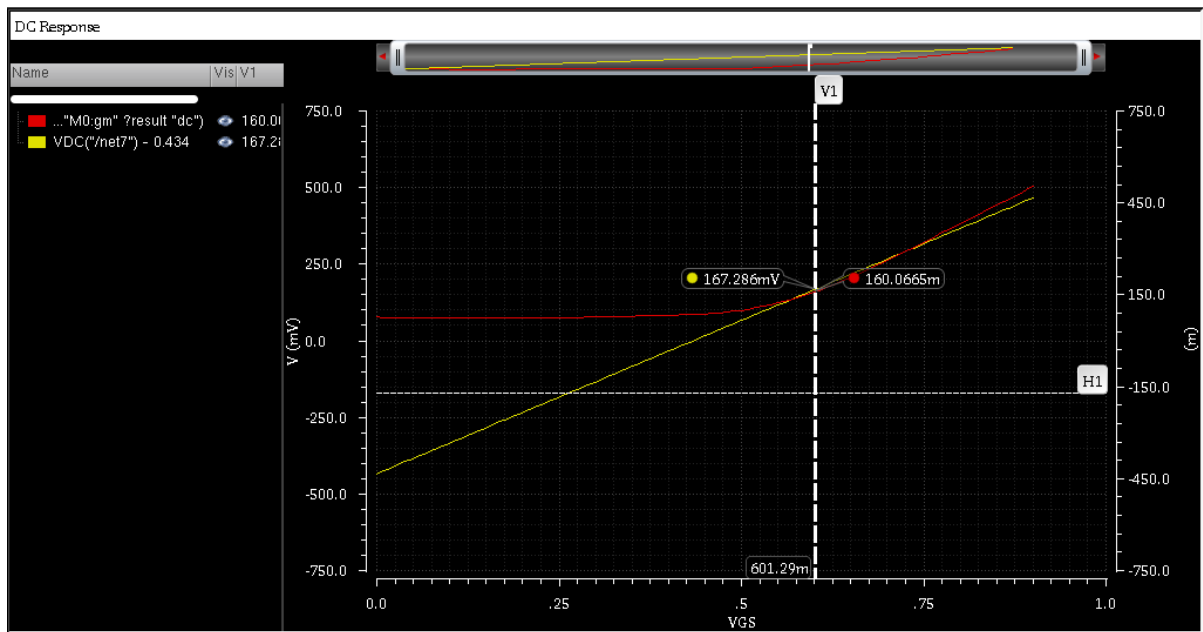


5) Calculator Expressions for V^* and V_{ov}

`VDC("/net7") - 0.434`
for V_{ov}

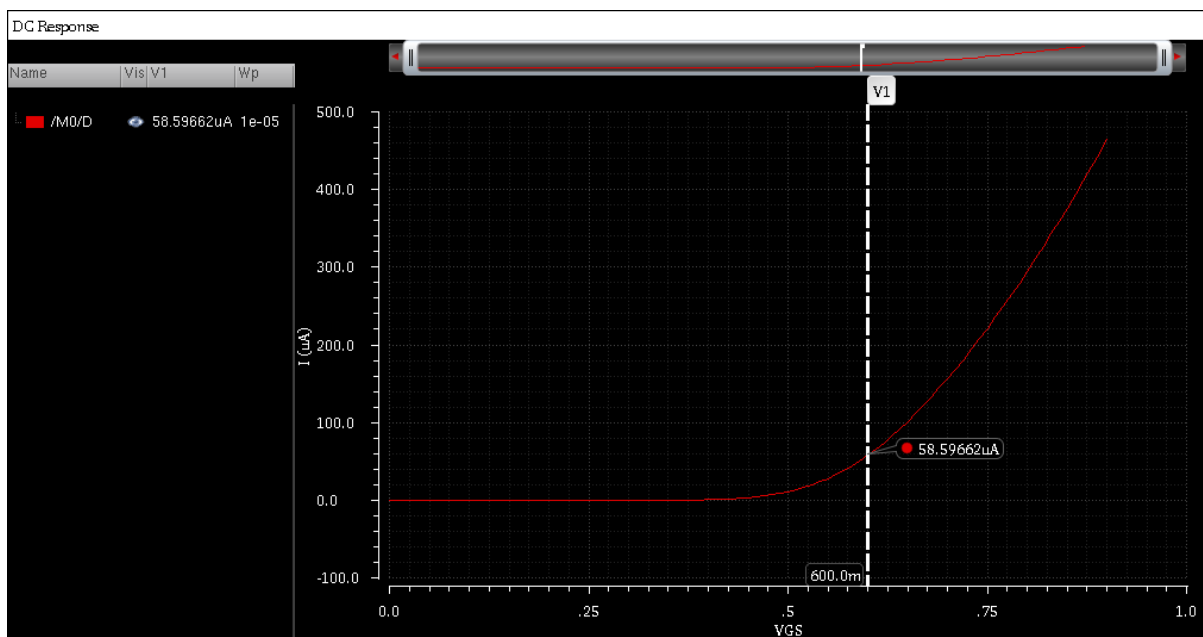
`2 * value(getData("/M0/D" ?result "dc") "Wp" 1e-05)/getData("M0:gm" ?result "dc")`
for V^*

6) The plot of V^* and V_{ov} against V_{GS} is shown



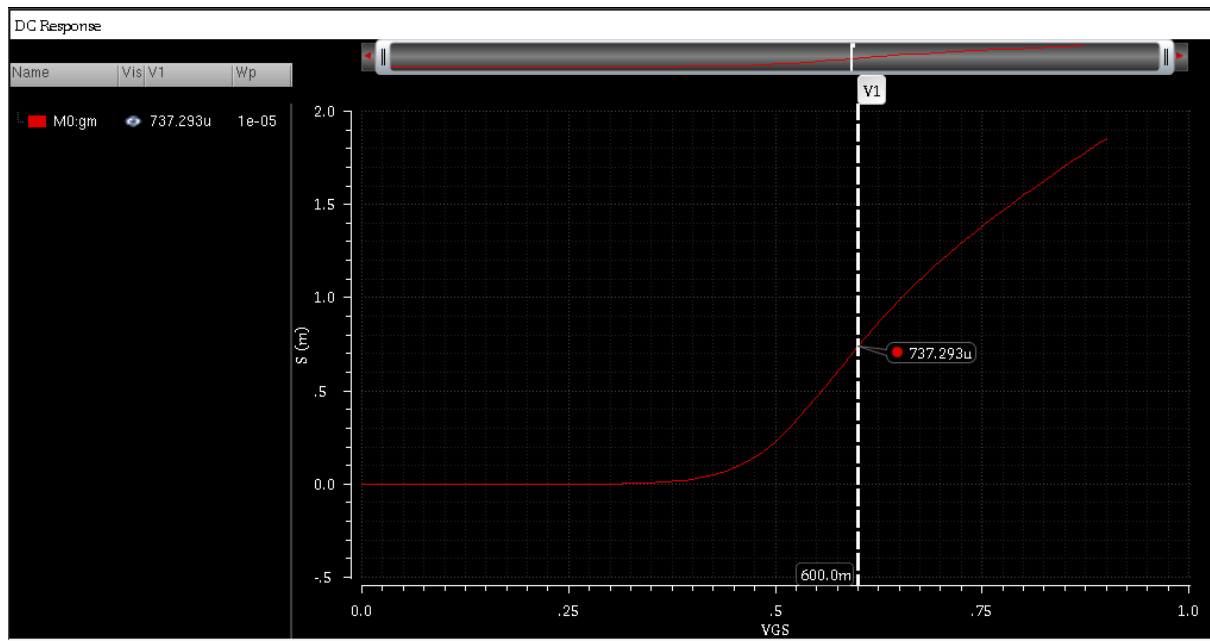
7) $V_{ovQ} = 167.3$, $V_{GSQ} = 0.6V$ @ $V^* = 160mV$

8) I_{DQ} vs V_{GS}



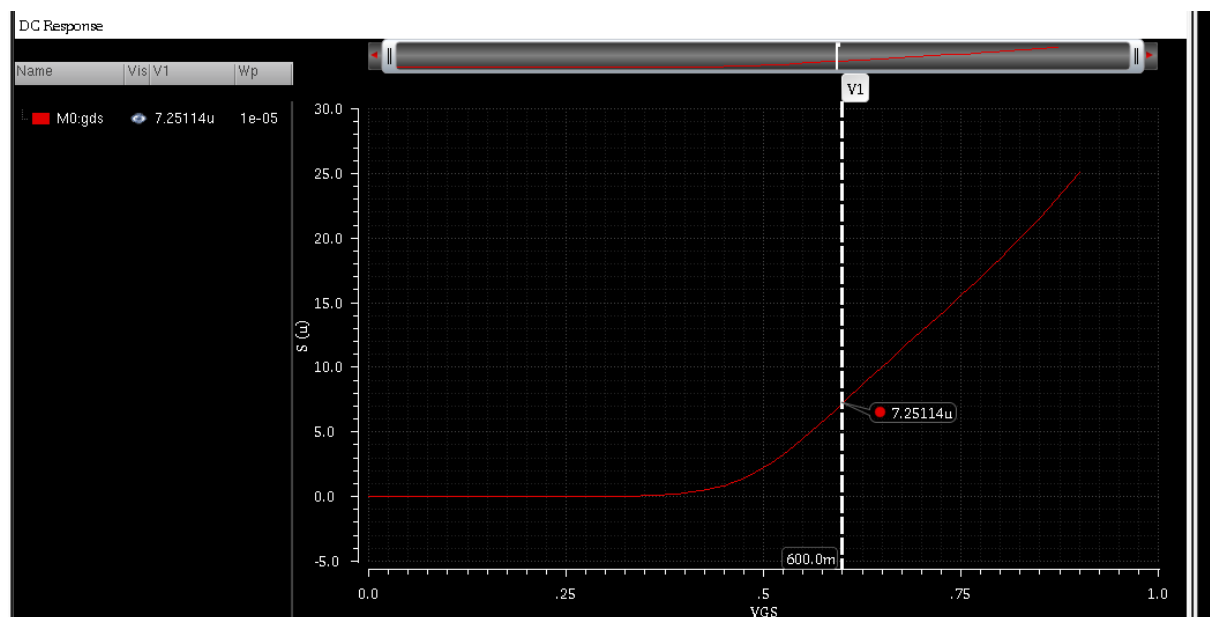
From the graph, $I_{DQ}^* = 58.6 \mu A$

gmX vs VGS



From the graph, $gmQ^* = 737.293\mu S$

gdsX vs VGS



From the graph, $gdsQ^* = 7.25114\mu S$

9) $W_{new} = IDQ * W_{old} / IDQ^* = 15 * 10 / 58.6 = 2.56 \mu m$

10) By cross multiplication:

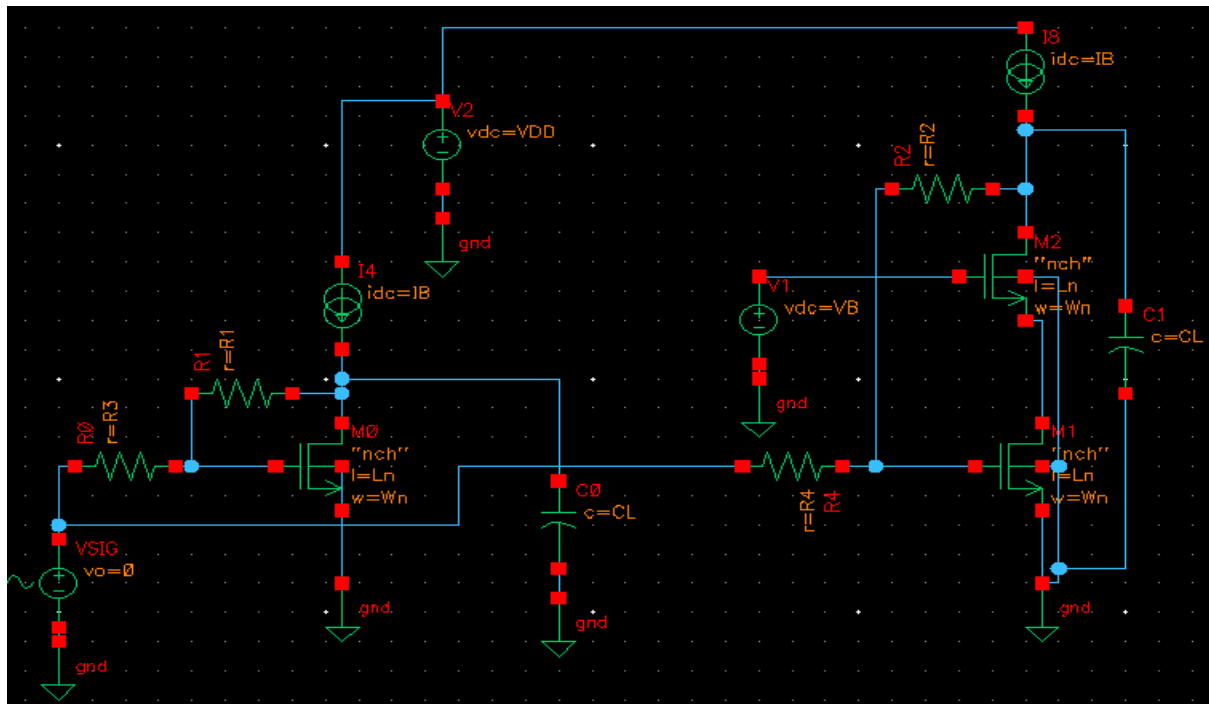
$$gmQ = gmQ^* * W_{old} / W_{new} = 737.293\mu S * 2.56\mu m / 10\mu m = 188.7\mu S$$

$$gdsQ = gdsQ^* * W_{old} / W_{new} = 7.25114\mu S * 2.56\mu m / 10\mu m = 1.856\mu S$$

PART 2: Cascode for Gain

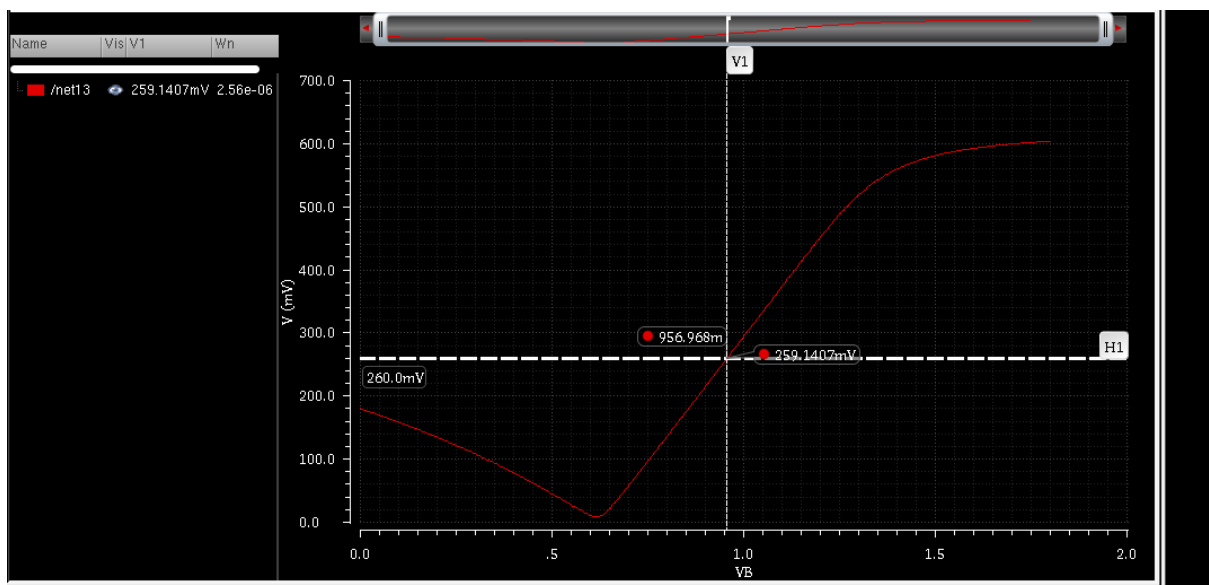
1. OP Analysis

1) The circuit schematic is shown



The specified parameters were assigned.

2) A sweep over VB was performed. The plot of VDS vs VB is shown. At the point where $V_{DS} = V^* + 100\text{mV} = (160 + 100)\text{ mV} = 260\text{ mV}$, the value of VB is recorded and it equals 956.968 mV, which approximates to $V_B = 0.957\text{V}$



3) The appropriate values for resistances were set. Requirement satisfied.

4) The required parameters are shown.

For M1

M1: id	20.0u
M1: vgs	626.46994mV
M1: vds	626.46994mV
M1: vth	442.41174mV
M1: vdsat	142.36617mV
M1: gm	220.859u
M1: gds	2.44037u
M1: gmbs	60.0156u
M1: cdb	-2.0953fF
M1: cgd	-1.2102fF
M1: cgs	-9.2008fF
M1: csb	-4.5365fF
M1: region	2.0

For M2

M2: id	20.0u
M2: vgs	631.794mV
M2: vds	259.038mV
M2: vth	445.144mV
M2: vdsat	144.082mV
M2: gm	216.3u
M2: gds	5.591u
M2: gmbs	58.85u
M2: cdb	-2.3218fF
M2: cgd	-1.2585fF
M2: cgs	-9.2185fF
M2: csb	-4.5231fF
M2: region	2.0

For M3

M3: id	20.0u
M3: vgs	696.4806mV
M3: vds	373.6699mV
M3: vth	519.3601mV
M3: vdsat	146.3255mV
M3: gm	221.7u
M3: gds	3.38u
M3: gmbs	54.82u
M3: cdb	-2.1039fF
M3: cgd	-1.221fF
M3: cgs	-9.1439fF
M3: csb	-4.0875fF
M3: region	2.0

5) For M1, M2, and M3 $V_{DS} > V_{GS} - V_{TH}$, hence all transistors are in saturation. This is also signified by all transistors being in region 2.

6) No, not all transistors have the same V_{TH} . This is

7) For all transistors, $g_m > g_{ds}$. In fact, $g_m \gg g_{ds}$.

8) For all transistors, $g_m > g_{mb}$.

9) For all transistors, $c_{gs} < c_{gd}$, but $|c_{gs}| \gg |c_{gd}|$.

10) For all transistors, $c_{sb} < c_{db}$, but $|c_{sb}| > |c_{gd}|$.

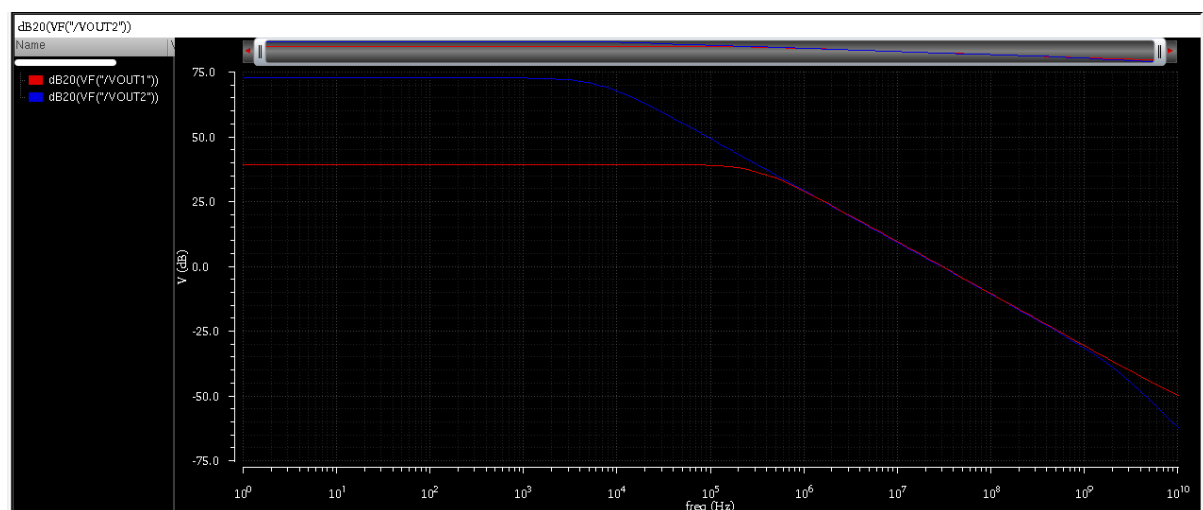
2. AC Analysis

- 1) Simulation parameters are set as required. Satisfied.
- 2) The required expressions were calculated and exported to adexl as shown.

The calculated values are also shown to the right

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab1:lab3_part2:1	dB20(VF("/VOUT1"))				
lab1:lab3_part2:1	ymax(dB20(VF("/VOUT1")))	39.3			
lab1:lab3_part2:1	ymax(mag(VF("/VOUT1")))	92.24			
lab1:lab3_part2:1	bandwidth(VF("/VOUT1") 3 "low")	323.9k			
lab1:lab3_part2:1	gainBwProd(VF("/VOUT1"))	29.95M			
lab1:lab3_part2:1	dB20(VF("/VOUT2"))				
lab1:lab3_part2:1	ymax(dB20(VF("/VOUT2")))	72.57			
lab1:lab3_part2:1	ymax(mag(VF("/VOUT2")))	4.253k			
lab1:lab3_part2:1	bandwidth(VF("/VOUT2") 3 "low")	6.846k			
lab1:lab3_part2:1	gainBwProd(VF("/VOUT2"))	29.19M			
lab1:lab3_part2:1	unityGainFreq(VF("/VOUT1"))	30.18M			
lab1:lab3_part2:1	unityGainFreq(VF("/VOUT2"))	29.44M			

- 3) The Bode Plot of CS (red) and Cascode (blue) are shown, overlaid.

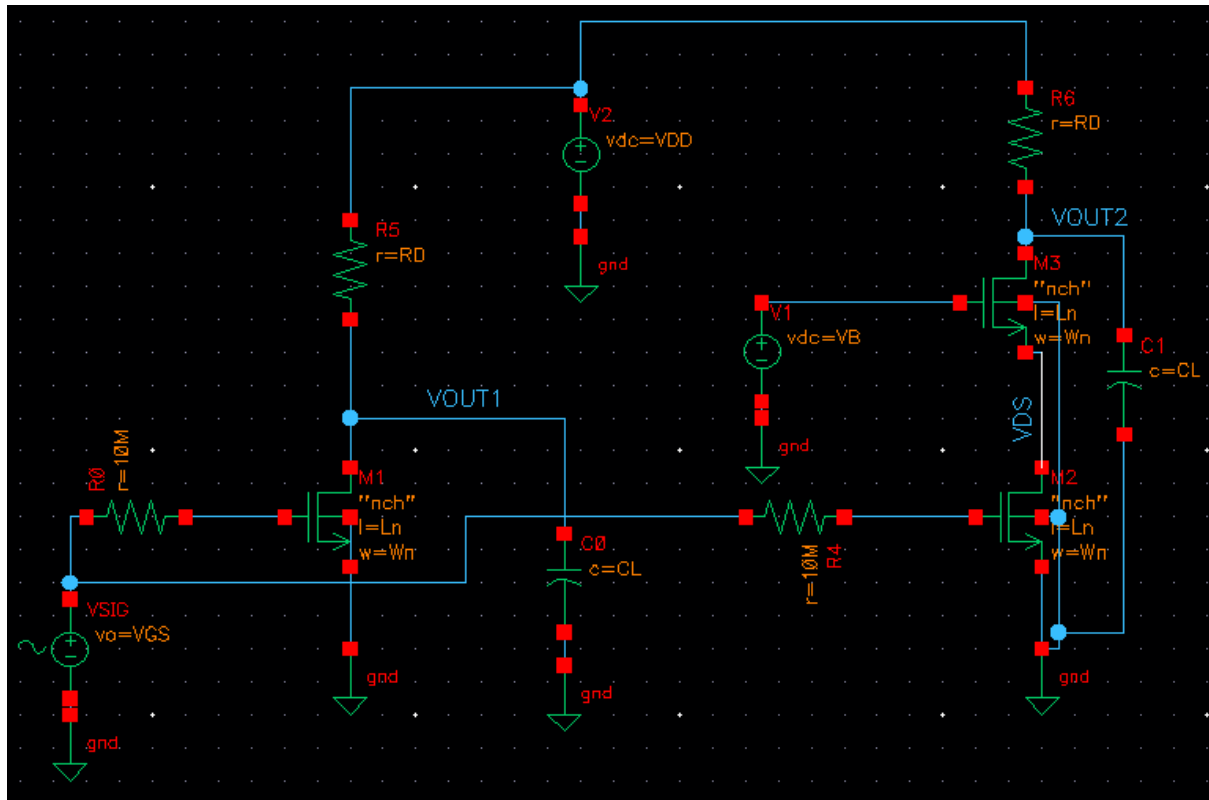


- 4) As per the lab announcement, this part is not required anymore.
- 5) As per the lab announcement, this part is not required anymore.
- 6) The cascade amplifier has a lower BW. This is due to its higher Rout which comes at the expense of the BW. However, as we would expect, the cascade amplifier has a higher gain. Also, the gainBWProd are very close, which signifies that both amplifiers have a similar value of maximum frequency at which they can operate.

[optional] PART 3: Cascode for BW

1. OP Analysis

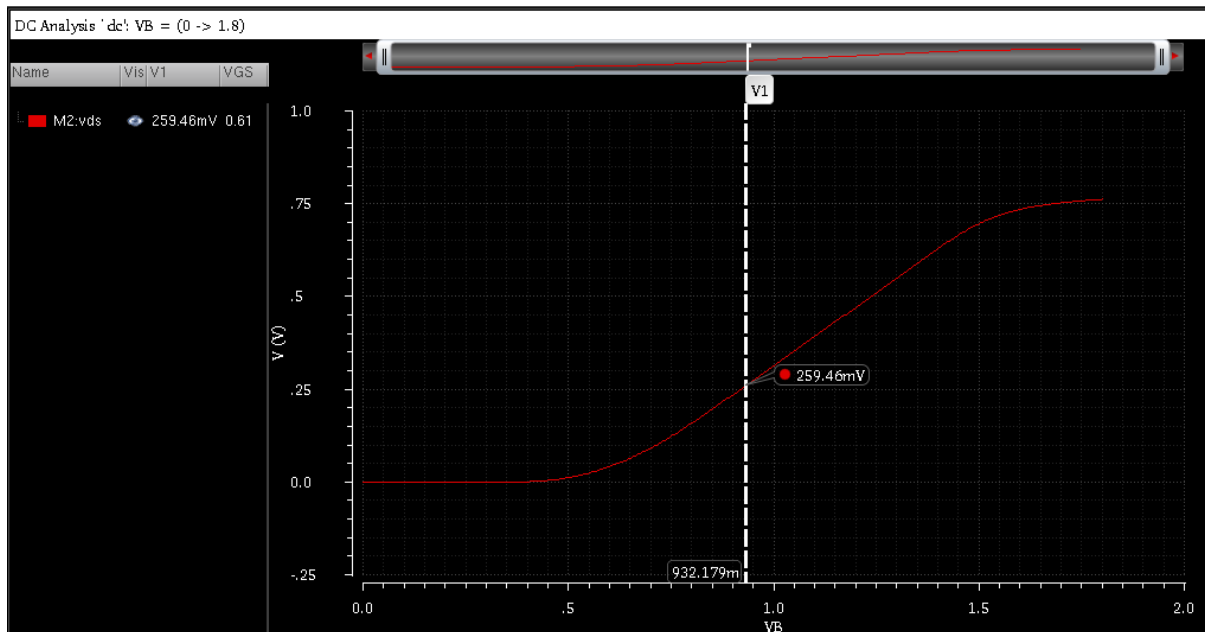
1) The modified schematic is shown



2) $R_D = V_{RD} / I_D = (V_{DD}/2) / 15\mu A = (1.8/2)/15\mu A = 60k \text{ ohms}$

3) Noted.

4) A sweep of VDS against VB is performed to select a suitable value for VB.



At $V_{DS} = V^* + 100\text{mV} = 260\text{mV}$, $V_B = 0.932\text{ V}$, approximately.

The required parameters are shown.

For M1

DC Analysis 'dc' VB = (0 -> 1.8)		
Name	Vis	V1
M1:id	16.8778u	
M1:vgs	610.0mV	
M1: vds	787.3306mV	
M1:vth	441.2157mV	
M1: vdsat	132.2559mV	
M1:gm	201.862u	
M1:gds	2.07112u	
M1:gmb	55.0108u	
M1:cdb	-2.0315fN	
M1:cgd	-1.2089fN	
M1:cgs	-9.1673fN	
M1:csb	-4.5311fN	
M1:region	2.0	

For M2

DC Analysis 'dc' VB = (0 -> 1.8)		
Name	Vis	V1
M2:id	15.5785u	
M2:vgs	610.0mV	
M2: vds	260.3619mV	
M2:vth	445.1338mV	
M2: vdsat	129.6676mV	
M2:gm	189.63u	
M2:gds	4.0813u	
M2:gmb	51.806u	
M2:cdb	-2.3144fN	
M2:cgd	-1.2471fN	
M2:cgs	-9.1755fN	
M2:csb	-4.5164fN	
M2:region	2.0	

For M3

DC Analysis 'dc' VB = (0 -> 1.8)		
Name	Vis	V1
M3:id	15.57u	
M3:vgs	672.569mV	
M3: vds	606.704mV	
M3:vth	517.845mV	
M3: vdsat	131.067mV	
M3:gm	195.1u	
M3:gds	2.139u	
M3:gmb	48.35u	
M3:cdb	-2.006fN	
M3:cgd	-1.2092fN	
M3:cgs	-9.0864fN	
M3:csb	-4.0807fN	
M3:region	2.0	

5) For M1, M2, and M3 $V_{DS} > V_{GS} - V_{TH}$, hence all transistors are in saturation. This is also signified by all transistors being in region 2.

2.AC Analysis

1) AC simulation parameters are set as required.

Sweep Variable

☒ Frequency

☐ Design Variable

☐ Temperature

☐ Component Parameter

☐ Model Parameter

Sweep Range

☒ Start-Stop Start Stop

☐ Center-Span

Sweep Type

☒ Points Per Decade

☐ Number of Steps

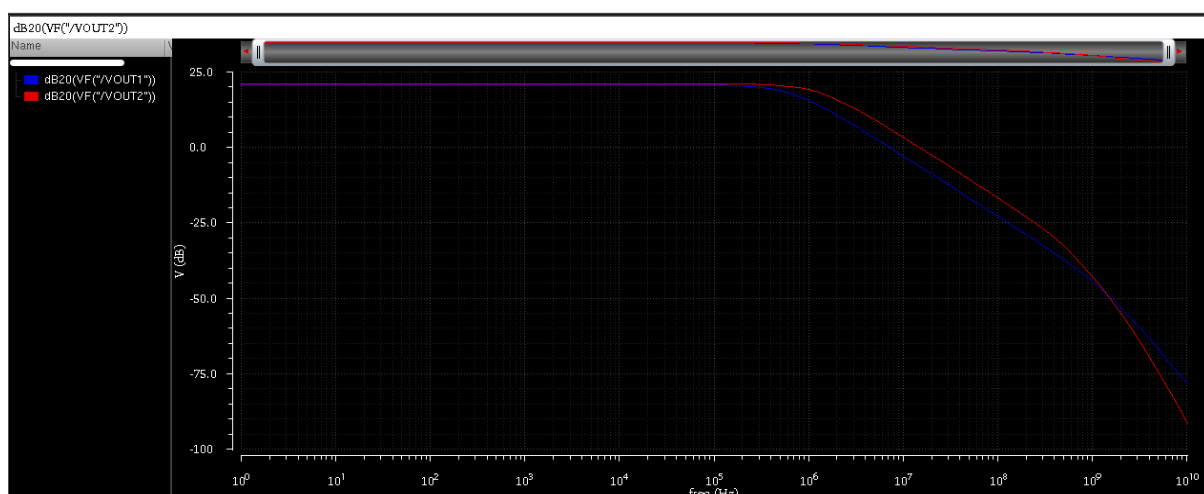
Logarithmic ☒

2) Calculator Expressions are shown, and the values are shown into the right.

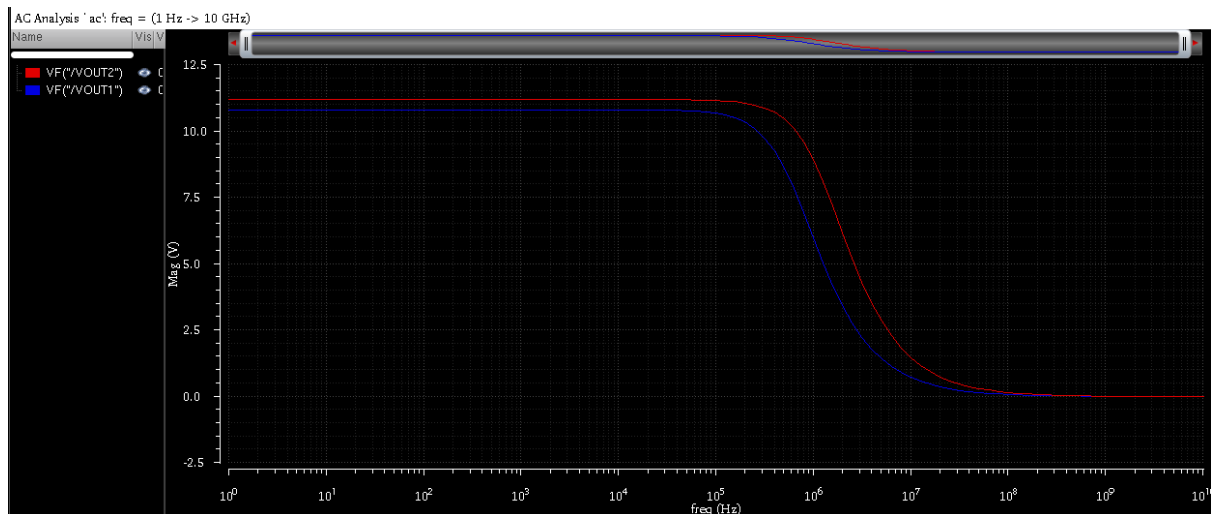
Test	Output	Nominal	Spec	Weight	Pass/Fail
lab1:lab3part2number3:1	dB20(VF("/VOUT1"))				
lab1:lab3part2number3:1	ymax(dB20(VF("/VOUT1")))	20.65			
lab1:lab3part2number3:1	mag(VF("/VOUT1"))				
lab1:lab3part2number3:1	ymax(mag(VF("/VOUT1")))	10.77			
lab1:lab3part2number3:1	bandwidth(VF("/VOUT1") 3 "low")	664k			
lab1:lab3part2number3:1	gainBwProd(VF("/VOUT1"))	7.17M			
lab1:lab3part2number3:1	unityGainFreq(VF("/VOUT1"))	7.213M			
lab1:lab3part2number3:1	dB20(VF("/VOUT2"))				
lab1:lab3part2number3:1	ymax(dB20(VF("/VOUT2")))	20.96			
lab1:lab3part2number3:1	mag(VF("/VOUT2"))				
lab1:lab3part2number3:1	bandwidth(VF("/VOUT2") 3 "low")	1.322M			
lab1:lab3part2number3:1	gainBwProd(VF("/VOUT2"))	14.79M			
lab1:lab3part2number3:1	unityGainFreq(VF("/VOUT2"))	14.85M			

3) The bode plots of the CS(blue) and the cascade(red) are shown.

db20



Magnitude



4) As per the lab announcement, this part is not required anymore.

5) As per the lab announcement, this part is not required anymore.

Additional Insights:

As we replaced the current sources with resistances, the value of R_{out} decreases, and hence a lower gain for both amplifiers.

Comparing to part 2, as a result of the omission of the feedback resistance, the BW increased, which is the target of this requirement. That was a tradeoff with the gain, which decreased.