Information Technology Institute (ITI)

CMOS ANALOG IC DESIGN

LAB 2

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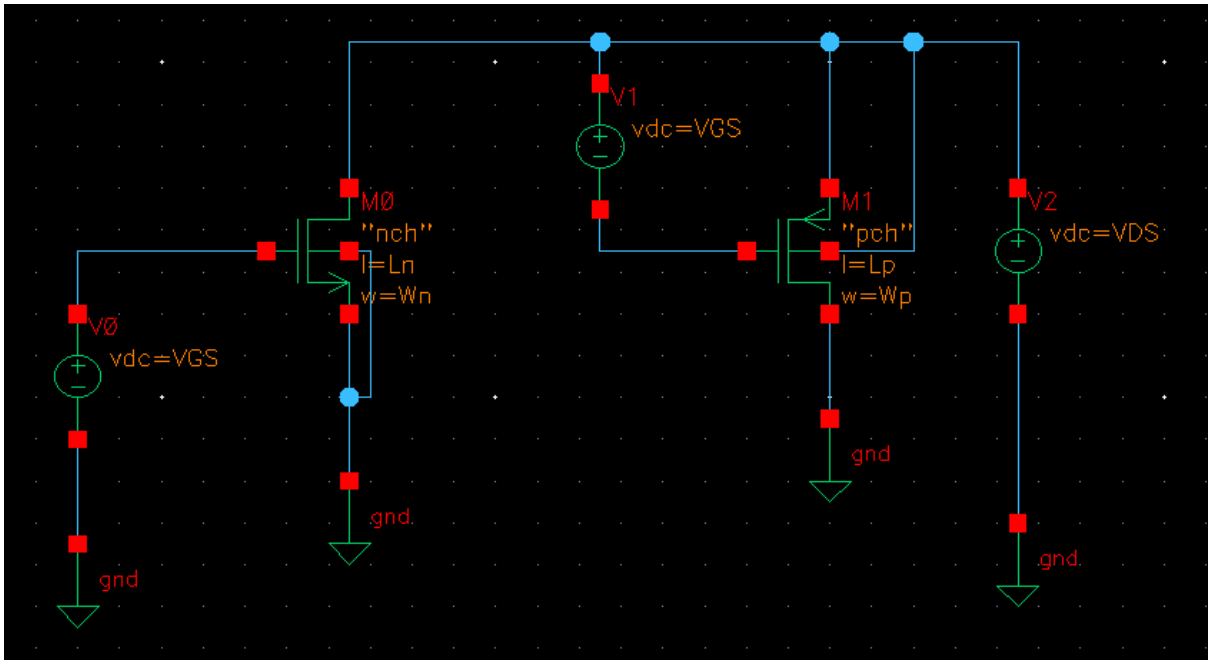
PART 1: Sizing Chart

The circuit schematic is shown



1),2),3) satisfied

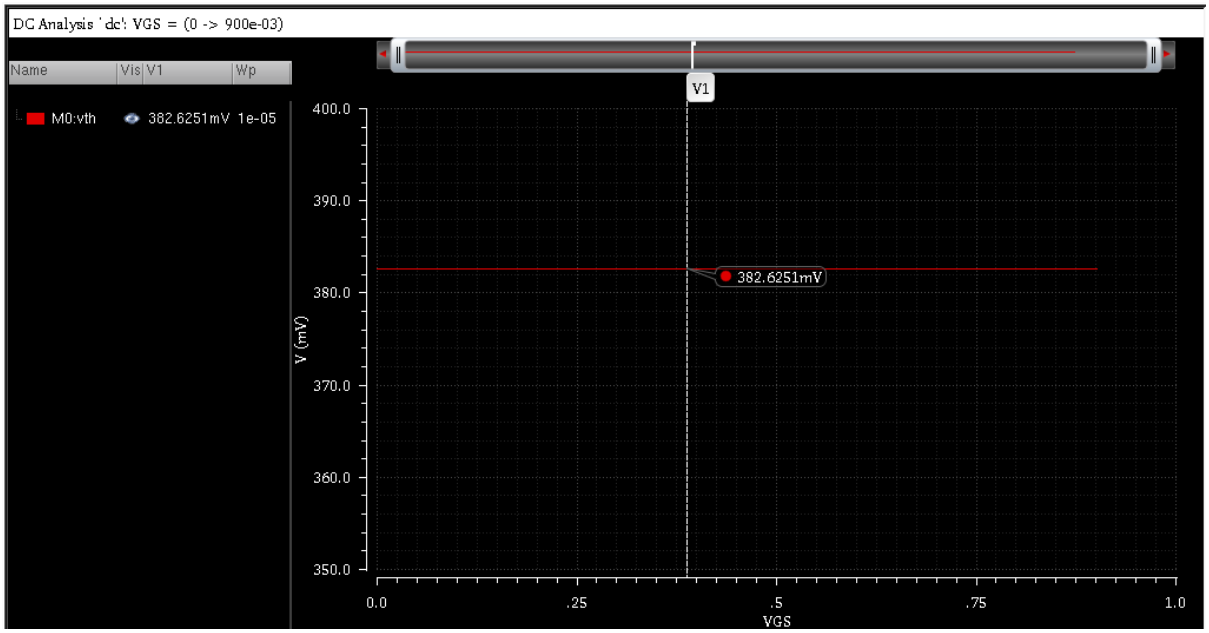
4) RD = (VDD/2) / Ibias = (1.8/2) / 150 uA = 6k ohms

5) V*Q = (2 * VRD) / |Av| = (2 * 0.9) / |-6| = 0.3V

6) satisfied.

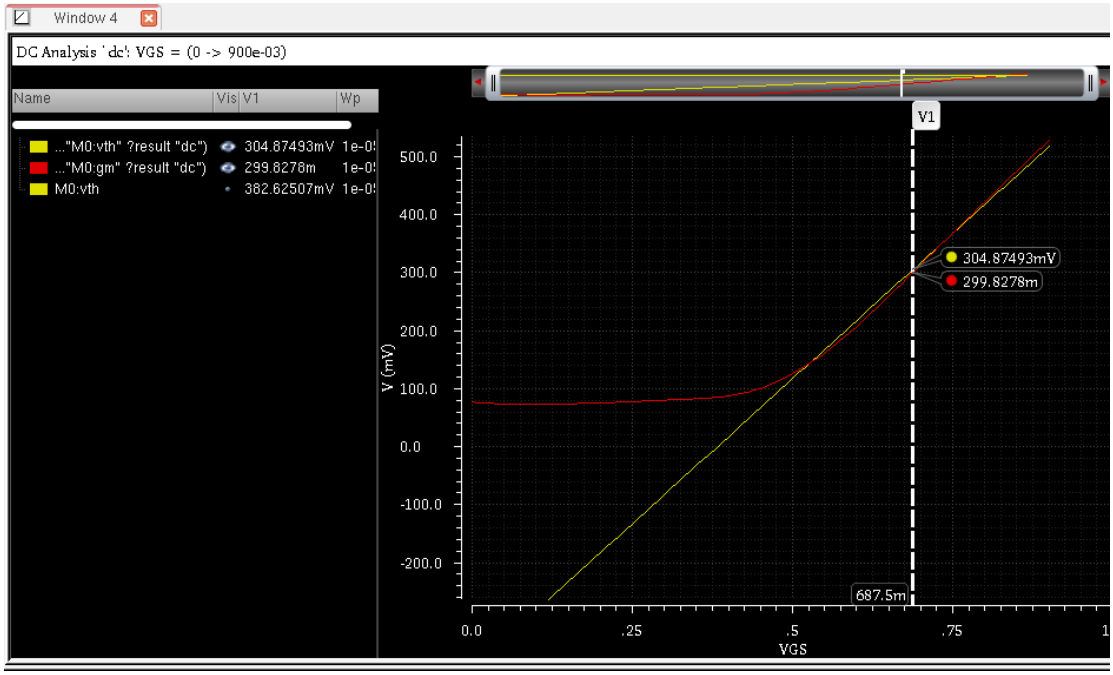
7) We can obtain the value of VTH from the graph of ID vs VGS. VGS = VTH at the point where ID starts to go above zero (roughly). However, it is better to use the cadence tools to get VTH.

We can plot the graph of VTH to observe its value. From the following graph we can see that VTH = 0.383 V, approximately.



8) Satisfied. Expressions were exported to adexl.

9) V* and Vov are shown overlaid.

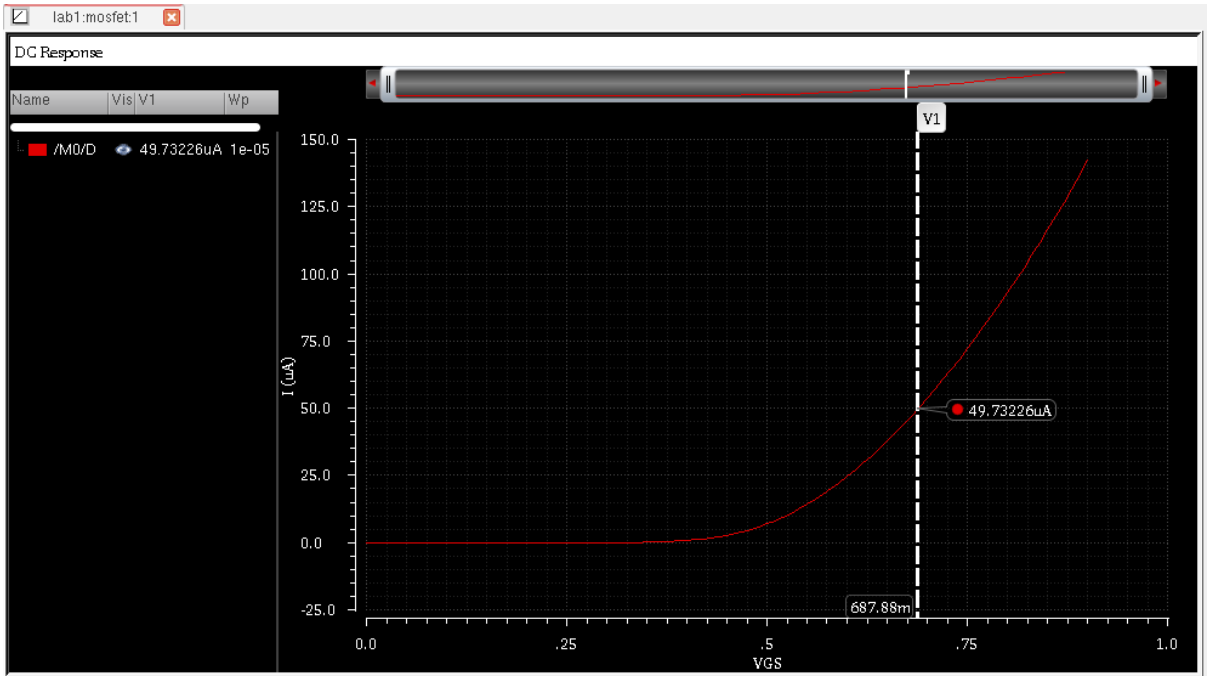


10)At V* = VQ*= 0.3 V, VovQ = 0.305 V, They are approximately equal.

VGSQ = 0.687.5 V = 0.69 V.

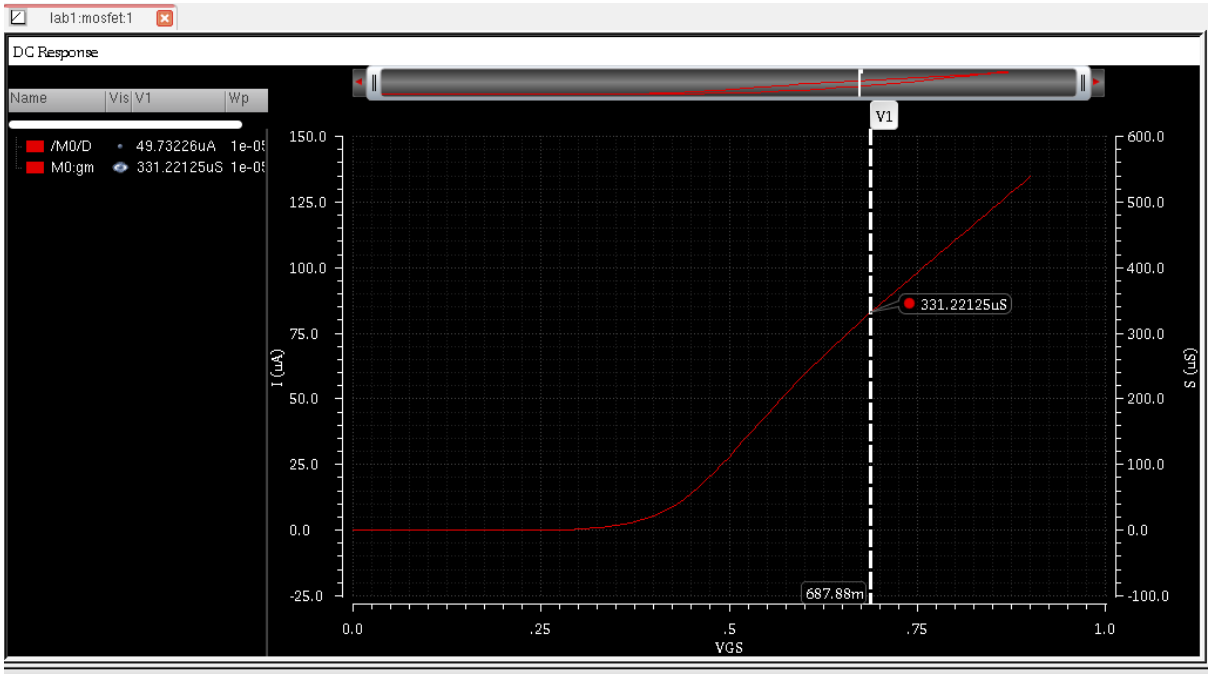
11) The required plots are shown.

ID vs VGS.



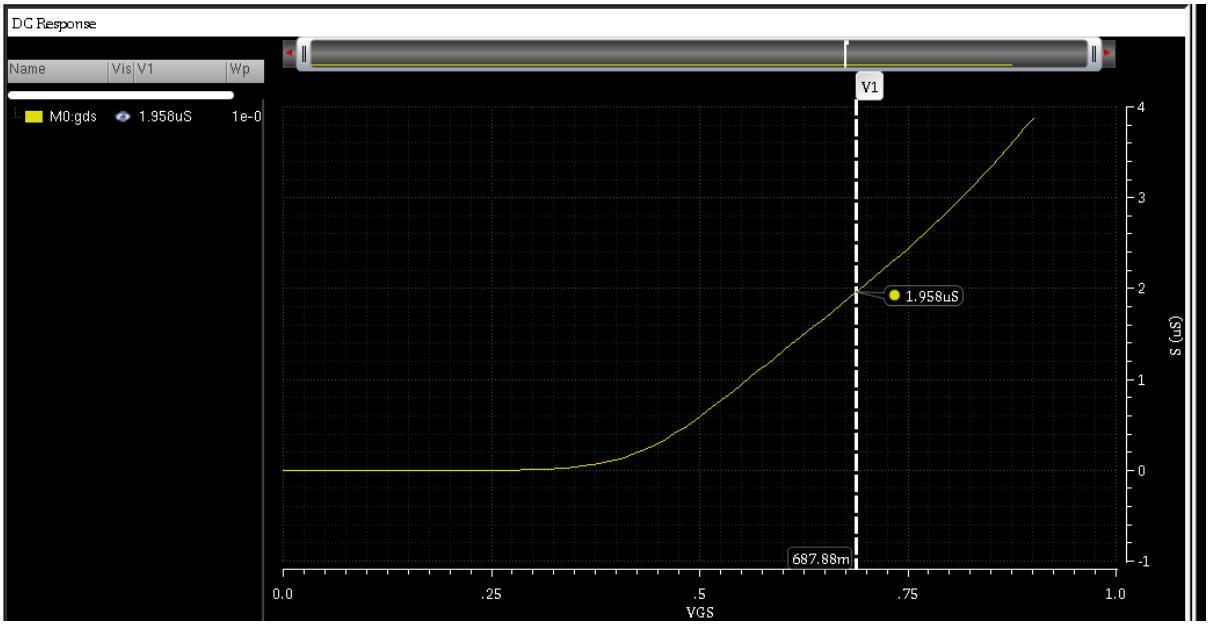
From the graph, IDQ* = 49.73225uA

gm vs VGS



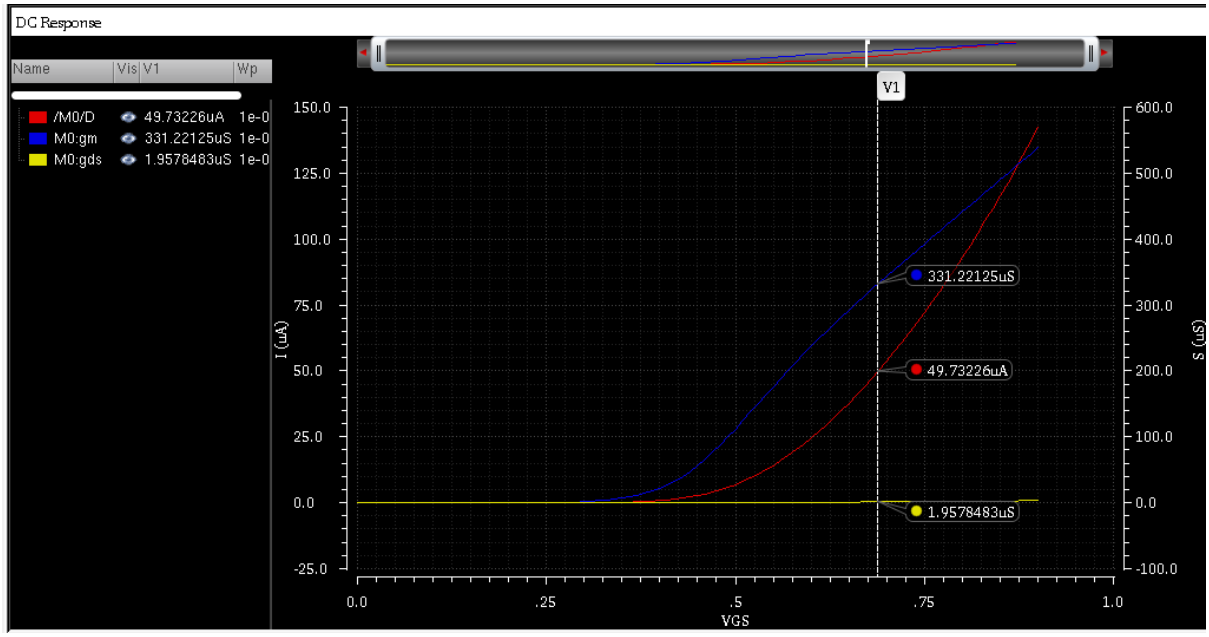
From the graph, gmQ* = 331.22125uS

gds vs VGS



From the graph, gdsQ* = 1.958uS

The three of them are plotted overlaid on the following graph.



12) 10/W = 49.7/150. So W = 30 um

13) By cross multiplication:

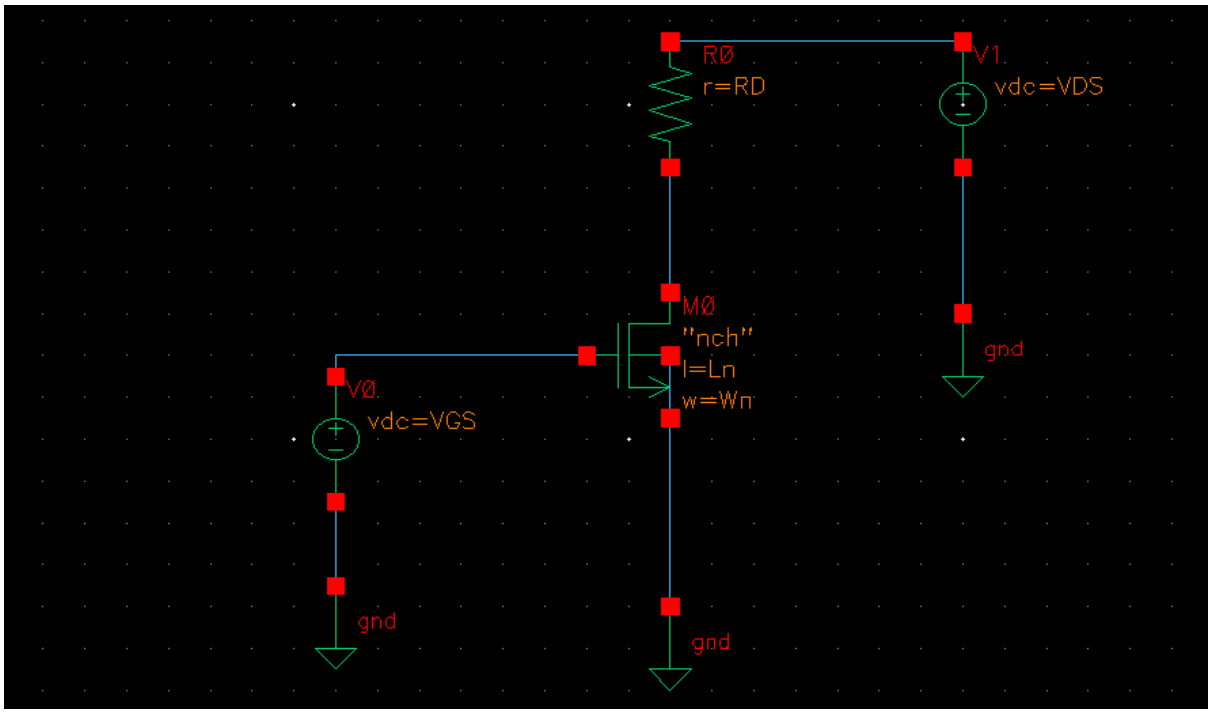
gmQ = gmQ* Wold / Wnew = 331.22125uS * 30um / 10um = 993.67uS

gdsQ = gdsQ* Wold / Wnew = 1.958uS * 30um / 10um = 5.874uS

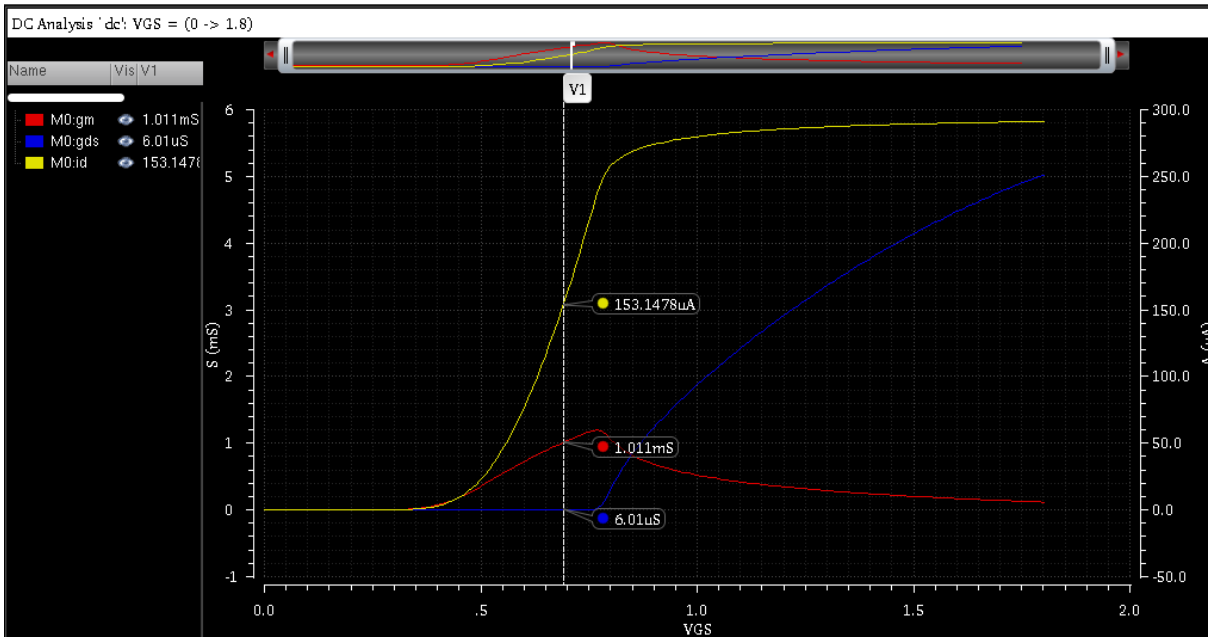
PART 2: CS AMPLIFIER

1. OP and AC Analysis

1) The circuit schematic is shown



2) The DC Q-point parameters(gm, gds, ID) are shown overlaid in the following plot.



Comparing to the values obtained in part 1:

3) ro = 1 / gds = 1 / 6u = 167 kohms

So RD // ro = 6k // 167k approximately equal to 6k = RD

Hence the assumption of ignoring ro is justified.

If we neglect it, however, the error will increase.

If we use min L, ro decreases, and therefore the error decreases.

4) Av = -gmro = -1 * 167kohm * 1.011 mS = -169, |Av| = 169

5) Analytic Calculation:

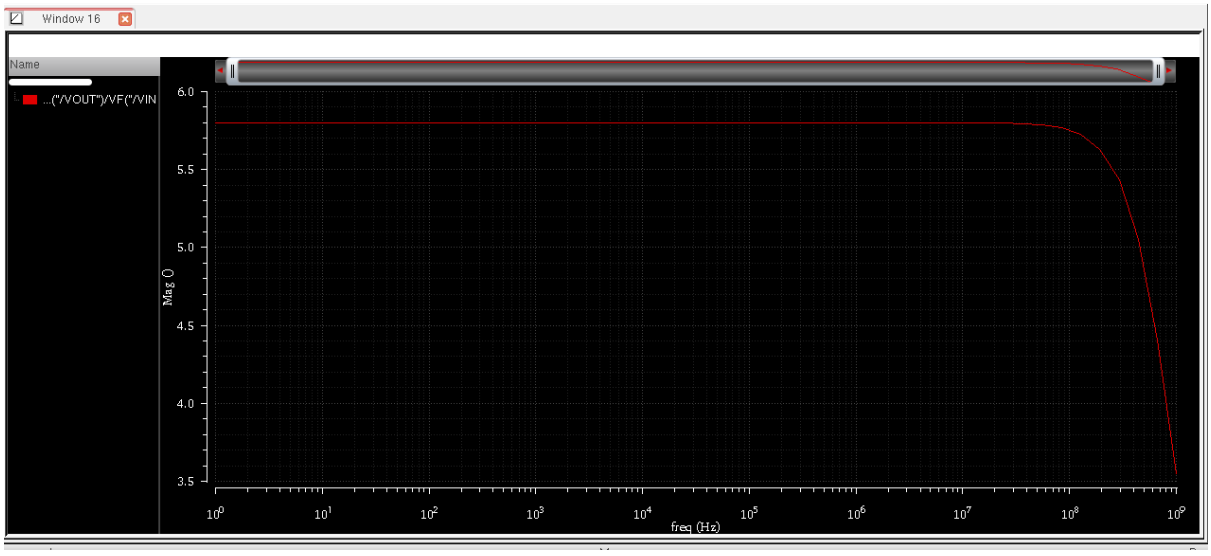
Av = GmRout, Gm = - gm, Rout = ro(1 + gmRs) // RD = ro // RD

So Av = -gm * (ro//RD) = -1.011mS * (167k // 6k) = -5.856

So |Av| = 5.86

The intrinsic gain much higher than the actual gain, and this affirms our knowledge that the intrinsic gain is an upper bound on the amplifier gain.

6)Vo/Vin plot is shown



Expressions are shown:

Test	Name	Type	Expression/Signal/File	EvalType	Plot	Save
lab1:mo...	DC gain	expr	ymax(mag((VF("/VOUT") / VF("/VIN"))))	point	☑	☐
lab1:mo...	Av	expr	(VF("/VOUT") / VF("/VIN"))	point	☑	☐

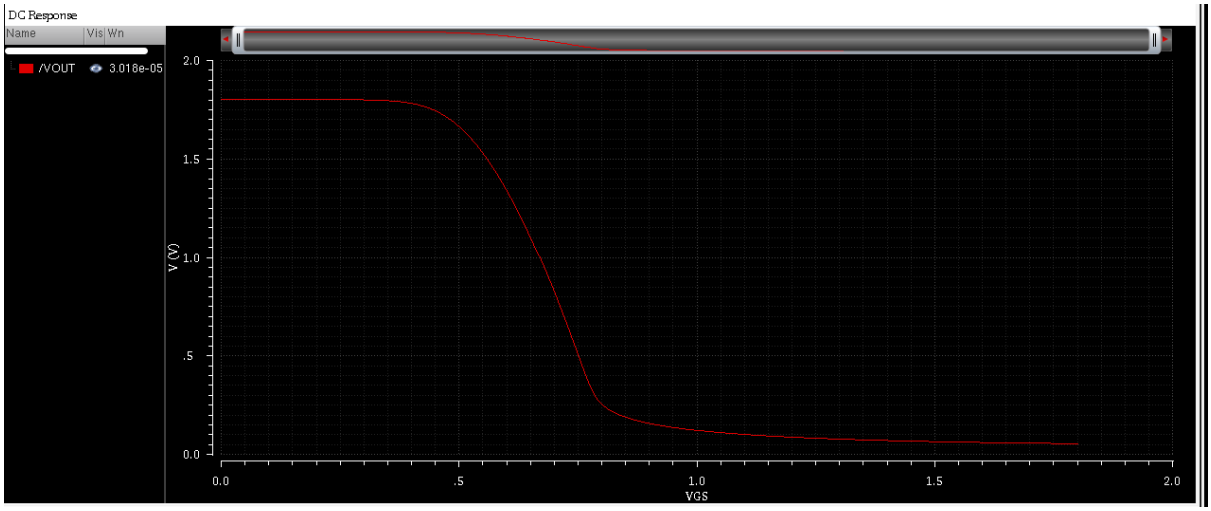
Gain and DC gain values are shown

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab1:mosfet_lab2_part2:1	DC gain	5.798			
lab1:mosfet_lab2_part2:1	Av				

2. Gain Non-linearity

1) Requirement done on Cadence.

2) Vout vs Vin (VGS) is shown



VGS = VIN and VDs = VOUT as the source is connected to the ground, ID = k'(VGS - VTH)^2 in the saturation region and VDS = VDD — ID * RD = (VDD — VDS)/RD = k(VGS — VTH)^2 which illustrates a quadratic relation between

VDS (VOUT) and VGS(VIN), so slope (delta VOUT / delta VIN) is linear (in the region VTH < VGS < 0.75).

VGS = VIN and VDS = VOUT as the source is connected to the ground, ID=k[(VGS - VTH) (VDS) — VDS^2/2] in the triode region, VDS^2/2 could be neglected due to the small value of VDS, therefore ID= k[(VGS - VTH) (VDS)]

VDS = VDD— ID * RD => (VDS — VTH)/RD = k[(VGS — VTH) (VDS)] which illustrates a linear relation between VDS (VOUT) and VGS(VIN), so slope

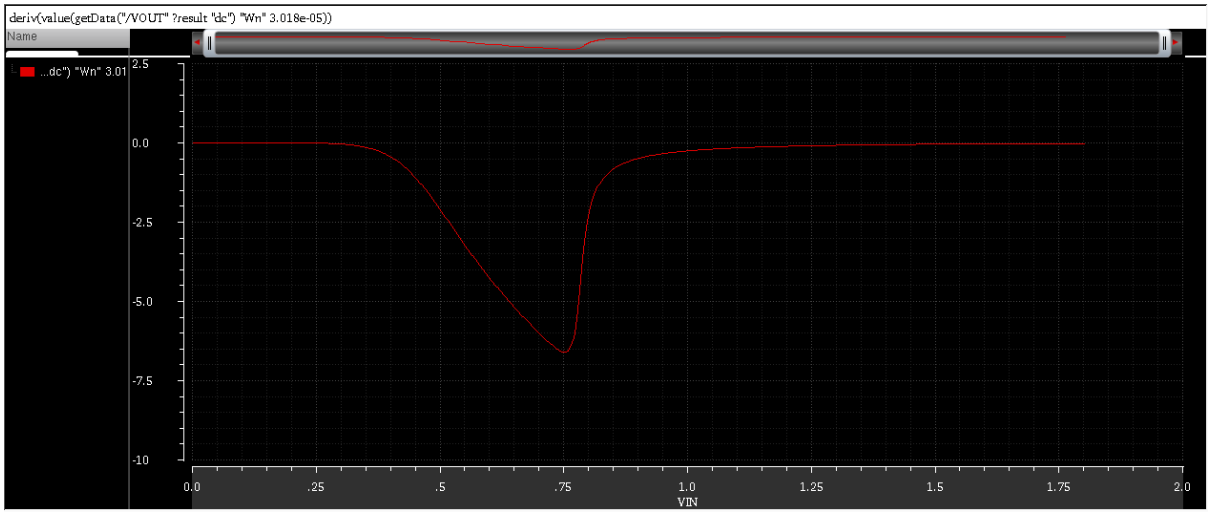
(delta VOUT / delta VIN) is constant (in the region VGS > 0.75 & VGS < VTH).

In conclusion, the relation between VOUT and VIN can be reasonably approximated by the Small Signal Model to be linear in the saturation region.

3) Calculator Expression for the derivative of Vout

```
deriv(value(getData("/VOUT" ?result "dc") "Wn" 3.018e-05))
```

The derivative of VOUT vs VIN



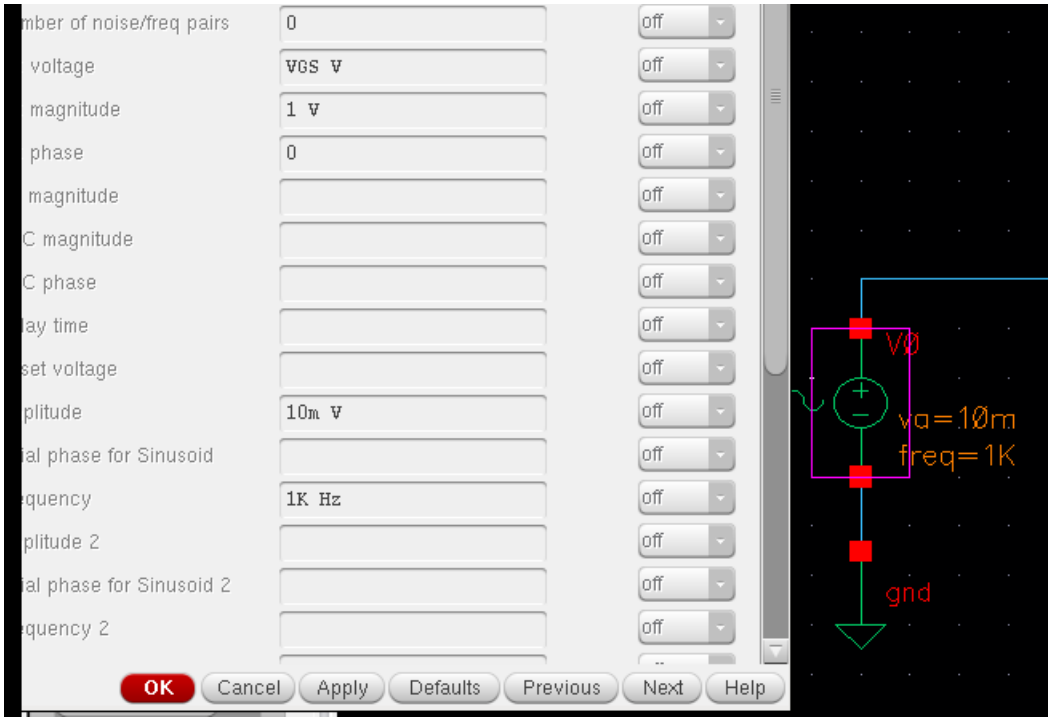
Av = -gm * (RD//ro).

gm = 2*ID/(VGS – VTH)

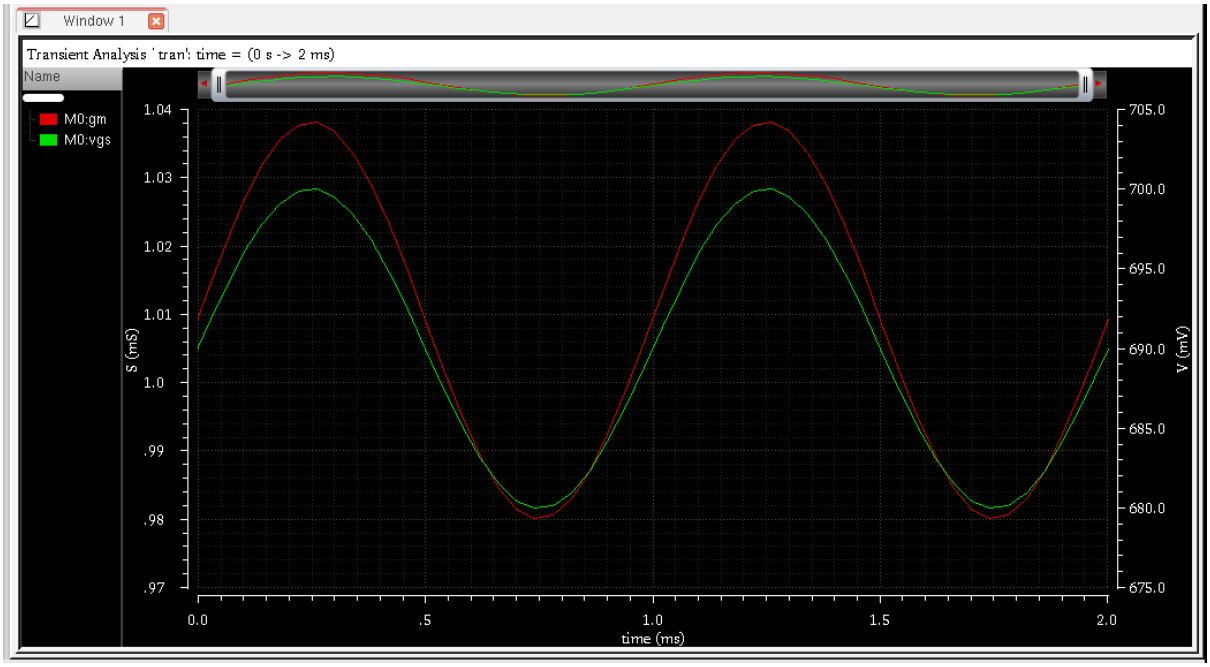
gm is a function of VGS. VGS is affected by the input signal.

So the gain depends on the input signal, so it is not linear.

4) Required parameters are set. The following figure illustrates.



5) gm vs time and vgs vs time are show below. Yes, gm varies with time. As the input signal varies with time, Vgs varies with time, and since gm is a function of Vgs, it too varies with time.

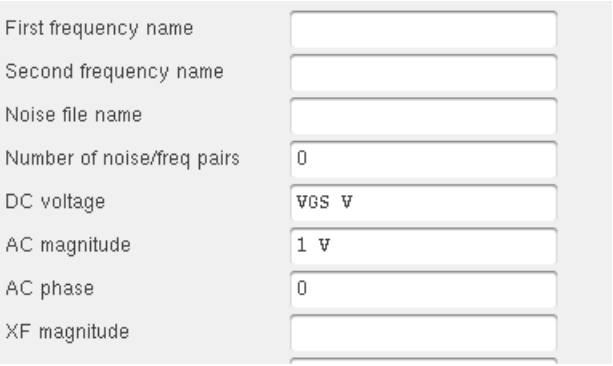


6) Is this amplifier linear? Comment. No, the gain is a function of gm which varies with the input signal, so the gain is not linear, hence the amplifier is not linear; the amount of amplification depends on the input signal.

3. [optional] Maximum Gain

1) VGS is set to the value obtained in part 1 at 0.69

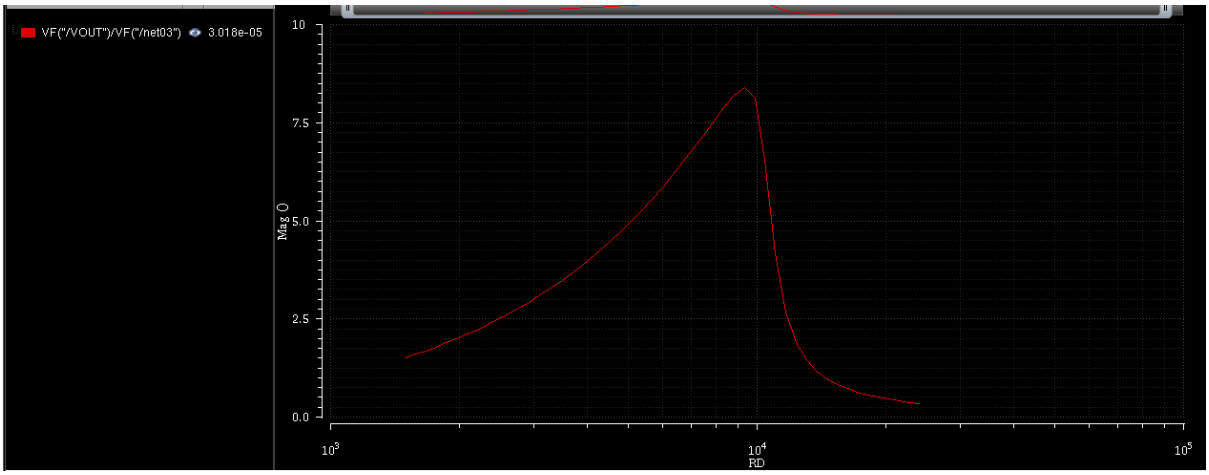
2) The parameters are shown, VGS is constant at 0.69



3) The calculator expression for the gain is shown

```
VF("/VOUT")/VF("/VIN")
```

The plot of gain (Vout/Vin) is shown vs RD



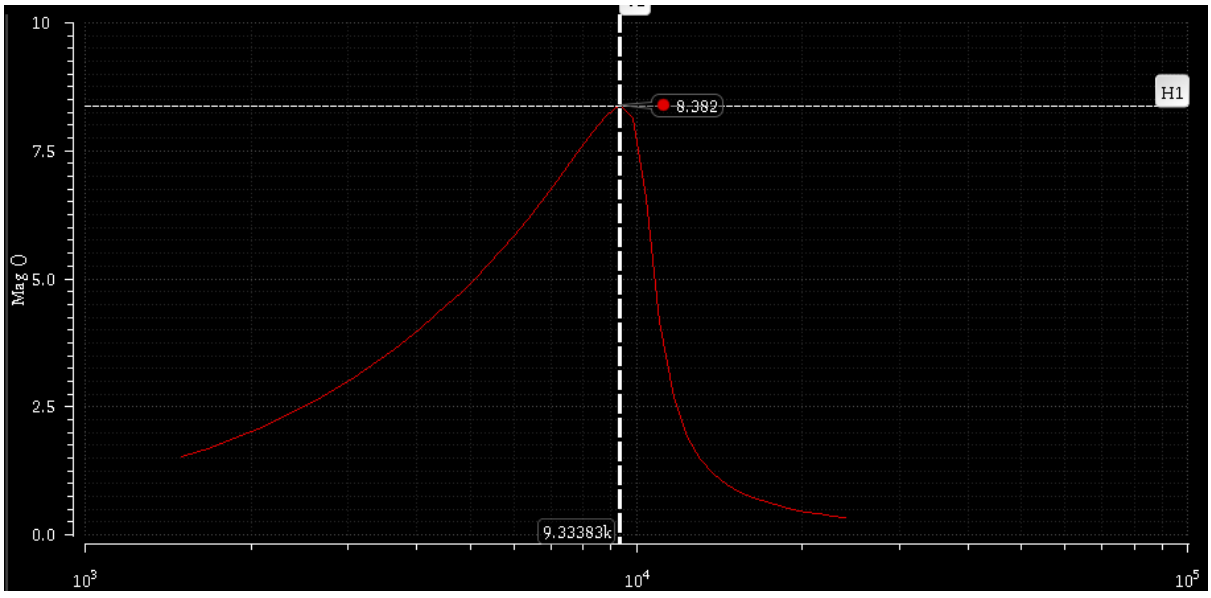
4) gm = 2*ID/Vov,

Av = -gm*RD = - 2*VRD/Vov

As we can see, Av increases with RD.

As RD increases, VDS decreases until it reaches a value at which the transistor exits the saturation region and re-enters the triode region, where ID decreases significantly, so gm decreases, and so does the gain.

5) From the graph, as shown the value of RD at highest gain is 9.3k and the highest gain is 8.382.



6) As stated before, after reaching max gain, the transistor starts to enter into the triode region. We can assume that VDS = Vov = VovQ = 305mV.

RD = (VDD – Vov)*ID = (1.8 – 0.305)V / 150uA = 9.967k ohms

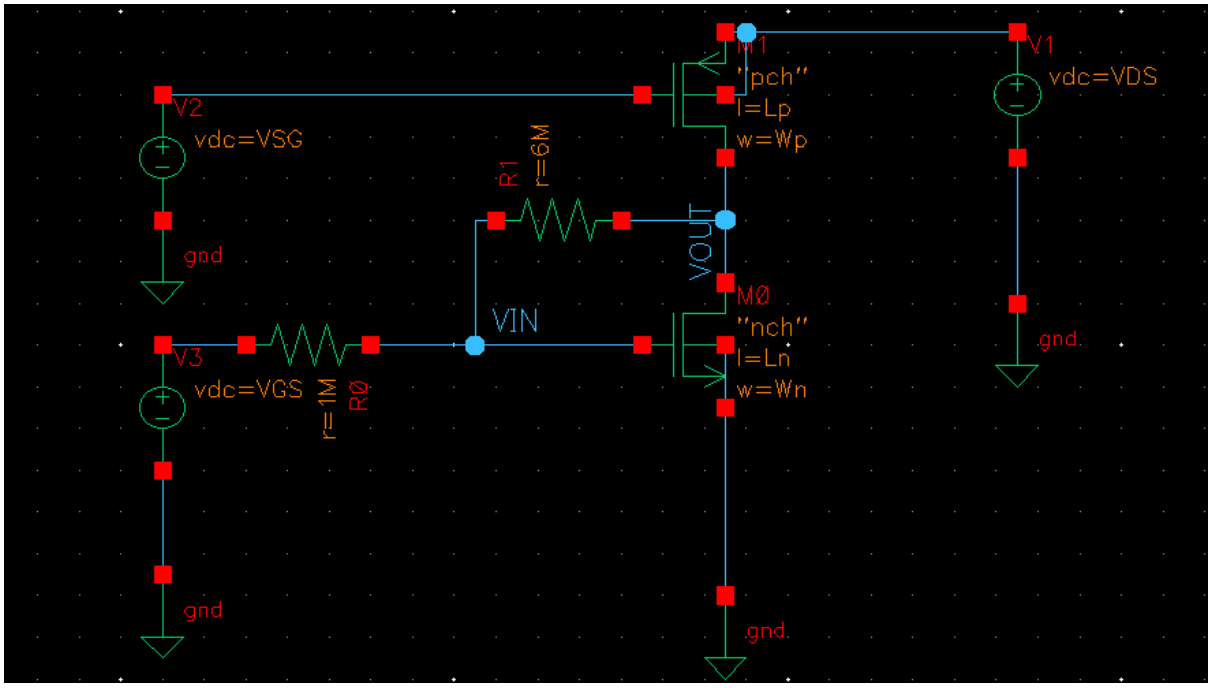
So Av=-gmRD = -(2*ID/Vov)*RD= -(2*150uA/0.305V)*9.967k ohms = -9.8

7) At max gain, the transistor begins to enter the triode,

8) No, scaling down the supply voltage reduces the upper bound on the maxium value of Vout, hence the gain is reduced.

4. [optional] Gain Linearization (feedback)

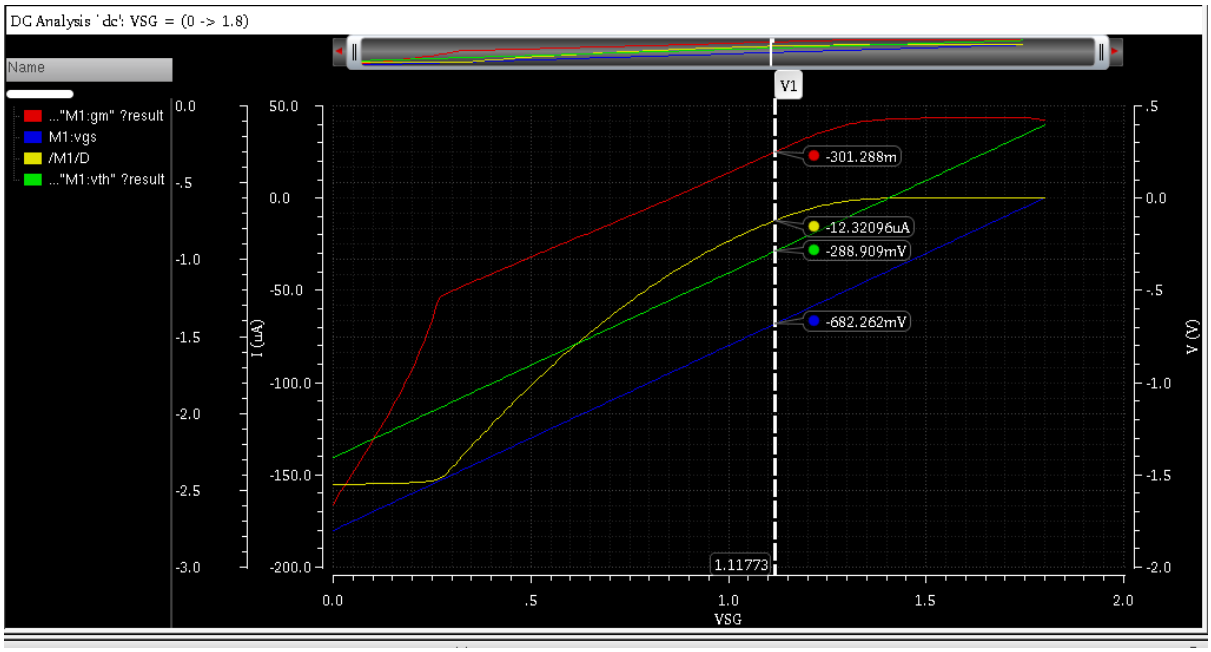
The circuit schematic is shown.



1) , 2) Satisfied.

3) The sweep was performed and the important parameters are shown.

Vgs(blue), ID(yellow) for the PMOS, Vov(green), gm(red).



From the graph we can see that IDx(in yellow) = -12.32096 uA at V* = 0.3V

Taking absolute value and approximating, so IDx = 12 uA

VSGQ = -682.262 mV,

Approximating and taking absolute value, VGSQ = 682 mV

V* = 0.3V at VSG = 1.11773V

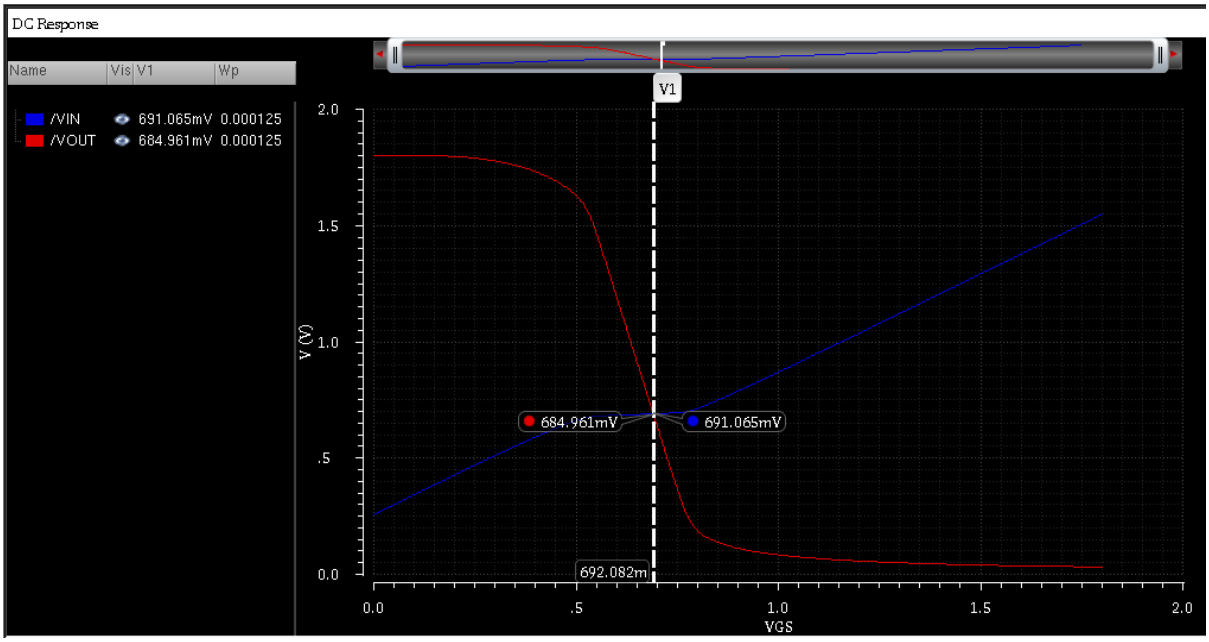
By cross multiplication Wnew = IDQ * Wold / IDx = 150 * 10 / 12 = 125 um

4) Noted.

5) Rf = Rin * |Av| = 1M * |-6| = 6M ohms

6) Satisfied.

7) The plot of VIN (blue) and VOUT (red) vs VSIG are shown overlaid.

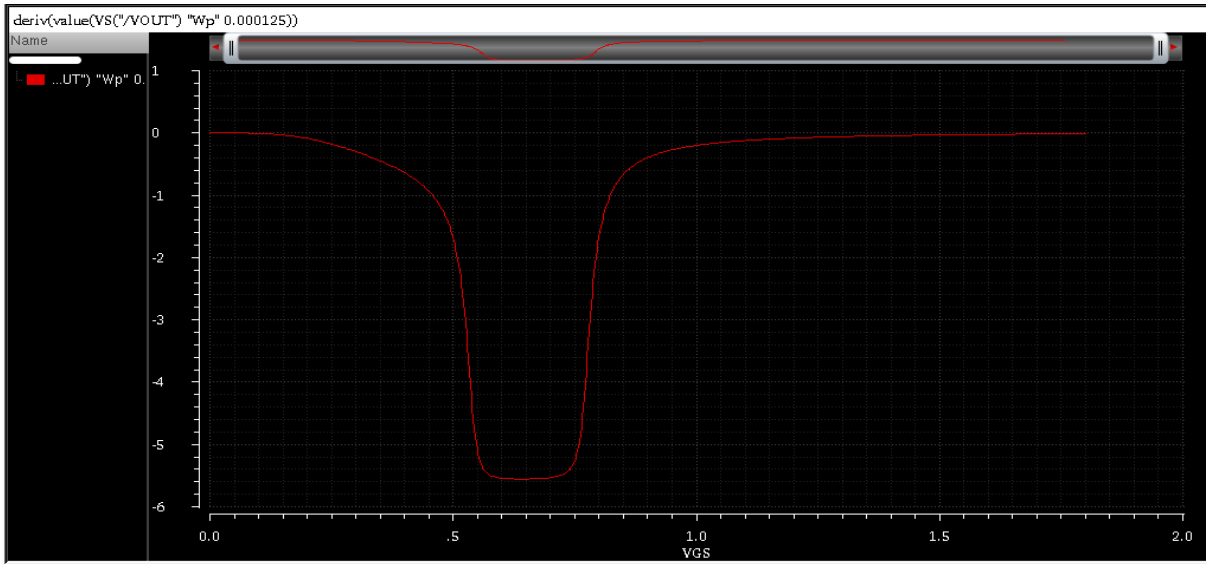


The two voltages cross at 0.692V. This value is reasonable, it is almost equal to the value we obtained for VGSQ.

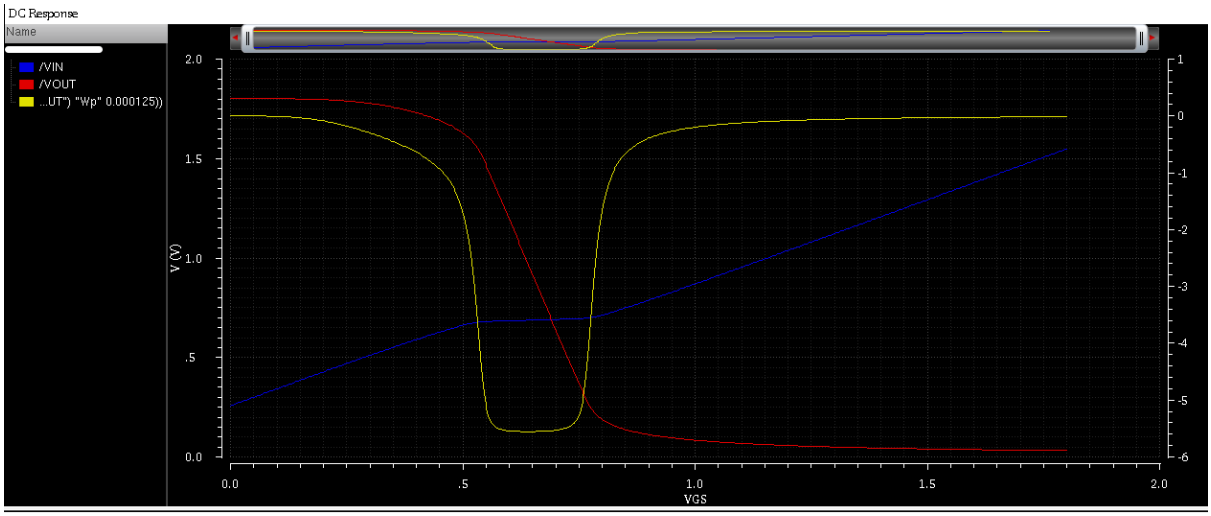
8) Is VOUT linear with VSIG?

VOUT is linear with respect to VSIG in the region where both tranistors are properly biased into saturation; in that region the gain Av doesn't depend on the input signal, and hence it is linear. Else, either the NMOS or the PMOS enter the triode region and the linearity of gain is lost. VOUT and VSIG change with the same value; have the same slope, so VIN is constant.

9) The derivative of VOUT is shown

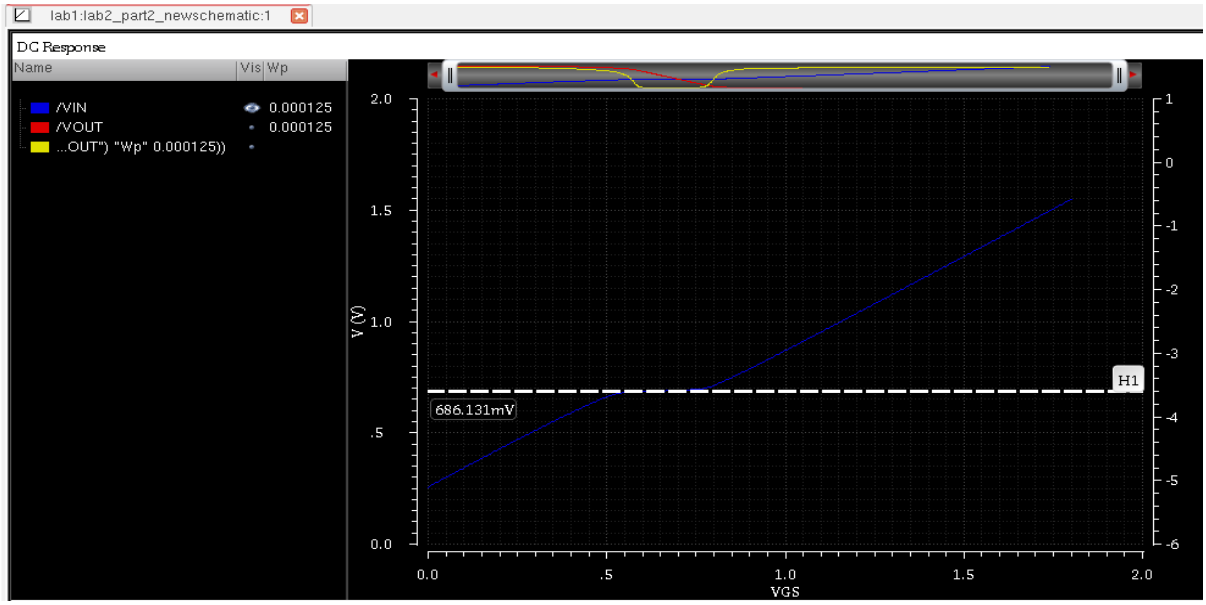


Derivative of VOUT is plotted with VIN and VOUT itself is shown.



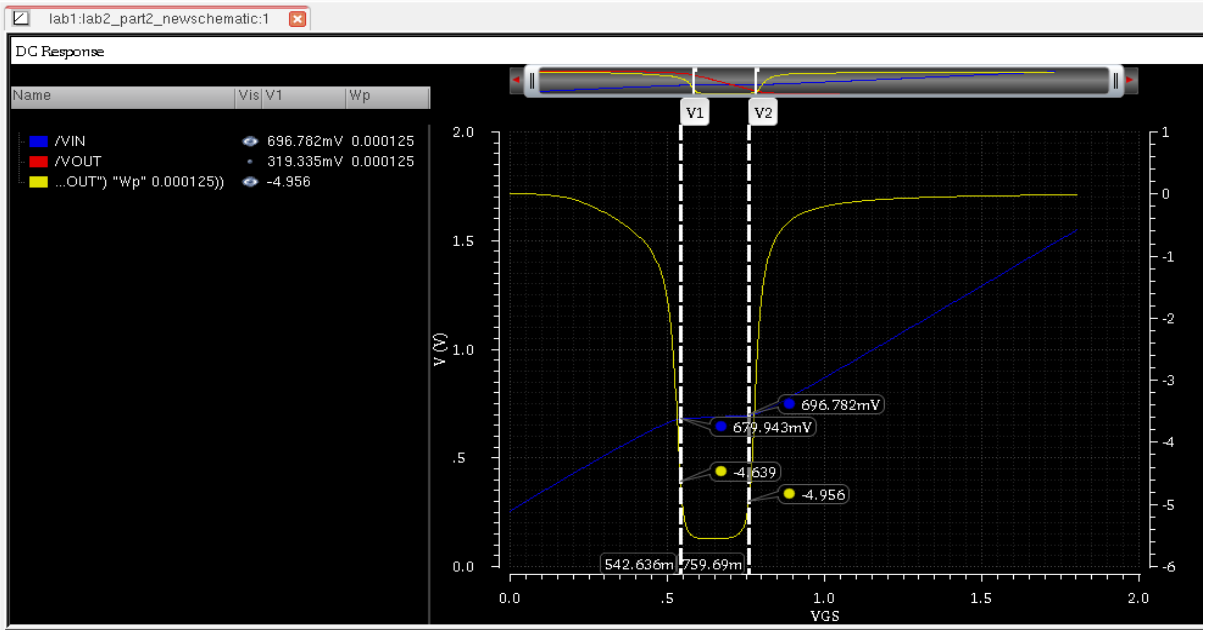
For a wide range (the part of the shown graph where the plot is almost flat), the gain is linear; This is due to the effect of feedback. As we get below or above that value of VGS, either the NMOS or the PMOS leave the saturation region, and enter the saturation region, where the gain is no more linear. Also the feedback resistance decreases the dependency over gm, contributing to gain linearity.

10) The value of VIN for which the gain is linear can be obtained from the following graph.



As we can see that value is 686mV, approximately. That is the value around which the gain is linear. The range around that value was obtained by sweeping horizontally across the curve to be 60mV.

By sweeping the cursor across the part of the gain curve which is linear.



we can obtain that Vin in that region has a range of about 759.69 – 542.636 = 217mV.

11) Analytically the input range value = (VDD – 2*V)/|Av| = (1.8 – 2 * 0.3)/|5.5| = 218mV. The value is close to the value calculated from the graph.