Credit Hours System

ELCN101

Electronics-1

Cairo University

Faculty of Engineering

Project
“Diode Circuit and Design”

Prepared by:

Alhussein Gamal Hussein Ali (1200399)

Aley Eldin Hisham Mohamed Mostafa (1200475)

Program: CCEE

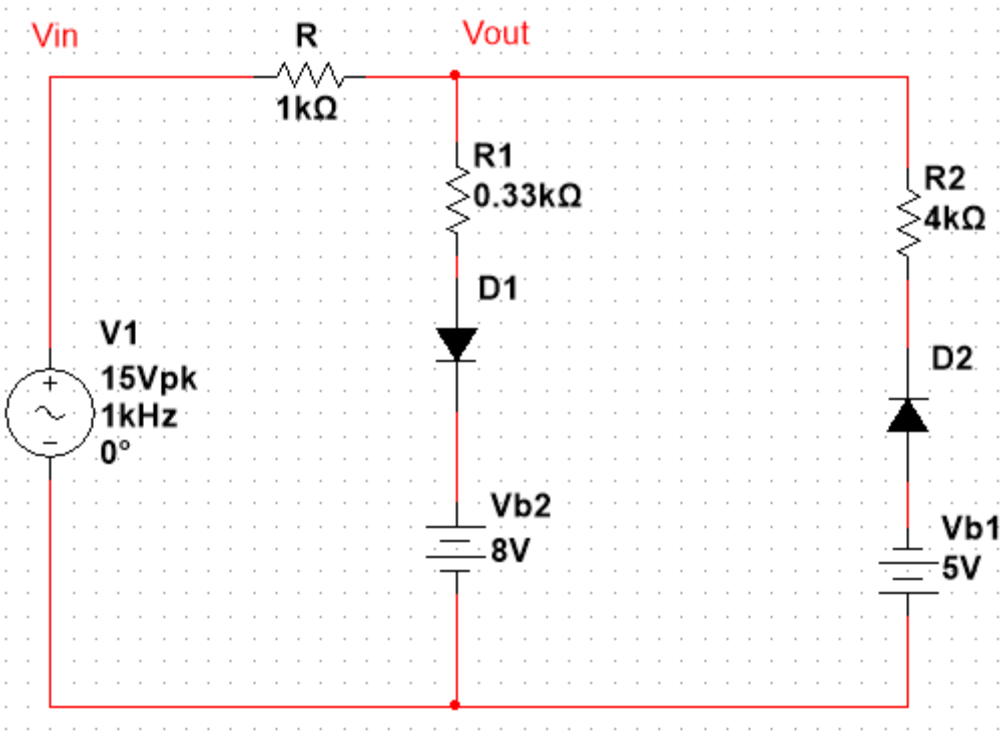
Submitted to:

Dr. Ahmed Hussien

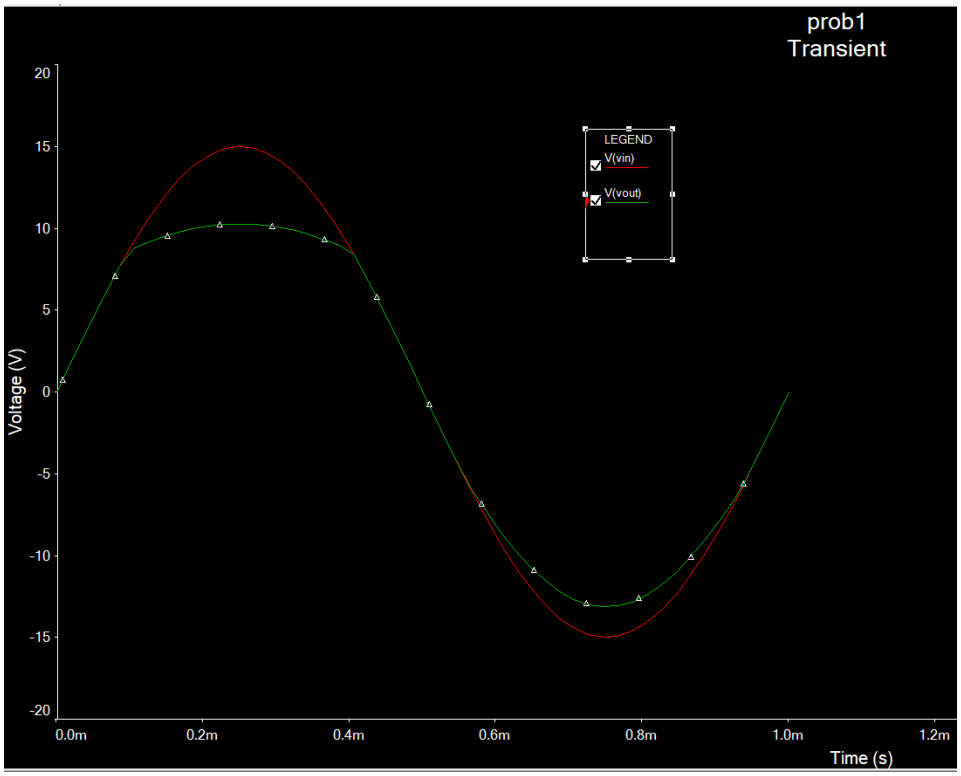
Dr. Amal Samir

Problem 1: Double Soft Sided Limiter

Schematic:



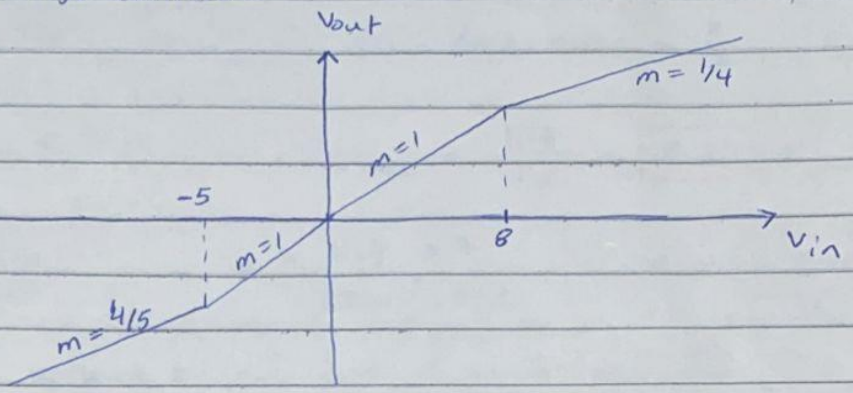
Transient Analysis:



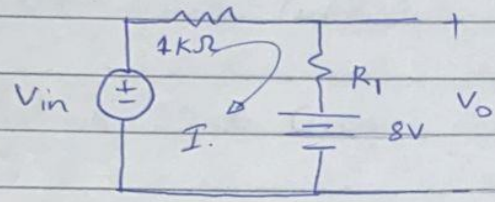
Calculations

Problem 1 :

Double Sided Soft Limiter :



when $V_{in} > 8$:



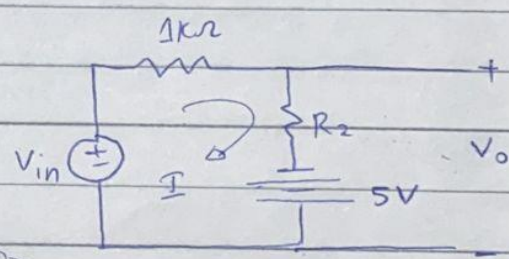
$V_o = 8 + I R_1$

$I = \frac{V_{in} - 8}{1 + R_1}$

$V_o = 8 + R_1\left(\frac{V_{in} - 8}{1 + R_1}\right)$, $V_o = 8 + \frac{R_1 V_{in}}{1+R_1} - \frac{8R_1}{1+R_1}$

$\frac{R_1}{1+R_1} = \frac{1}{4}$, $4R_1 = 1 + R_1$, $\boxed{R_1 = 1/3\ K\Omega}$, $\boxed{V_{b_2} = 8V}$

when $V_{in} < -5$:



$V_o = -5 + I R_2$, $I = \frac{V_{in} - -5}{1 + R_2}$

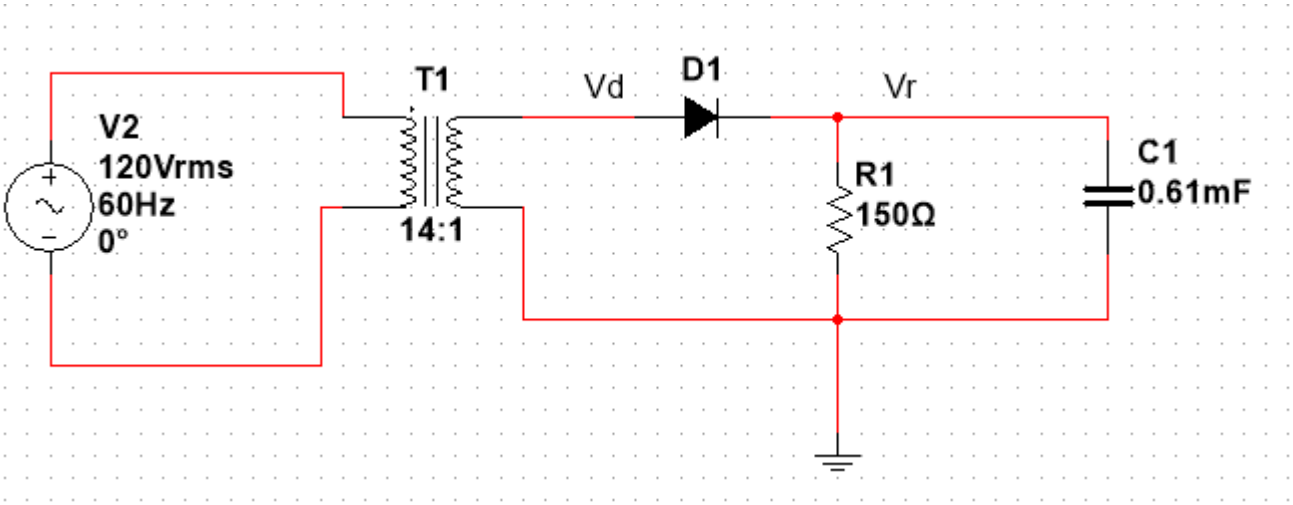
$V_o = -5 + \left(\frac{V_{in} + 5}{1 + R_2}\right) R_2$, $V_o = -5 + \frac{V_{in} R_2}{1+R_2} + \frac{5R_2}{1+R_2}$.

$\frac{4}{5} = \frac{R_2}{1+R_2}$, $\boxed{R_2 = 4K\Omega}$, $\boxed{V_{b_1} = 5V.}$

Problem 2: Rectifier Circuits

Part 1: Half wave Rectifier

Schematic:



problem 2 : Rectifier Circuits:

i- Half wave Rectifier Circuit:-

a) $V_{DC} = (V_p - V_{D_{ON}}) - \frac{V_r}{2}$, $10 = V_p - 0.7 - \frac{2}{2}$

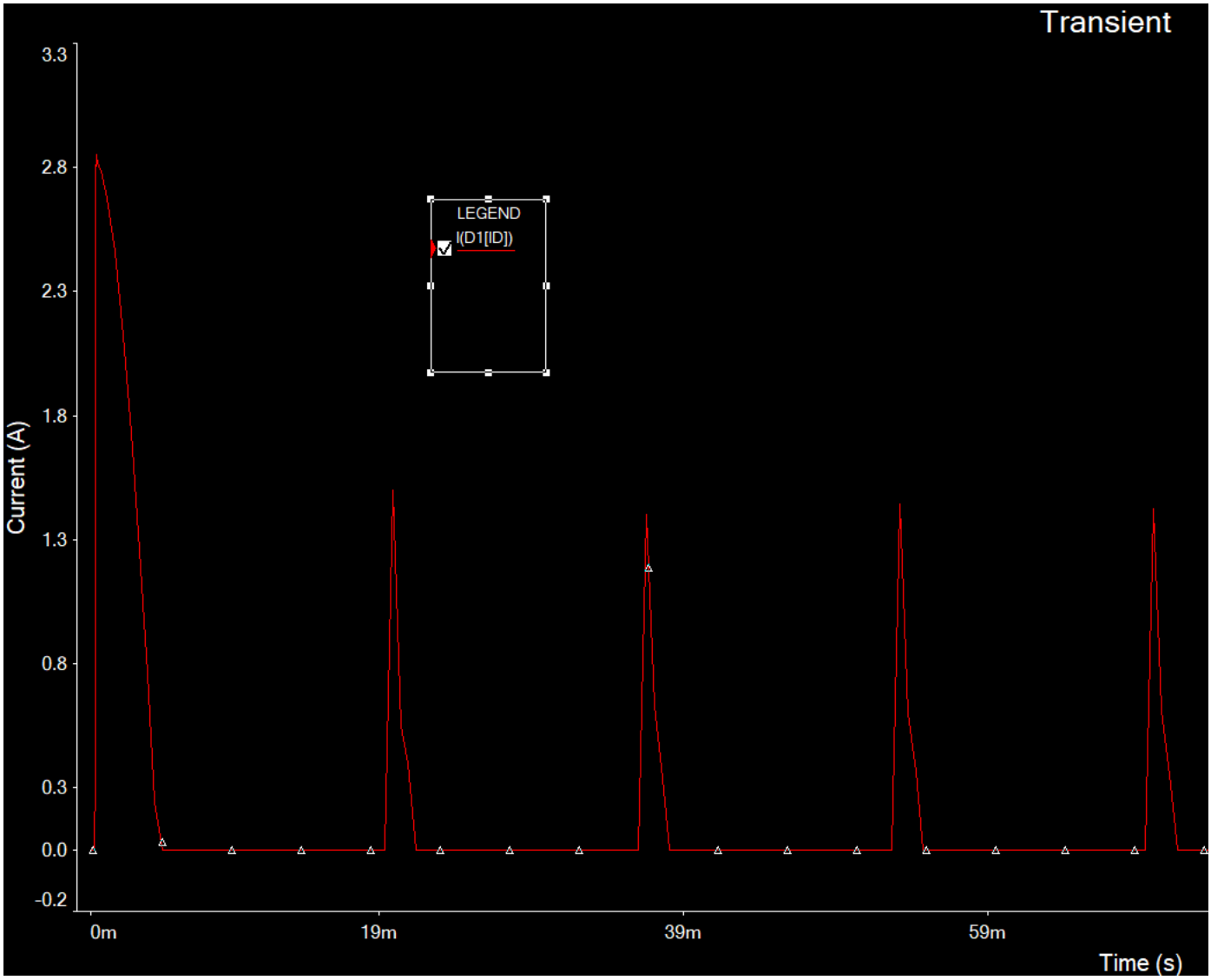
$V_p = 11.7\ V$, $V_{rms} = \frac{11.7}{\sqrt{2}} = \boxed{8.273V}$

b) $V_r = \frac{V_p - V_{D_{ON}}}{fRC} \Rightarrow 2 = \frac{11.7 - 0.7}{60 \times 150 \times C}$, $C = \boxed{611.11\ \mu f.}$

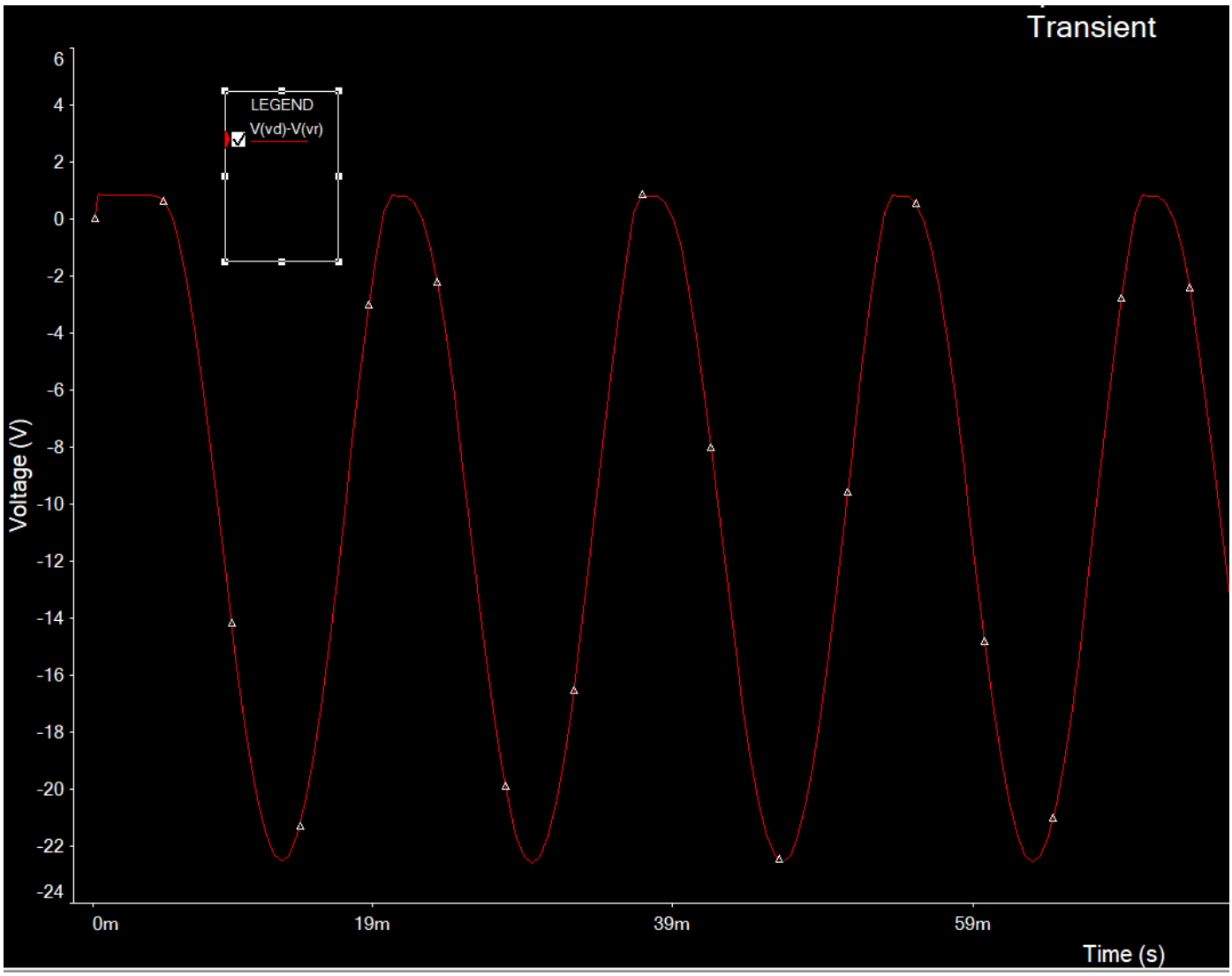
c) Max. reverse voltage $= -V_p - (V_p - V_r) = \boxed{-21.4\ V.}$

d) Avg Diode current $= \frac{V_{DC}}{R}\left(1 + \pi\sqrt{\frac{2V_p}{V_r}}\right) = \boxed{0.783\ mA}$

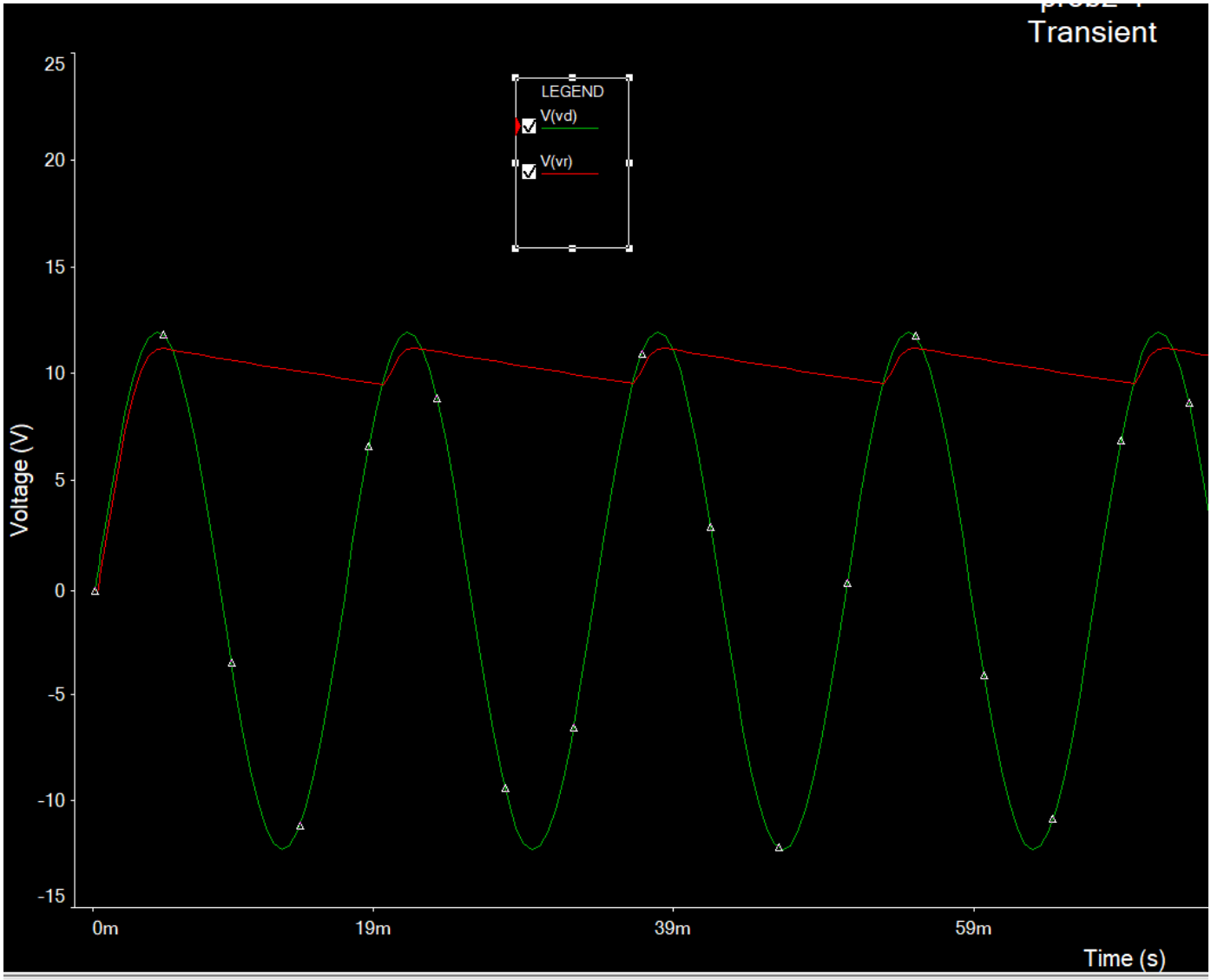
e) Peak Diode Current $= C\omega V_p\sqrt{\frac{2V_r}{V_p}} + \frac{V_p}{R} = \boxed{1.654\ A}$



Diode Current

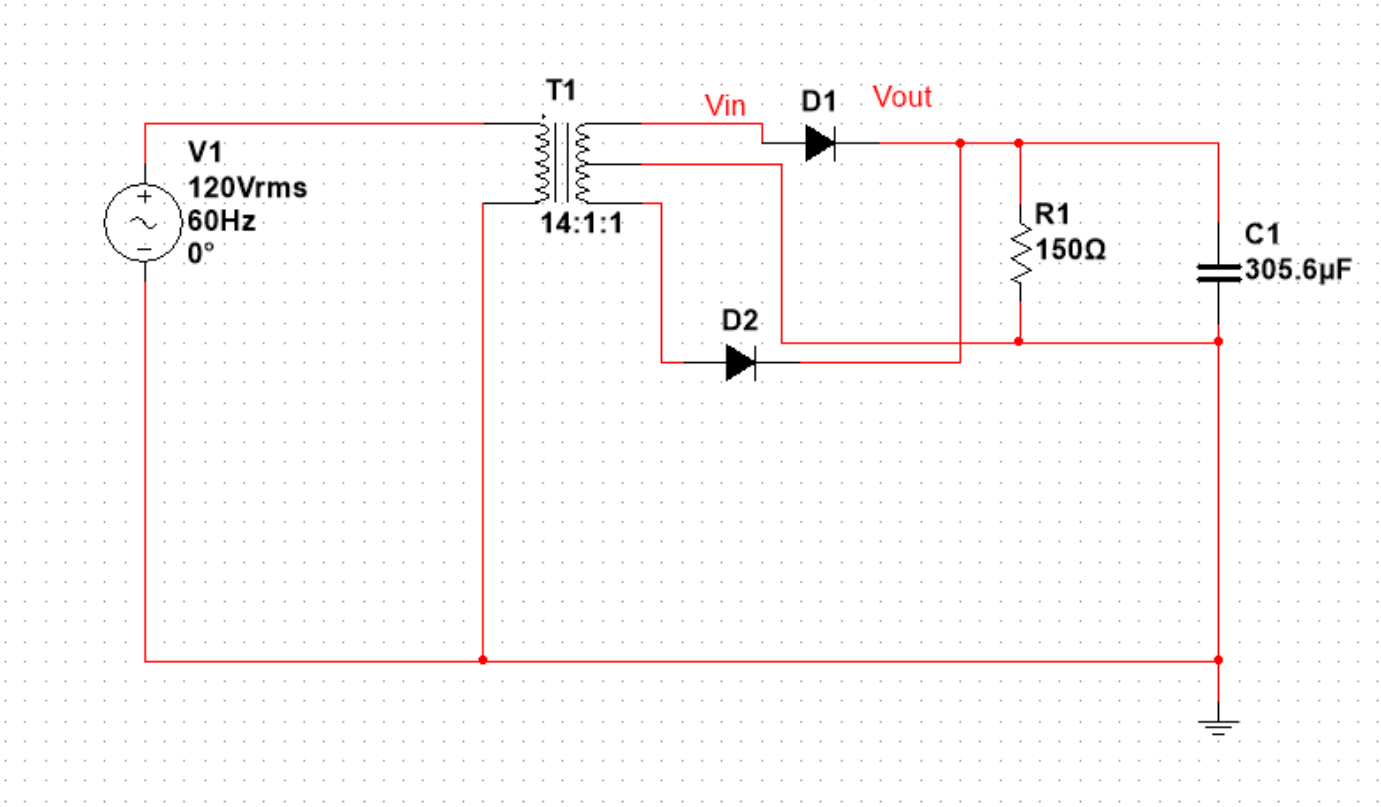


Diode Voltage



Load Voltage vs Secondary Voltage

Part 2: Full Wave Rectifier



Calculations

ii- Full wave Rectifier.

a) $V_{DC} = (V_p - V_{D_{ON}}) - \frac{V_r}{2}$, $10 = (V_p - 0.7) - \frac{2}{2}$

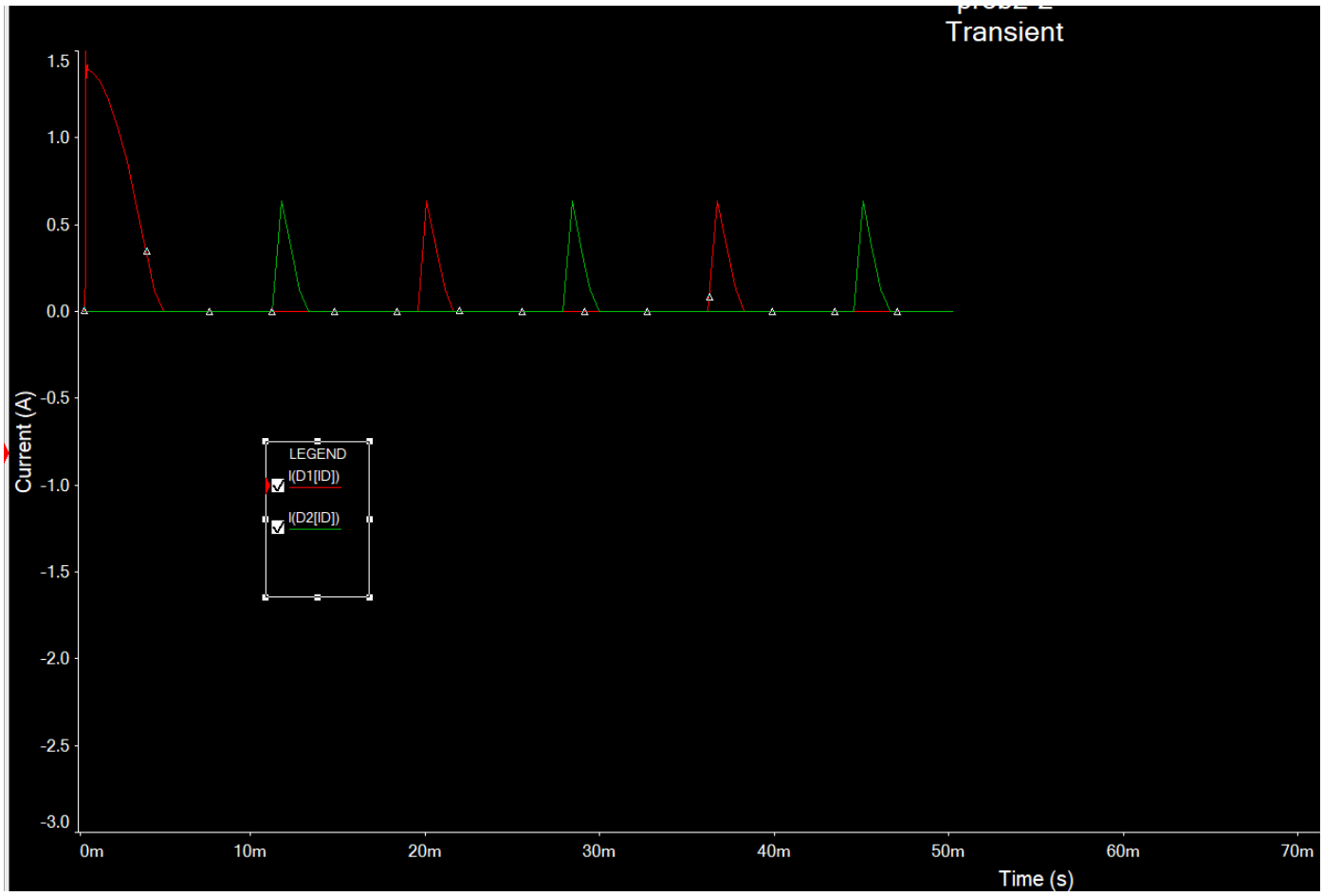
$V_p = 11.7\ V$, $V_{p_{rms}} = \frac{11.7}{\sqrt{2}} = \boxed{8.273\ V}$

b) $V_r = \frac{V_p - V_{D_{ON}}}{2fRC}$, $2 = \frac{11.7 - 0.7}{2 \times 60 \times 150 \times C}$, $C = \boxed{305.55\ \mu f}$

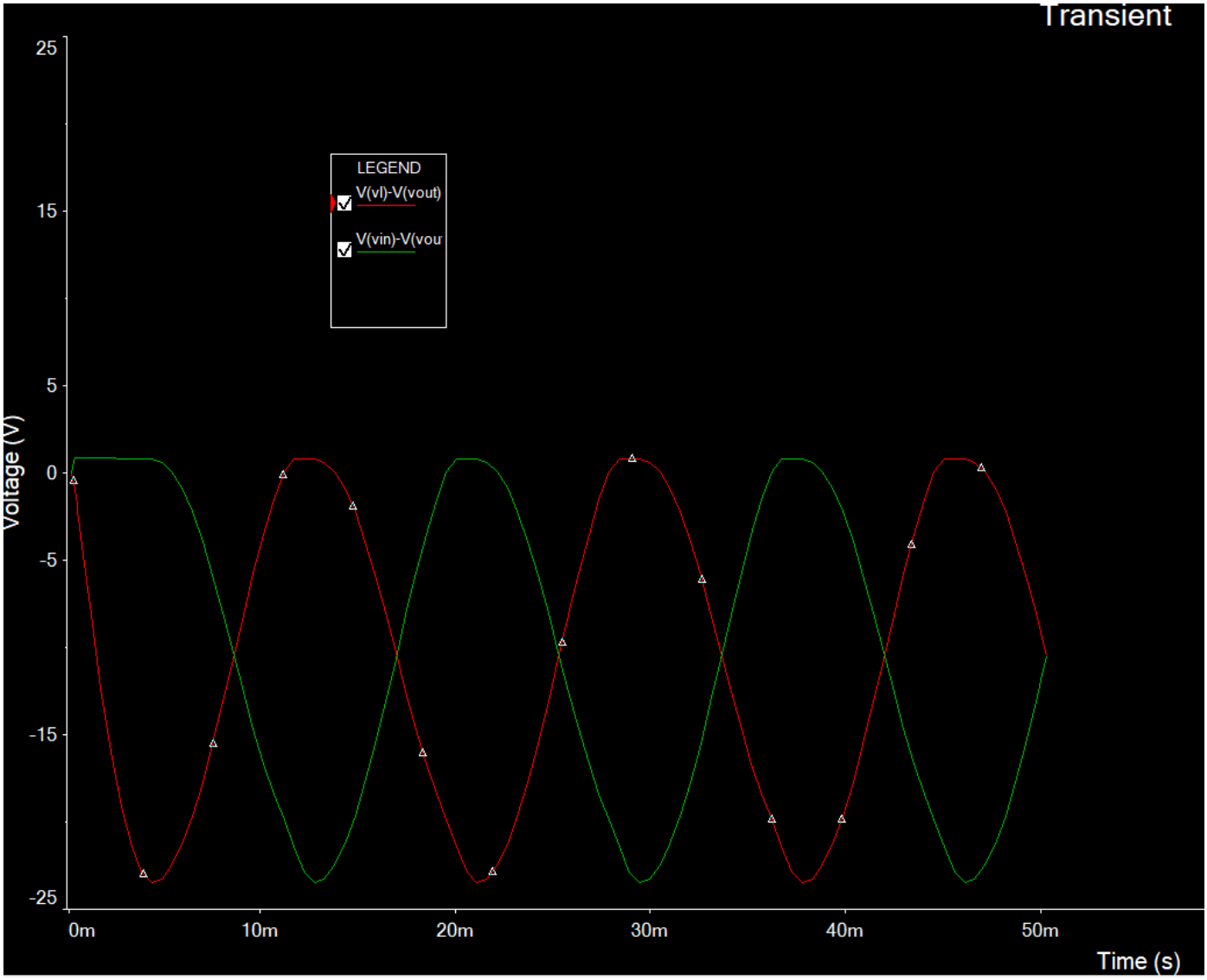
c) Max. Reverse voltage $= -V_p - (V_p - V_r) = \boxed{-21.4\ V}$

d) Avg Diode Current $= \frac{V_{DC}}{R}\left(1 + \pi\sqrt{\frac{2V_p}{V_r}}\right) = \boxed{0.783\ mA}$

e) peak Diode Current $= CWV_p\sqrt{\frac{2V_r}{V_p}} + \frac{V_p}{R} = \boxed{0.866\ A}$

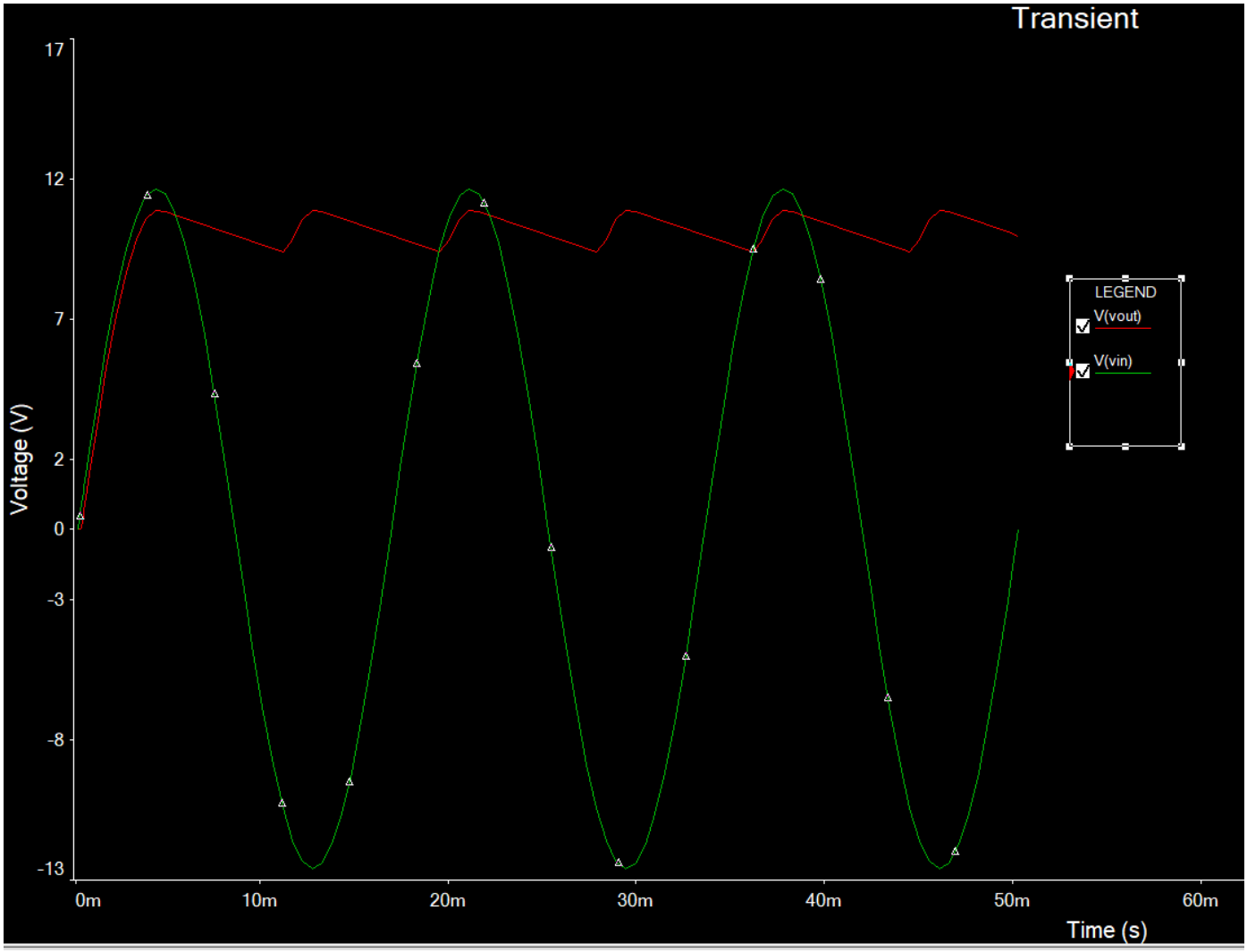


Diode Currents



Diode Voltages

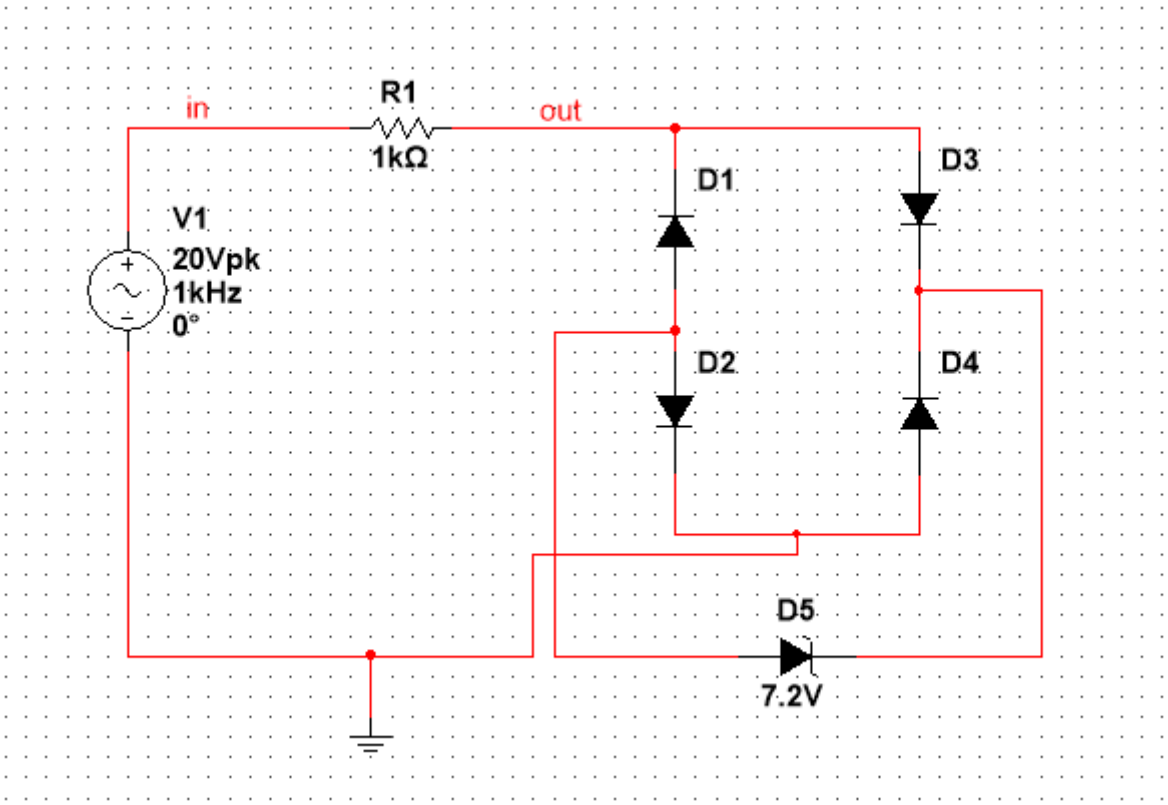
Notice the overlap in the curve of diode voltages



LOAD VOLTAGE VS SECONDARY VOLTAGE

Problem 3: Limiters Involve Zener

Schematic:



Calculations

problem 3:

Limiters Involve Zener:

$$V_z = V_{z_0} + I_z r_z$$

$$7.5 = V_{z_0} + \left(\frac{15}{1000} \times 20\right), \quad V_{z_0} = 7.2V.$$

* If $V_{in} < 0.85$
  - D_{13} is reverse $\Rightarrow V_{in} = V_{out}$

* $0.85 < V_{in} < \overset{8.05}{(0.85 + 7.2)}$ "$8.05 = V_{on} + V_z$"
  - Zener in reverse region $\Rightarrow V_{in} = V_{out}$

* $8.05 < V_{in} < 8.9$ "$8.9 = 2V_{on} + V_z$"
  - D_{42} is reverse $\Rightarrow V_{in} = V_{out}$

* $V_{in} > 8.9$
  - D_{13} & D_{42} 're ON
  - Zener in Breakdown region

$$V_{out} = 8.9 + IR, \quad I = \frac{V_{in} - 8.9}{(1000 + 50 + 50 + 20)}$$

$$V_{out} = 8.9 + \left(\frac{V_{in} - 8.9}{1120}\right)(120)$$

$50 + 50 + 20$ ← $r_D + r_D + r_z$

* $-0.85 < V_{in} < 0$

- D_{Z3} is reverse $\Rightarrow$ $V_{out} = V_{in}$

* $-8.9 < V_{in} \leq -0.85$

- Zener in reverse region

$V_{out} = V_{in}$

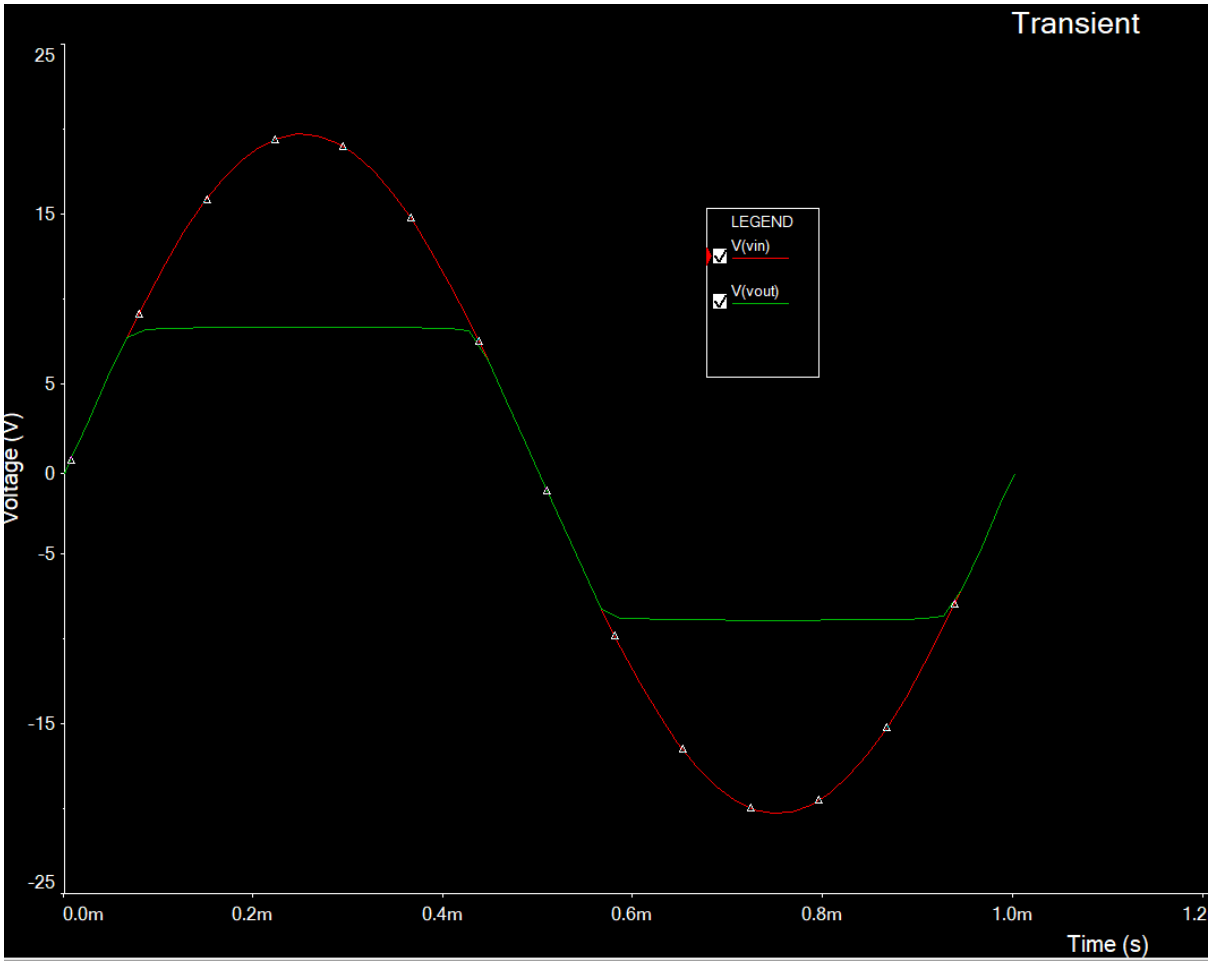
* $V_{in} < -8.9$

- D_{Z3} & D_{H2} are ON
- Zener in Breakdown Region.

$V_{out} = 8.9 - IR.$, $I = \frac{8.9 + V_{in}}{1120}$

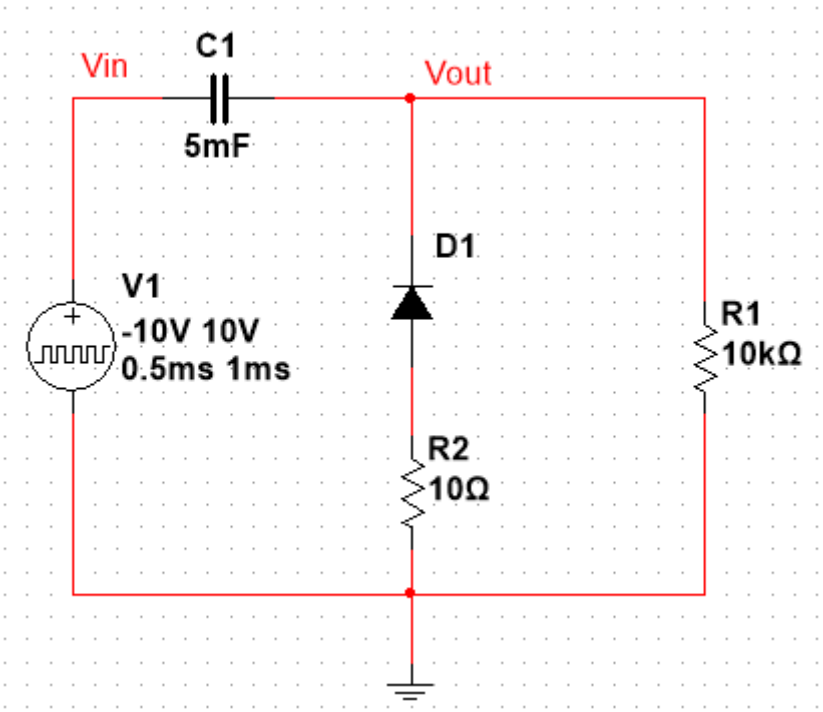
$V_{out} = 8.9 - \left(\frac{8.9 + V_{in}}{1120}\right)(120).$

Transient Analysis:

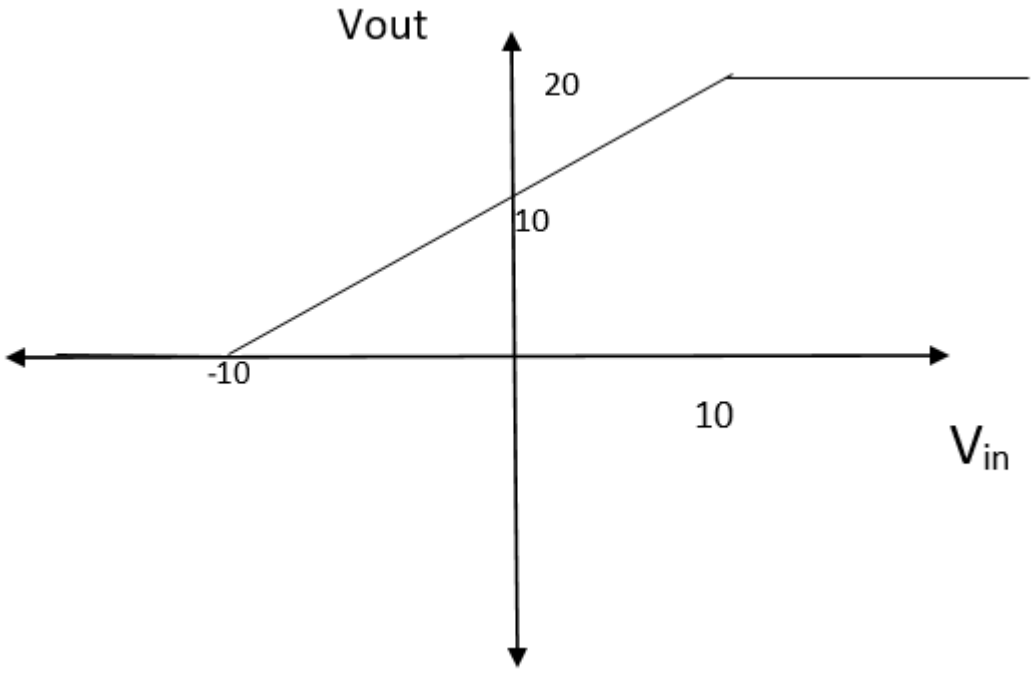


Problem 4: Clamping Circuit

Schematic:



A)



Notes and Observations:

- Initially, the capacitor can be assumed to be fully charged
- Values of Rload and C are chosen such that RC >> T.
- Since $RC >> T$, the capacitor takes a relatively large to time to discharge compared to T, so Vc is always approximately $-10V$.
- The resistance in in series with the diode is small, as is the case practically.

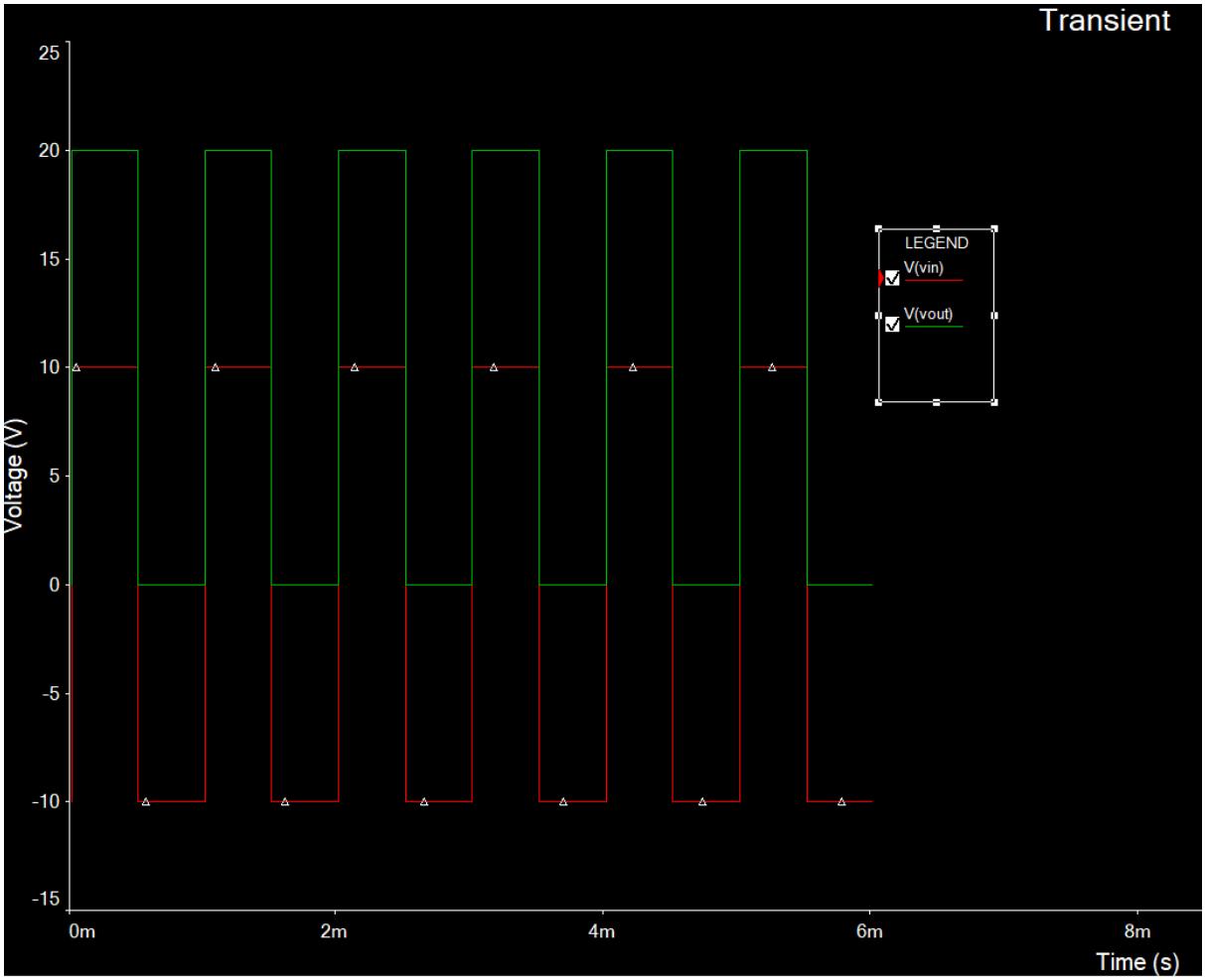
B)

Most positive output level= Vin – Vc = 10 - (-10) = 20V

Most negative output level= Vin – Vc = -10 - (-10) =0V

C)

Transient Analysis:



Output Voltage vs Input Voltage