Credit Hours System

Cairo University

Faculty of Engineering

ELCN201 - Electronics-2

Project 2: Frequency Response & Current Mirror

Program: CCEE

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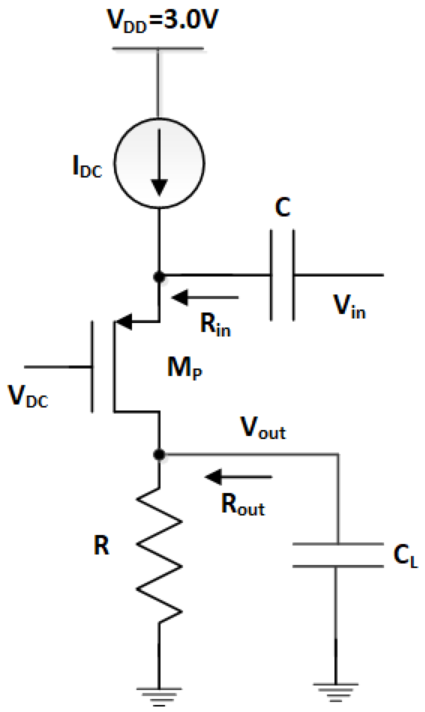
Problem (1): Frequency Response

Design the amplifier with the following specifications:

- A_v (mid-band gain) ≥ 26dB
- Accommodate an input signal with frequency
- band from 500Hz to 30 MHz
- Current consumption ≤ 100µA
- C_L = 0.5 pF



Design Procedure:

Note: Kp = 40uA/V^2 from the model parameters

We choose ID = 95uA

By direct analysis on the schematic or using the SSM:

$$KCL: \frac{Vout}{R} = \frac{Vin - Vout}{ro} + gmVsg, \qquad Vsg = Vin,$$

$$Substituting\ and\ rearranging:$$

$$Vout\left(\frac{1}{ro} + \frac{1}{R}\right) = Vin\left(\frac{1}{ro} + gm\right) \rightarrow \frac{Vout}{Vin} = Av = \left(\frac{1}{ro} + gm\right)(R\,//\,ro)$$

$$lambda = 0 \rightarrow ro = infinity \rightarrow\ Rout = (R\,//\,ro) = R, \qquad Rin = \frac{1}{gm}, \qquad Av = gmR$$

$$From\ the\ gain\ spec: Av \geq 26dB \rightarrow To\ leave\ a\ margin, let\ Av = 28dB \rightarrow\ Av = 10^{\frac{28}{20}} \cong 25$$

AC Analysis:

$$f_L = \frac{1}{2\pi * Rin * C} = \frac{gm}{2\pi * C} = 500\ Hz$$

$f_H = \frac{1}{2\pi * Rout * CL} = \frac{1}{2\pi * R * CL} = 30\ MHz \rightarrow R = 10.61\ kohm \rightarrow let\ R = 12\ kohm$ to make some margin for ignoring ro.

$$Hence, gm = \frac{Av}{R} \cong 2\ mS \rightarrow substituting\ in\ f_L = \frac{gm}{2\pi * C} \rightarrow C \cong 637\ nF$$

$$ID = \frac{Kp}{2} * (|VSG| - |Vtp|)^2$$

$gm = sqrt\left(up * Cox * \left(\frac{W}{L}\right) * ID * 2\right) \rightarrow \frac{W}{L} = 526 \rightarrow let\ L = 1um$ and $W = 526um$

$$Using\ Square\ law: ID = \frac{1}{2} * up * Cox * \frac{W}{L} * Vov^2 \rightarrow Vov = 0.095 \cong 0.1$$

$$From\ Sat. Condition : VDG \leq |Vtp| \rightarrow I_{DC} * R - V_{DC} \leq 0.8 \rightarrow V_{DC} \geq 0.34 \rightarrow let\ V_{DC} = 0.5V$$

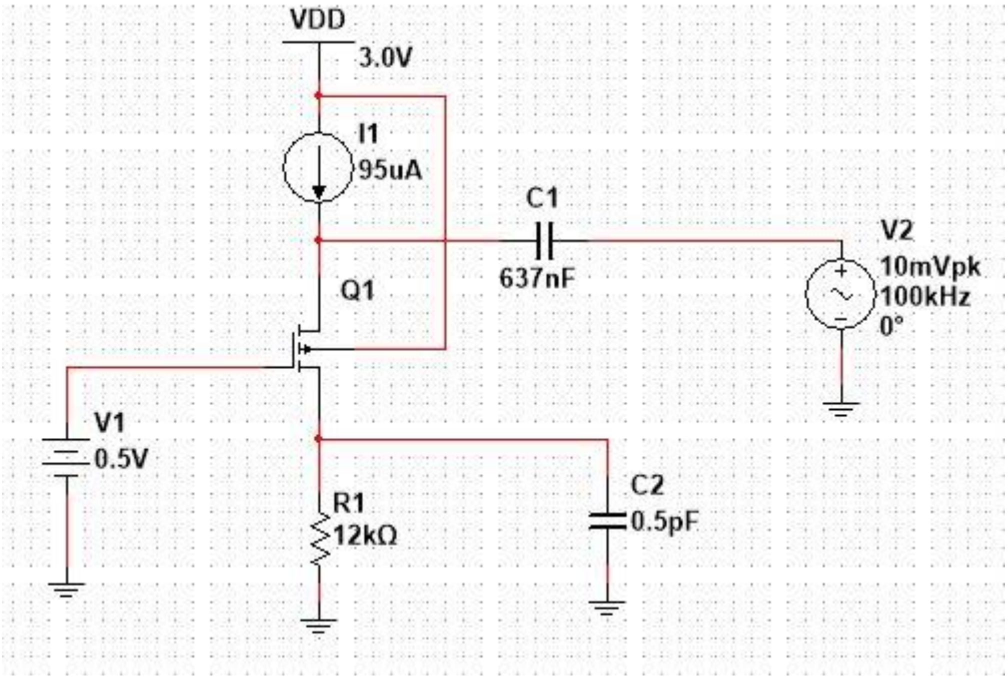
a) Calculate the input linear range and the output signal swing for your design.

$$LIR: Vin \leq 0.2 * Veff = 0.02V$$

$$Swing: \text{Voutmin} = 0\text{V}, \text{Voutmax} - \text{VG} \leq |\text{Vtp}| \rightarrow Voutmax = 1.3V, \ \ Swing = 1.3V$$

Document the design procedure and the results of the following simulations:

Circuit Schematic



<u>DC analysis and show the Q-point (ISD, VSD, Veff), and VDC</u>

DC Operating Point

Design1

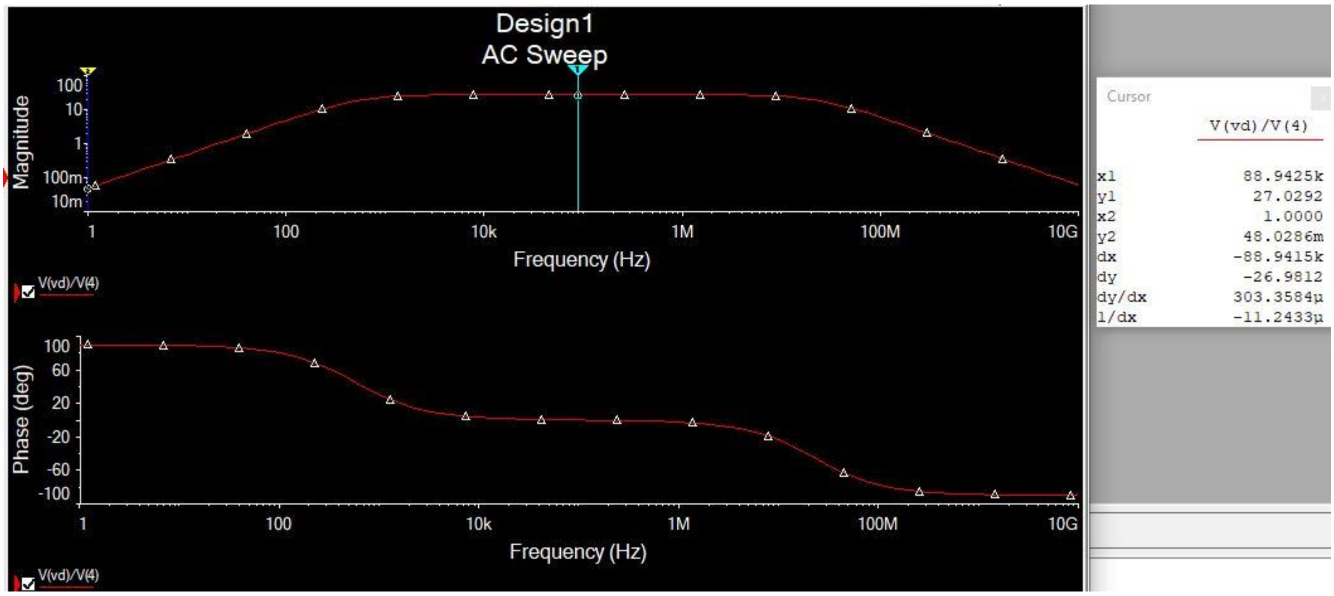
DC Operating Point Analysis

	Variable	Operating point value
1	V(vg)	500.00000 m
2	V(vs)-V(vd)	451.10681 m
3	V(vs)-V(vg)-0.8	291.10681 m
4	I(MQ1[IS])	95.00000 u

VDC = 0.5V, VSD = 0.45V, Veff = 0.29V, ID = 95uA

AC analysis and show the gain (frequency response) up to 1GHz.

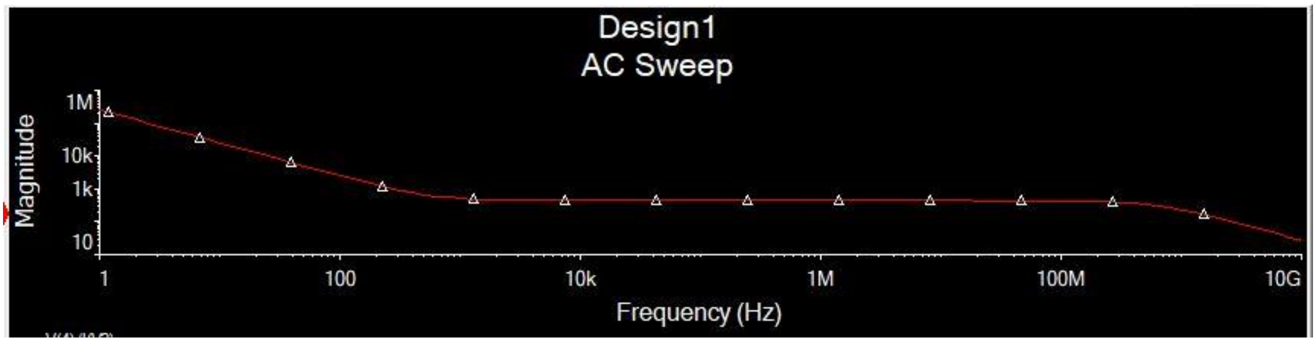
Magnitude and Phase are both shown. The gain is annotated on the right.



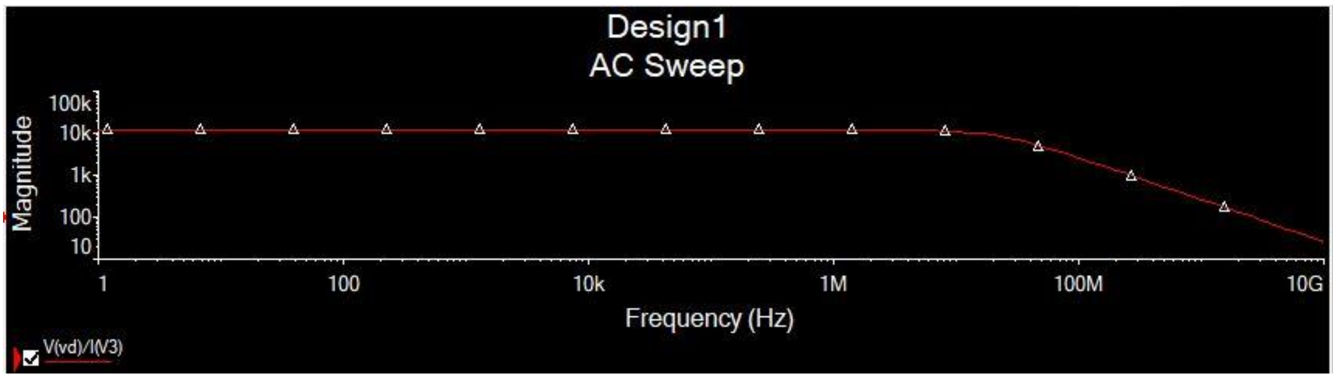
Gain = 27 ~= 28.6dB. The requirement is satisfied

AC analysis and show Rin, and Rout vs. frequency (up to 10GHz).

Rin vs frequency

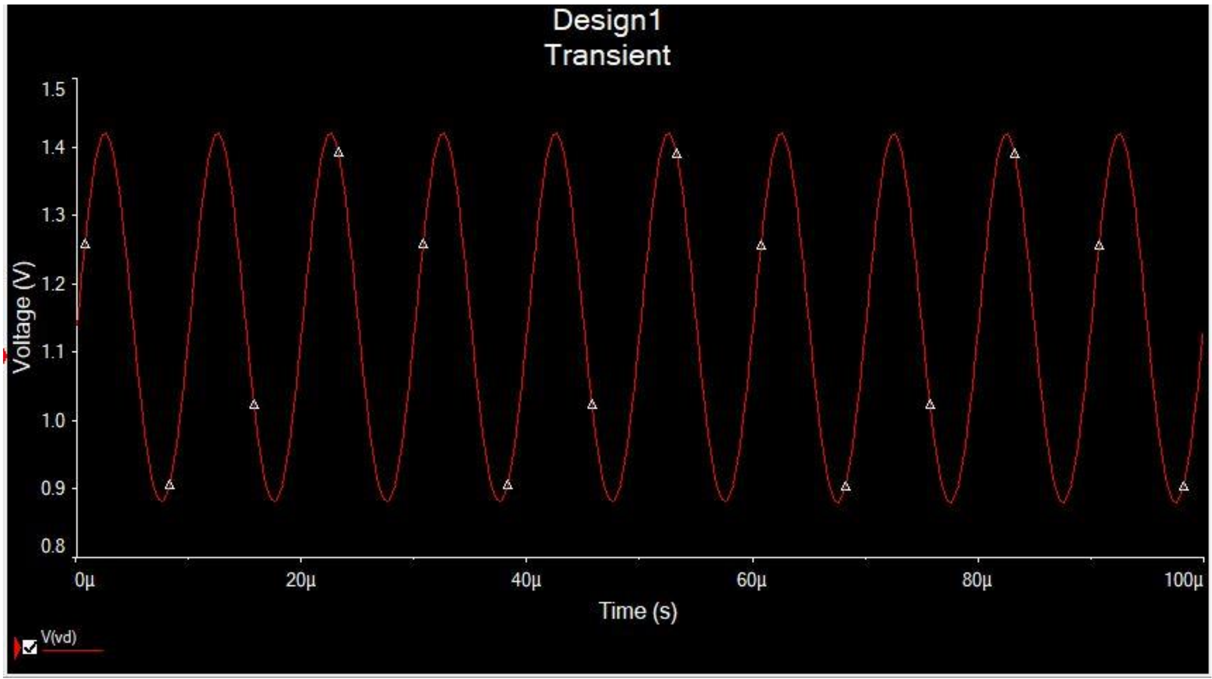


Rout vs frequency

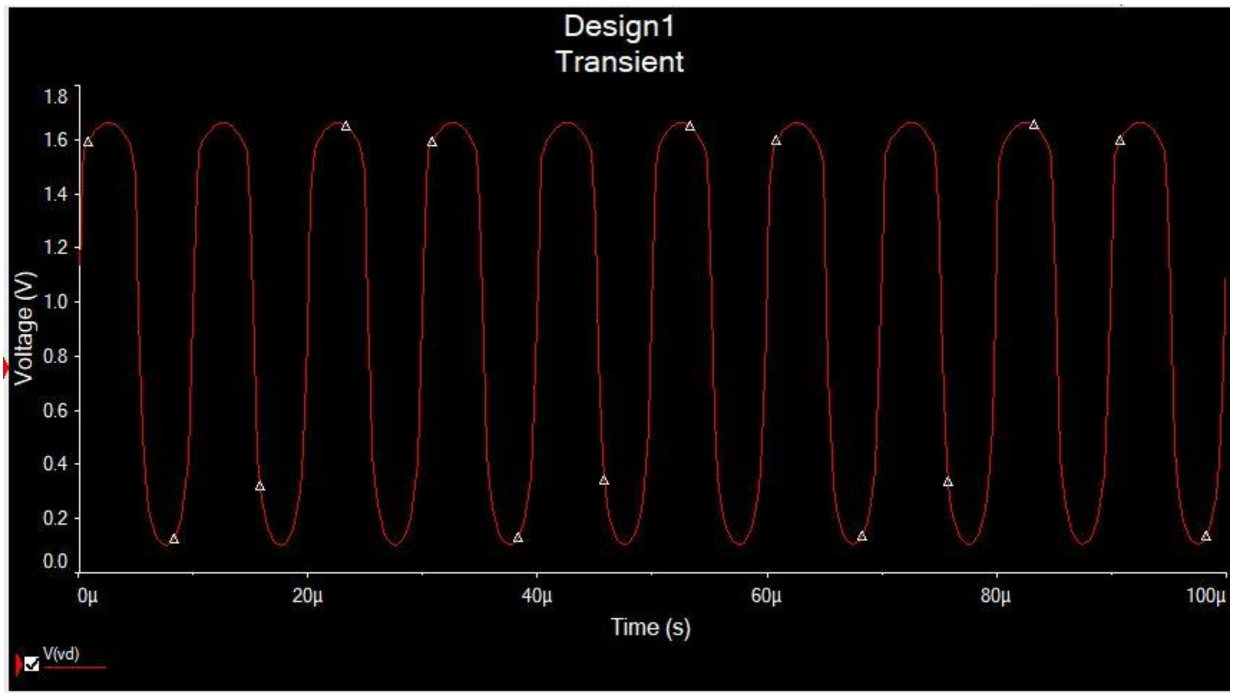


Transient analysis with Vin=A.sin(2πft) and plot Vout. Where A=10mV and f=100kHz

A = 10mV



A = 100mV

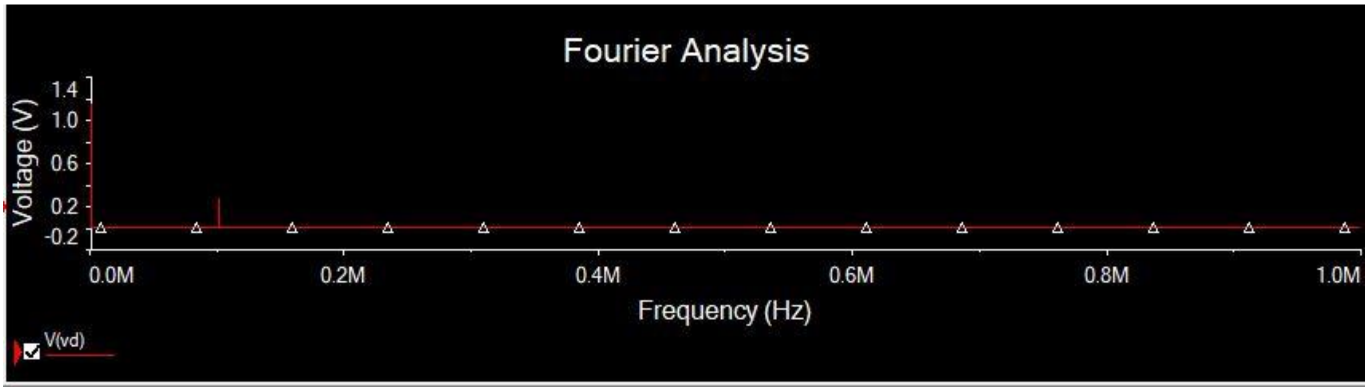


Perform Fourier analysis for the same two cases of the transient analysis and. plot Vout in the frequency domain. Calculate HD2, HD3, and THD.

Case 1: A = 10mV

Design1

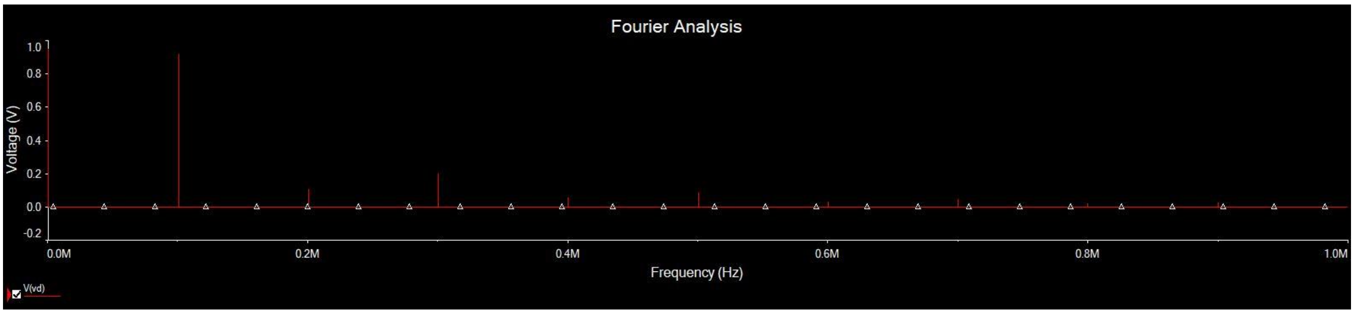
1	Fourier analysis for V(vd):					
2	DC component:	1.14457				
3	No. Harmonics:	9				
4	THD:	2.34722 %				
5	Grid size:	256				
6	Interpolation Degree:	1				
7						
8	Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
9	0	0	1.14457	0	4.24715	0
10	1	100000	0.269492	0.0690633	1	0
11	2	200000	0.00632336	-89.409	0.023464	-89.478
12	3	300000	0.00016594	-0.25145	0.000615753	-0.32051
13	4	400000	1.32494e-05	-13.002	4.91644e-05	-13.071
14	5	500000	1.01877e-05	2.35491	3.78034e-05	2.28585
15	6	600000	8.57151e-06	2.98916	3.18062e-05	2.9201
16	7	700000	7.24366e-06	4.20279	2.6879e-05	4.13372



HD= (Harmonic/fundamental) * 100
HD2= (0.0063/0.2695) * 100=2.346 %
HD3= (0.000166/0.2695) * 100=0.0616 %
THD=2.347 %

Case 2: A = 100mV

1	Fourier analysis for V(vd):					
2	DC component:	0.950619				
3	No. Harmonics:	9				
4	THD:	27.4828 %				
5	Grid size:	256				
6	Interpolation Degree:	1				
7						
8	Harmonic	Frequency	Magnitude	Phase	Norm. Mag	Norm. Phase
9	0	0	0.950619	0	1.03284	0
10	1	100000	0.920397	-0.11399	1	0
11	2	200000	0.10514	89.6692	0.114233	89.7832
12	3	300000	0.196823	-0.3918	0.213846	-0.27782
13	4	400000	0.0565486	89.4757	0.0614394	89.5897
14	5	500000	0.0850352	-0.7111	0.0923897	-0.59712
15	6	600000	0.031003	89.2762	0.0336843	89.3902
16	7	700000	0.0440795	-1.0866	0.0478919	-0.97263



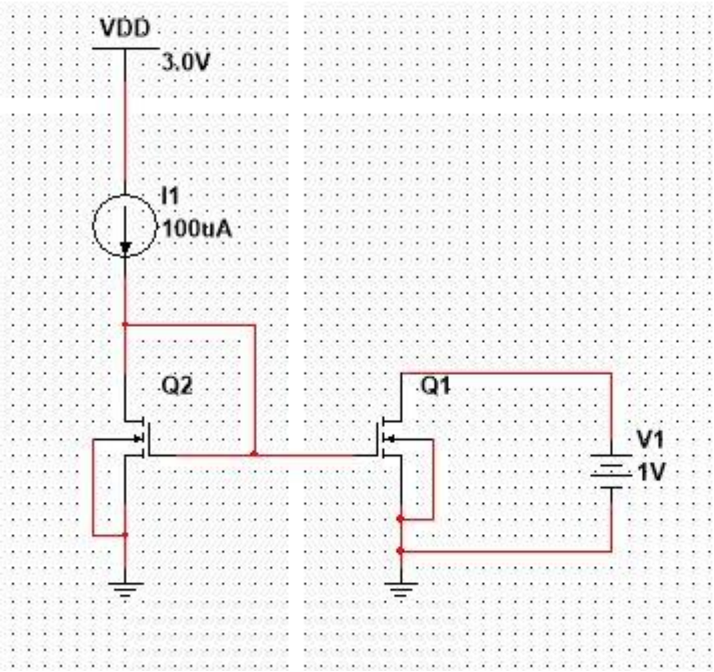
HD= (Harmonic/fundamental) * 100
HD2= (0.10514/0.920397) * 100=11.4 %
HD3= (0.196823/0.920397) * 100=21.4 %
THD=27.48 %

Discussion:

- The specs on the gain and current consumption are satisfied by a good margin.
- Rin and Rout are the close to the hand calculations.
- The circuit doesn't consume a large DC voltage and could have even worked reasonably with a lower current consumption.
- For Vin's amplitude = 10mV – within Vin's linear input range -- the presence of distortion harmonics is almost negligible and hence there's little or no distortion.
- For Vin's amplitude = 100mV – beyond Vin's linear input range -- the presence of distortion harmonics is noticeable and the signal is visibly distorted.
- The distortion increases as the value of Vin exceeds it linear range as elaborated through the transient simulations on signals with amplitudes 10mV and 100mV and also as can be seen from the value of the THD.
- By careful inspection of the harmonics, we can notice that the odd harmonics make for a larger distortion.

Problem (2): Current Mirror

Circuit Schematic



(a) Design the simple current mirror in Fig. 2(a) such that Iin=100µA, Iout=200µA, and Veff is 0.2V for all transistors. Use L=1µm.

Design Procedure

From the given model parameters: Kn = unCox = 120uA/V^2, Vtn = 0.7

Given that L1 = L2 = 1um, Veff = 0.2V, In = 100uA, Iout = 200uA

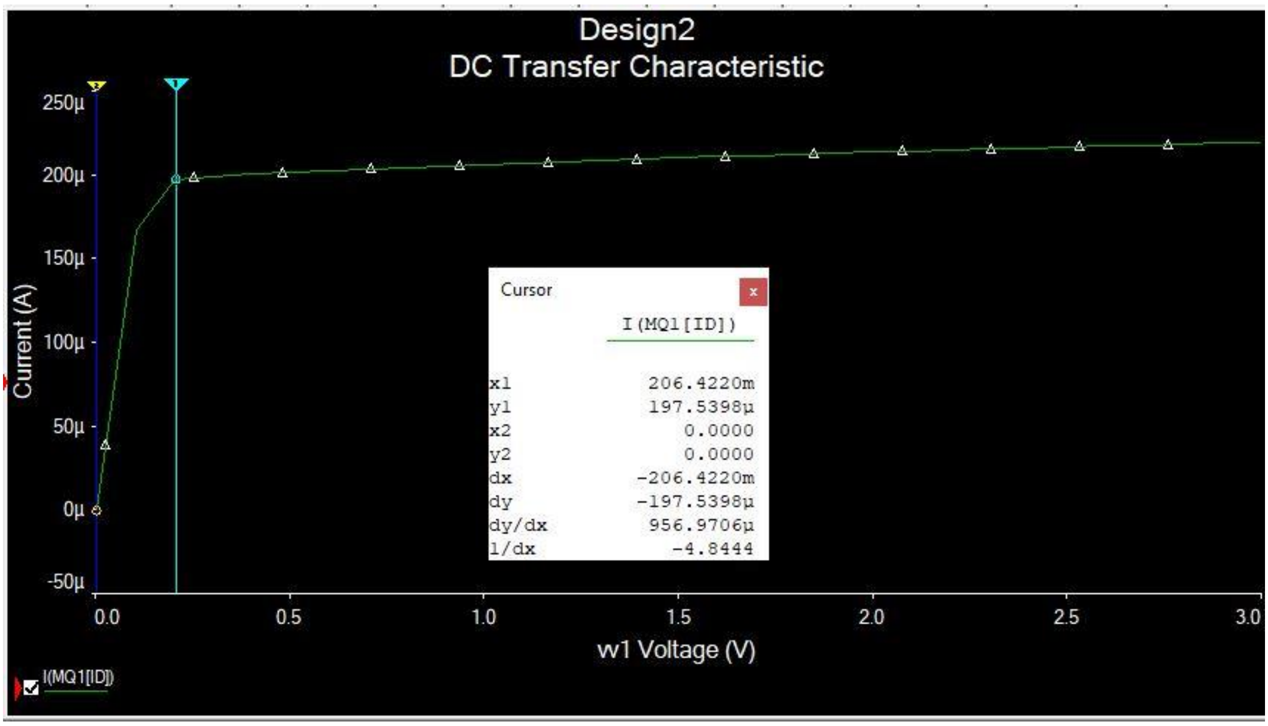
ID = UnCox/2 * (W/L) * Vov^2 ➔ W/L = 41.6667 ~= 42

L1 = 1um ➔ W1 = 42um

To get Iout = 200uA = 2 * Iin ➔ W2 = 2*W1 = 84um

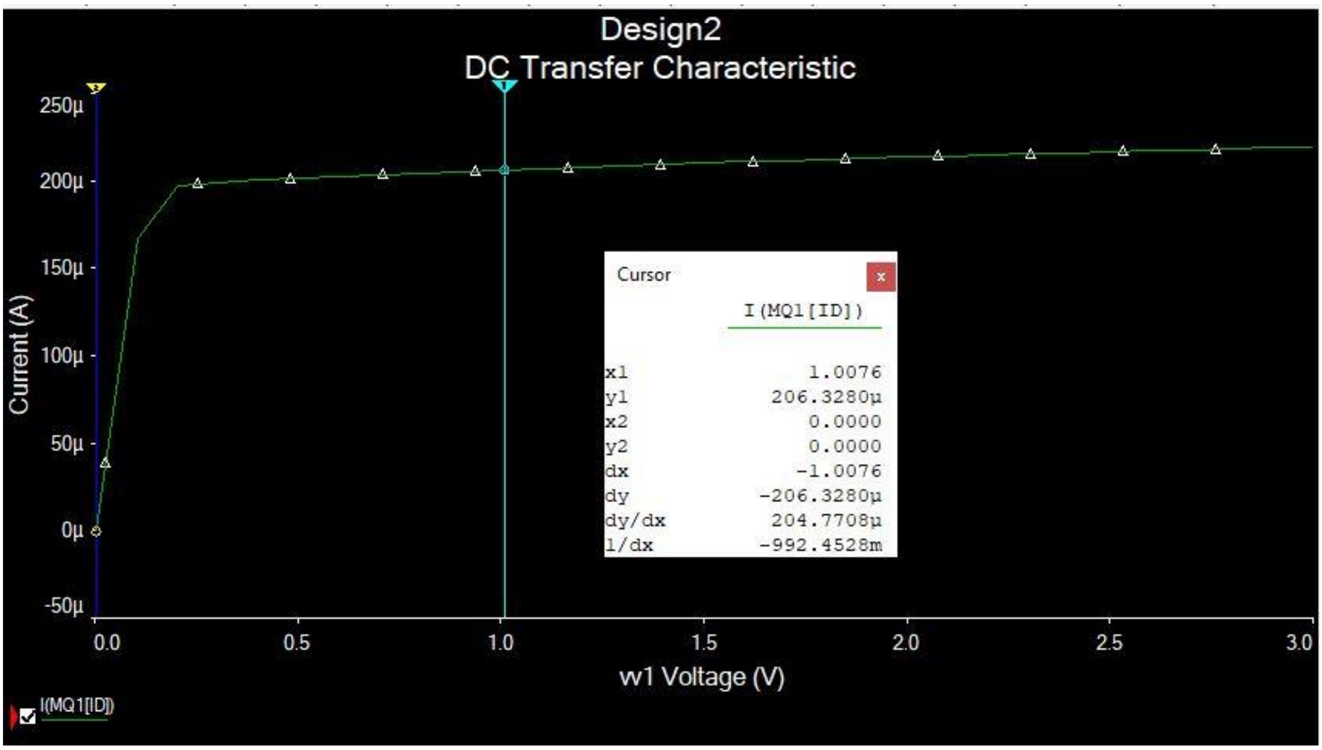
Vcompliance = Veff = 0.2V

Iout vs Vout



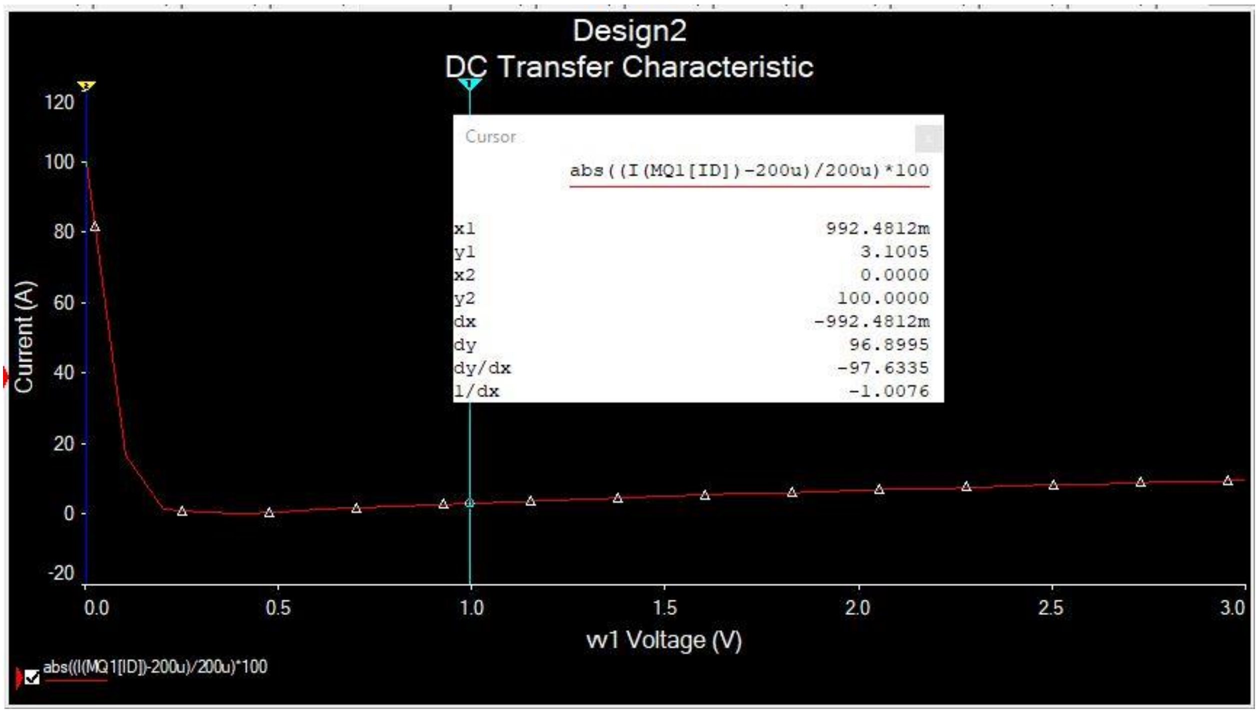
Vcompliance = 206mV. Close to analytical value.

Iout vs Vout (cursor at Vout = 1V)



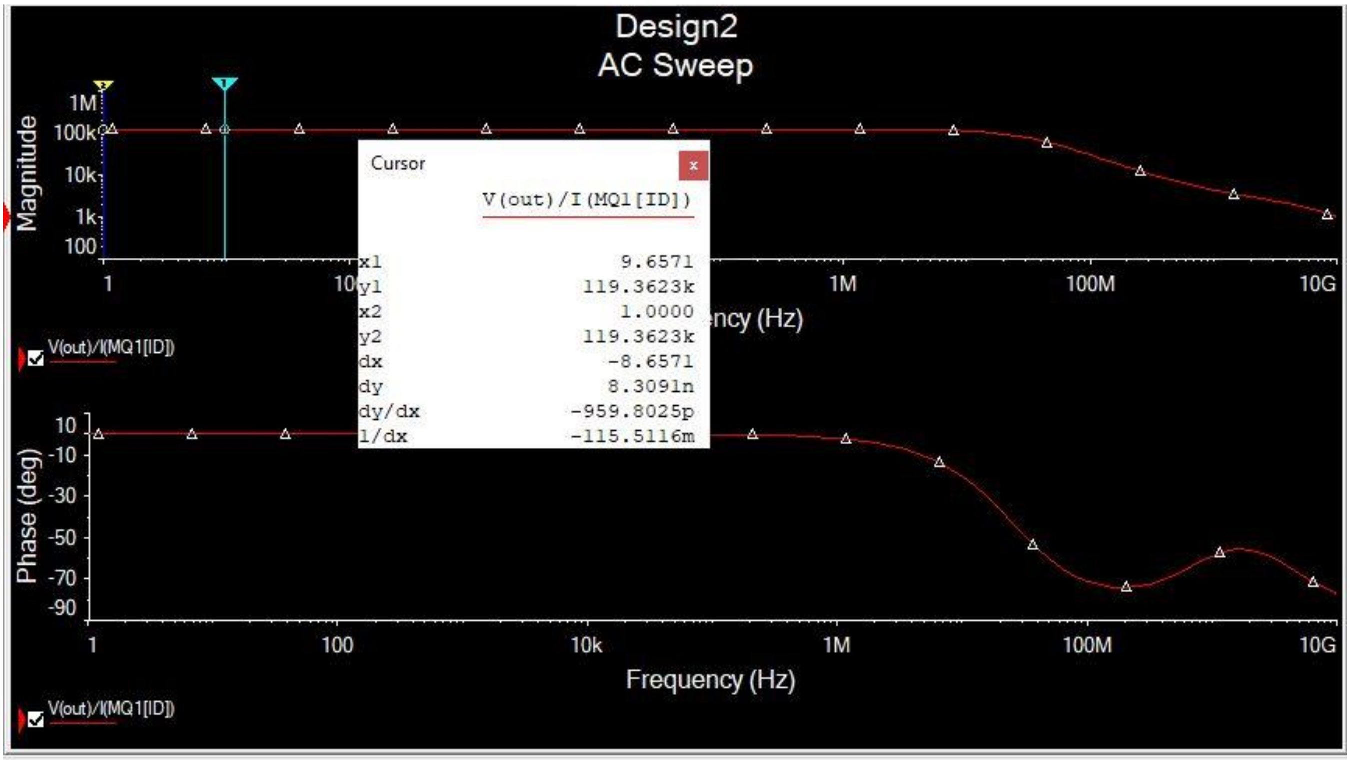
Error = ((206-200)/200) * 100= 3%

Percentage of Error graph of (Iout vs Vout) cursor at Vout = 1V



From the cursor, Error = 3.1%. This the same result obtained above.

Rout vs frequency



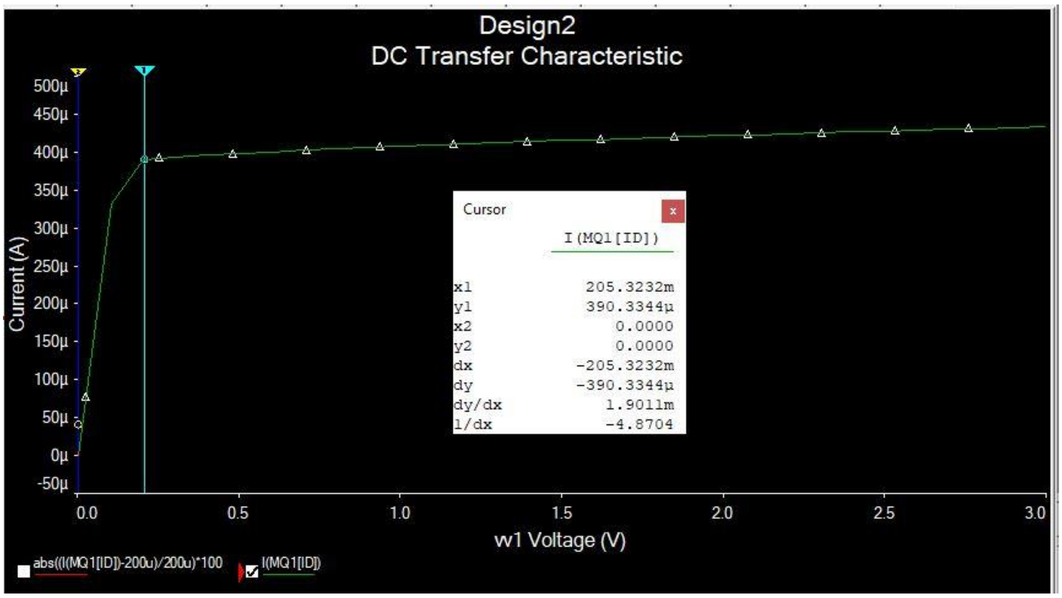
Rout = 119.4kohm

Repeat (a) for Iin=200µA and Iout=400µA. Veff should be kept at 0.2V.

Iin = 200uA, Iout = 400uA

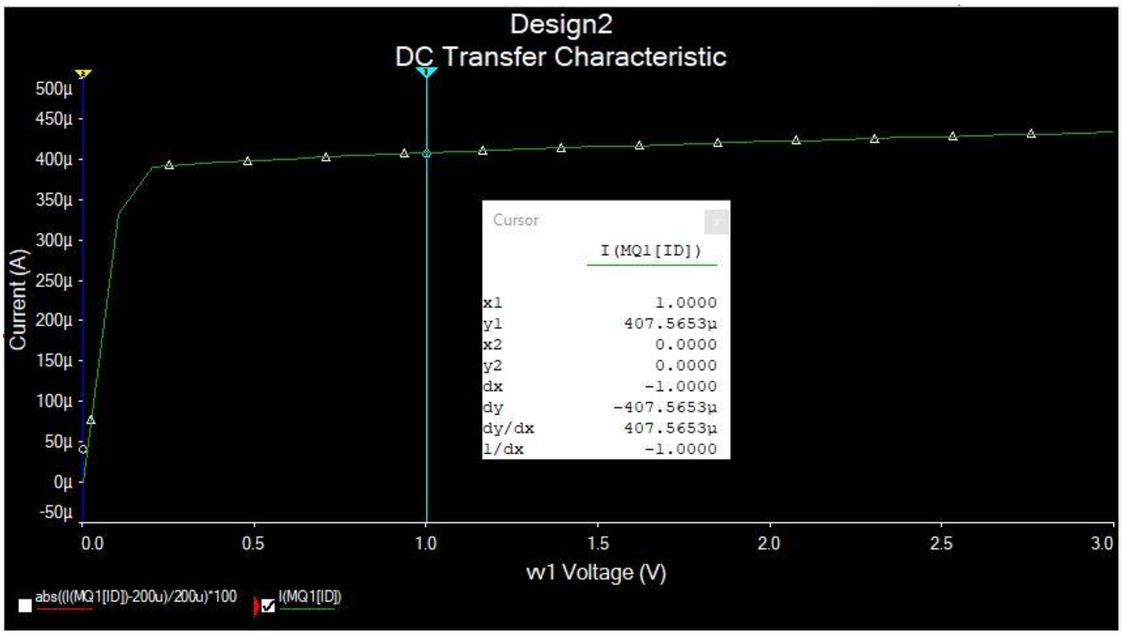
It is required to keep Veff at 0.2V. Since we double the current, we need to double the device width also. So W1 = 84um and W2 = 168um

Iout vs Vout



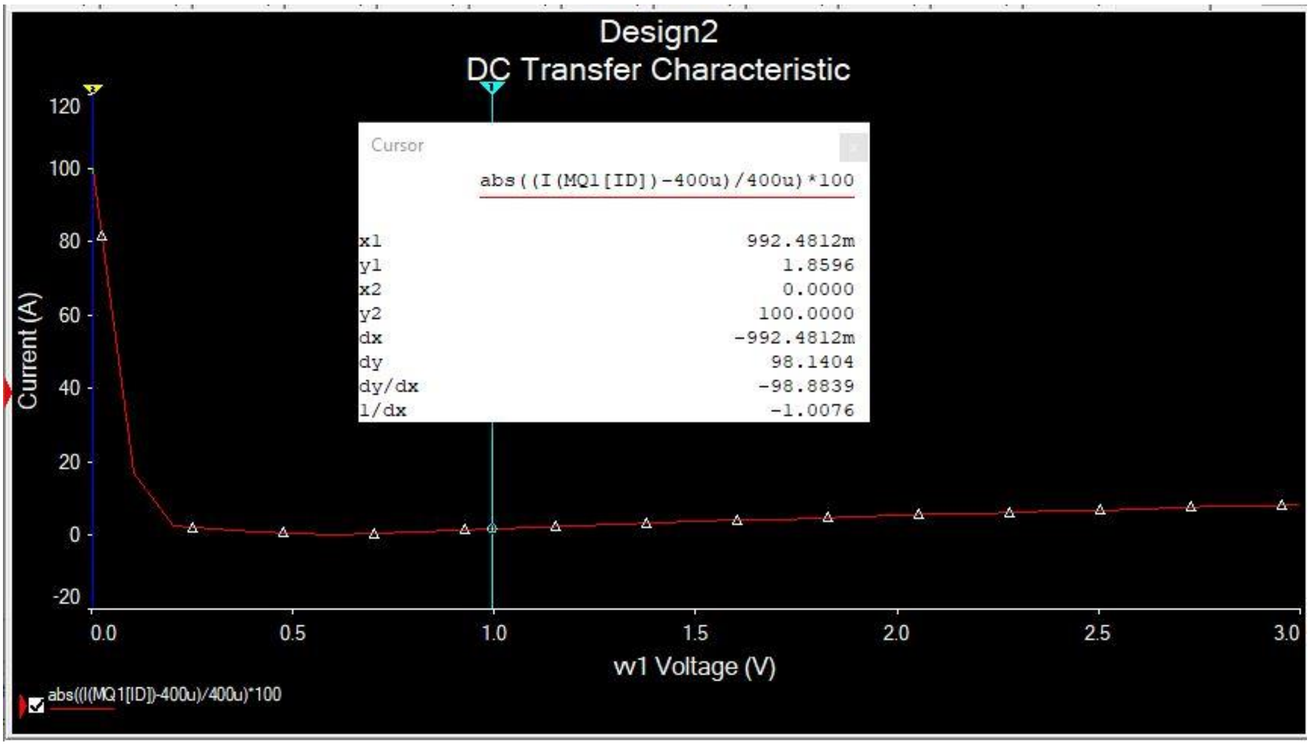
Vcompliance = 205mV

Iout vs Vout (cursor at Vout = 1V)



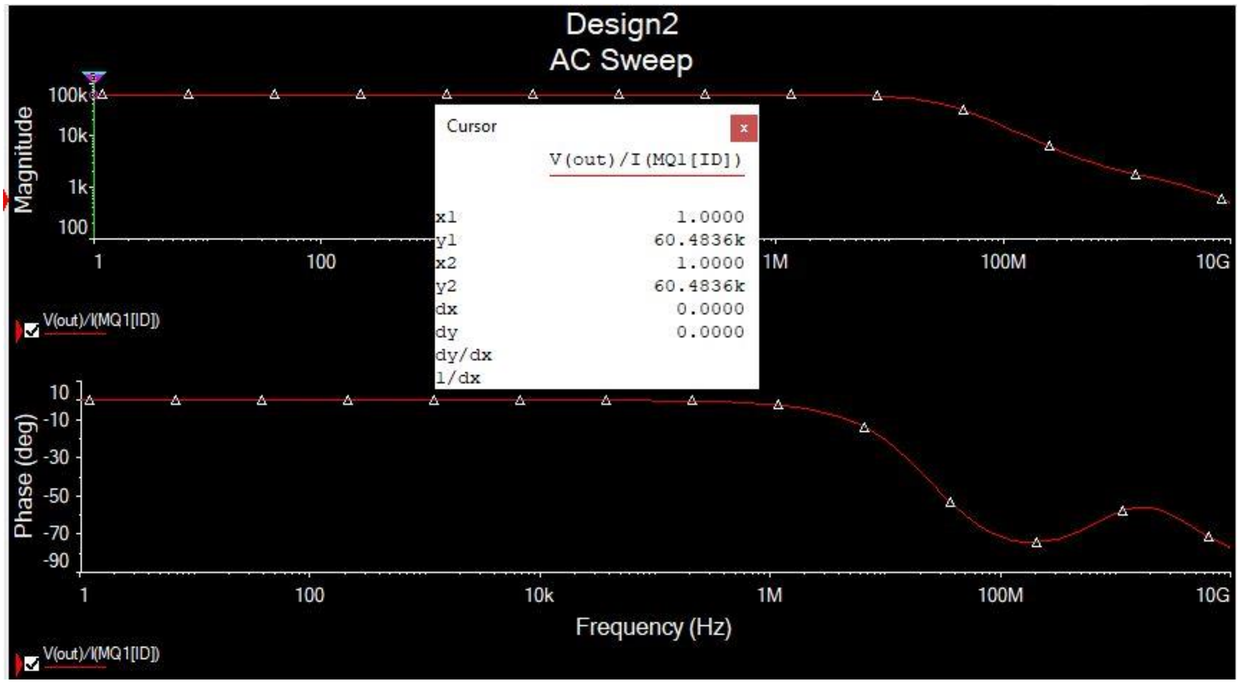
Error = ((407.56-400)/400) * 100= 1.8%

Percentage of Error graph of (Iout vs Vout) cursor at Vout = 1V



From the cursor, Error = 1.86%, Almost same Result obtained above

Rout vs frequency



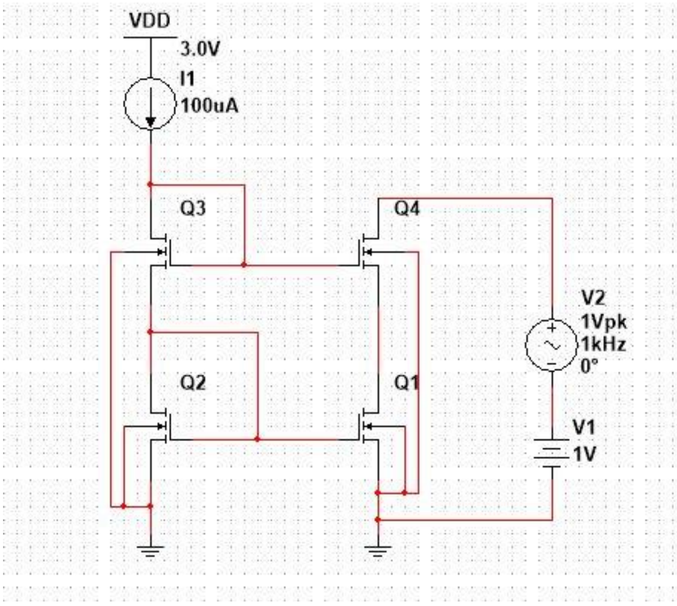
Rout = 60.5kohm.

As Iout is doubled, Rout is almost exactly halved.

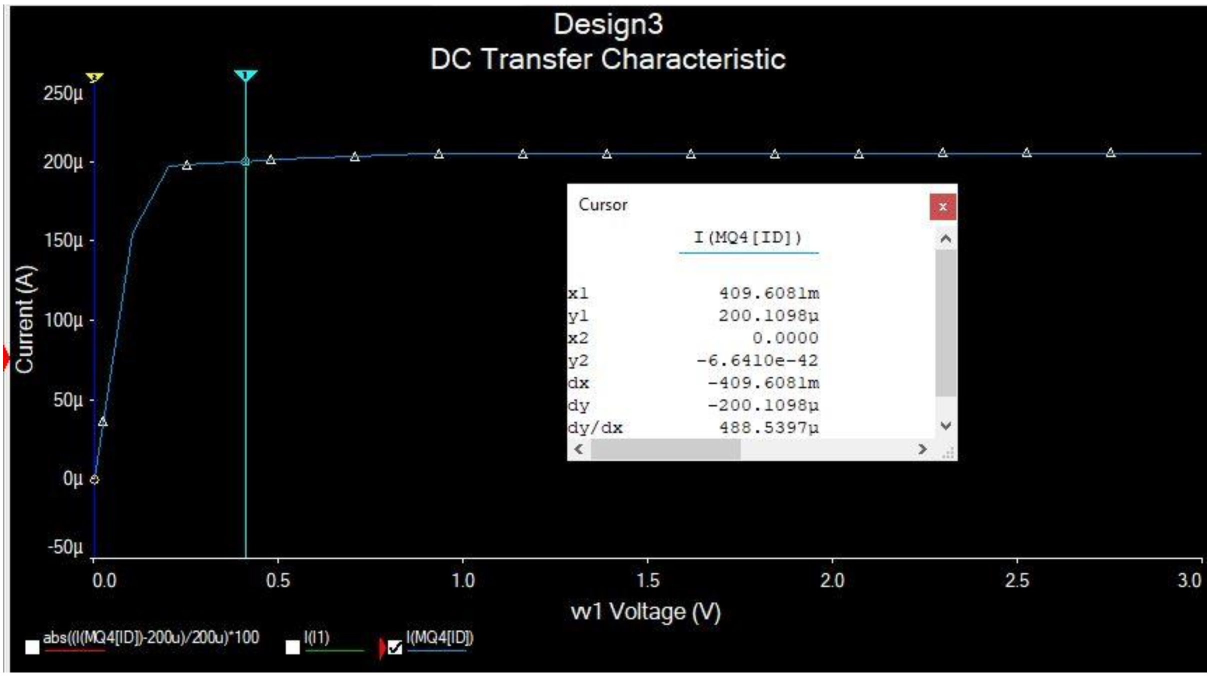
<u>(b) Use the same design from Fig. 2(a) to construct the cascode current mirror in Fig.2(b). Repeat the same simulations.</u>

Cascode Current Mirror

Circuit Schematic

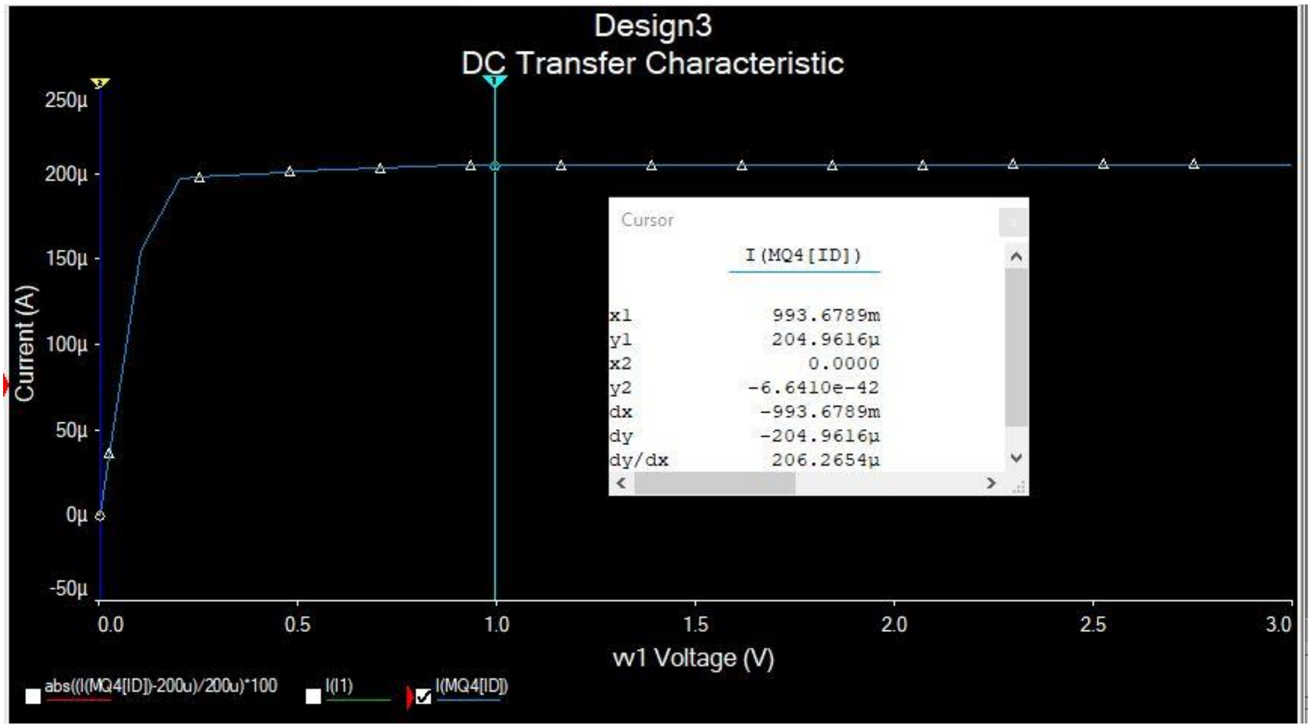


Iout vs Vout



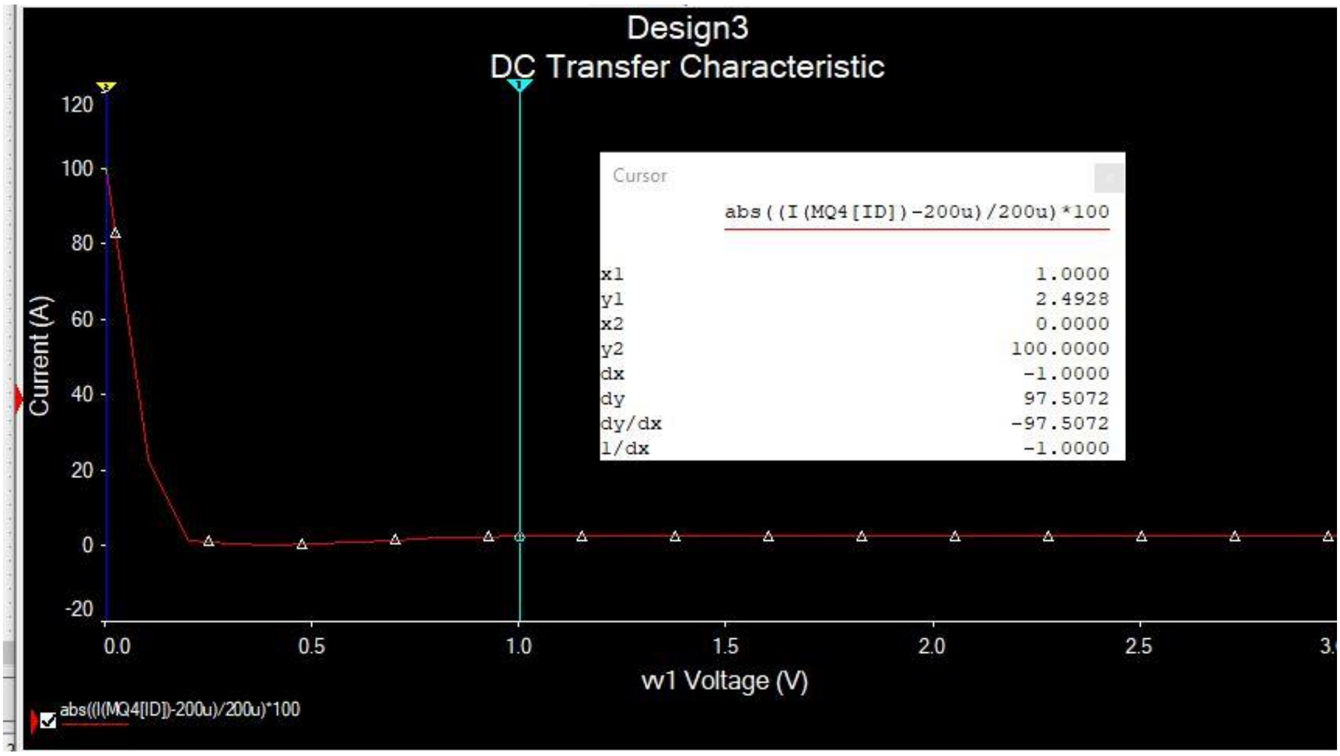
Vcompliance = 409mV

Iout vs Vout (cursor at Vout = 1V)



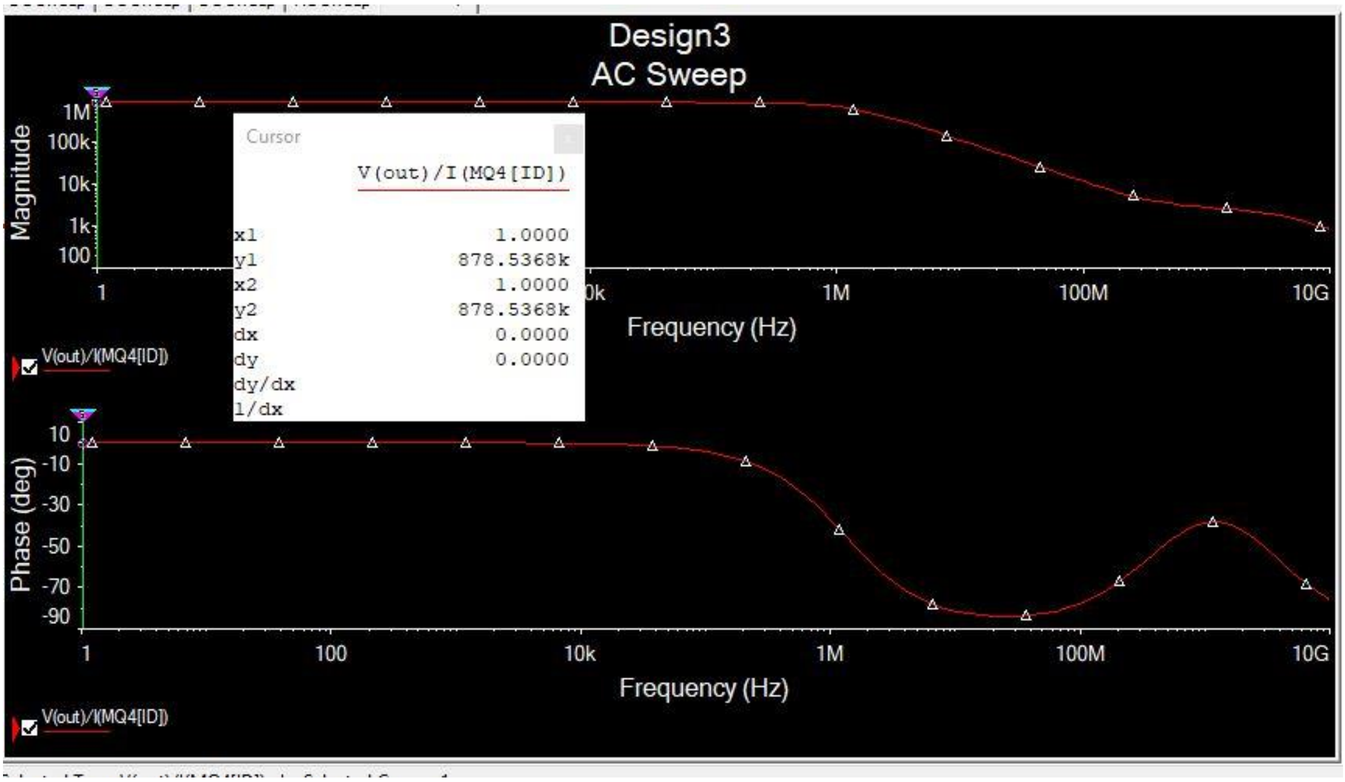
Error = ((205-200)/200) * 100= 2.5%, a slight decrease in the error compared to the normal current mirror

Percentage of Error graph of (Iout vs Vout) cursor at Vout = 1V



From the cursor, Error = 2.49%, Almost same Result obtained above.

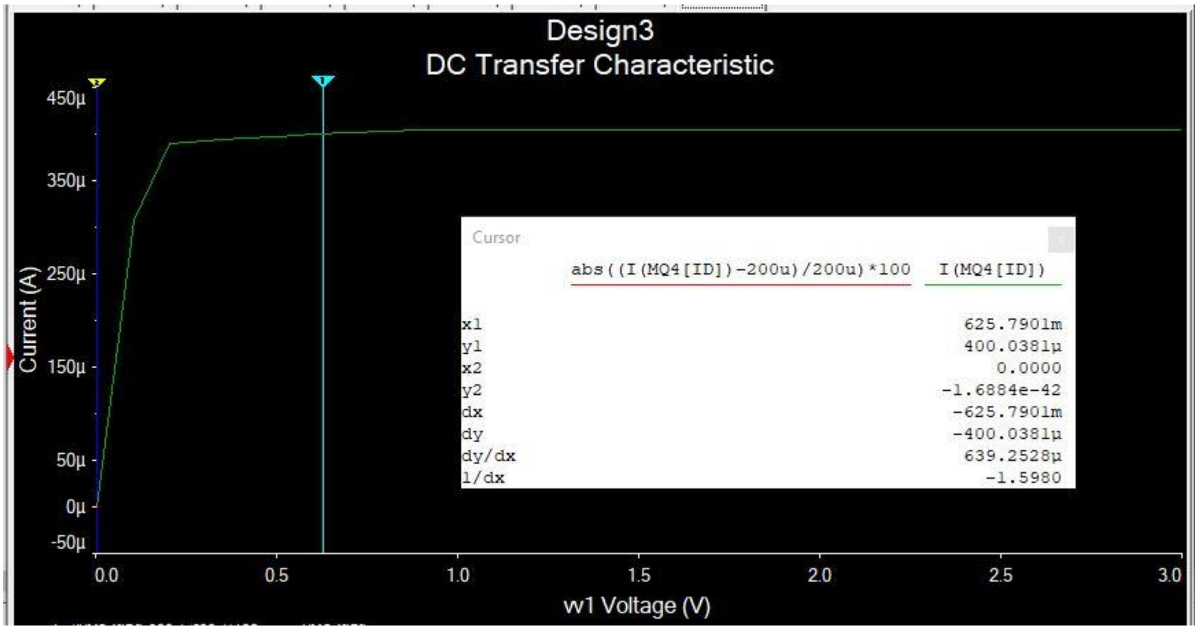
Rout vs frequency



Rout = 878.5kohm, which is a massive increase compared to the normal current mirror at the same conditions.

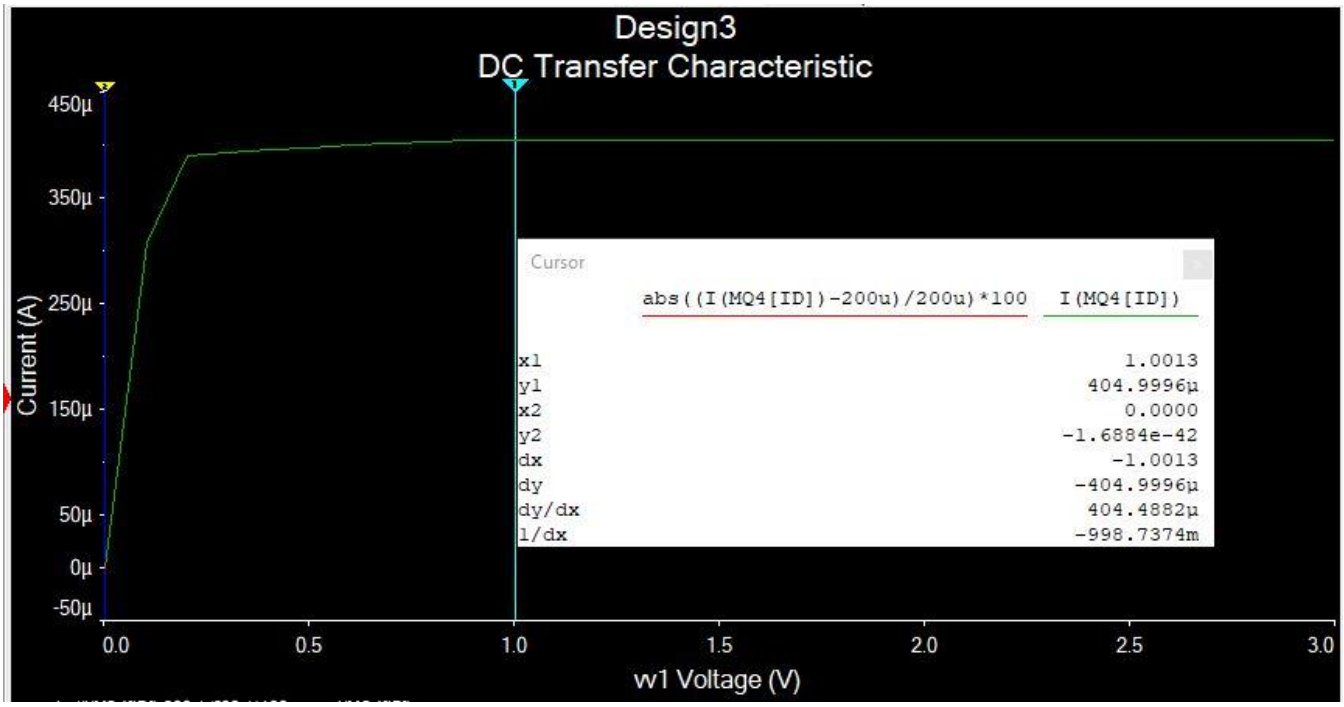
Iin = 200uA, Iout = 400uA

Iout vs Vout



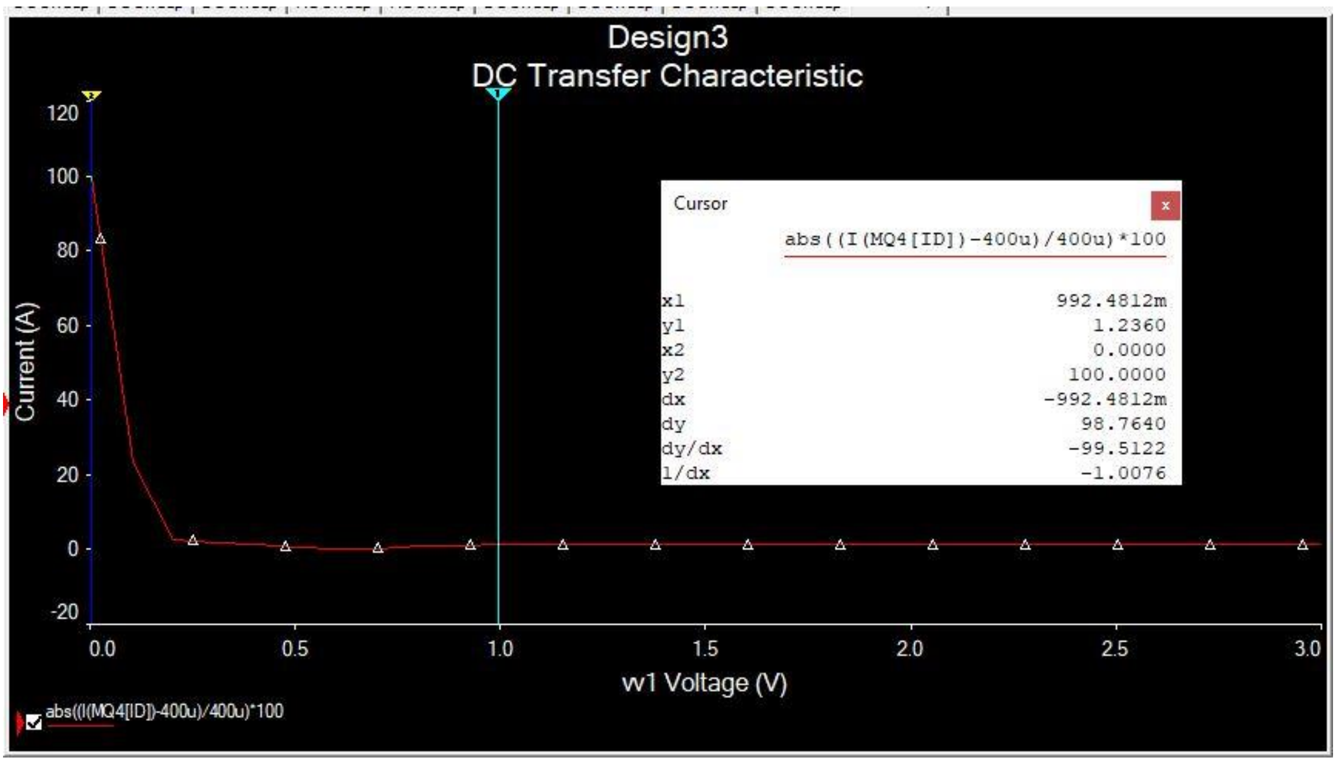
Vcompliance = 609mV

Iout vs Vout (cursor at Vout = 1V)



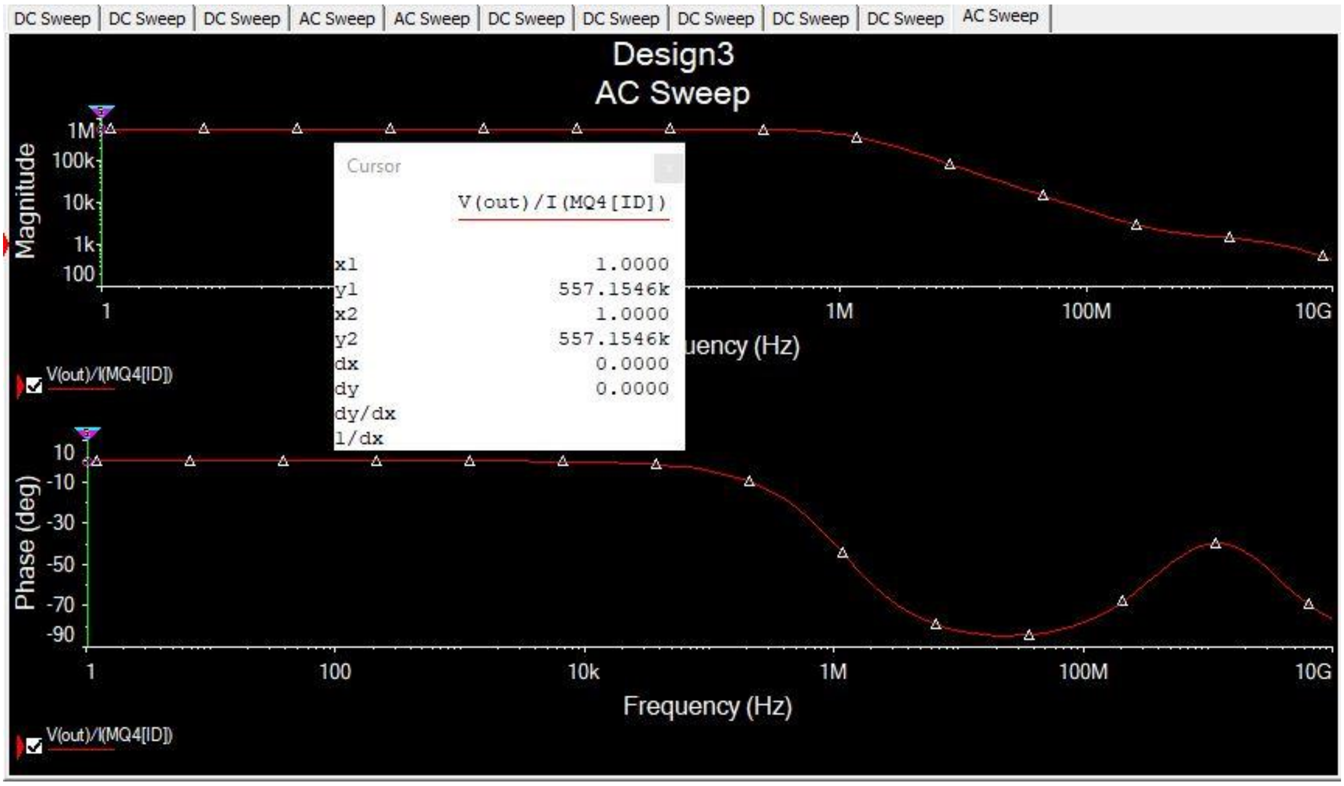
Error = ((405-400)/400) * 100= 1.25.5%, a slight decrase in the error compared to the normal current mirror.

Percentage of Error graph of (Iout vs Vout) cursor at Vout = 1V



From the cursor, Error = 1.24%, Almost same Result obtained above.

Rout vs frequency



Rout = 557kohm, which is a massive increase compared to the normal current mirror at the same conditions.

Compared to the cascode with Iin = 100uA, Iin=200uA decreases Rout quite a bit.

Performance Comparison

	Simple Current Mirror		Cascode Current Mirror	
Iin	100uA	200uA	100uA	200uA
Vcompliance	206mV	205mV	409mV	609mV
Error in Current (at 1V)	3.1%	1.86%	2.5%	1.25%
Rout	120 kohm	60 kohm	879 kohm	557 kohm

Note: 1V was taken as a reference value for measuring the error in the current, but any voltage beyond Vcompliance will show the same trend.

Discussion:

- Iout isn’t exactly equal to Iin. This can be due to ignoring the early effect or the differences in the VDS values, and more importantly in real life it is due to mismatches.
- As Iout is increases, Rout decreases.
- The cascode current mirror greatly boosts Rout, resulting in a much more reliable current mirror. This is demonstrated by the almost constant curve of Iout in the case of the cascode as opposed to the normal current mirror where Iout continues to increase as Vout increases. This was also demonstrated by the lower percentage errors in the currents.
- Generally, as Iout increases, the mismatching effect is less apparent, and the error decreases whether it is a cascode or a simple current mirror.
- The cascode current mirror, however, requires a larger compliance voltage for proper operation as a current mirror. This decreases the voltage headroom.
- For this reason, the cascode isn’t preferred in recent applications where the supply voltage is already low.