Information Technology Institute (ITI)

CMOS ANALOG IC DESIGN

LAB 3

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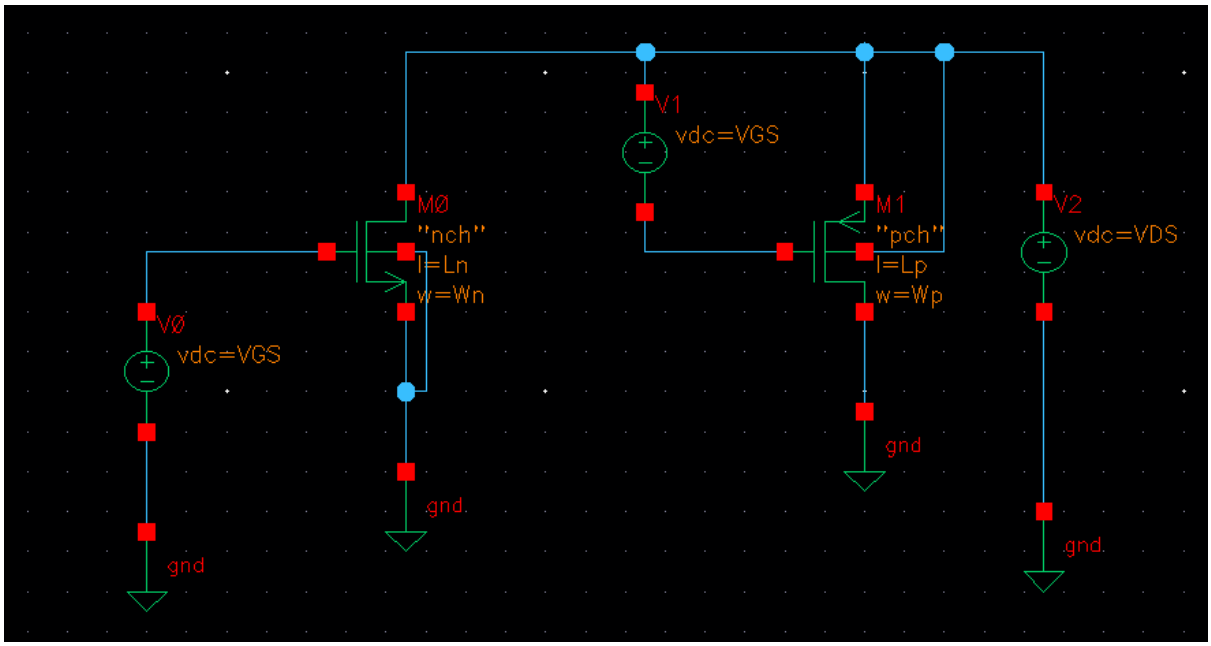
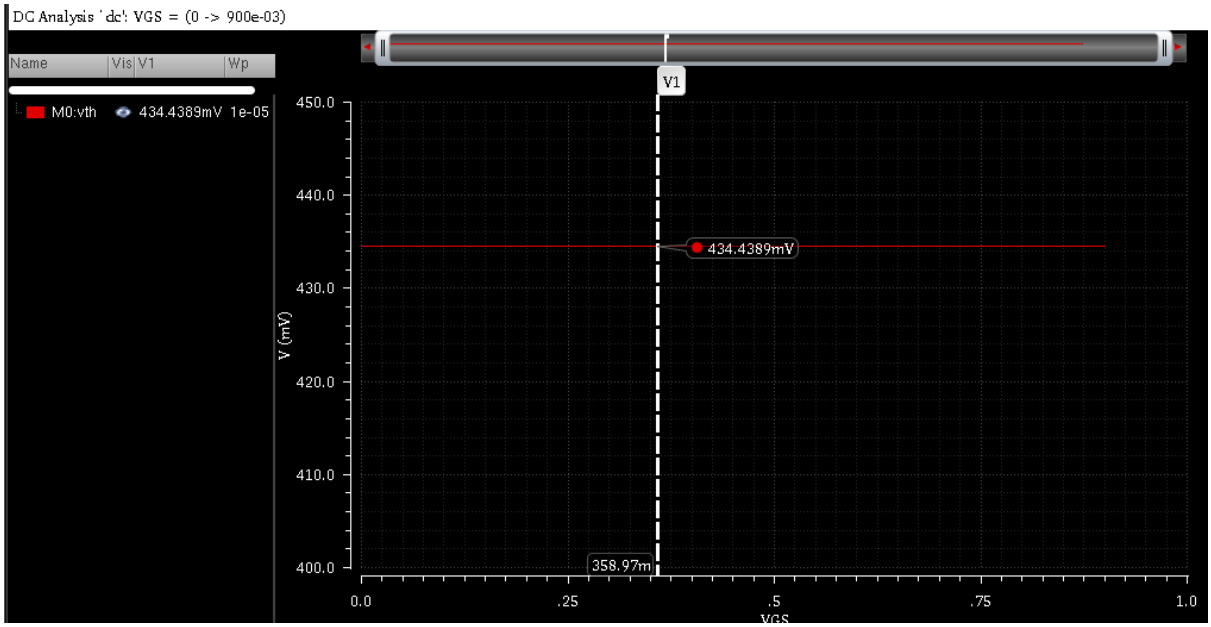
PART 1: Sizing Chart

The circuit schematic is shown

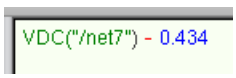


1), 2), 3) are satisfied

4) The value of VTH is shown = 0.434 V.



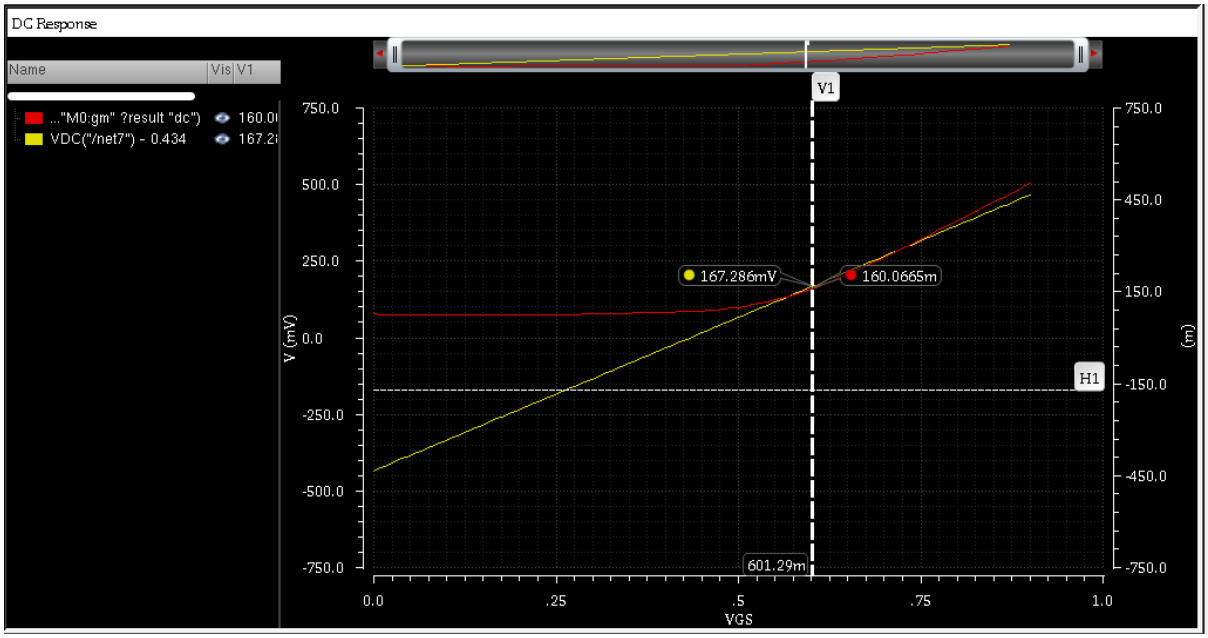
5) Calculator Expressions for V* and Vov



for Vov

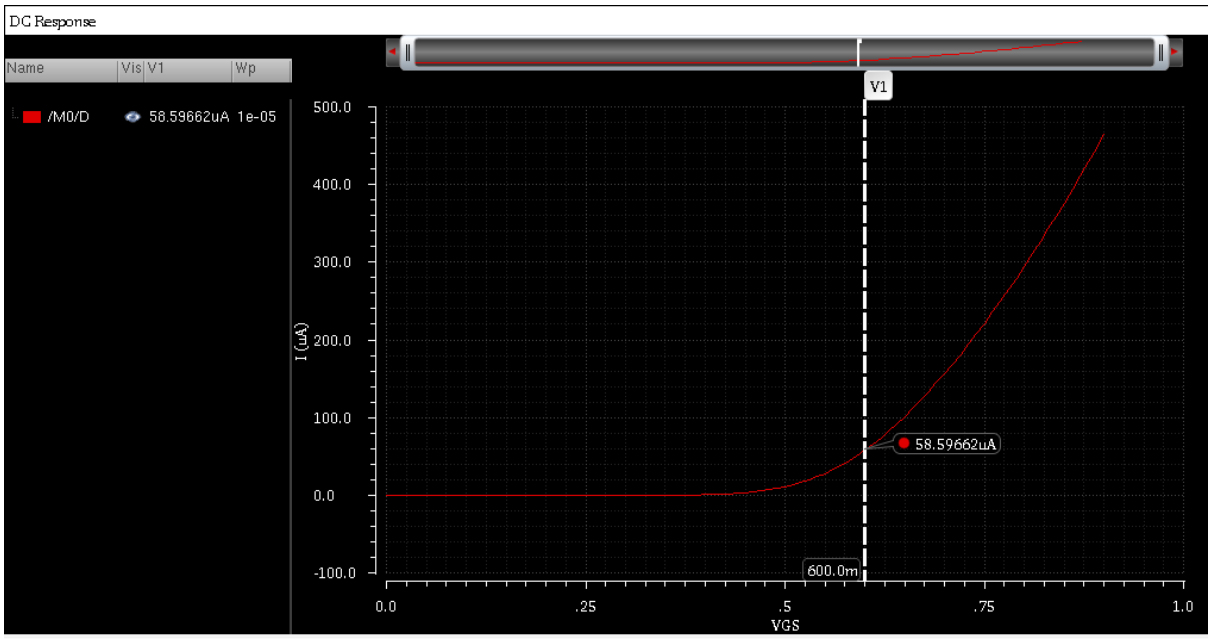
for V*

6) The plot of V* and Vov against VGS is shown



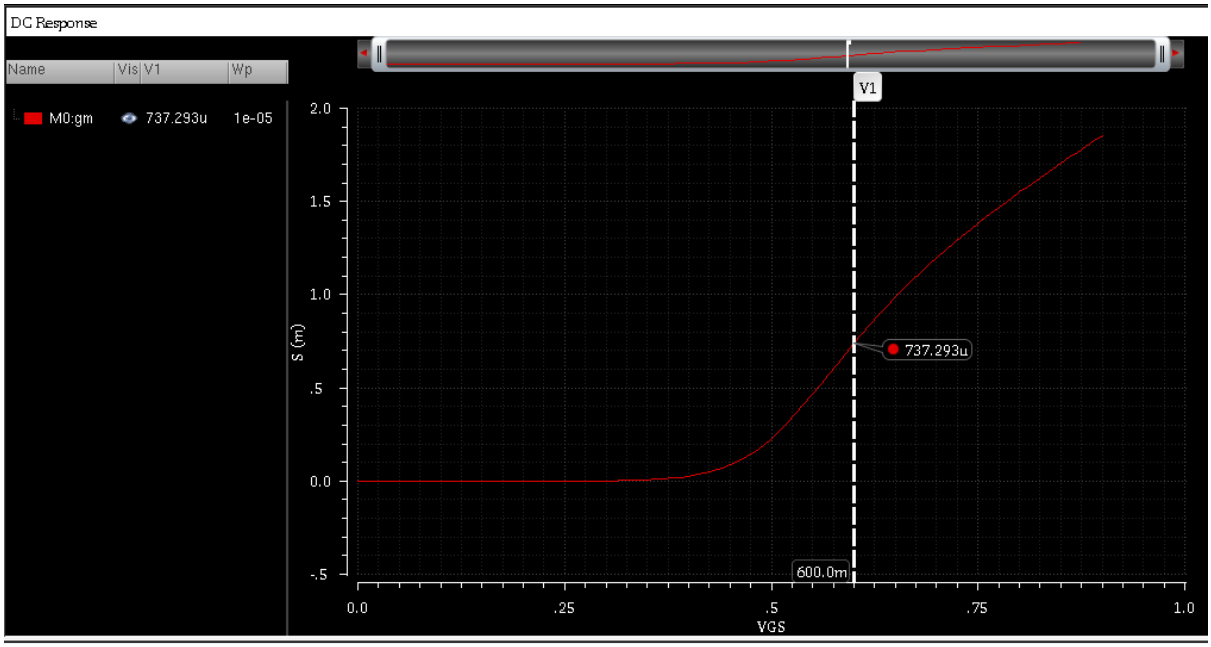
7) VovQ = 167.3, VGSQ = 0.6V @ V* = 160mV

8) IDX vs VGS



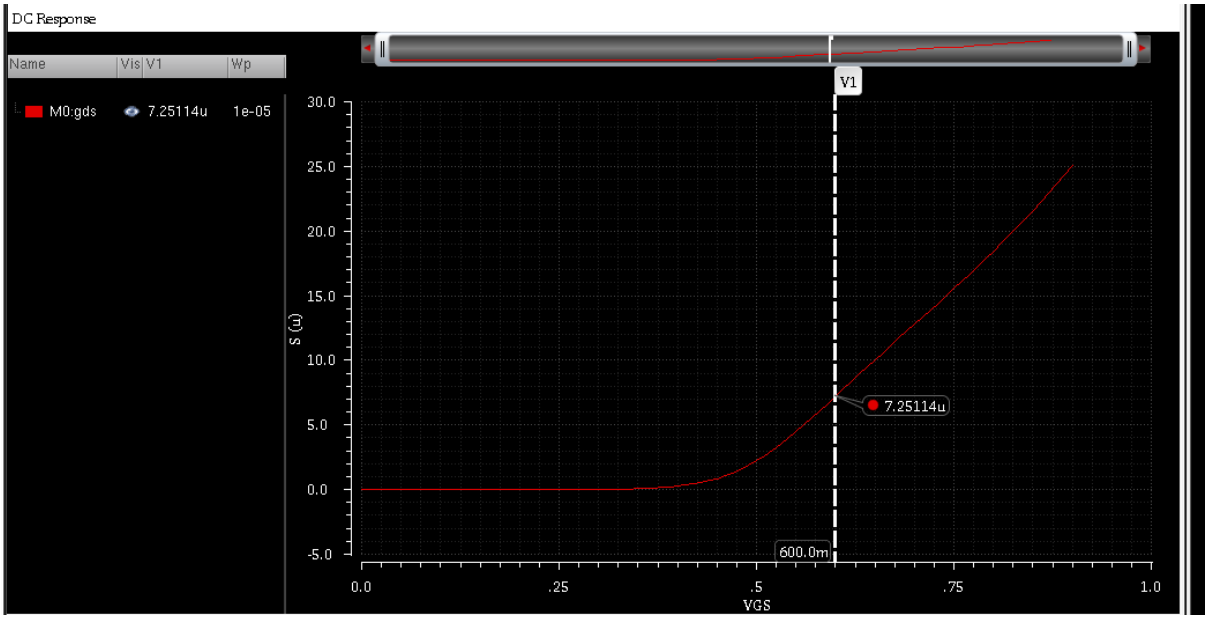
From the graph, IDQ* = 58.6 uA

gmX vs VGS



From the graph, gmQ* = 737.293uS

gdsX vs VGS



From the graph, gdsQ* = 7.25114uS

9) Wnew = IDQ * Wold / IDQ* = 15 * 10 / 58.6 = 2.56 um

10) By cross multiplication:

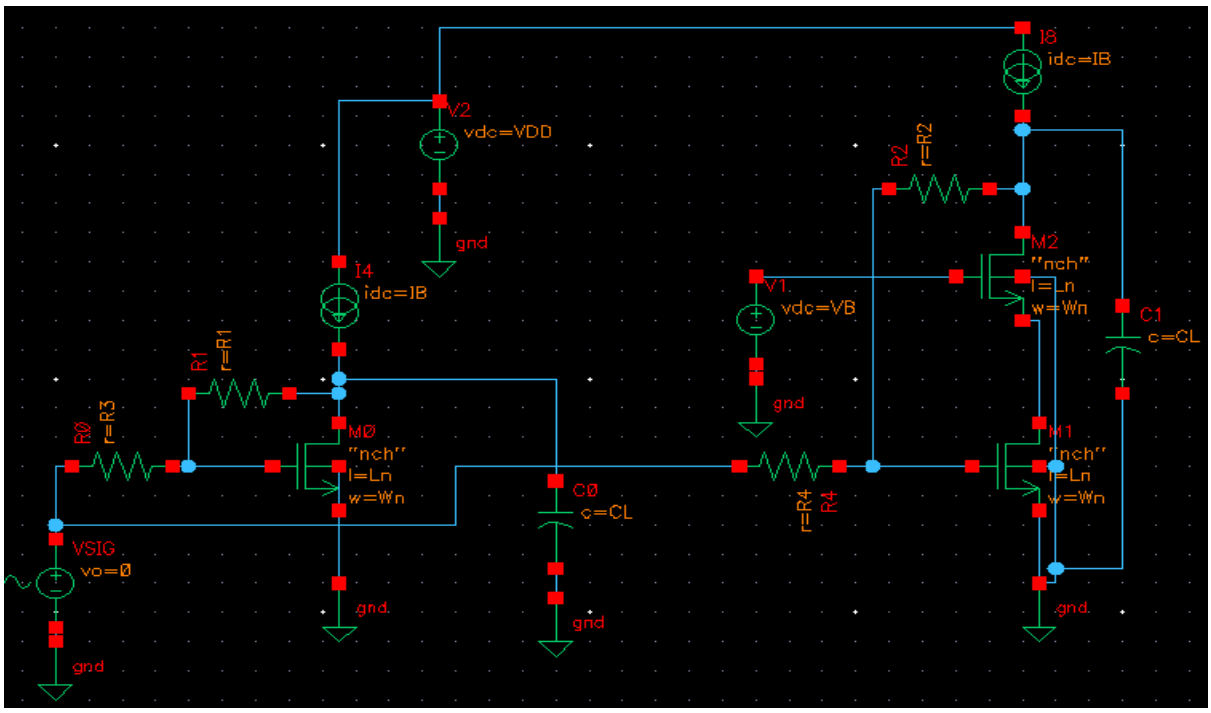
gmQ = gmQ* Wold / Wnew = 737.293uS * 2.56um / 10um = 188.7uS

gdsQ = gdsQ* Wold / Wnew = 7.25114uS * 2.56um / 10um = 1.856uS

PART 2: Cascode for Gain

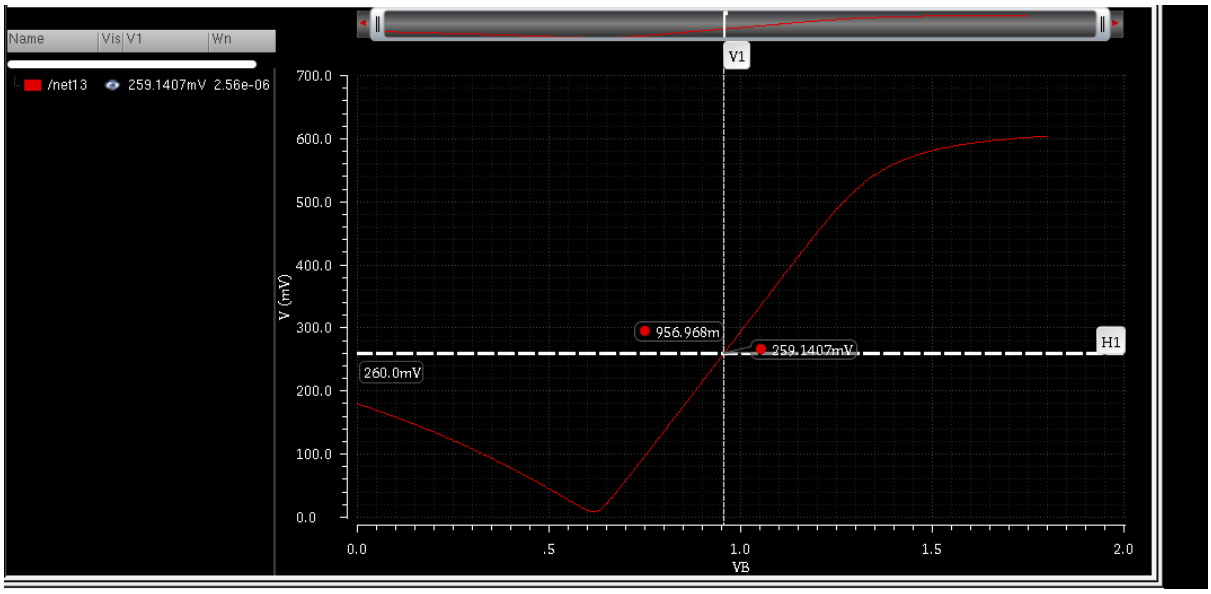
1. OP Analysis

1) The circuit schematic is shown



The specified parameters were assigned.

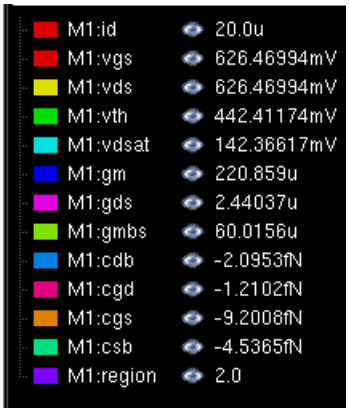
2) A sweep over VB was performed. The plot of VDS vs VB is shown. At the point where VDS = V* + 100mv = (160 + 100) mV = 260 mV, the value of VB is recorded and it equals 956.968 mV, which approximates to VB = 0.957V



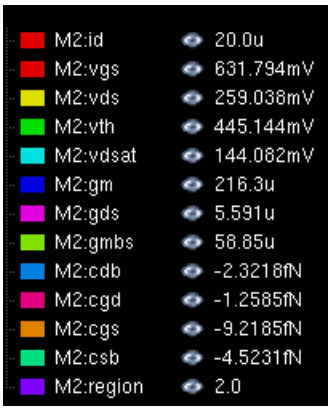
3) The appropriate values for resistances were set. Requirement satisfied.

4) The required parameters are shown.

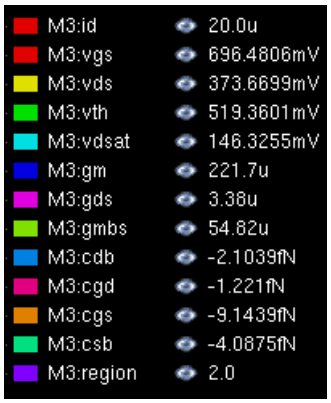
For M1



For M2



For M3



5) For M1, M2, and M3 VDS > VGS – VTH, hence all transistors are in saturation. This is also signified by all transistors being in region 2.

6) No, not all transistors have the same VTH. This is

7) For all transistors, gm > gds. In fact, gm >> gds.

8) For all transistors, gm > gmb.

9) For all transistors, cgs < cgd, but |cgs| >> |cgd|.

10) For all transistors, csb < cdb, but |csb| > |cgd|.

2. AC Analysis

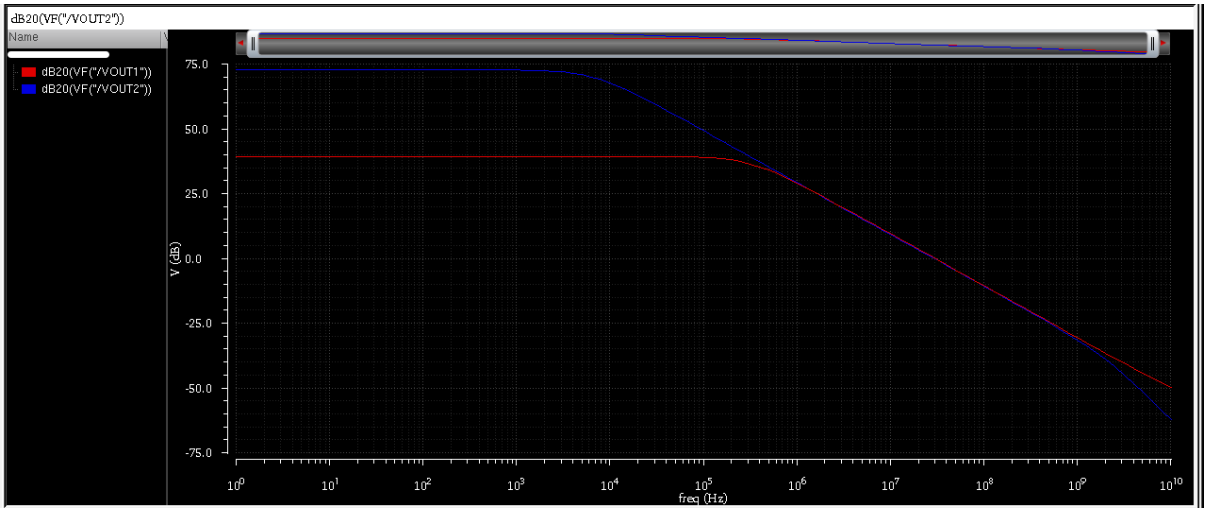
1) Simulation parameters are set as required. Satisfied.

2) The required expressions were calculated and exported to adexl as shown.

The calculated values are also shown to the right

Test	Output	Nominal	Spec	Weight	Pass/Fail
lab1:lab3_part2:1	dB20(VF("/VOUT1"))				
lab1:lab3_part2:1	ymax(dB20(VF("/VOUT1")))	39.3			
lab1:lab3_part2:1	ymax(mag(VF("/VOUT1")))	92.24			
lab1:lab3_part2:1	bandwidth(VF("/VOUT1") 3 "low")	323.9k			
lab1:lab3_part2:1	gainBwProd(VF("/VOUT1"))	29.95M			
lab1:lab3_part2:1	dB20(VF("/VOUT2"))				
lab1:lab3_part2:1	ymax(dB20(VF("/VOUT2")))	72.57			
lab1:lab3_part2:1	ymax(mag(VF("/VOUT2")))	4.253k			
lab1:lab3_part2:1	bandwidth(VF("/VOUT2") 3 "low")	6.846k			
lab1:lab3_part2:1	gainBwProd(VF("/VOUT2"))	29.19M			
lab1:lab3_part2:1	unityGainFreq(VF("/VOUT1"))	30.18M			
lab1:lab3_part2:1	unityGainFreq(VF("/VOUT2"))	29.44M			

3) The Bode Plot of CS (red) and Cascode (blue) are shown, overlaid.



4) As per the lab announcement, this part is not required anymore.

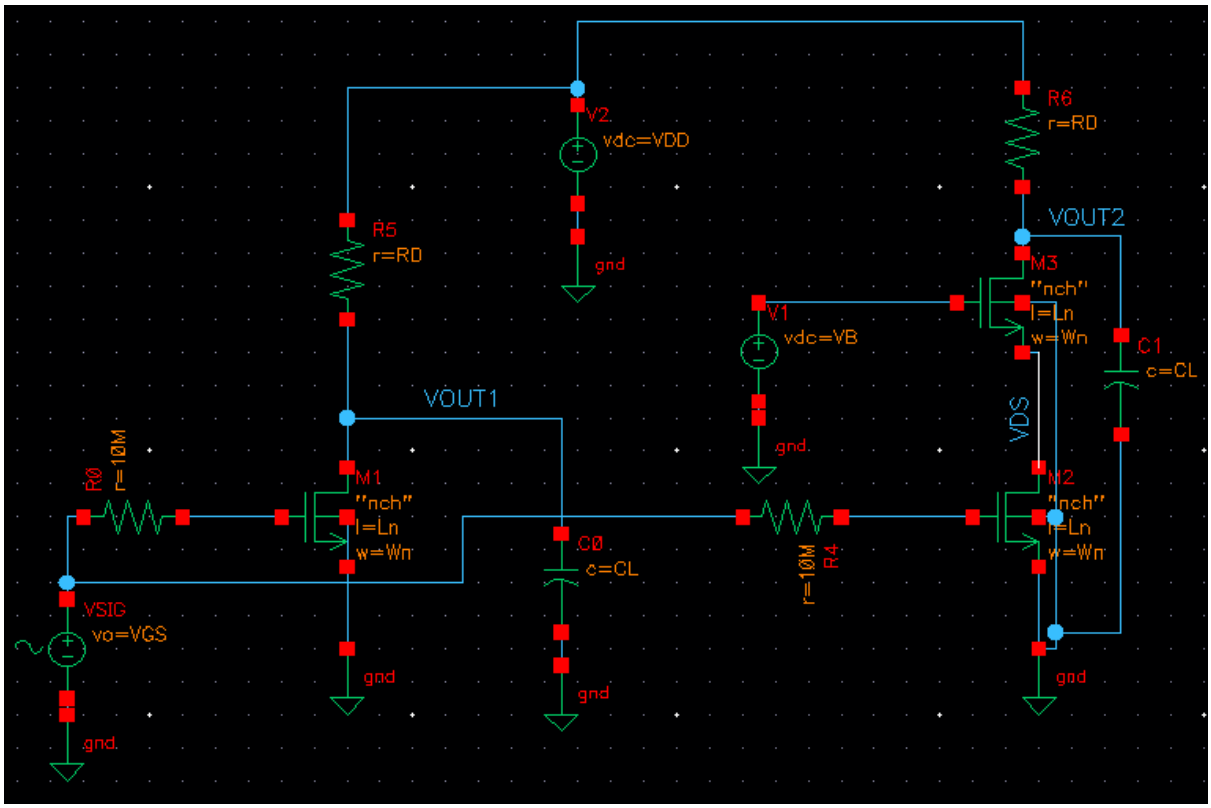
5) As per the lab announcement, this part is not required anymore.

6) The cascade amplifier has a lower BW. This is due to its higher Rout which comes at the expense of the BW. However, as we would expect, the cascade amplifier has a higher gain. Also, the gainBWProd are very close, which signifies that both amplifiers have a similar value of maximum frequency at which they can operate.

[optional] PART 3: Cascode for BW

1. OP Analysis

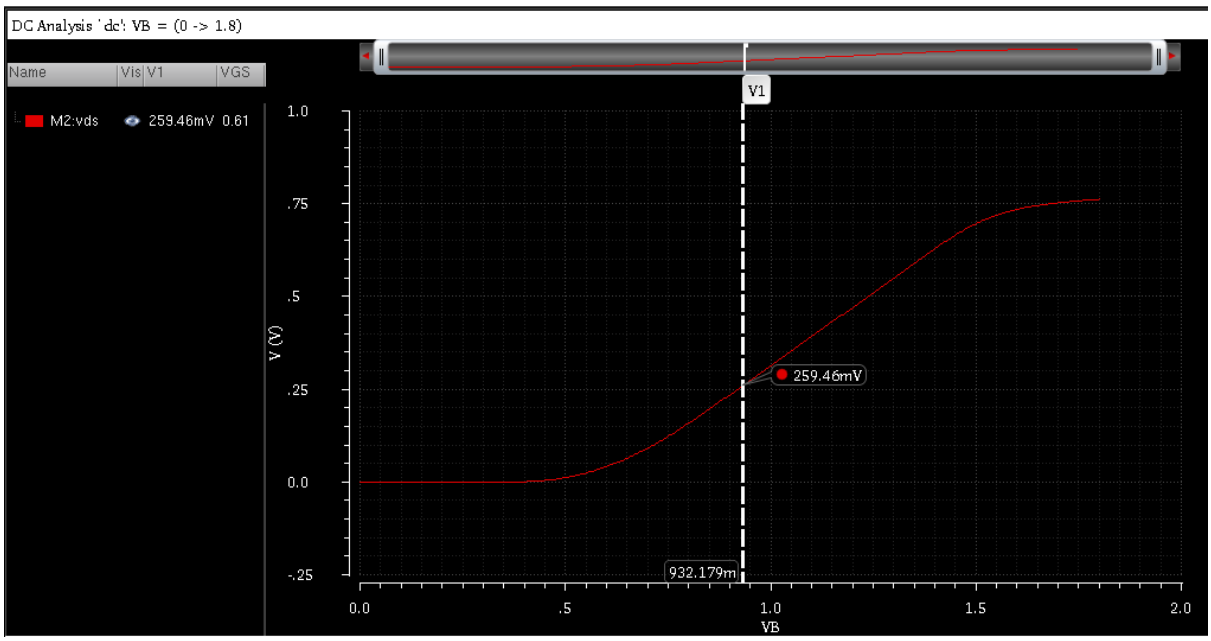
1)The modified schematic is shown



2) RD = VRD / ID = (VDD/2) / 15uA = (1.8/2)/15uA = 60k ohms

3) Noted.

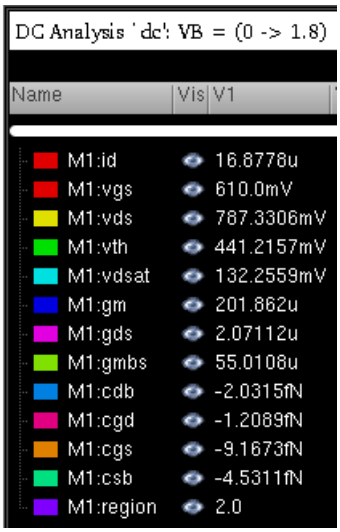
4) A sweep of VDS against VB is performed to select a suitable value for VB.



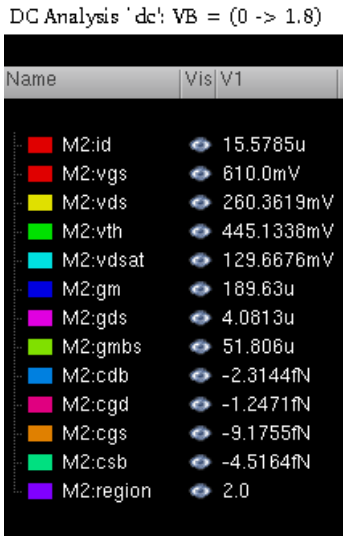
At VDS = V* + 100mV = 260mV, VB = 0.932 V, approximately.

The required parameters are shown.

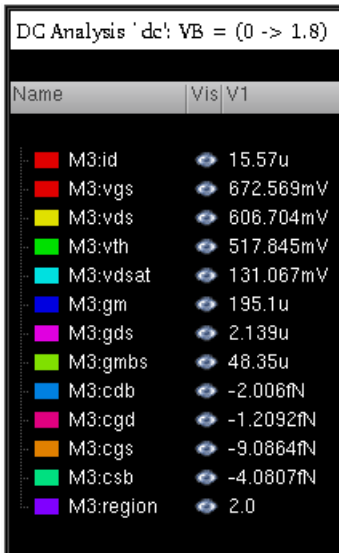
For M1



For M2



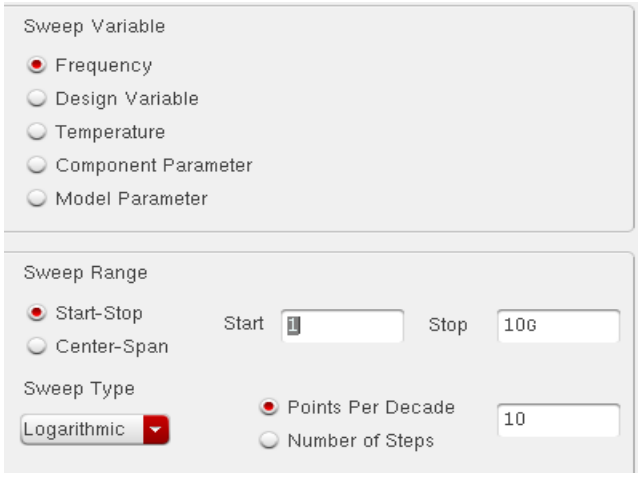
For M3



5) For M1, M2, and M3 VDS > VGS – VTH, hence all transistors are in saturation. This is also signified by all transistors being in region 2.

2.AC Analysis

1) AC simulation parameters are set as required.

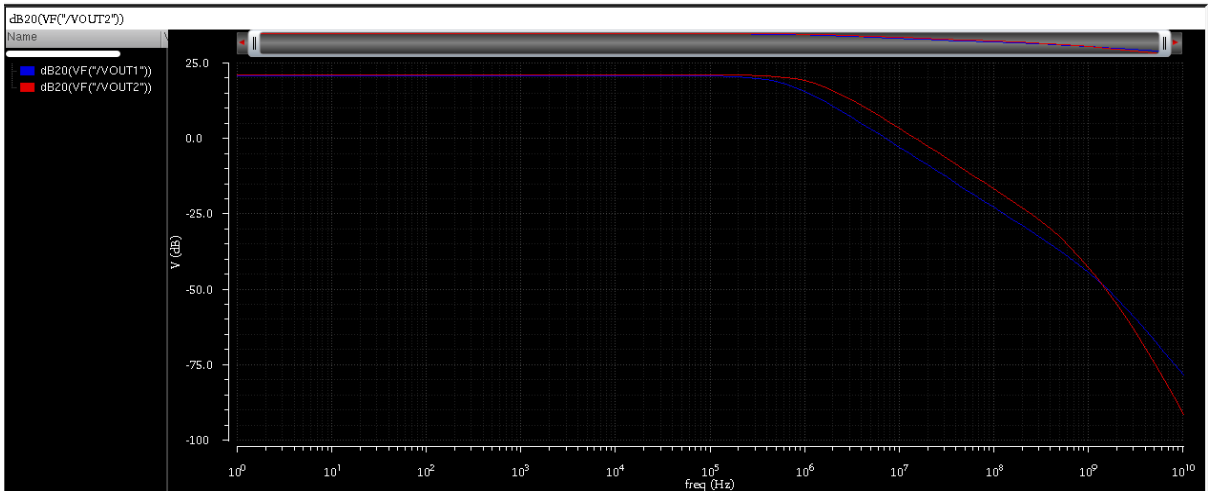


2) Calculator Expressions are shown, and the values are shown into the right.

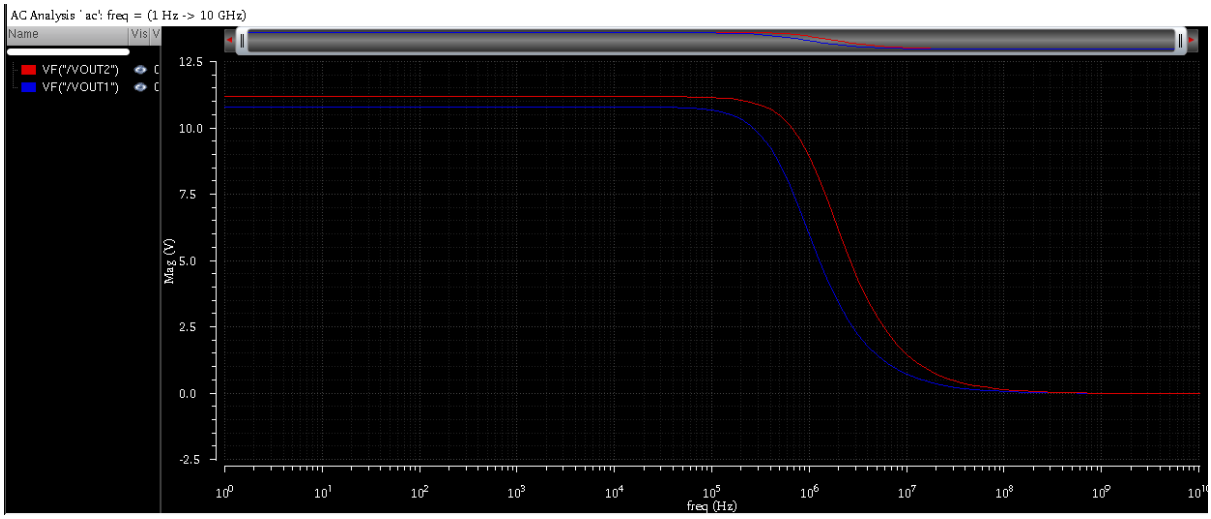
Test	Output	Nominal	Spec	Weight	Pass/Fail
lab1:lab3part2number3:1	dB20(VF("/VOUT1"))				
lab1:lab3part2number3:1	ymax(dB20(VF("/VOUT1")))	20.65			
lab1:lab3part2number3:1	mag(VF("/VOUT1"))				
lab1:lab3part2number3:1	ymax(mag(VF("/VOUT1")))	10.77			
lab1:lab3part2number3:1	bandwidth(VF("/VOUT1") 3 "low")	664k			
lab1:lab3part2number3:1	gainBwProd(VF("/VOUT1"))	7.17M			
lab1:lab3part2number3:1	unityGainFreq(VF("/VOUT1"))	7.213M			
lab1:lab3part2number3:1	dB20(VF("/VOUT2"))				
lab1:lab3part2number3:1	ymax(dB20(VF("/VOUT2")))	20.96			
lab1:lab3part2number3:1	mag(VF("/VOUT2"))				
lab1:lab3part2number3:1	bandwidth(VF("/VOUT2") 3 "low")	1.322M			
lab1:lab3part2number3:1	gainBwProd(VF("/VOUT2"))	14.79M			
lab1:lab3part2number3:1	unityGainFreq(VF("/VOUT2"))	14.85M			

3) The bode plots of the CS(blue) and the cascade(red) are shown.

db20



Magnitude



4)As per the lab announcement, this part is not required anymore.

5) As per the lab announcement, this part is not required anymore.

Additional Insights:

As we replaced the current sources with resistances, the value of Rout decreases, and hence a lower gain for both amplifiers.

Comparing to part 2, as a result of the omission of the feedback resistance, the BW increased, which is the target of this requirement. That was a tradeoff with the gain, which decreased.