University of Central Florida

Department of Computer Science

CDA 5106: Fall 2020

Machine Problem 1: Cache Design, Memory Hierarchy Design

by

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Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

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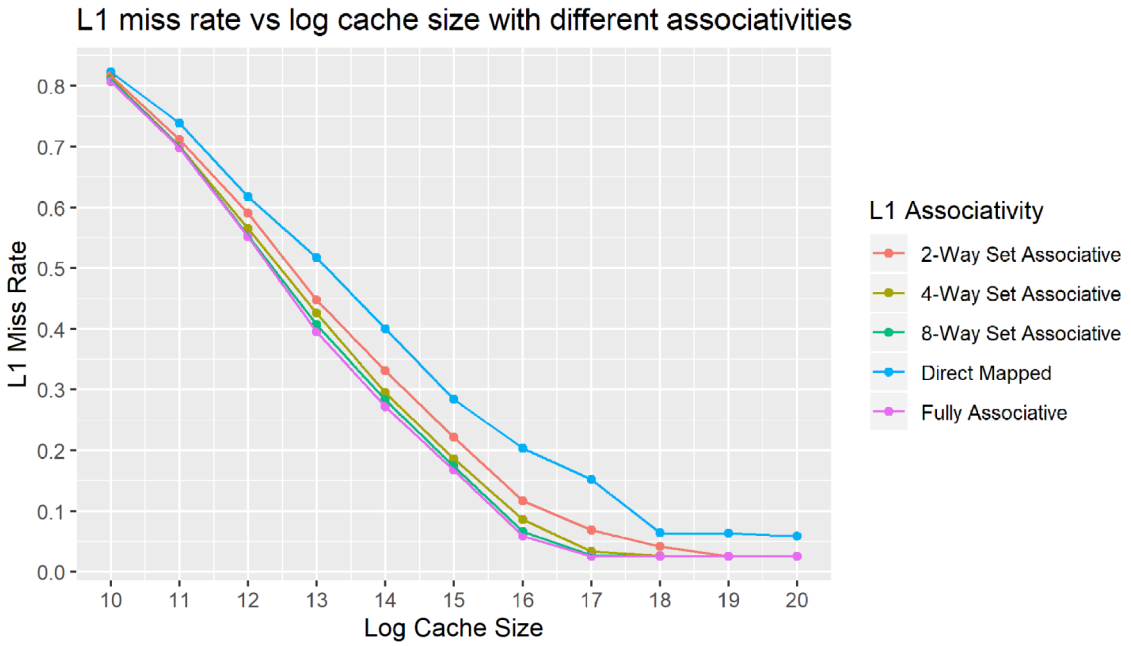
(sign by typing your name)

Graph1



1. For a given associativity, increasing cache size reduces the miss rate up to a point (2^18 bytes in our case), at which point miss rate remains mostly the same and becomes unaffected by further cache size increases.
For a given cache size, increasing associativity, reduces the miss rate. This is expected since higher associativity don't suffer as much from conflict misses as lower associativity.
For small cache sizes capacity misses outweighs the effects of conflict misses due to associativity, so we see that the curves almost start from the same miss rate and then diverge for mid size caches. When cache size gets larger, the effect of compulsory misses outweigh the effects of conflict misses, so the curves converge again, except for direct mapped, since it's most heavily effected by conflict misses.

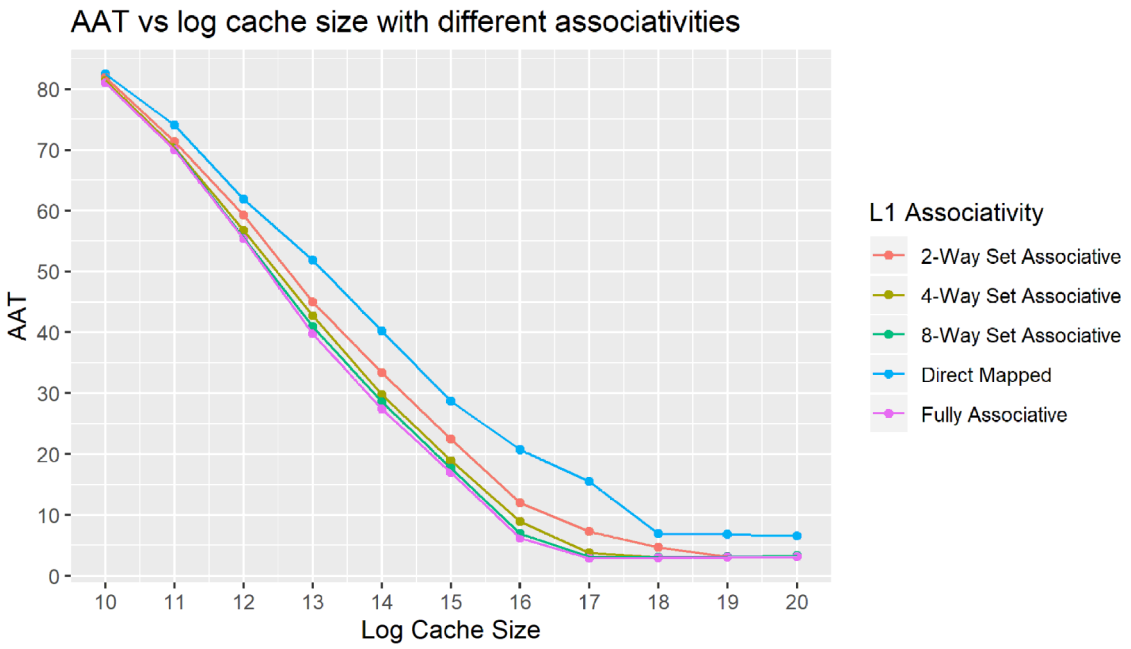
2. Since compulsory miss rate is unchanged under cache size and associativity changes, we can estimate it from the flat part at the end of fully associative curve. We select fully associative curve because it's also unaffected by associativity changes. We can estimate compulsory miss rate to be about 0.02582.

3. Since fully associative cache does not suffer from conflict miss, any increase above its curve is mostly due to conflict miss for lower associativity. As we discussed above, the effect of conflict miss is more pronounced for mid-sized caches, so we take the maximum difference between an n-way set associative and fully associative as an estimate of conflict miss rate for the n-way associative. Table 1 shows the results.

Associativity	Conflict Miss Rate
Direct Mapped	0.14497
2-Way Set Associative	0.05912
4-Way Set Associative	0.03009
8-Way Set Associative	0.01156
Fully Associative	0

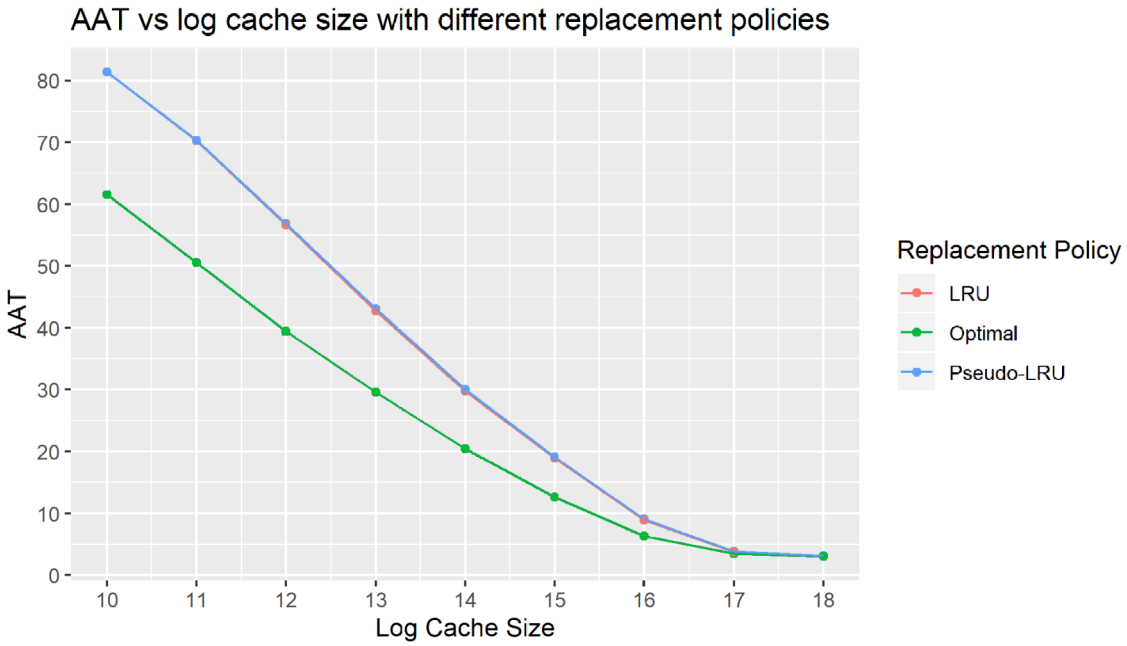
Table 1. Conflict miss rate for different cache associativity

Graph 2



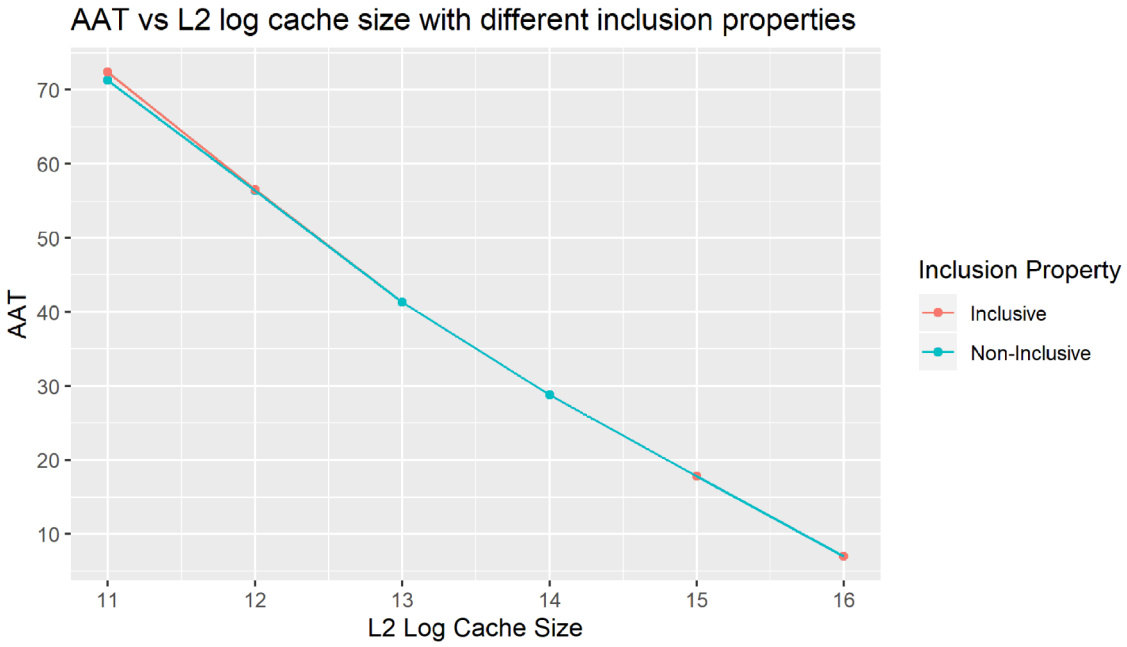
1. For all cache sizes fully associative yields the lowest AAT, but from a practical point of view, 8-way set associative closely follows it but with the advantage of cheaper and easier implementation.

Graph 3



1. For all replacement policies, as the cache size increases, AAT decreases, since there's less capacity misses. Also we see that the difference in AAT between different replacement policies decreases as cache size increases, and becomes insignificant when we go beyond 2^17 bytes of cache size.
Optimal replacement policy performs the best with lowest AAT, but since it's not a practical replacement policy, Pseudo-LRU would be the best practical choice due to it being more efficient than LRU. Technically LRU performs better but the difference is not noticeable and in the graph it almost completely overlaps Pseudo-LRU.

Graph 4



1. For all inclusion properties, as the cache size increases, AAT decreases, since there's less capacity misses. Also we see that the difference in AAT between different inclusion properties decreases as cache size increases, and becomes insignificant when we go beyond 2^12 bytes of cache size.
Non-inclusive is better in terms of lower AAT, since it doesn't invalidate L1 cache blocks when evicting cache blocks from L2, but the difference in AAT is not very significant compared to inclusive.