WESTERN SYDNEY
UNIVERSITY

WESTERN SYDNEY
UNIVERSITY

Implementation of Leaky Integrate-and-Fire (LIF) Neurons

International Centre for Neuromorphic Systems (ICNS)

Prerequisites:

WESTERN SYDNEY UNIVERSITY

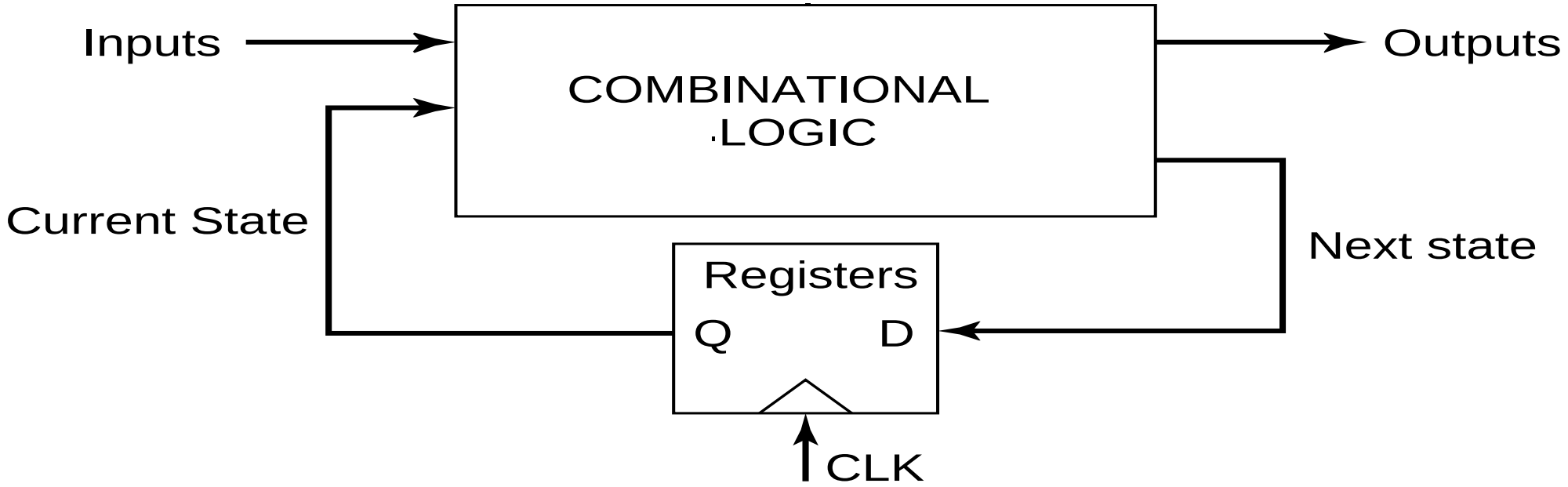
- Basic knowledge of digital circuit design (Practical lecture 1)
- Understanding one of the Hardware design languages (Verilog or VHDL) (Practical lecture 1)
- Basic knowledge of biological neurons (Introduction to Neuroscience 800230)
- Understanding design a LIF neuron circuit using Verilog (lecture 1)

Contents:

WESTERN SYDNEY UNIVERSITY

- Pipeline parallel
- Time multiplexing
- **Group work: Design a LIF neuron network using** Time multiplexing and Pipeline parallel

Sequential Logic



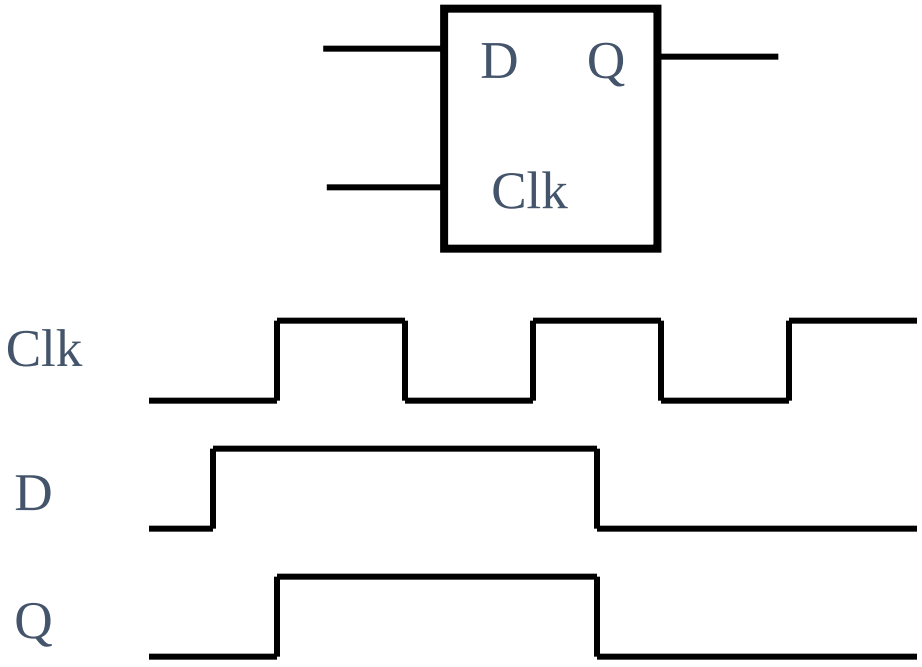
2 storage mechanisms

- positive feedback
- charge-based

Latch versus Register

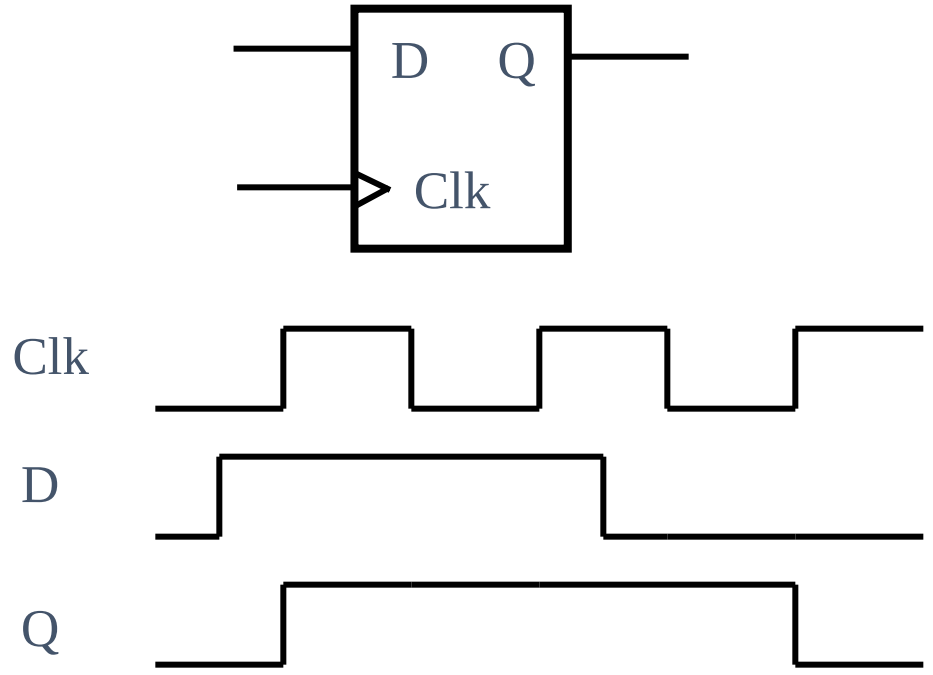
- Latch

  stores data when clock is low

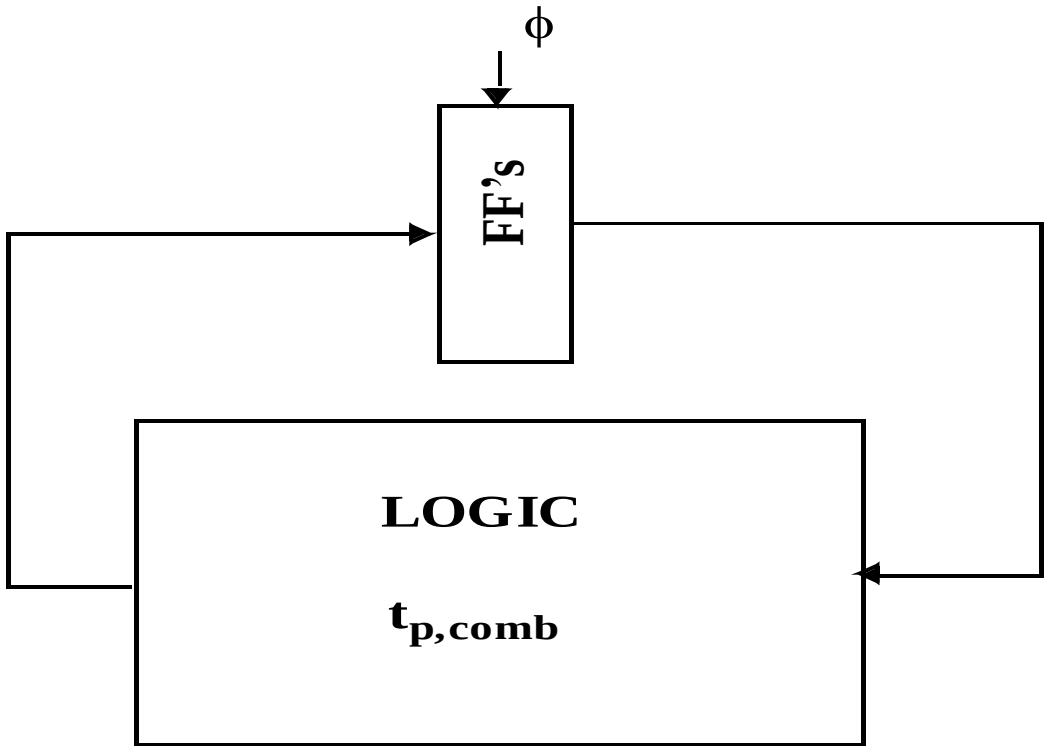


- Register

  stores data when clock rises



Maximum Clock Frequency



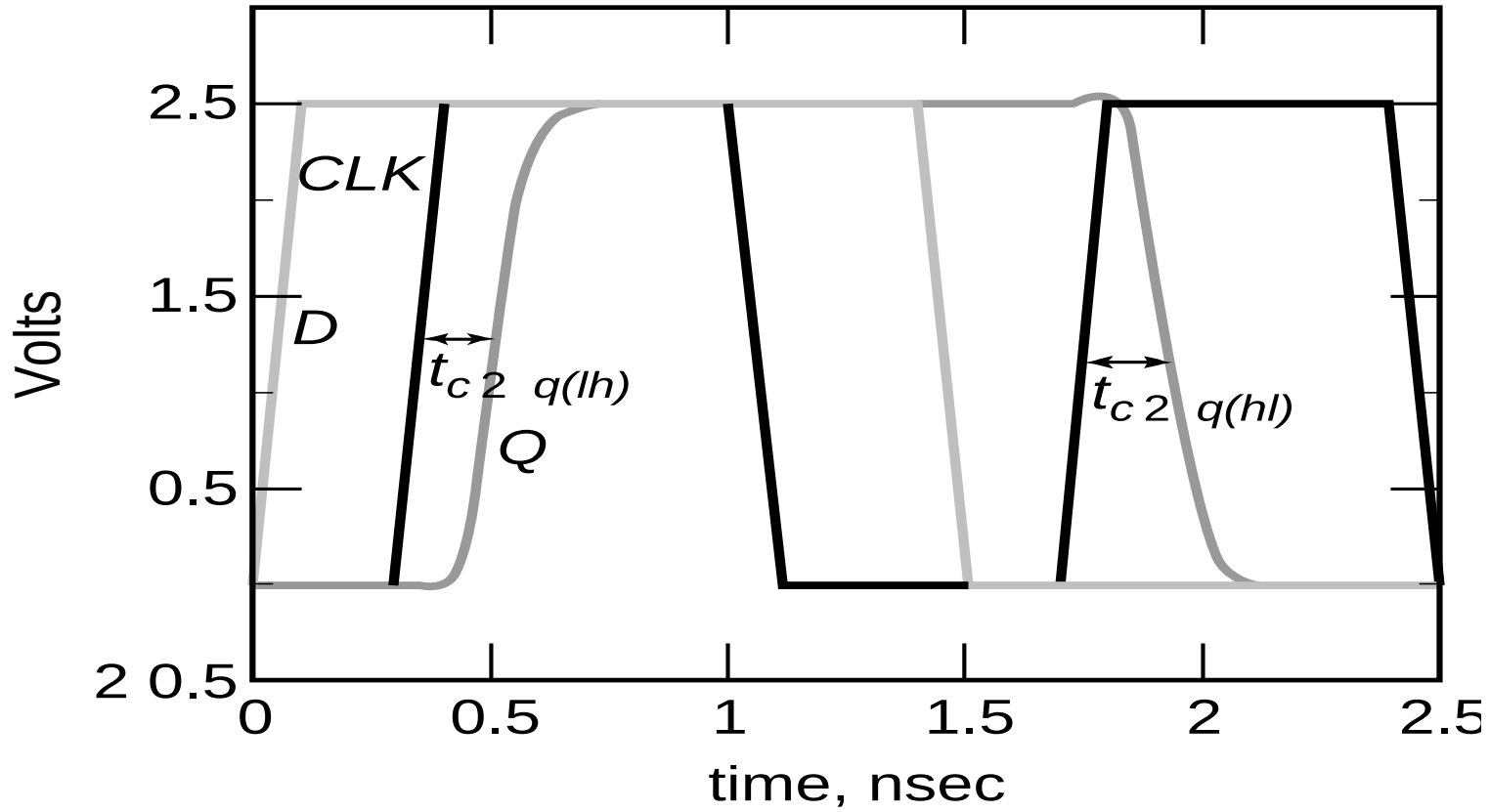
$t_{clk\text{-}Q} + t_{p,comb} + t_{setup} = T$

Also:

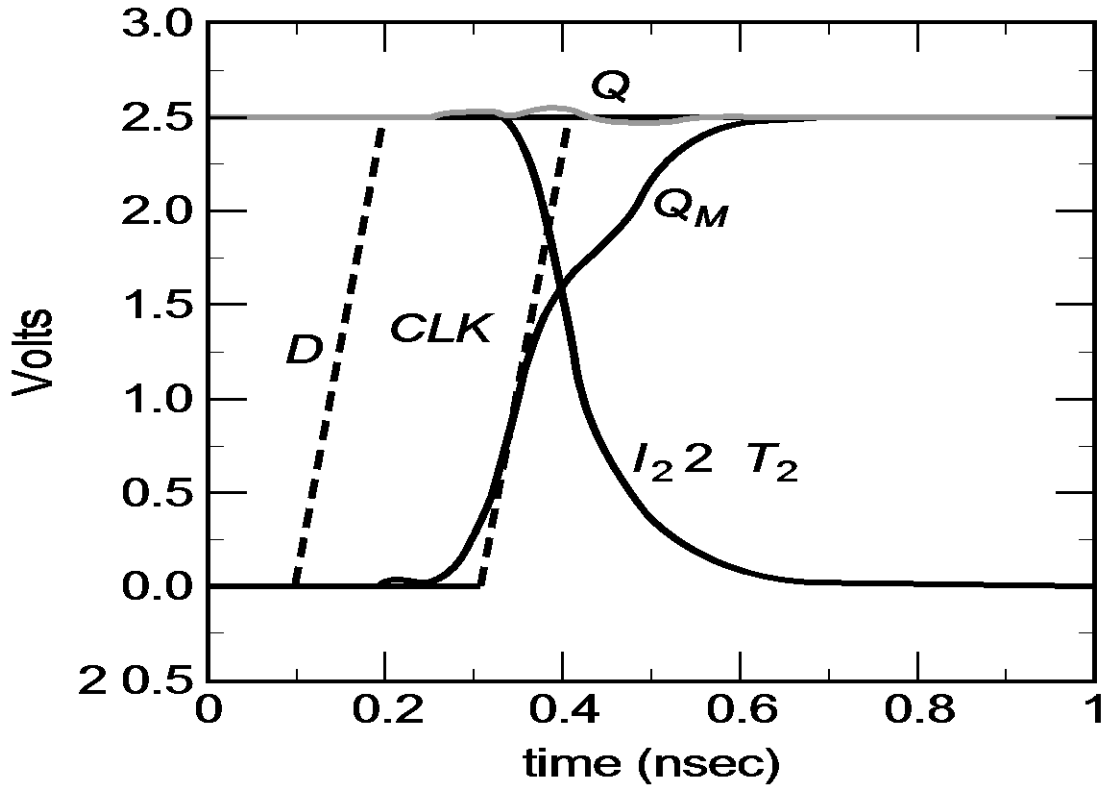
$t_{cdreg} + t_{cdlogic} > t_{hold}$

t_{cd}: contamination delay = minimum delay

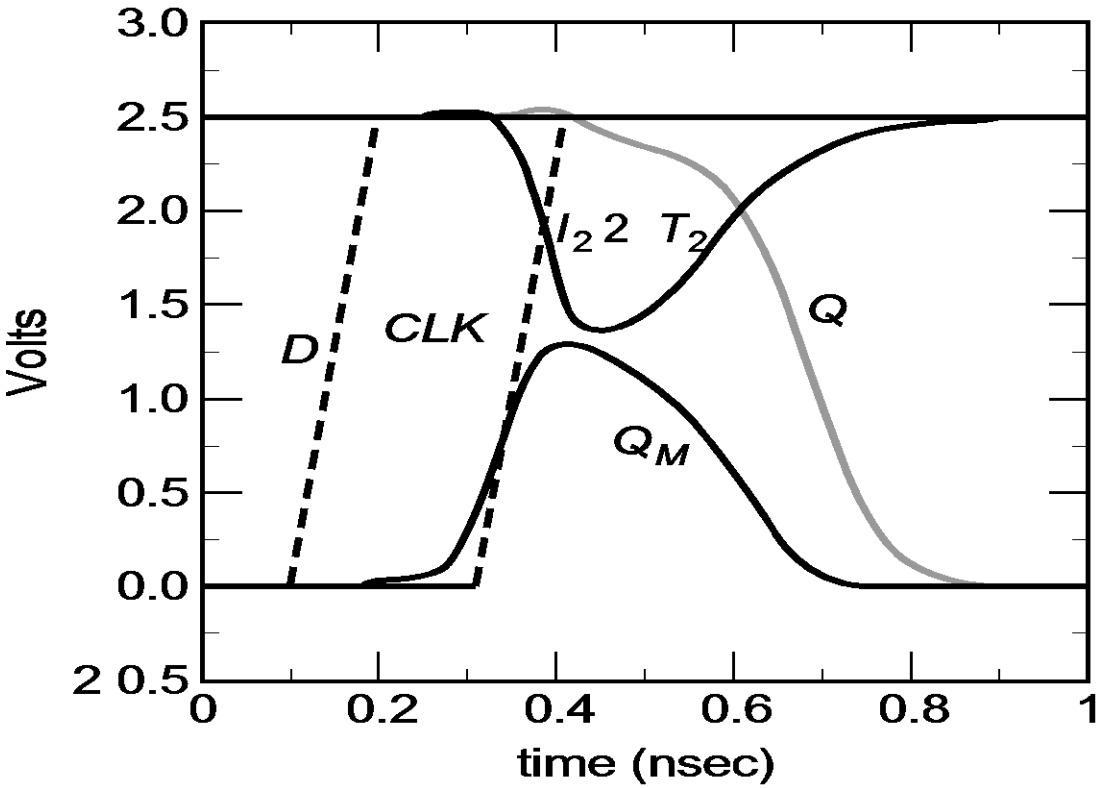
Clk-Q Delay



Setup Time



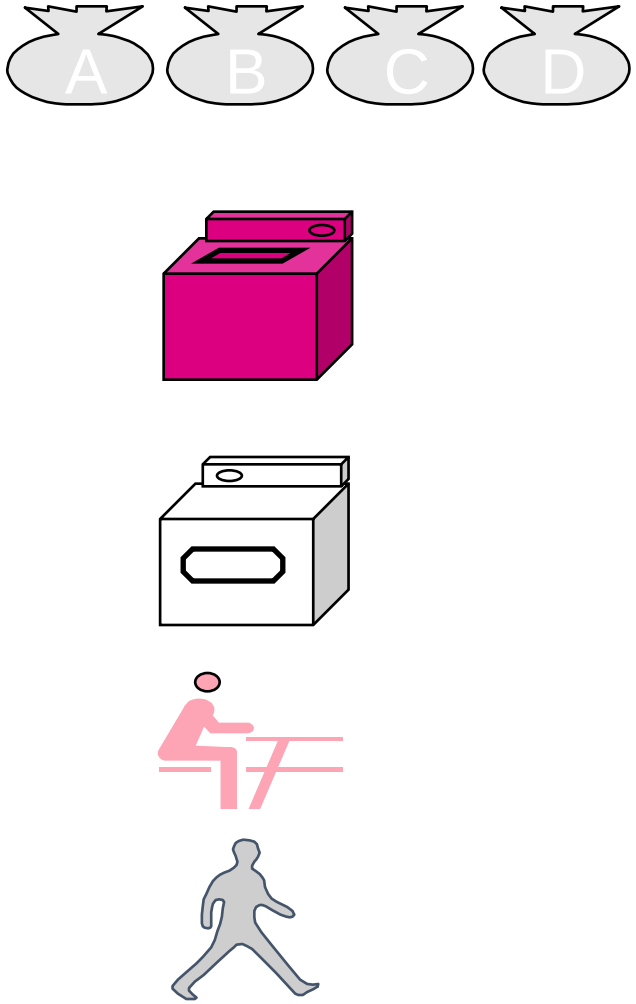
(a) T_{setup} 5 0.21 nsec



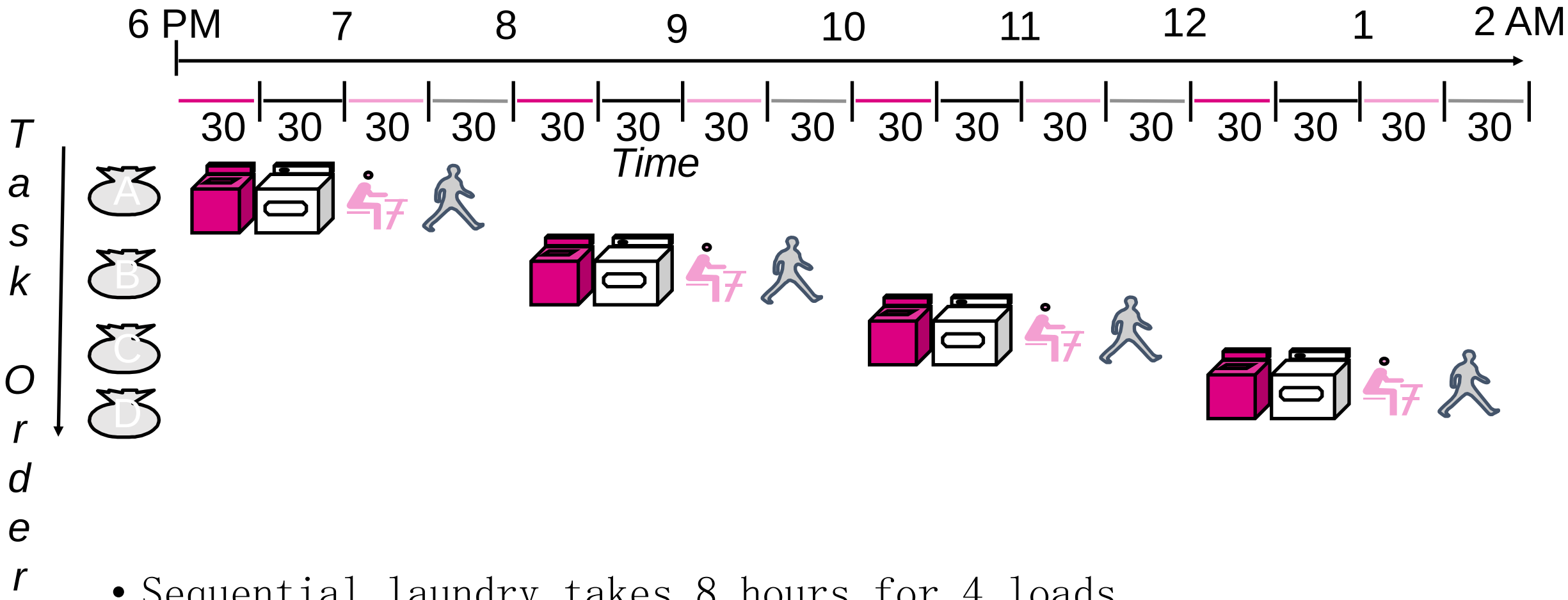
(b) T_{setup} 5 0.20 nsec

Pipelining is Natural!

- Laundry Example
- Sammy, Marc, Griffy, Albert each have one load of clothes to wash, dry, and fold
- Washer takes 30 minutes
- Dryer takes 30 minutes
- “Folder” takes 30 minutes
- “Stasher” takes 30 minutes to put clothes into drawers

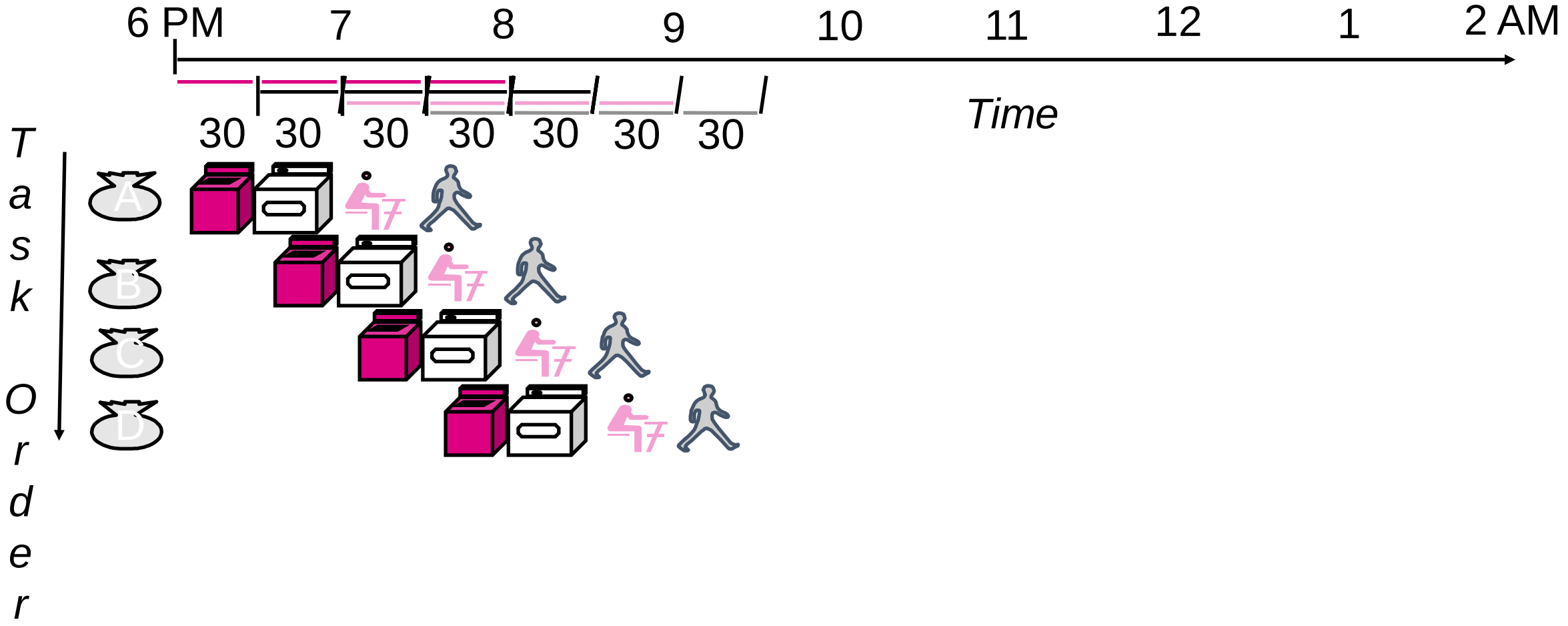


Sequential Laundry



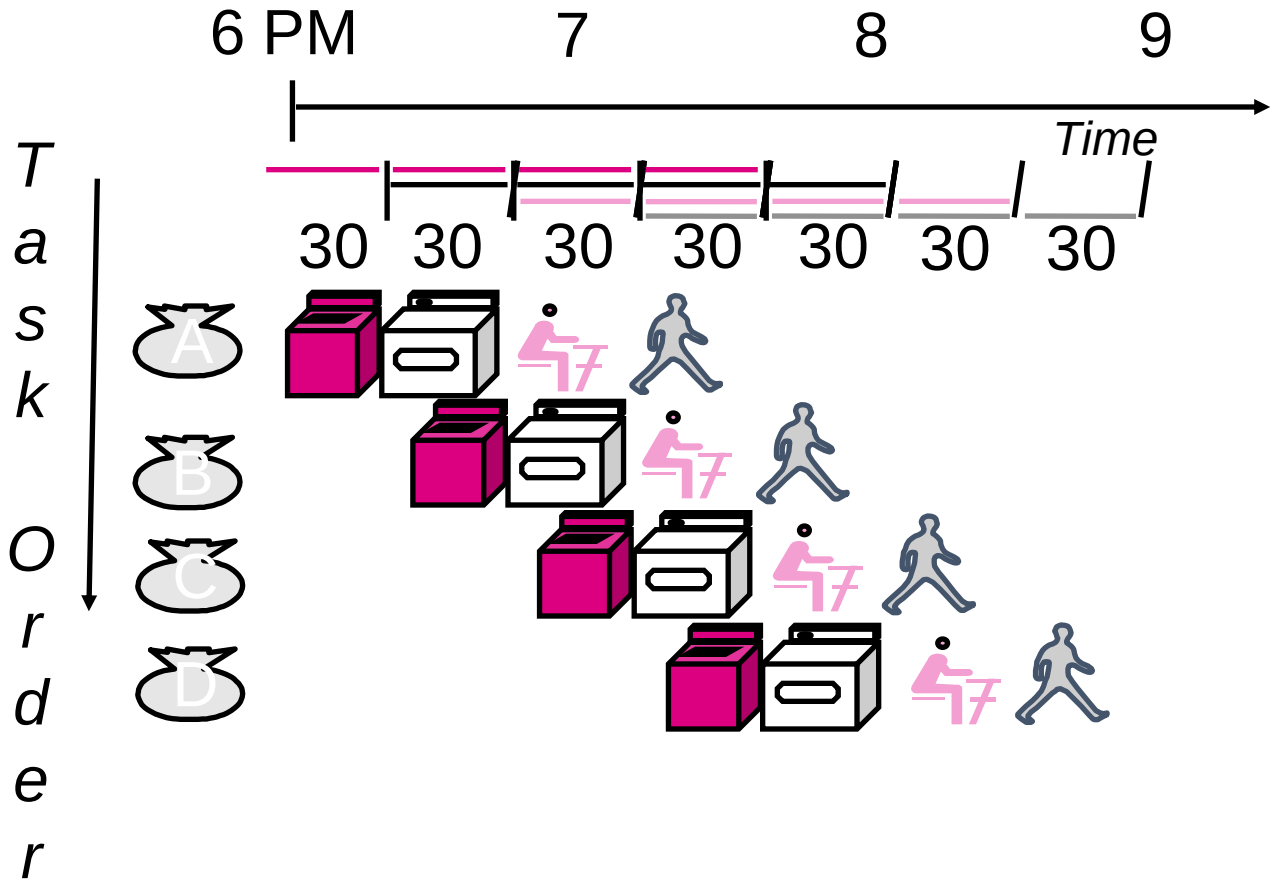
- Sequential laundry takes 8 hours for 4 loads
- If they learned pipelining, how long would laundry take?

Pipelined Laundry: Start work ASAP



- Pipelined laundry takes 3.5 hours for 4 loads!

Pipelining Lessons

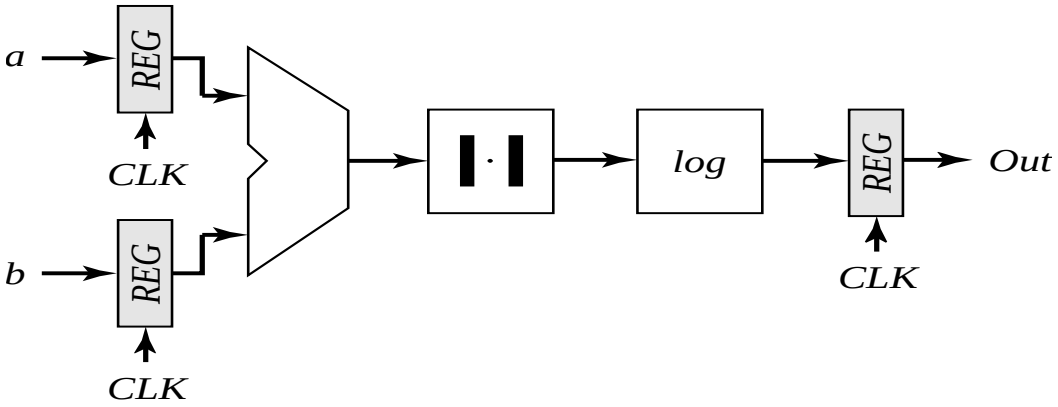


- Pipelining doesn't help latency of single task, it helps throughput of entire workload
- Multiple tasks operating simultaneously using different resources
- Potential speedup = Number pipe stages
- Pipeline rate limited by slowest pipeline stage
- Unbalanced lengths of pipe stages reduces speedup
- Time to "fill" pipeline and time to "drain" it reduces speedup
- Stall for Dependences

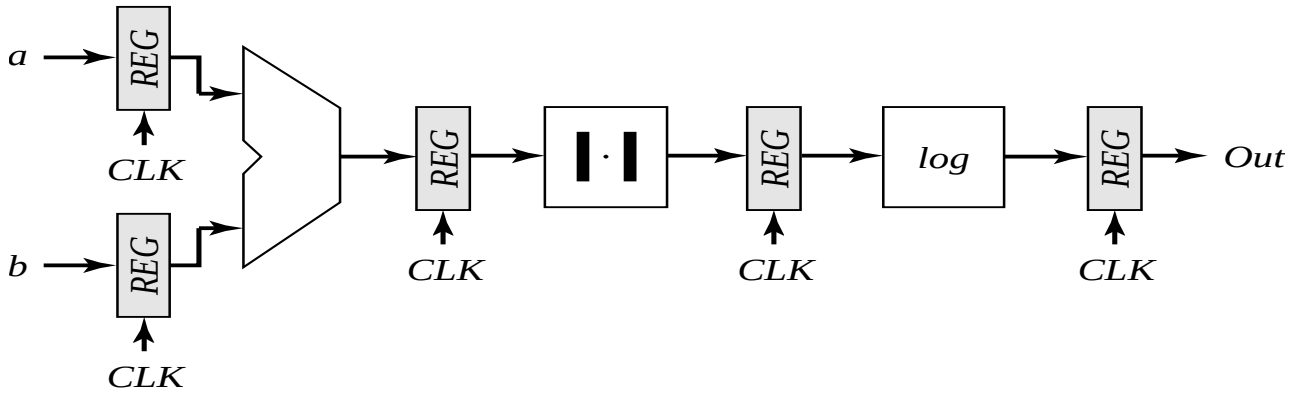
Why Pipeline?

- Suppose we execute 100 instructions
- Single Cycle Machine
  - 45 ns/cycle x 1 CPI x 100 inst = 4500 ns
- Multicycle Machine
  - 10 ns/cycle x 4.6 CPI (due to inst mix) x 100 inst = 4600 ns
- Ideal pipelined machine
  - 10 ns/cycle x (1 CPI x 100 inst + 4 cycle drain) = 1040 ns

Pipelining



Reference



Pipelined

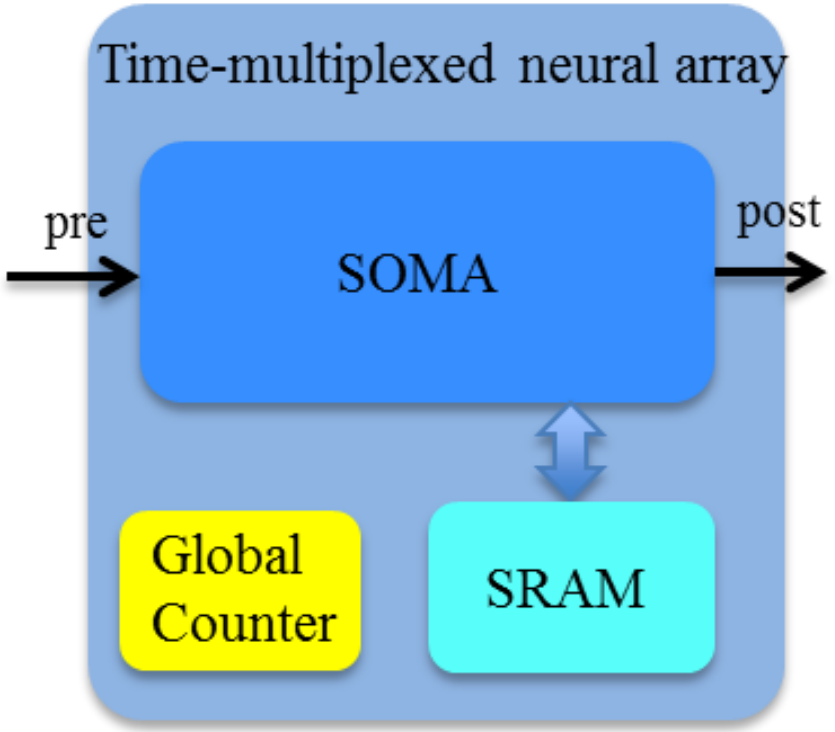
Clock Period	Adder	Absolute Value	Logarithm
1	$a_1 + b_1$		
2	$a_2 + b_2$	$\|a_1 + b_1\|$	
3	$a_3 + b_3$	$\|a_2 + b_2\|$	$\log(\|a_1 + b_1\|)$
4	$a_4 + b_4$	$\|a_3 + b_3\|$	$\log(\|a_2 + b_2\|)$
5	$a_5 + b_5$	$\|a_4 + b_4\|$	$\log(\|a_3 + b_3\|)$

Time-multiplexing:

WESTERN SYDNEY UNIVERSITY

- FPGAs are much faster than biological neurons; a single operation on the FPGA will take only 5 nanoseconds, while a millisecond resolution is generally acceptable for neural simulations.
- Therefore, we can time-multiplex a single physical neuron to simulate many time-multiplexed (TM) neurons such that up to 200,000 TM neurons can be simulated, each one updated every millisecond.
- Using a pipelined architecture, the result of calculating one time step for a TM neuron only has to be available just before that neuron's turn comes around again. The time to compute a single neuron's output is thus not a limiting factor in the size of the network

Time-multiplexing:



WESTERN SYDNEY
UNIVERSITY

Question and discussion time

Books and publications :

WESTERN SYDNEY UNIVERSITY

Verilog and FPGA:

https://west-sydney-primo.hosted.exlibrisgroup.com/permalink/f/afm582/UWS-ALMA2170487320001571

Analog VLSI: Circuits and Principles:

https://ezproxy.uws.edu.au/login?url=https://ieeexplore.ieee.org/book/6267299

Neuromorphic silicon neuron circuits:

https://ezproxy.uws.edu.au/login?url=https://www.frontiersin.org/articles/10.3389/fnins.2011.00073/full

Neuromorphic engineering systems and applications:

https://west-sydney-primo.hosted.exlibrisgroup.com/permalink/f/afm582/UWS-ALMA51173262710001571

Summary:

WESTERN SYDNEY UNIVERSITY

- Design a pipelined LIF neuron circuit using the time-multiplexing approach
- Simulate the neuron