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Introduction to Neuromorphic Engineering

André van Schaik

International Centre for Neuromorphic Systems
(ICNS)

https://www.westernsydney.edu.au/icns

Neuromorphic Engineering

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- Scientific goal:
  Understand the computational properties of biological neural systems by building electronic models.
- Engineering goal:
  Exploit the known properties of biological systems to design and implement efficient devices for engineering applications.

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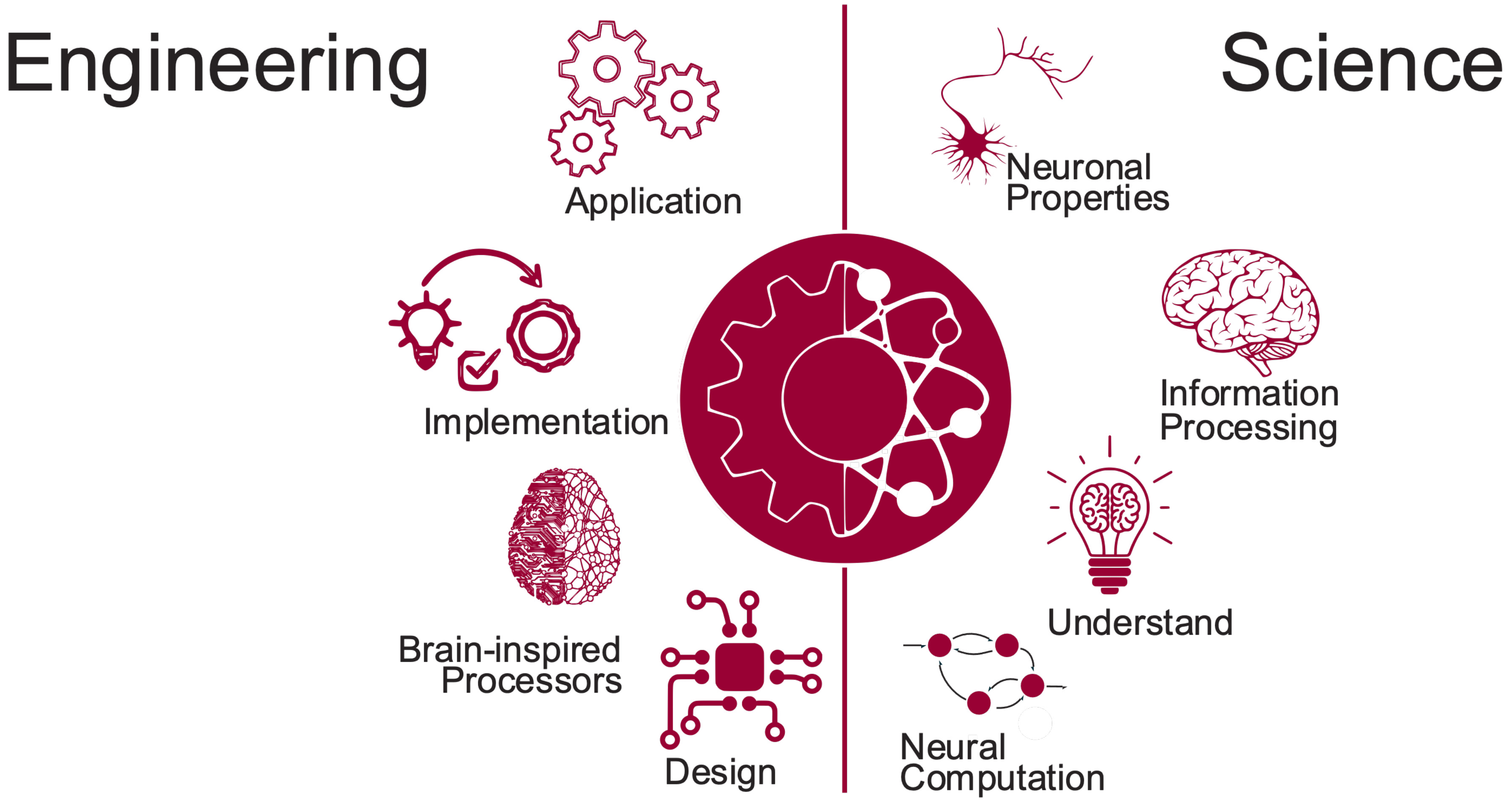
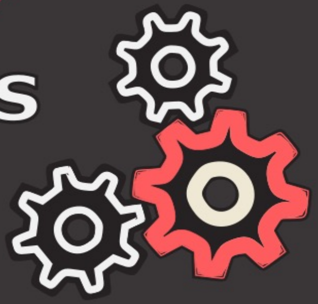
Neuromorphic Engineering



Our Mission at ICNS

Applications



International Centre for Neuromorphic Systems

History and Motivation (then)

History

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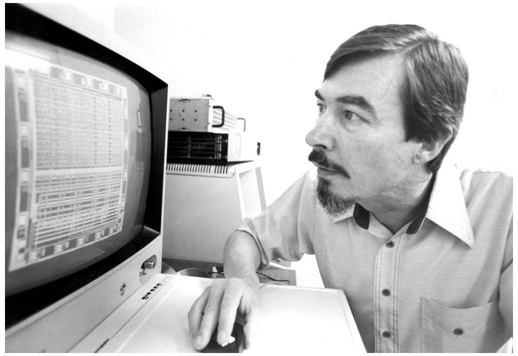
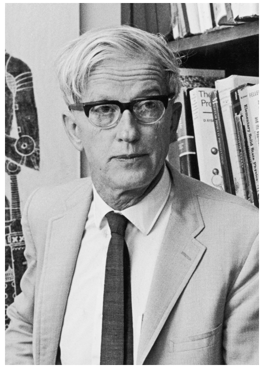


Carver Mead (Caltech)



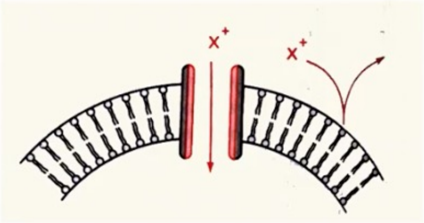
Max Delbrück (Caltech)

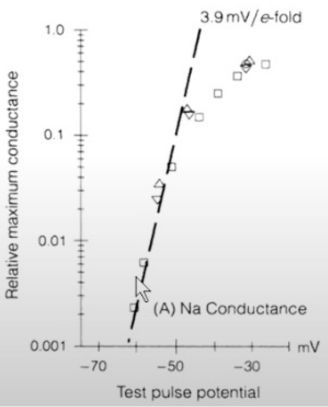
Richard Feynman (Caltech)

John Hopfield (Caltech)

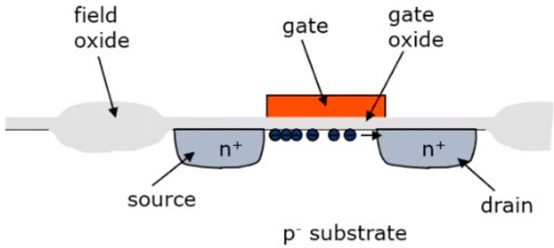
The physics of voltage activated membrane channels and transistors are closely related

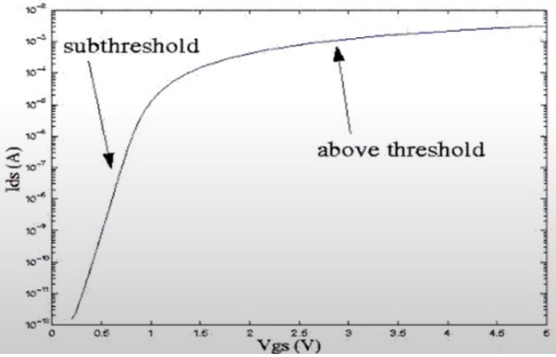
Voltage activated membrane channel





Transistor





Mead, C. How we created neuromorphic engineering. *Nat Electron* **3,** 434–435 (2020). https://doi.org/10.1038/s41928-020-0448-2

Similarities Between Neural and Electronic Processing

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- Processing of information
- Differences in electrical potential represent signals
- Communication by wires
- Change in output due to change in inputs
- Gain
- Power supply

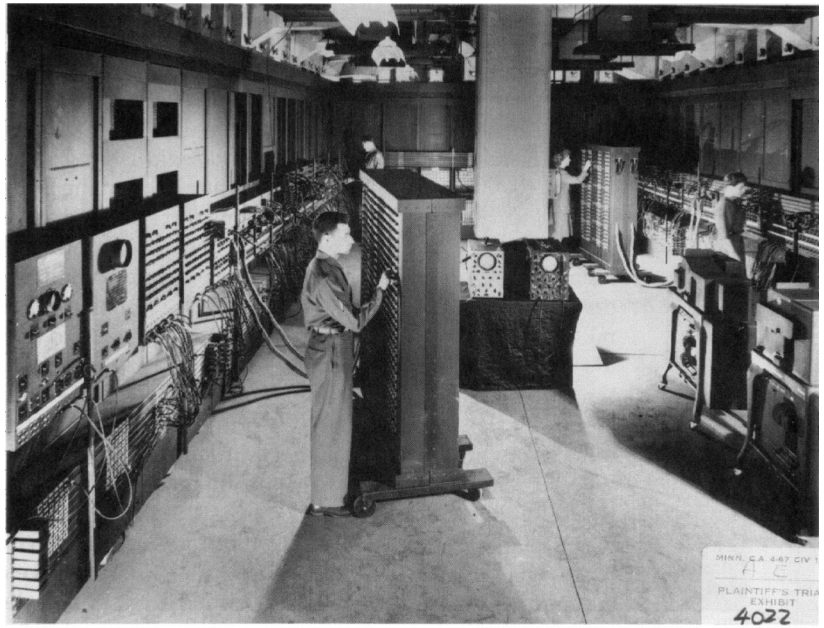
Similarity of Physics

- Neuromorphic engineering directly exploits the physics of analogue CMOS VLSI technology to implement the physical processes that underlie neural computation.
- Electrically charged particles interact with energy barriers
- The energy barriers are controlled by a control node
- Exponential variation of current with change in voltage
- Conservation of charge
- Time constants determined by thermal energy, which can be described by the Boltzmann distribution
- The elementary devices are not well controlled:
  system must be fault tolerant.

Energy Considerations

- ENIAC (1946)
  - 1,800 vacuum tubes
  - 174,000W of power.

- ENIAC on chip (1998)
  - 4mm^2 silicon chip
  - 1W.



Energy Considerations

- We are still far from duplicating the human brain's performance.
- The brain uses 10W to process 10 spikes/sec at each of 10^{15} synapses
- A state-of-the-art computer uses 100W to process 10^{9} instructions/sec.
- At this rate, a computer as powerful as the brain would burn 10^{9}W,
- This power consumption makes it impractical to build an artificial brain using computer technology.

Energy Considerations

- Computer technology is expected to improve by only one or two orders of magnitude in power before fundamental scaling limits are reached.
- Apparently, the nervous system has evolved vastly superior computational structures, and supremely effective signal representations.
- We can improve the energy efficiency of present-day computers dramatically by copying the organizing principles of the nervous system.

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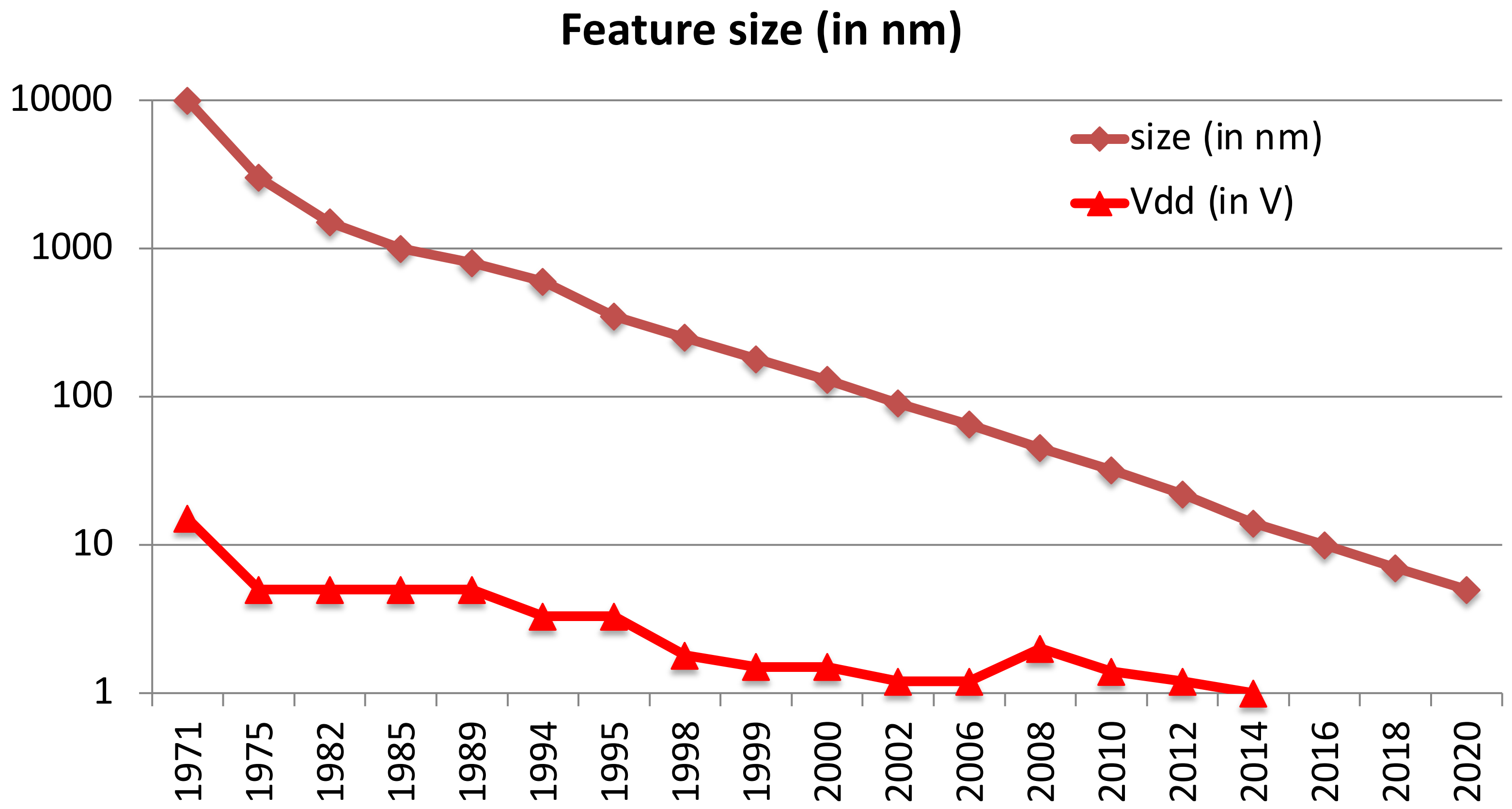
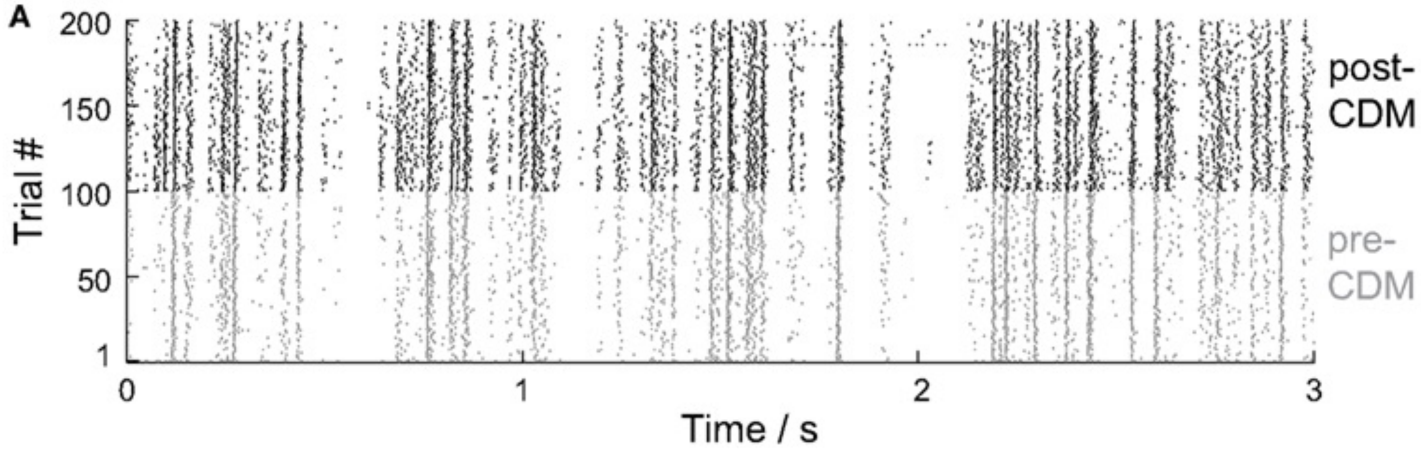
Semiconductors



Device mismatch and noise become a real issue for analogue VLSI

Inaccurate sensors

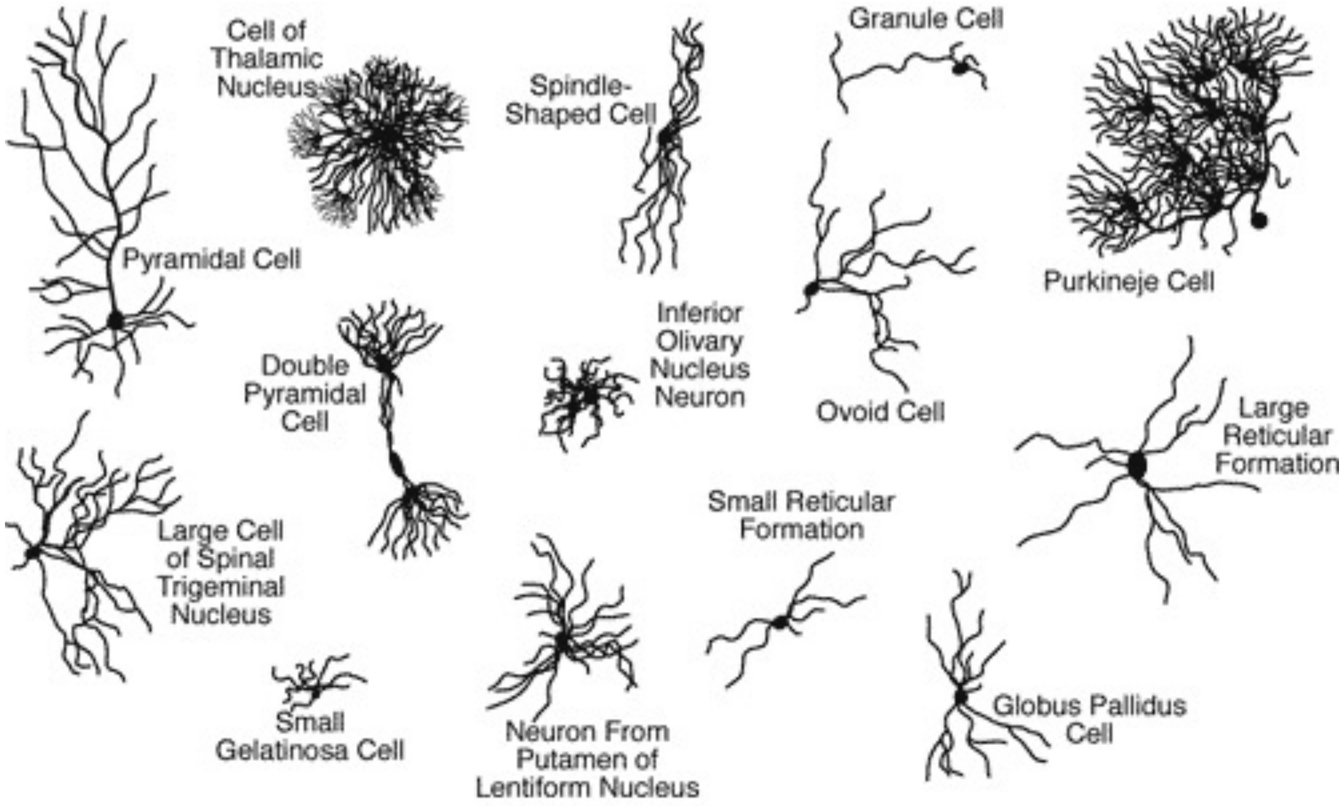
- Our biological senses are imprecise and noisy.



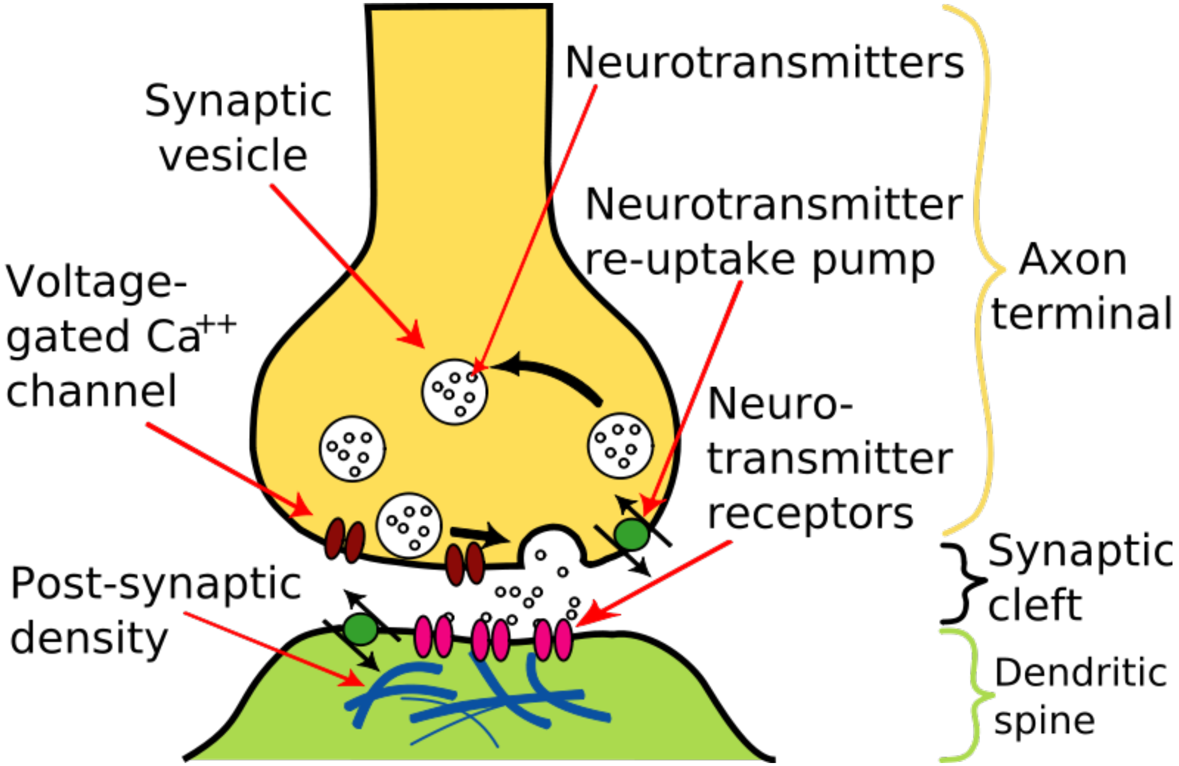
Response of the H2 Neuron in the blowfly
to repeated stimulation with the same stimulus.

(Longden & Krapp, Front. Syst. Neurosci., 23 November 2010)

Neurons are noisy and variable

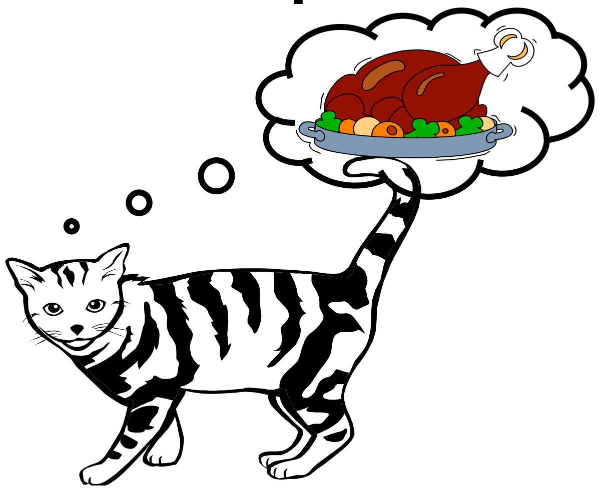


Synapses are stochastic

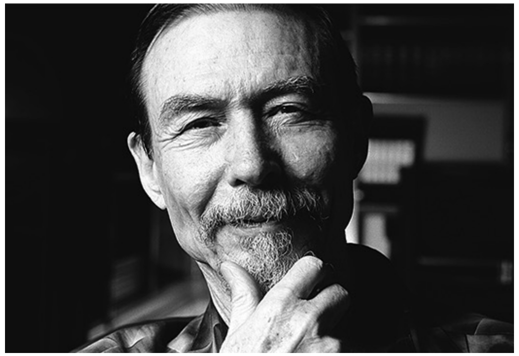


Neuromorphic tasks

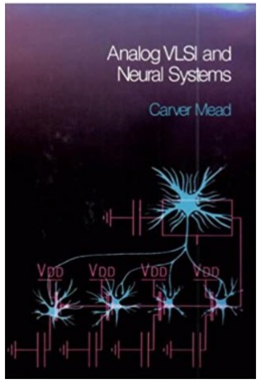
- Sensory processing / Perceptive tasks:
  - Brain better than traditional signal processing
  - Works with imprecise/unreliable elements
  - Need to understand & model neural processing



History



In 1984, professor of electrical engineering and computer science at Caltech, Carver Mead, published “Analog VLSI and Neural Systems”



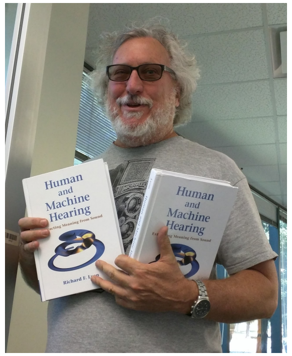
1989

Late 1980s, Silicon Retina

1988, Silicon Cochlea

1986, analogue circuits based on neural networking theories

Misha Mahowald (Caltech)



Richard F. Lyon (Google)

Federico Faggin (Design Intel 4004)

First product: Logitech Marble (1994)

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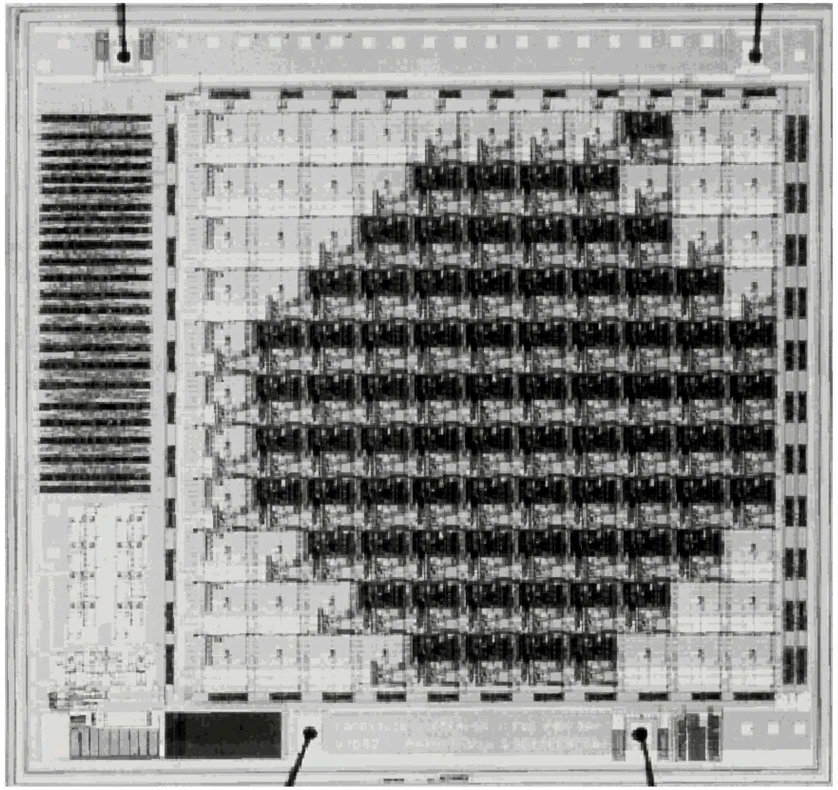
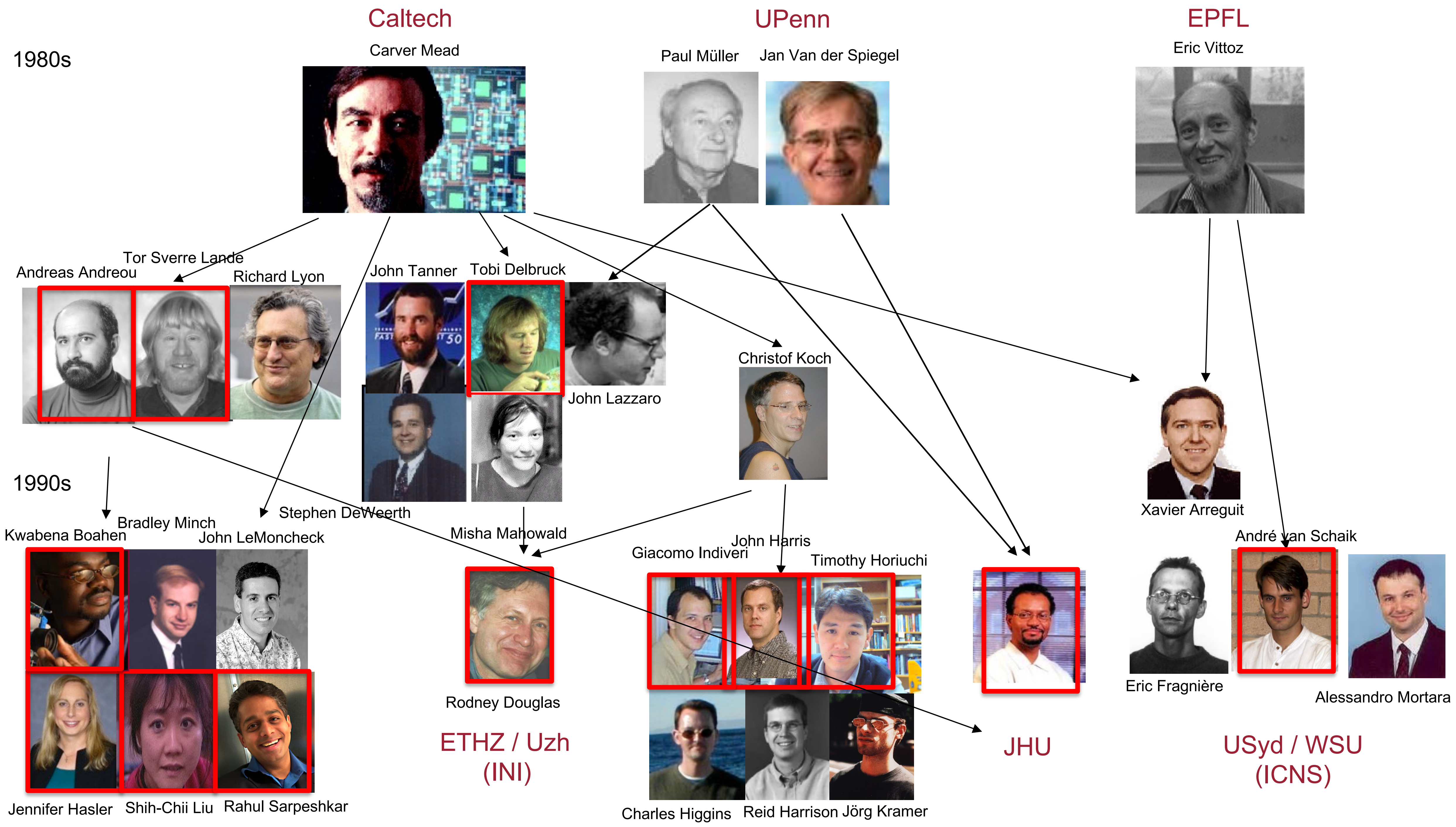
- Optical motion detection inspired by the fly's eye
- Designed by AvS
- Is still on the market in 2022!





Caltech
UPenn
EPFL
1980s
Carver Mead
Paul Müller
Jan Van der Spiegel
Eric Vittoz
Tor Sverre Lande
Andreas Andreou
Richard Lyon
John Tanner
Tobi Delbruck
John Lazzaro
Christof Koch
Xavier Arreguit
1990s
Kwabena Boahen
Bradley Minch
John LeMoncheck
Stephen DeWeerth
Misha Mahowald
Giacomo Indiveri
John Harris
Timothy Horiuchi
André van Schaik
Eric Fragnière
Alessandro Mortara
Rodney Douglas
Jennifer Hasler
Shih-Chii Liu
Rahul Sarpeshkar
Charles Higgins
Reid Harrison
Jörg Kramer
ETHZ / Uzh
(INI)
JHU
USyd / WSU
(ICNS)

Community

Telluride workshop on Neuromorphic Engineering

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- Started by Rodney Douglas, Christof Koch, and Terry Sejnowski in 1994
- Focus on :
- -Fostering the neuromorphic community,
- -tutorials, hands-on workgroups,
- -establishing long-lasting collaborations
- 3 weeks long each July, in the mountains in Colorado, USA
- 100 people each year, about half invited and half applicants.

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CapoCaccia - Cognitive Neuromorphic Engineering Workshop

- Started by Rodney Douglas and Giacomo Indiveri in 2007
- 2 weeks long a few kilometres from Alghero, Italy
- Place a greater emphasis than Telluride on a free-format program.
- Encourage social interactions by having all participants housed in one full-board hotel.

Organised since 2007 by the Institute of Neuroinformatics (INI), of the University of Zurich and ETH Zurich, in collaboration with the Institute of Neuromorphic Engineering

Neuromorphic publications

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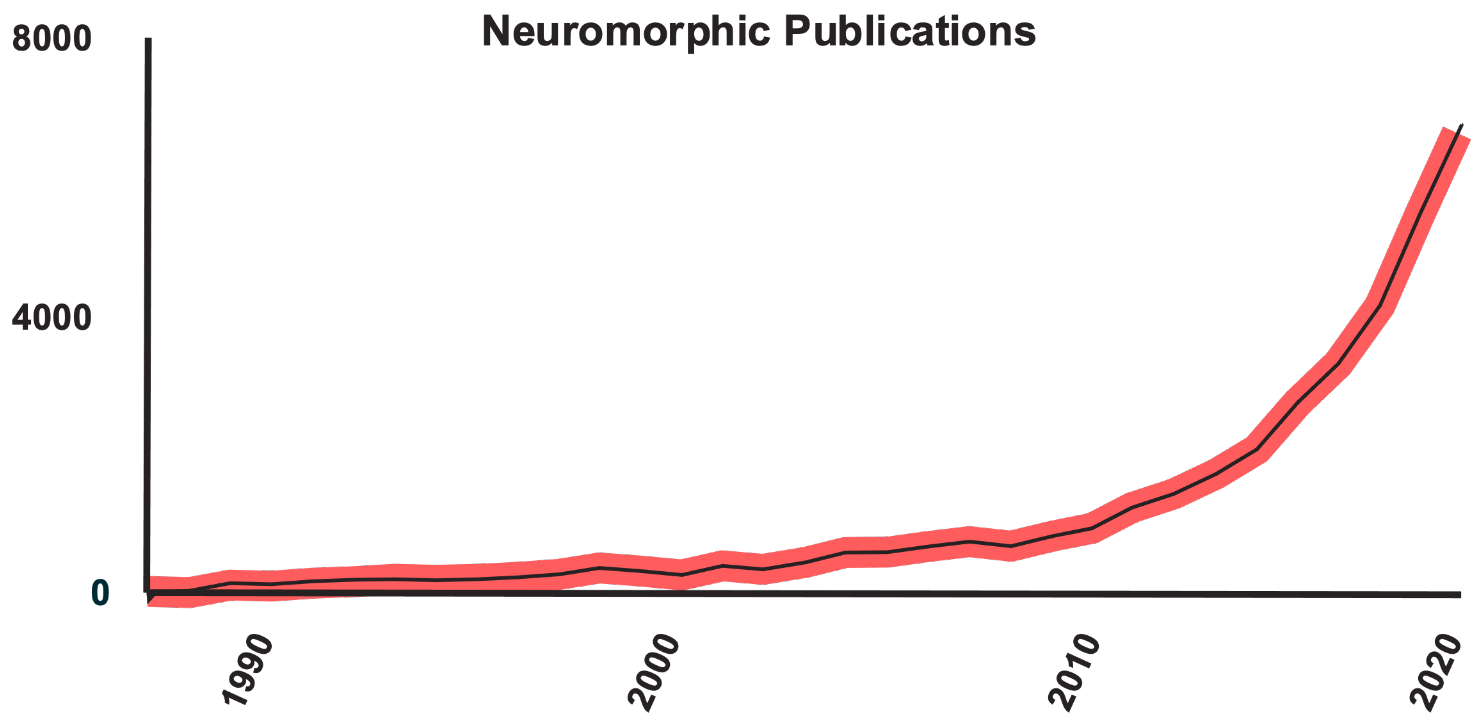


Motivation (Now)

Motivation

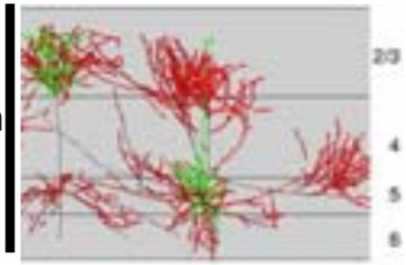
https://www.bioexplorer.net/animals-with-best-sensors.html/

Computer vs. Brain

Pentium 4

Cortex

1mm



Anderson et al. 2003

At the system level, brains are about 1 million times more power efficient than computers. Why?

Cost of elementary operation (turning on transistor or synapse) is about the same.
It's not some magic about physics.

Computer	Brain
Fast global clock	Self-timed
Bit-perfect deterministic logical state	Synapses are stochastic! Computation dances: digital→analog→digital
Memory distant to computation	Memory at computation
Fast high precision power hungry ADCs	Low precision adaptive data-driven quantizers
Devices frozen on fabrication	Constant adaptation and self-modification

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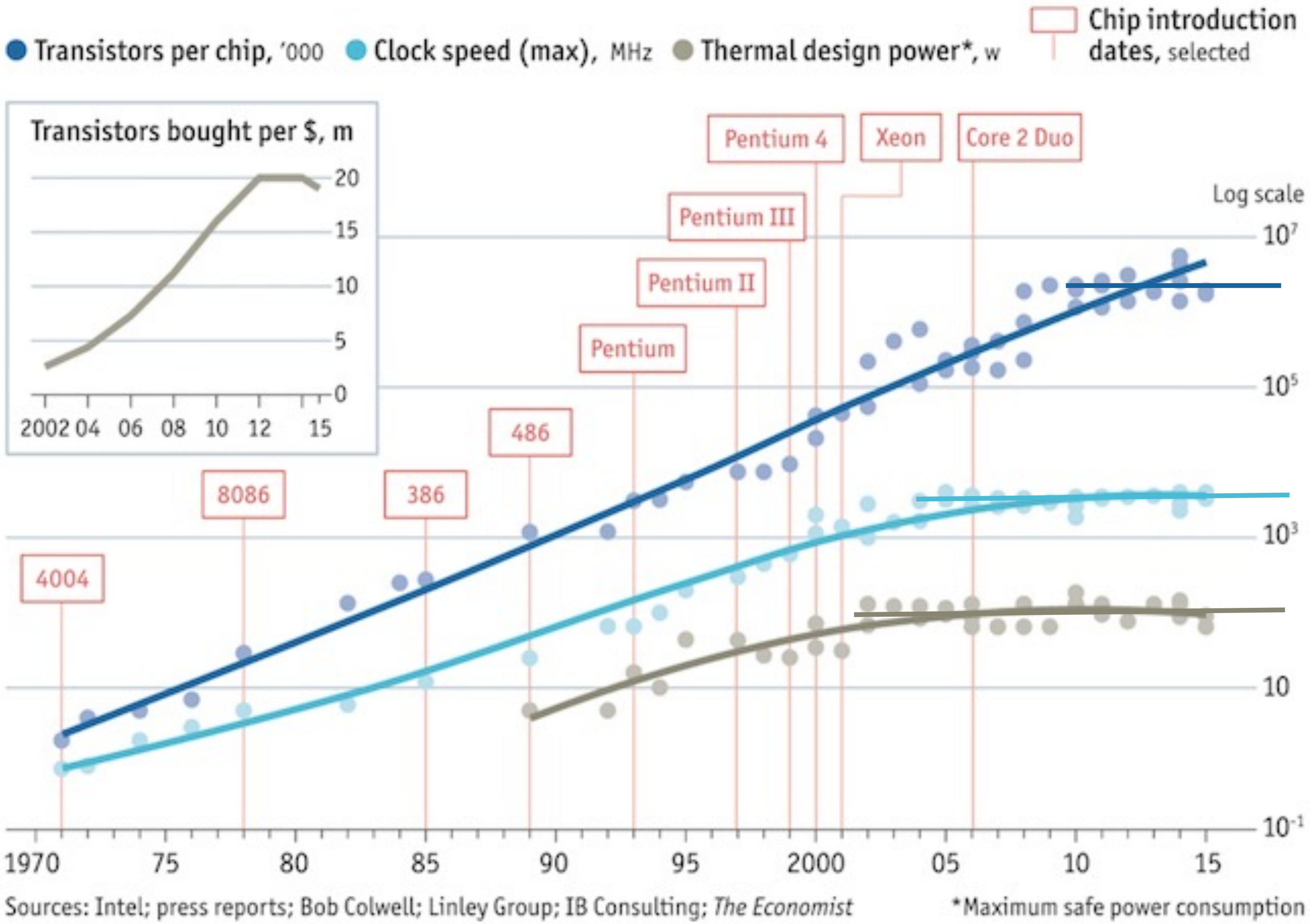
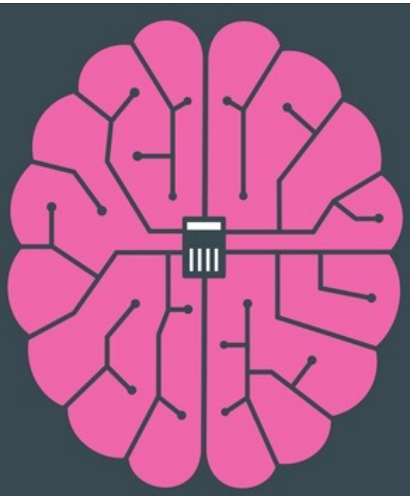
End of Moore’s Law



Neuromorphic Chips



10 Breakthrough Technologies 2014

Neuromorphic Chips

Microprocessors configured more like brains than traditional chips could soon make computers far more astute about what's going on around them.

Breakthrough

An alternative design for computer chips that will enhance artificial intelligence.

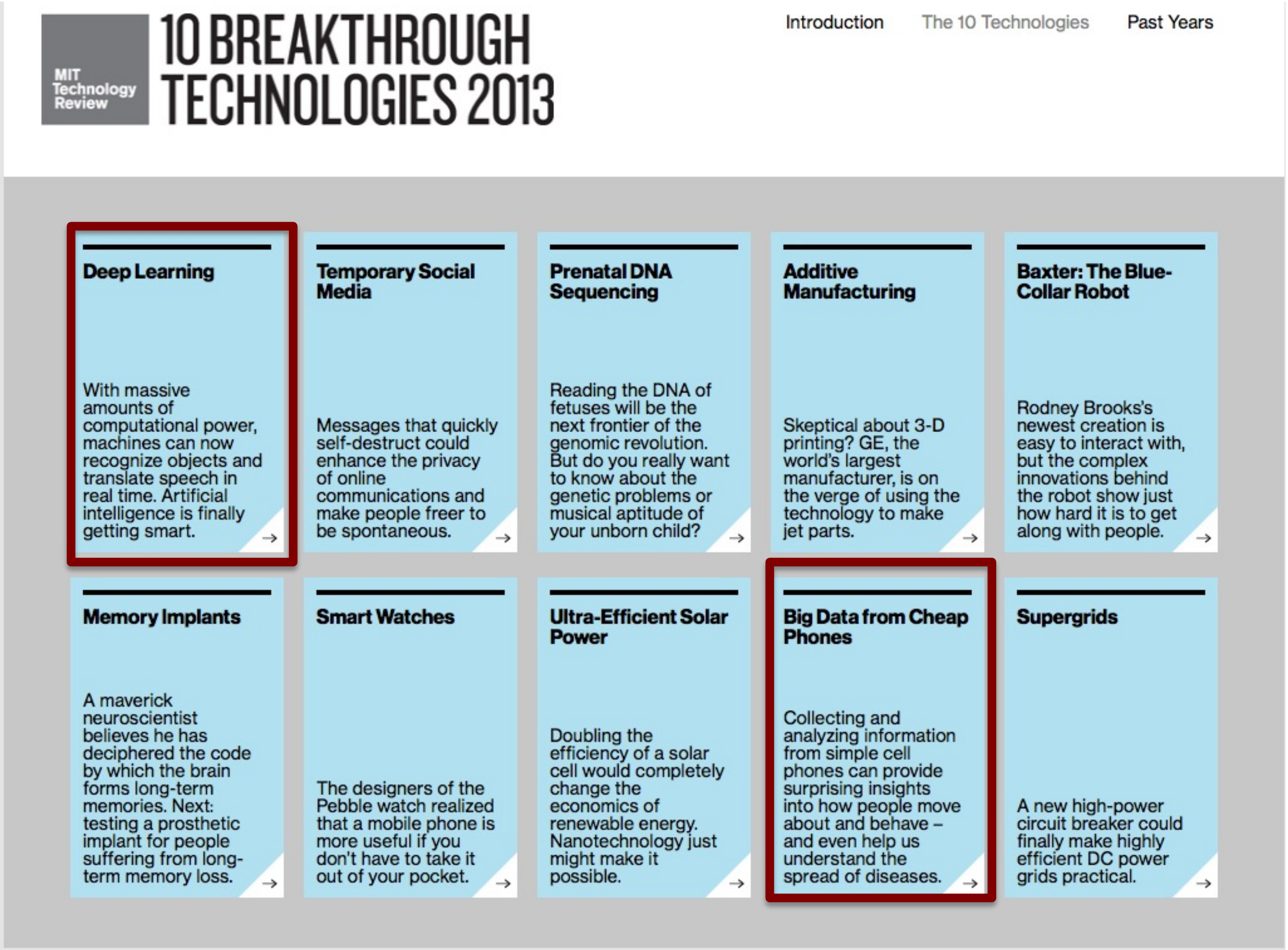
Why It Matters

Traditional chips are reaching fundamental performance limits.

Key Players

+ Qualcomm
+ IBM
+ HRL Laboratories
+ Human Brain Project

Machine Learning



MIT Technology Review

10 BREAKTHROUGH TECHNOLOGIES 2013

Introduction | The 10 Technologies | Past Years

Deep Learning

With massive amounts of computational power, machines can now recognize objects and translate speech in real time. Artificial intelligence is finally getting smart.

Temporary Social Media

Messages that quickly self-destruct could enhance the privacy of online communications and make people freer to be spontaneous.

Prenatal DNA Sequencing

Reading the DNA of fetuses will be the next frontier of the genomic revolution. But do you really want to know about the genetic problems or musical aptitude of your unborn child?

Additive Manufacturing

Skeptical about 3-D printing? GE, the world's largest manufacturer, is on the verge of using the technology to make jet parts.

Baxter: The Blue-Collar Robot

Rodney Brooks's newest creation is easy to interact with, but the complex innovations behind the robot show just how hard it is to get along with people.

Memory Implants

A maverick neuroscientist believes he has deciphered the code by which the brain forms long-term memories. Next: testing a prosthetic implant for people suffering from long-term memory loss.

Smart Watches

The designers of the Pebble watch realized that a mobile phone is more useful if you don't have to take it out of your pocket.

Ultra-Efficient Solar Power

Doubling the efficiency of a solar cell would completely change the economics of renewable energy. Nanotechnology just might make it possible.

Big Data from Cheap Phones

Collecting and analyzing information from simple cell phones can provide surprising insights into how people move about and behave – and even help us understand the spread of diseases.

Supergrids

A new high-power circuit breaker could finally make highly efficient DC power grids practical.

Rise of Intelligent Devices

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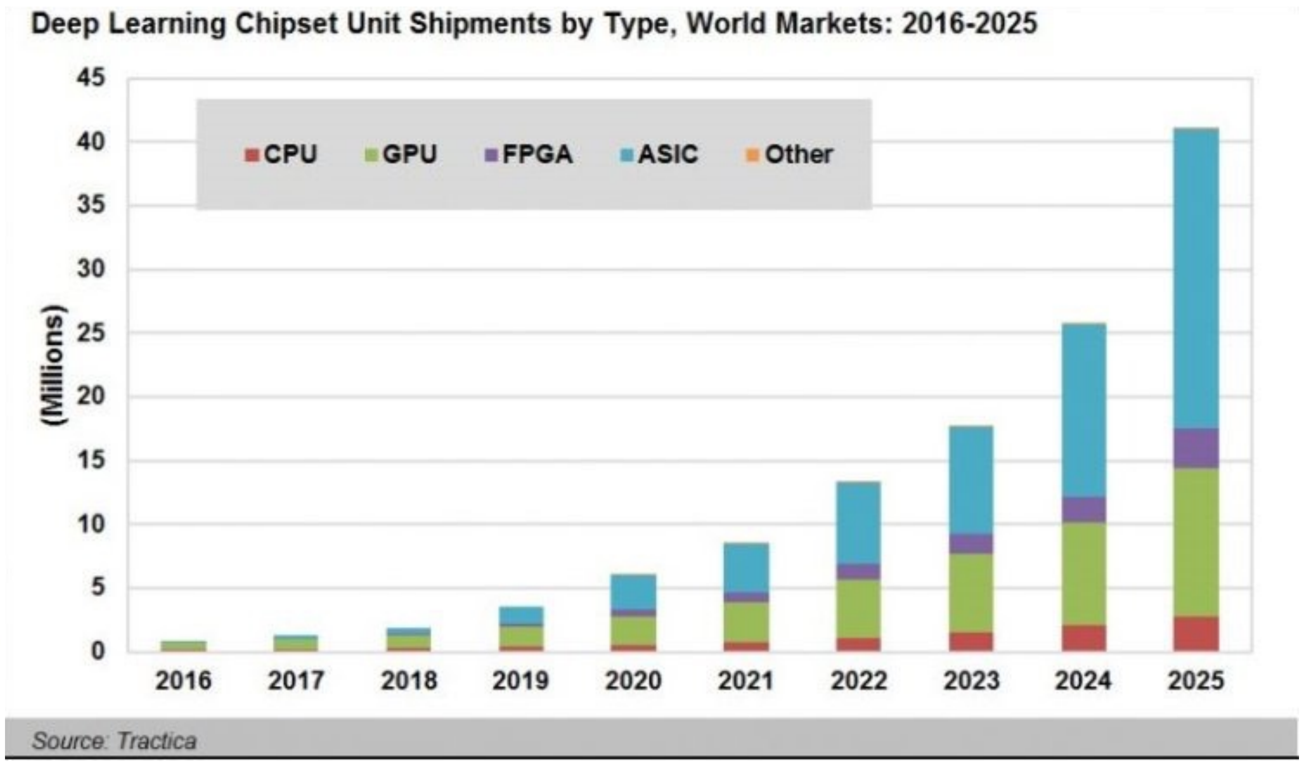

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Deep Learning

Hinton, LeCun, Bengio, Schmidhuber ↑ 2007

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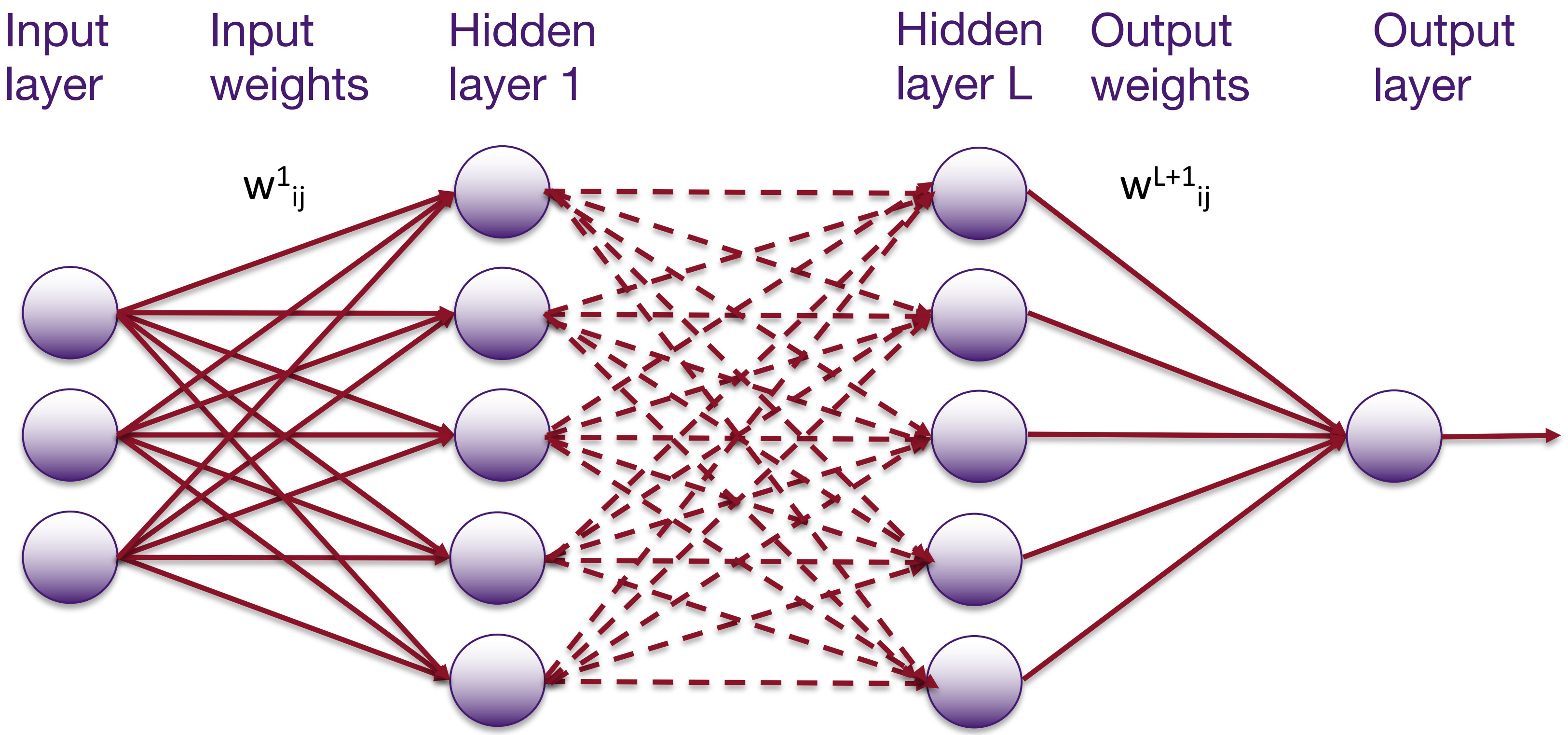

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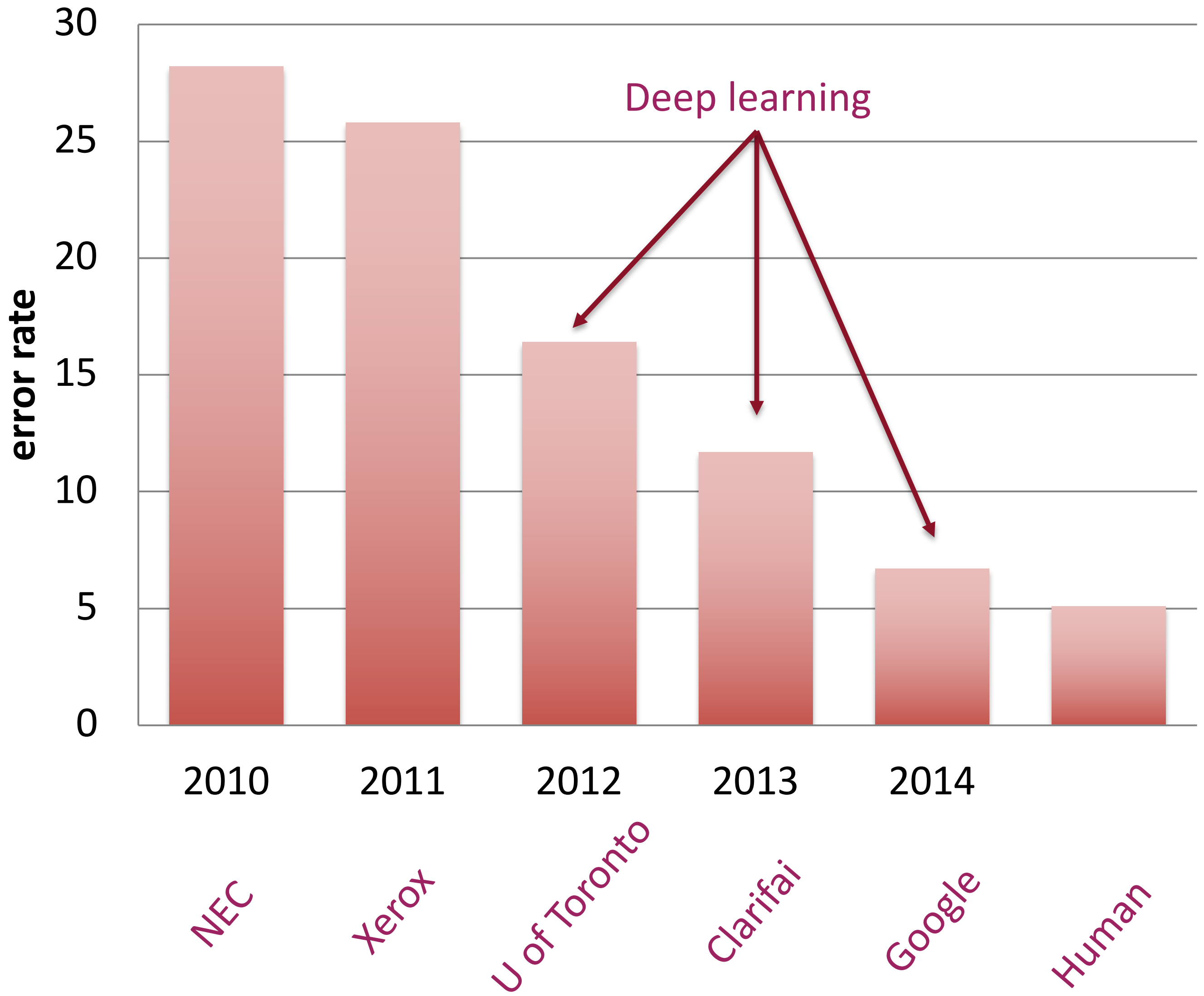
ImageNet

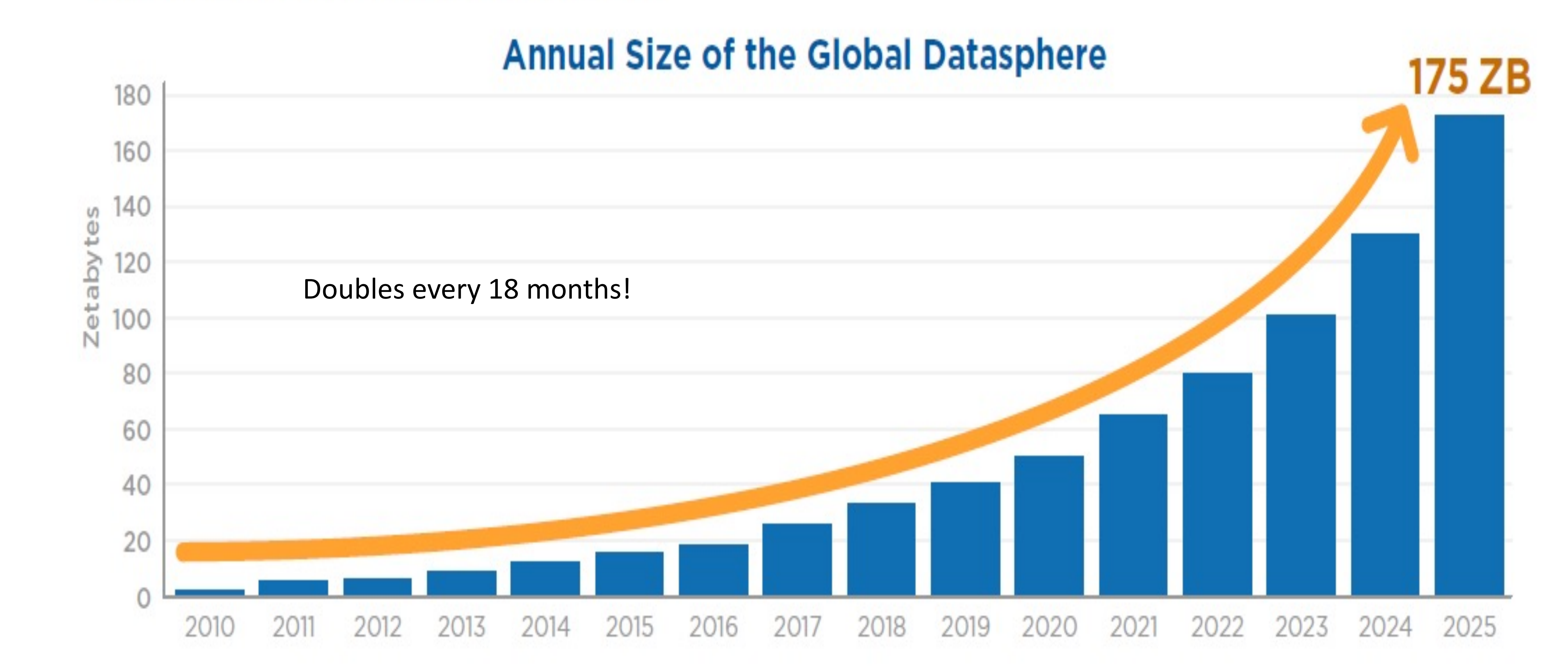
Large Scale Visual Recognition Challenge

- Labeled internet images
- Images: 1,461,406
- object classes: 1000
- task:
  detect if object is present

ILSVRC results



A Data Deluge



Less than 1% of data collected is analysed!

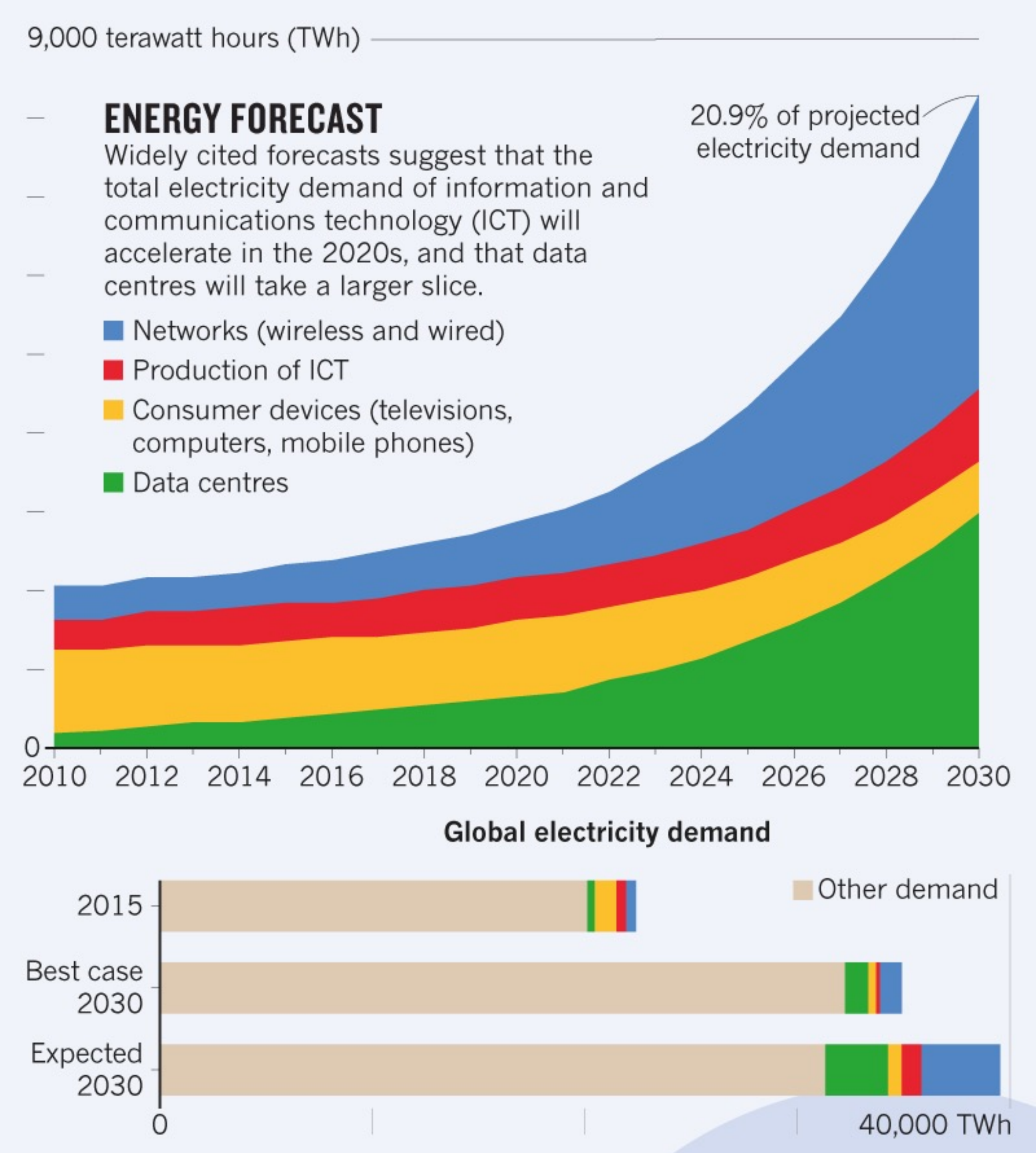
Problem 1: dumb data

- Much of the data collected is redundant.
- Much of the data collected adds no value.

Solution 1: smart sensors

- Process data locally to extract relevant info.
- Neuromorphic Engineering excels at this.

Problem 2: Power



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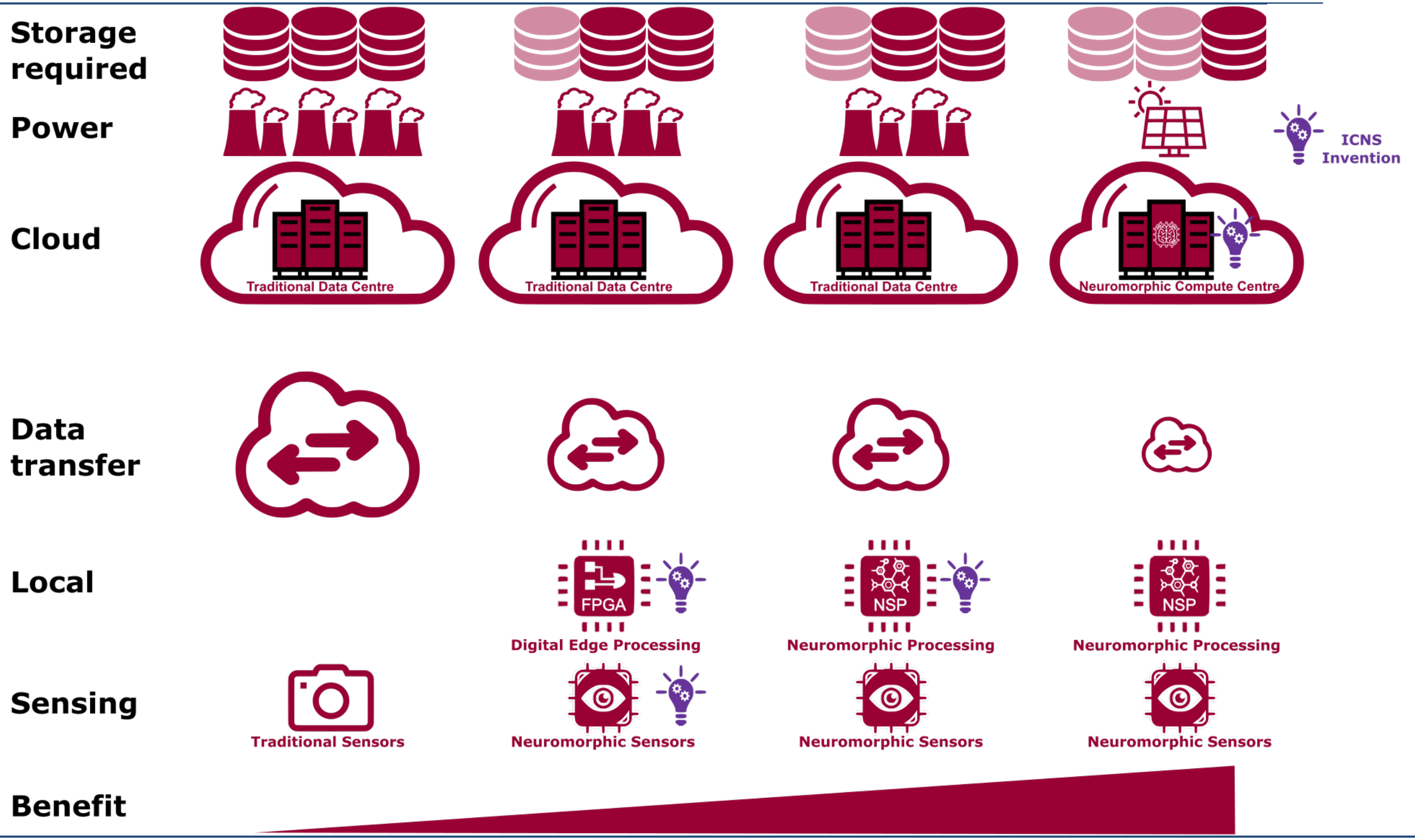
Solution 2: Neuromorphic Processing



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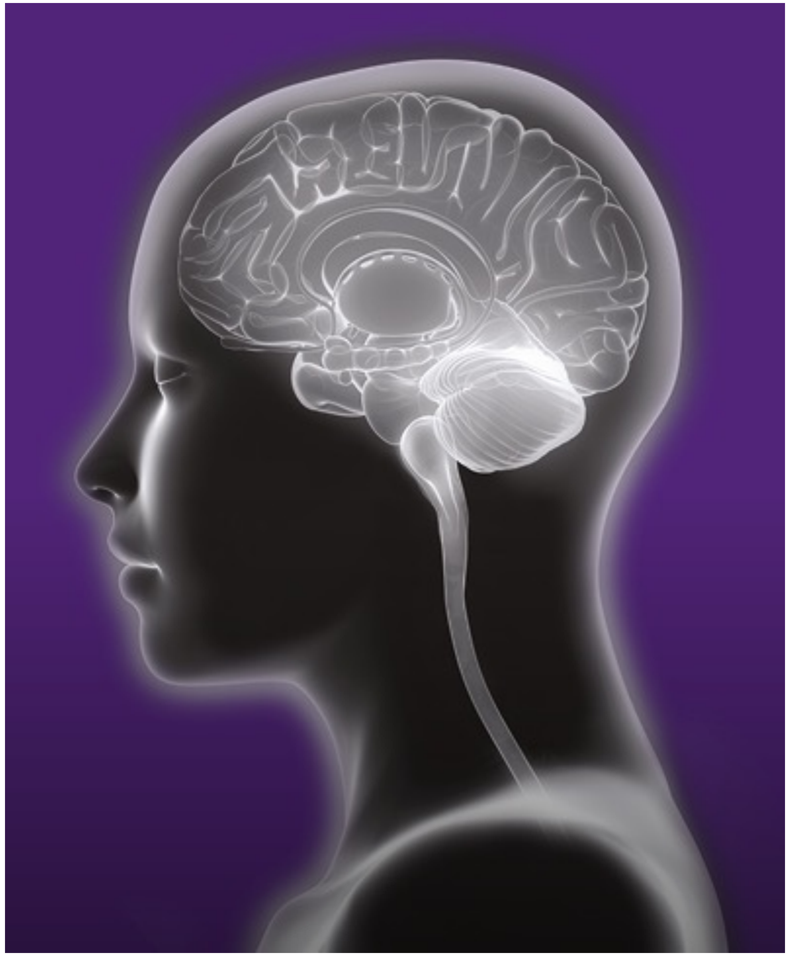
What is missing?

1. Algorithms / Models

- For edge processing
- For central data processing

- How do we compute on these neuromorphic platforms?
- Inspiration from Neuroscience, Engineering, and Mathematics.

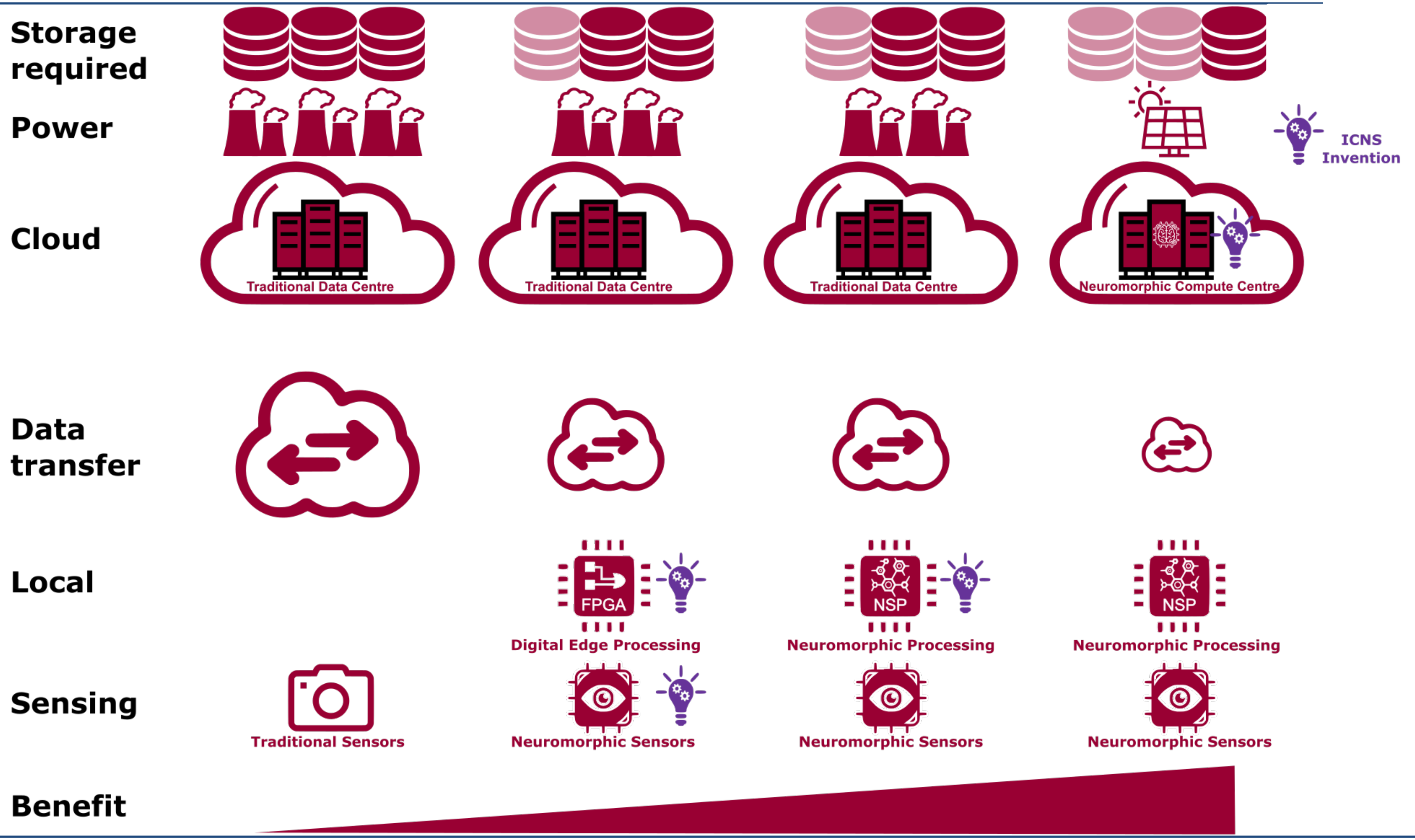


2. Real World Interaction

- Real time interaction needs local processing;
- Interaction means continuous stream of input;
- Interaction means decision making, active perception, living machines.

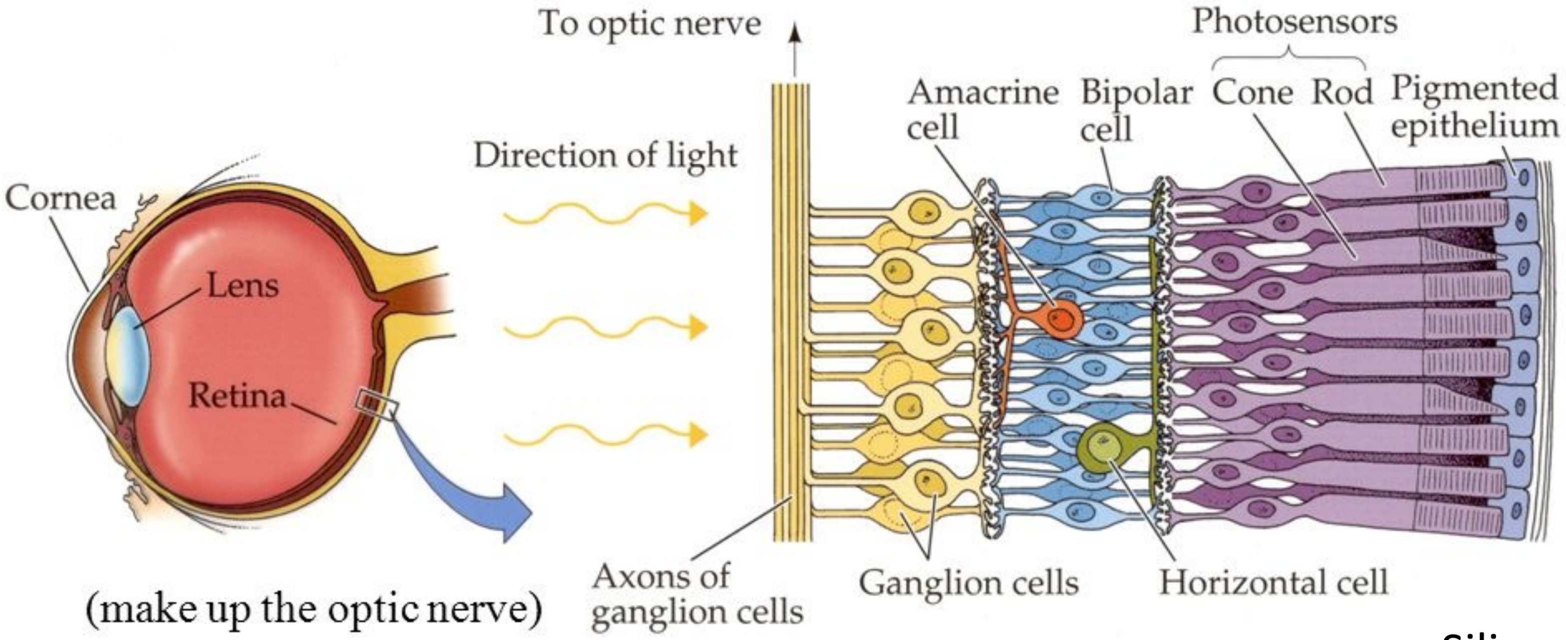
Part II: Roadmap

Roadmap for Neuromorphic Engineering



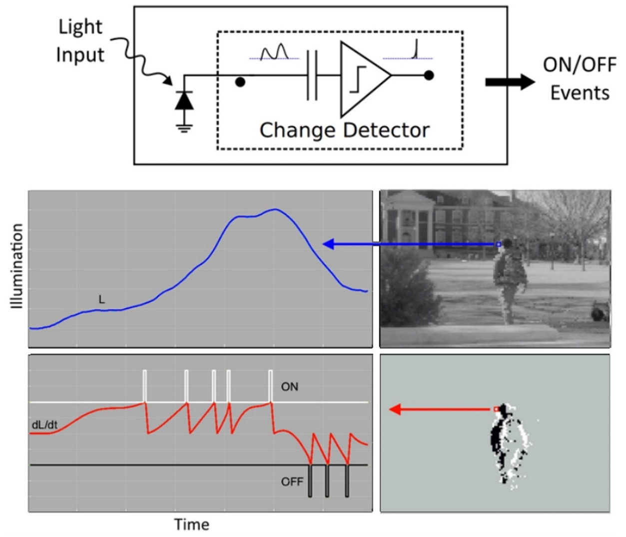
Modelling the eye

The eye

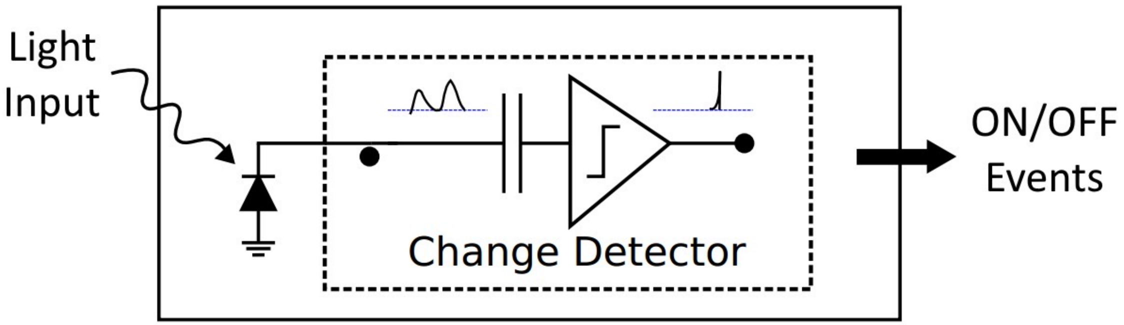


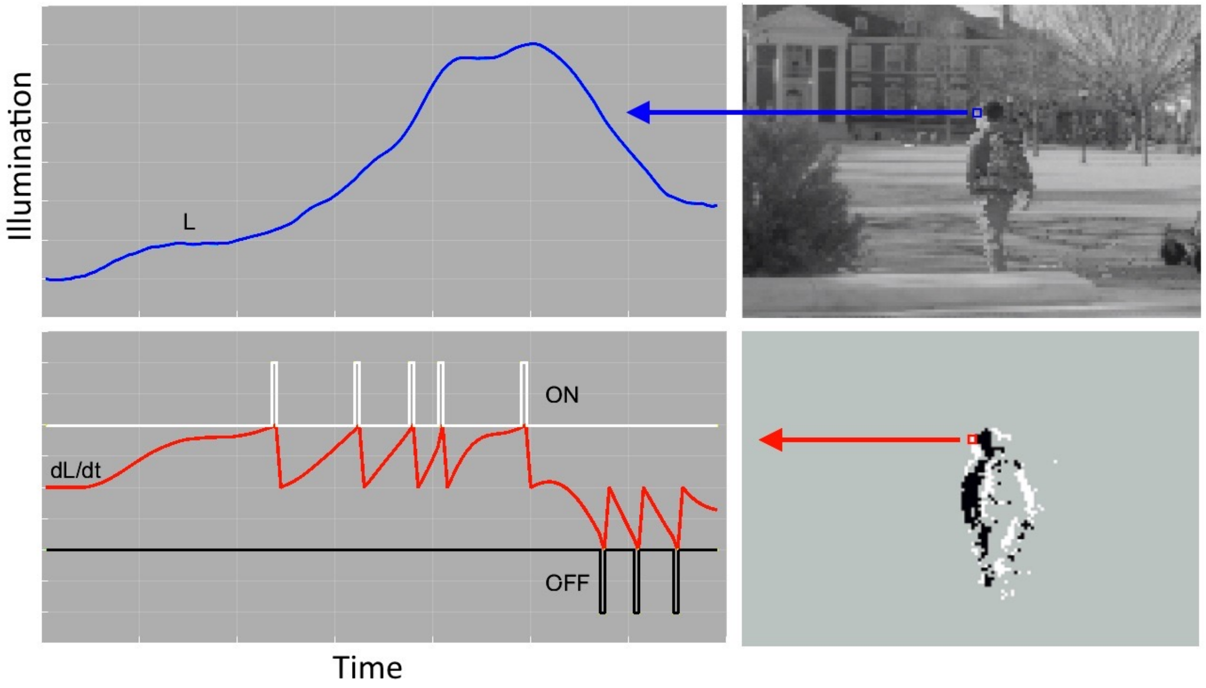
Silicon Retina

Single Event-Based Pixel



DVS Pixel


Light
Input
Change Detector
ON/OFF
Events


Illumination
L
ON
dL/dt
OFF
Time

The silicon retina

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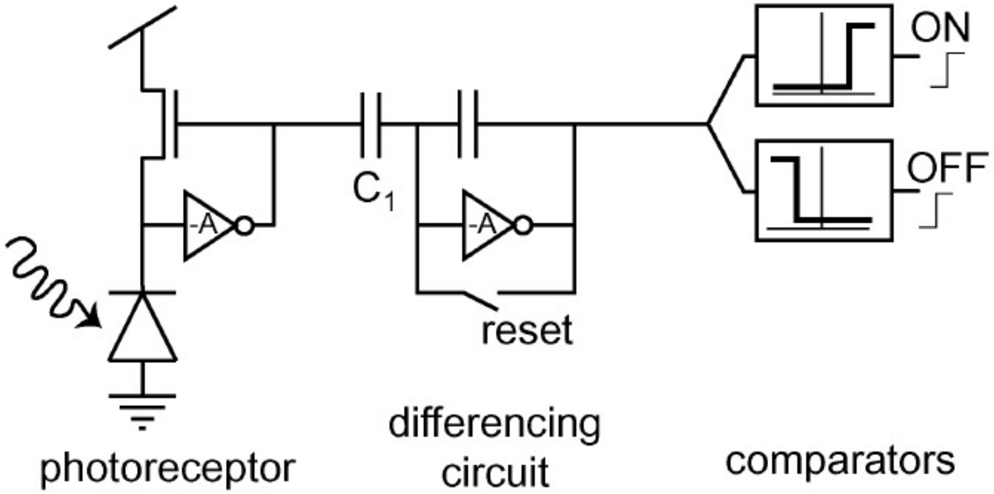
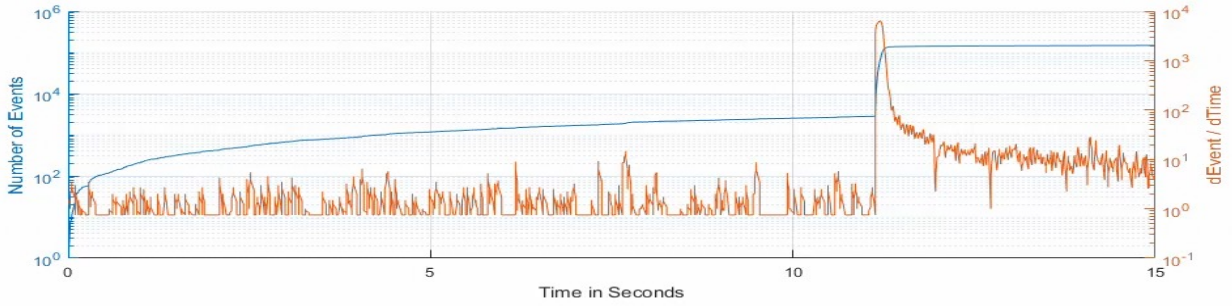


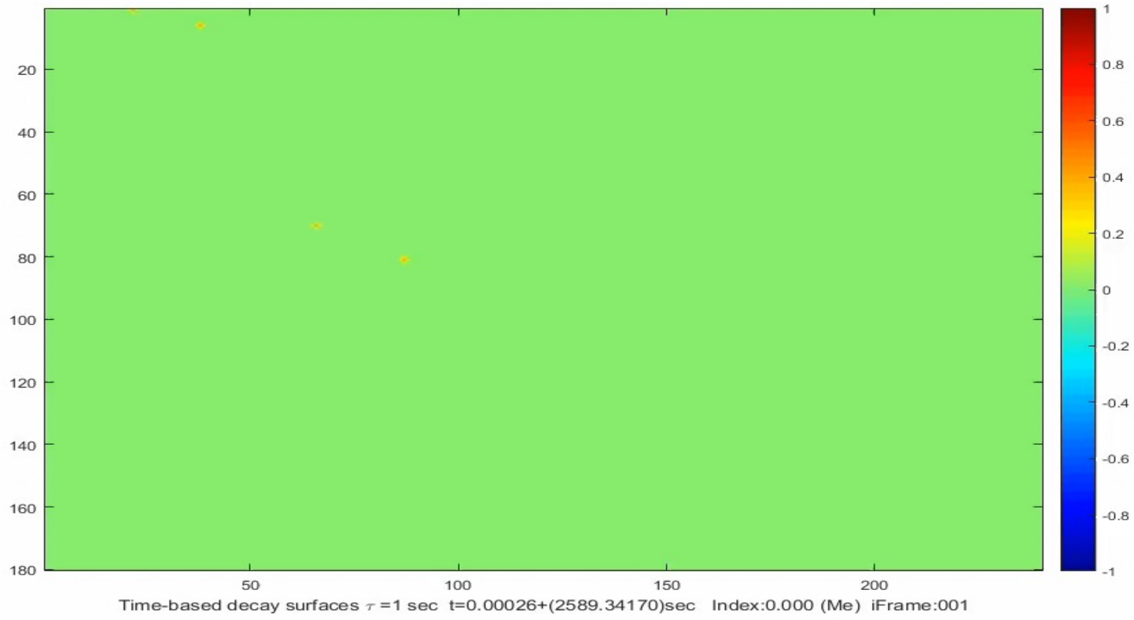
Year	2001	2003	2005	2006	2008	2009	2010	2010	2010
Source	Zaghloul, Boahen [30]	Rüedi et al. [16]	Mallik et al.[9, 32]	Lichtsteiner et al. [5, 33]	Massari et al. [27]	Ruedi et al.[31]	Posch et al. 2010 [34]	Linares-Barranco et al. [2]	Culurciello et al. [3]
Functionality	Asynchronous spatial and temporal contrast,	Frame-based spatial contrast and gradient direction, ordered output	Temporal frame-difference intensity change detection APS imager	Asynchronous temporal contrast dynamic vision sensor (DVS)	Binary spatial and temporal contrast	Digital log pixel + RISC proc.	Async. Time-based Image Sensor (ATIS)	Async. Weber Contrast (SC), with either rate or TTFS coding	Temporal intensity change or spatial difference can trigger readout
Type (Sec.3)	SC TD AE	SC FE	TD FE	TC AE	SD TD FE	SC, embedded	TC AE	SC AE	TD SD FE
Gray picture output			●			●	●	●	●
Pixel size um (lambda)	34x40 (170x200)	69x69 (276x276)	25x25 (**100x100**)	40x40 (200x200)	26x26.5 (130x130)	**14x14** (311x311)	30x30 (333x333)	80x80 (400x400)	16x21 (??)
Fill factor (%)	14%	9%	17%	8.1%	20%	20%	10%(TC)/20%(gray)	2.5%	**42%**
Fabrication process	0.35um 4M 2P	0.5um 3M 2P	0.5um 3M 2P	0.35um 4M 2P	0.35um 4M 2P	**180nm** 1P6M	**180nm** 4M 2P MIM	0.35um 4M 2P	**180nm** SiGe BiCMOS 7M
Pixel complexity T=MOS,C=cap	38T	>50T, 1C	**6T (NMOS) 2C**	26T(14 anal), 3C	45T	~80T, 1C	77T, 4C, 2PD	131T, 2C	**11T**
Array size	96x60	128x128	90x90	128x128	128x64	**320x240**	304x240	32x32	128x128
Die size mm^2	3.5x3.5	~10x10	3x3	6x6.3	11	5.2x8.4	9.9x8.2	2.5x2.6	??
Power consumption	62.7mW @ 3.3V	300mW @ 3.3V	30mW @ 5V (50 fps)	24mW @ 3.3V	**100uW@2V, 50fps**	**80mW** (11mW sensor)	50-175mW	0.66-6.6mW	<**1.4mW**@3V
Dynamic range	~50dB	120dB	51dB	120dB 2lux to >100 klux scene	100dB	**132dB** 6V/lux s 39dB SNR	**143dB** (static) 125dB@30FPS 56dB SNR	100dB 1lx to 100klx	2V/s/(uW/cm^2) @550nm. 1.14uV/e-
PD dark current@25C	?	300fA	?	4fA (~10nA/cm^2)	NA	44mV/s	1.6nA/cm^2	NA	
Response latency, frames/sec (fps), events/sec (eps)	~10Meps	< 2ms 60 to 500 fps	< 5ms? 200 fps?	15µs @ 1 klux chip illumination 2Meps	Max 4000fps	30fps	**3.2us**@1klux 30Meps peak, 6Meps sustained	100us @50klx 66Meps	200-800fps dep. on mode 13Meps
FPN matching	1-2 decades	2% contrast	**0.5%** of full scale, 2.1% TD change	2.1% contrast	10% contrast	**0.8%**		0.87% contrast	

T. Delbrück, B. Linares-Barranco, E. Culurciello and C. Posch, "Activity-driven, event-based vision sensors," Proceedings of 2010 IEEE International Symposium on Circuits and Systems, 2010, pp. 2426-2429, doi: 10.1109/ISCAS.2010.5537149.

Event-based data:

- Sparse during quiet, fast during bangs





Event-based data:

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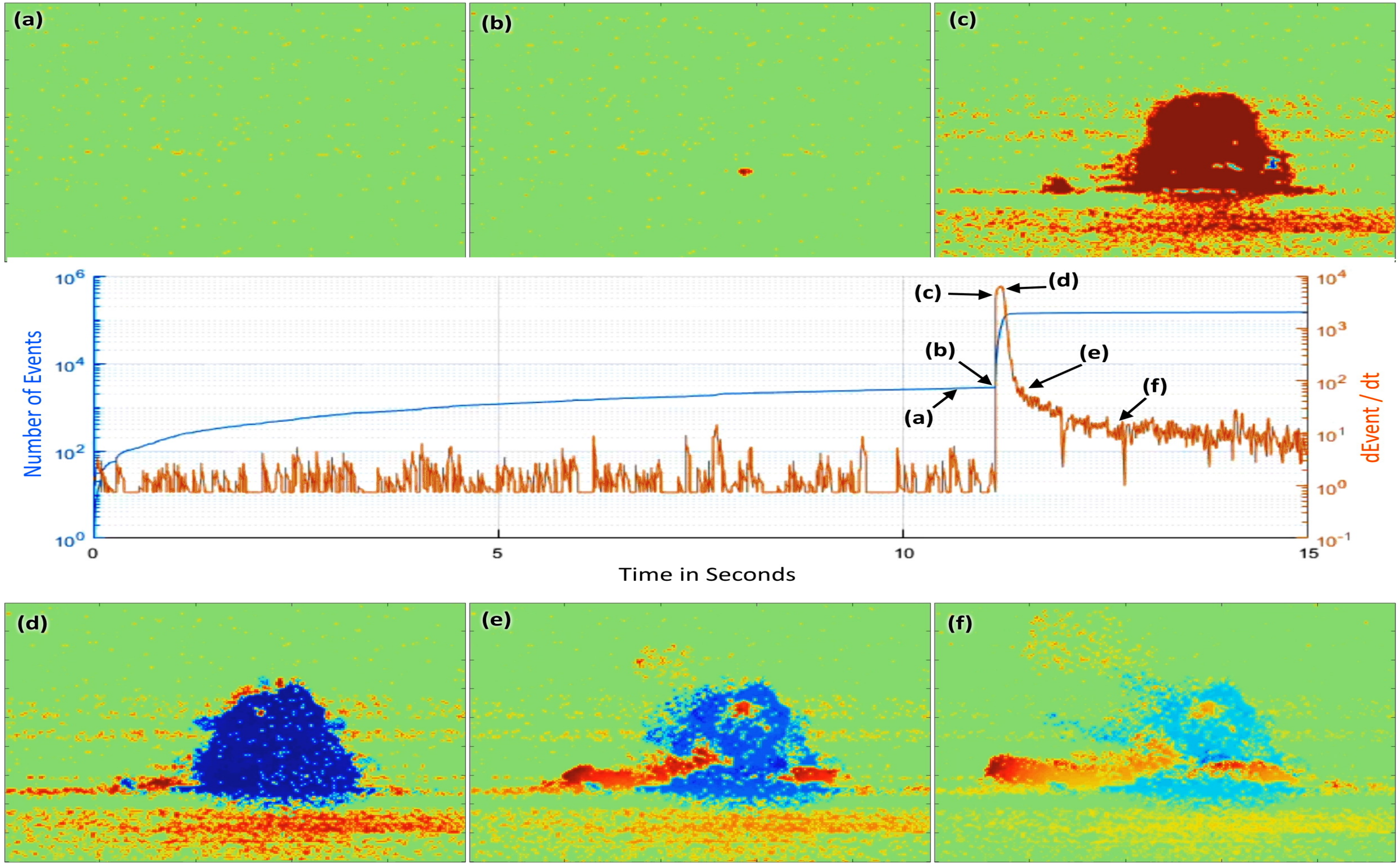
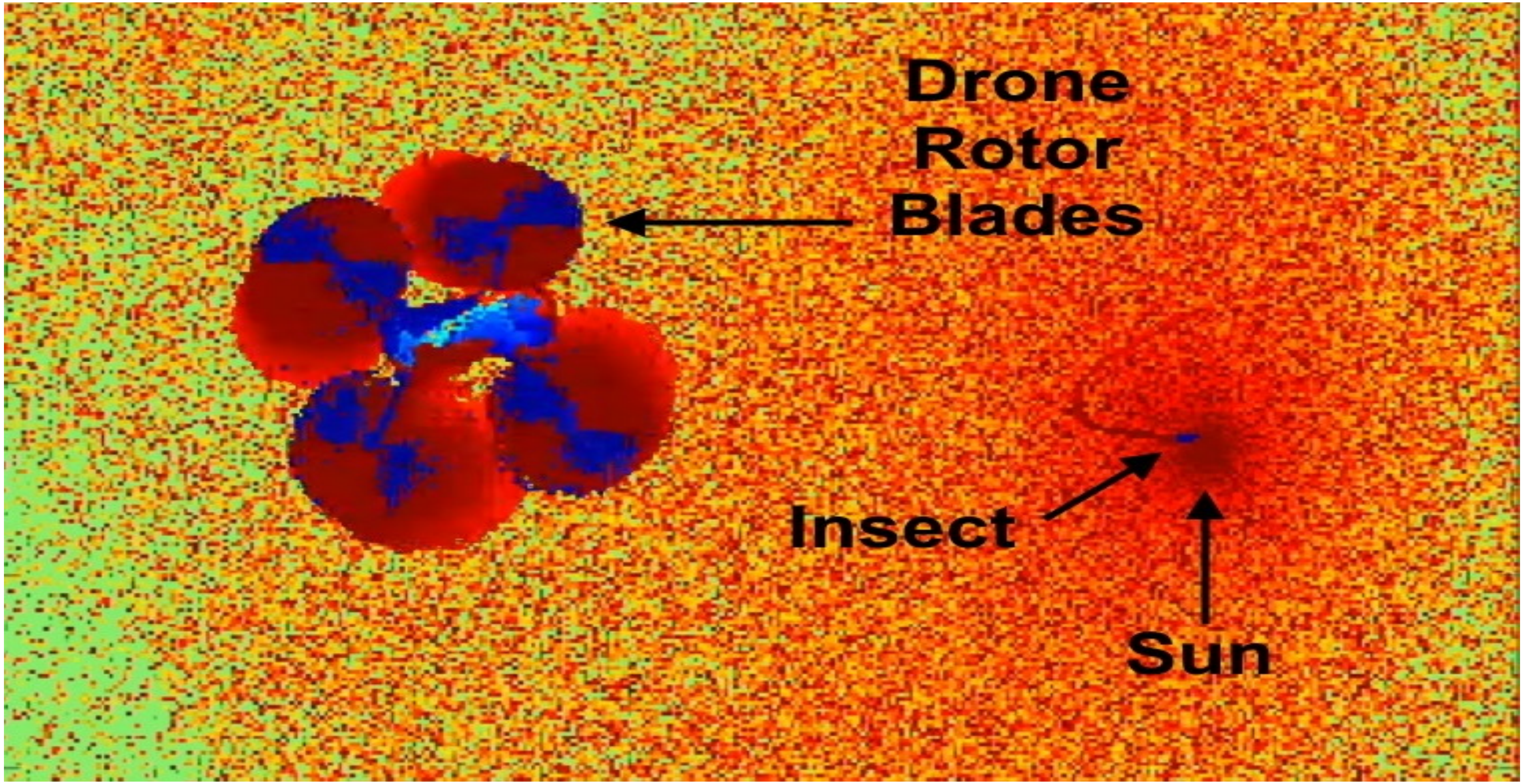
- Sparse during quiet, fast during bangs



Event-based data:

- High dynamic range



Modelling the ear

The cochlea

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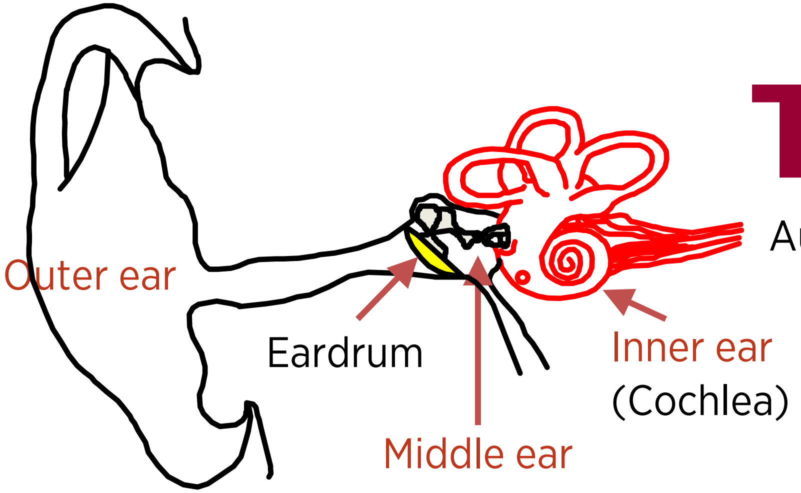
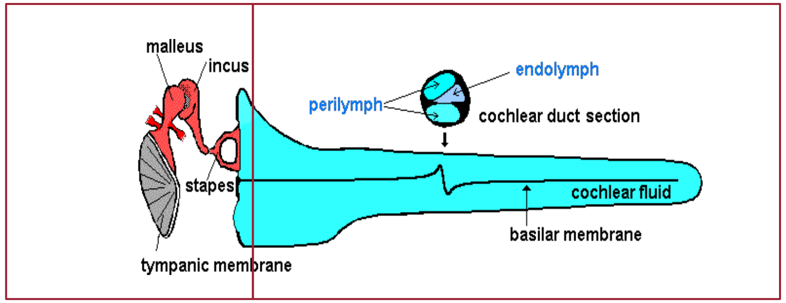
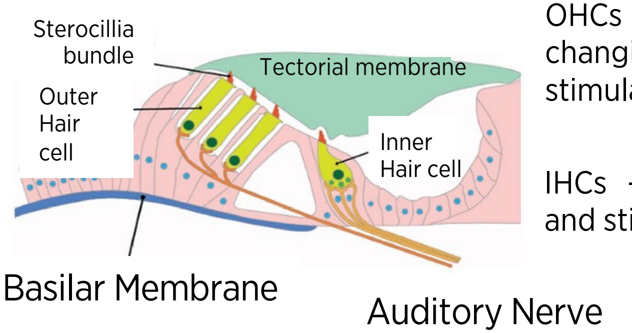


Uncoiled cochlea

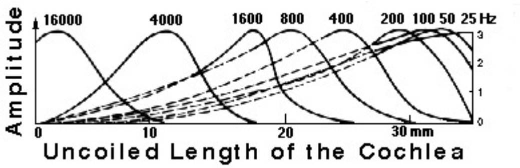
Position of maximum displacement on the BM varies as a function of frequency content of the input sound

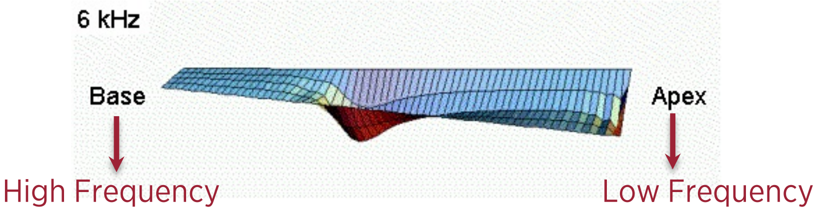




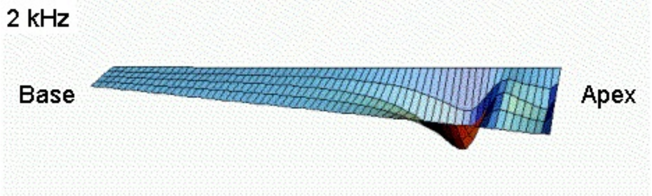
OHCs - actively amplify sound by changing their hair length under stimulation

IHCs - release neurotransmitter and stimulate the auditory nerve





Basilar membrane



BM: Basilar membrane
IHC: inner hair cell
OHC: outer hair cell

The silicon cochlea

- Analogue

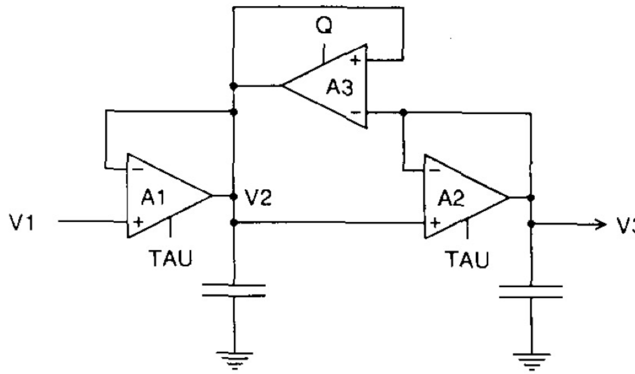


Fig. 7. Second-order filter section circuit. The TAU (τ) and Q control inputs set amplifier bias currents to control both the characteristic frequency and the peak height of the low-pass filter response.

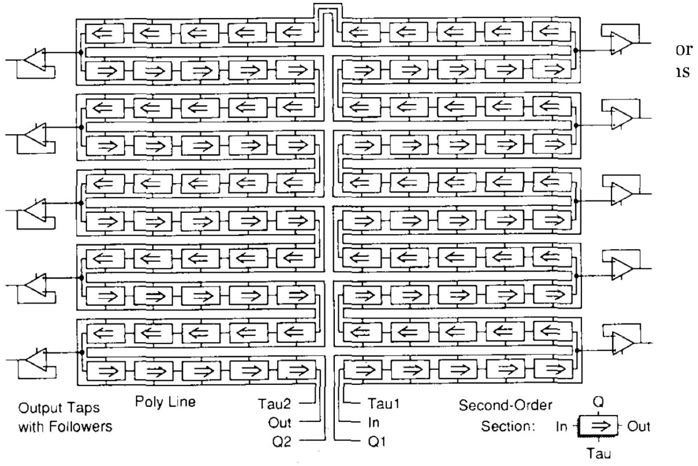
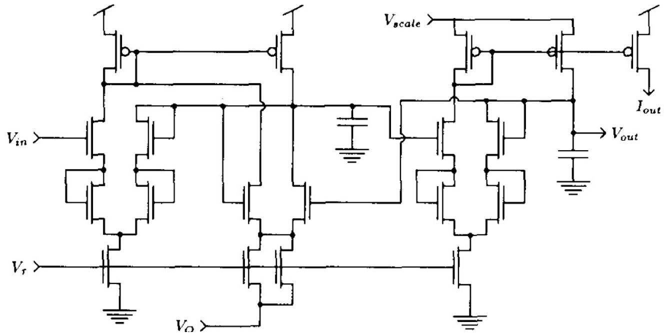
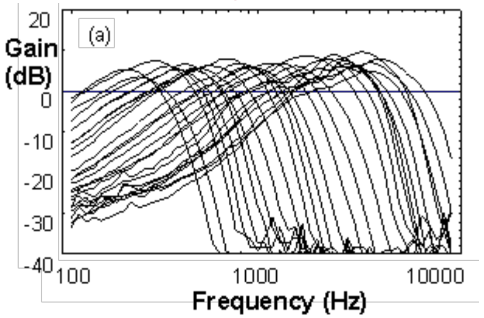


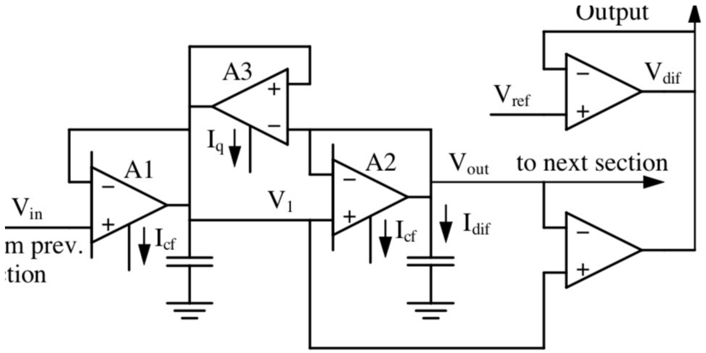
Fig. 8. Floorplan of 100-stage cochlea chip, in serpentine arrangement. The wires that are shown connecting the TAU and Q control terminals of the filter stages are built using a resistive polysilicon line, to act as a voltage divider that adjusts the bias currents in the cascade as an exponential function of distance from the input.

Lyon, Mead, 1988

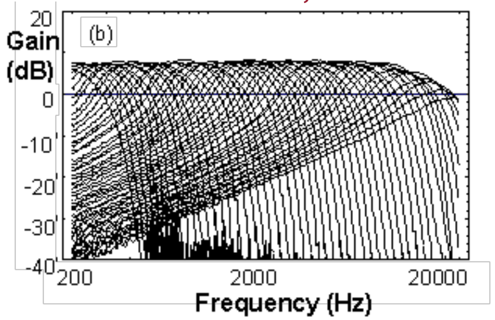


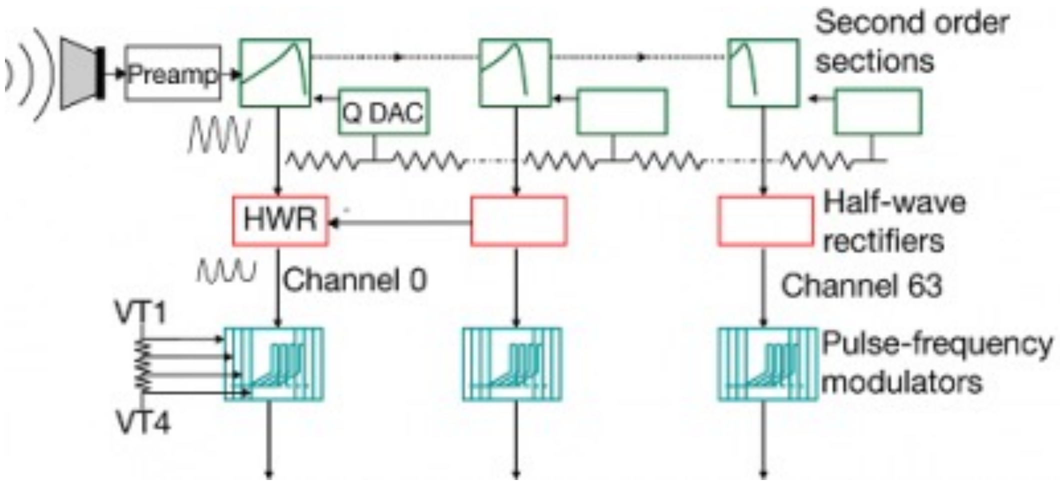
Watts, Kerns, Lyon, Mead, 1992





van Schaik, 1995

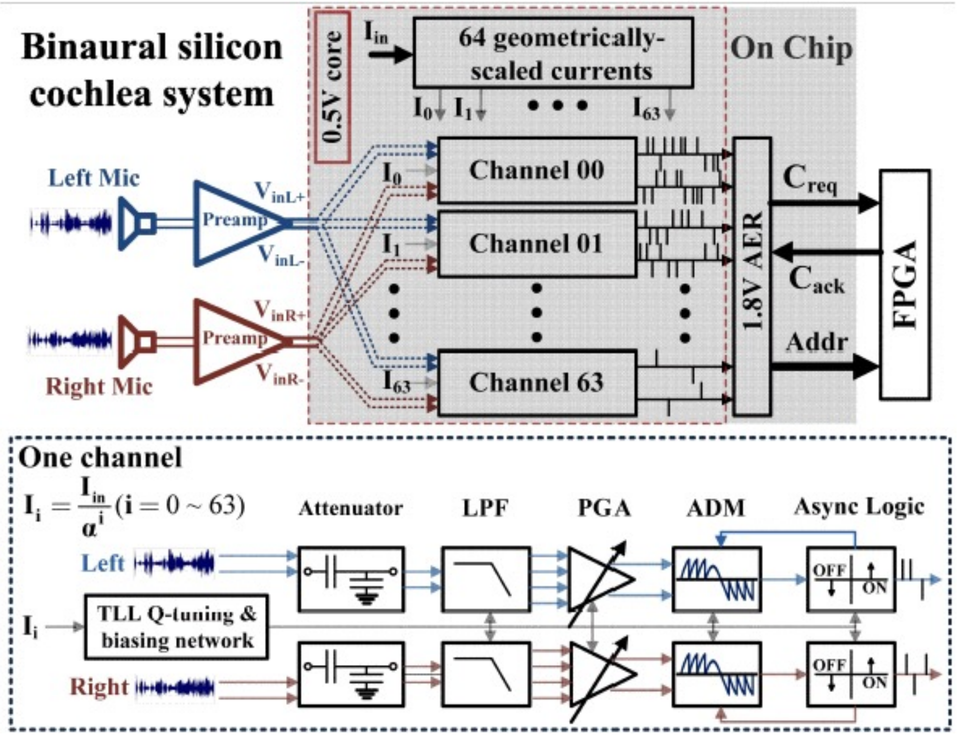




Liu, van Schaik, Minch, Delbruck, 2010

The silicon cochlea

- Analogue



Yang, Chien, Delbruck, Liu, 2016

Kiselev, Gao, Liu, 2022

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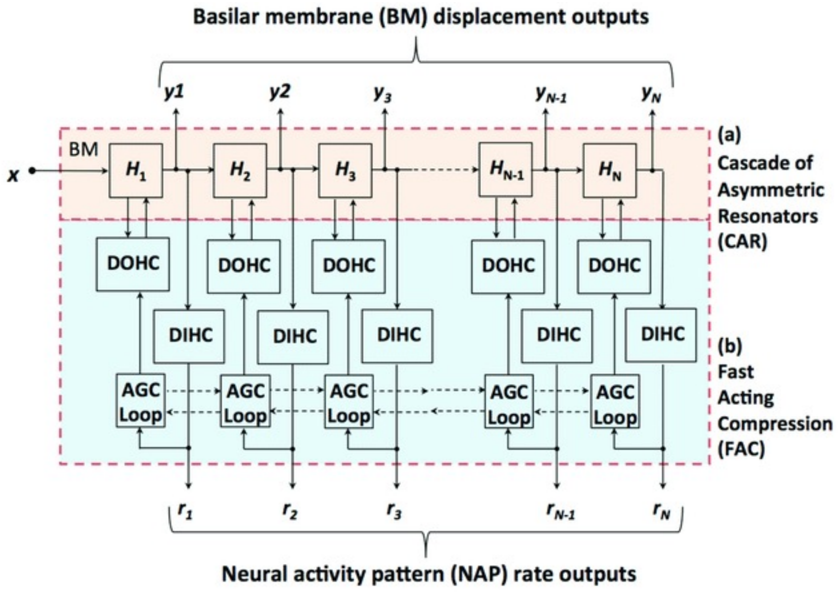
The silicon cochlea

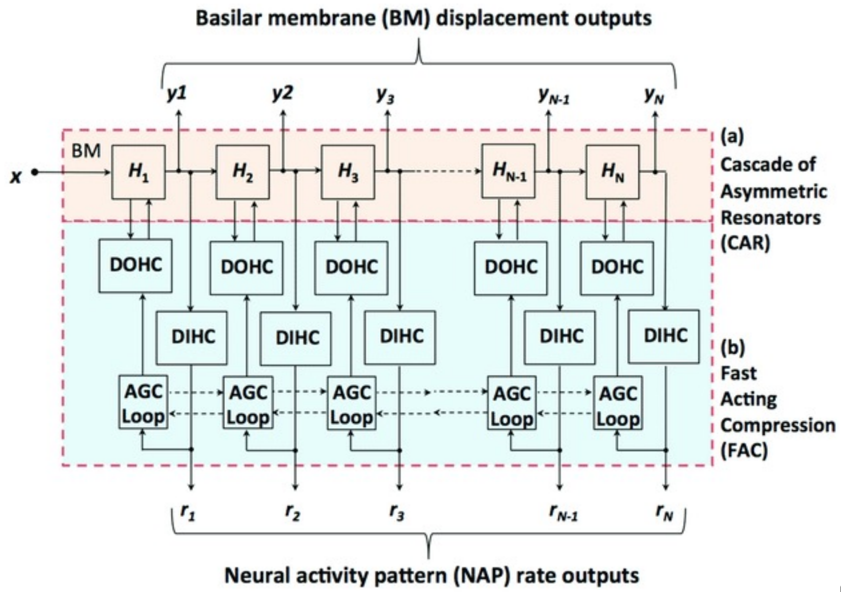
- Digital

CARFAC



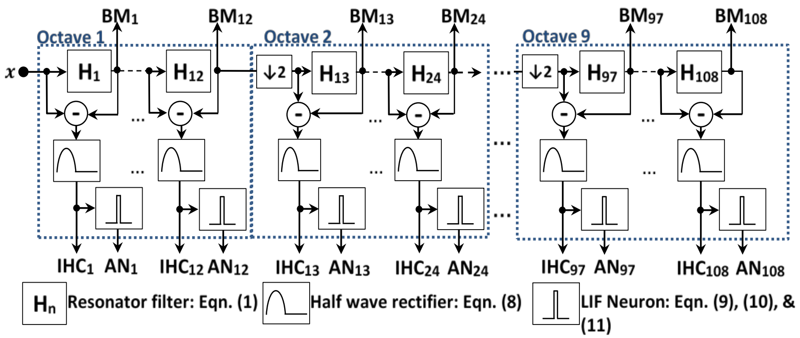
Dick Lyon, 2000

CARFAC



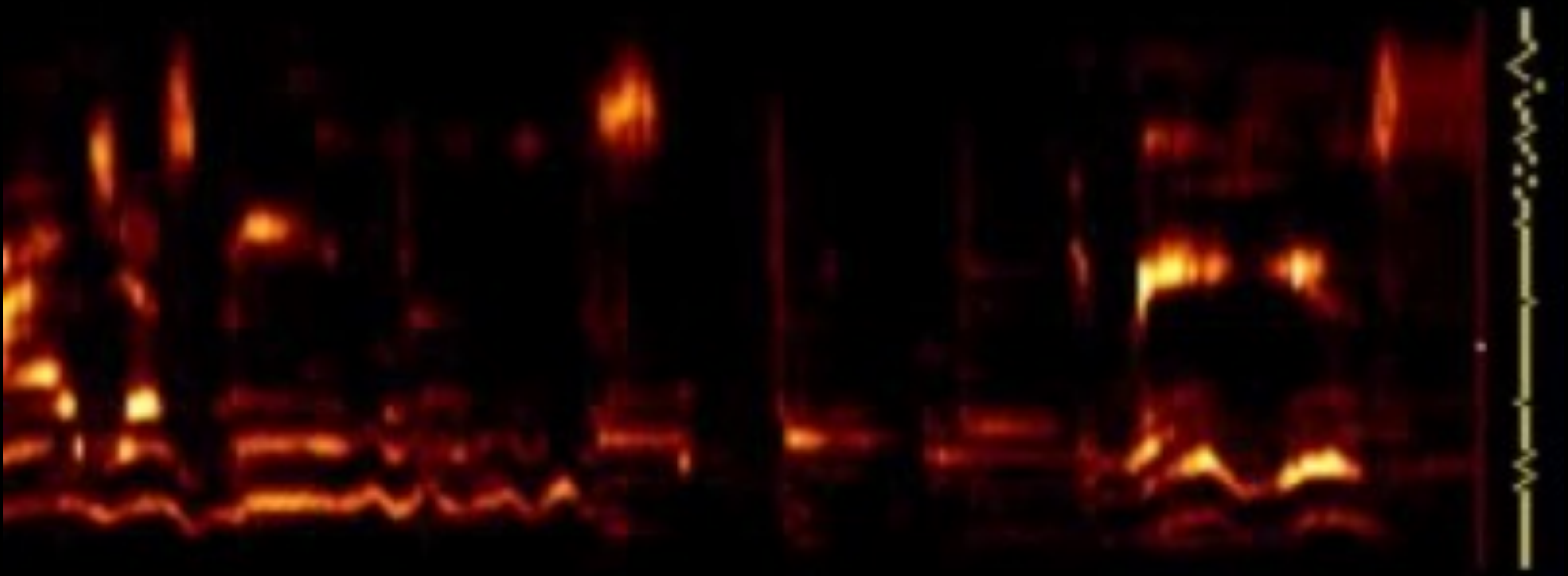
Ying Xu, 2018

CAR Lite



Ram Singh, 2018

Demonstration – a real-time CARFAC cochlear model



Other senses

- We have started work on Neuromorphic Olfaction (Smell)
- Some work is being done on Neuromorphic Tactile sensing (Touch)
- Some work on Neuromorphic Radar
- …

Applications

Neuromorphic space situational awareness

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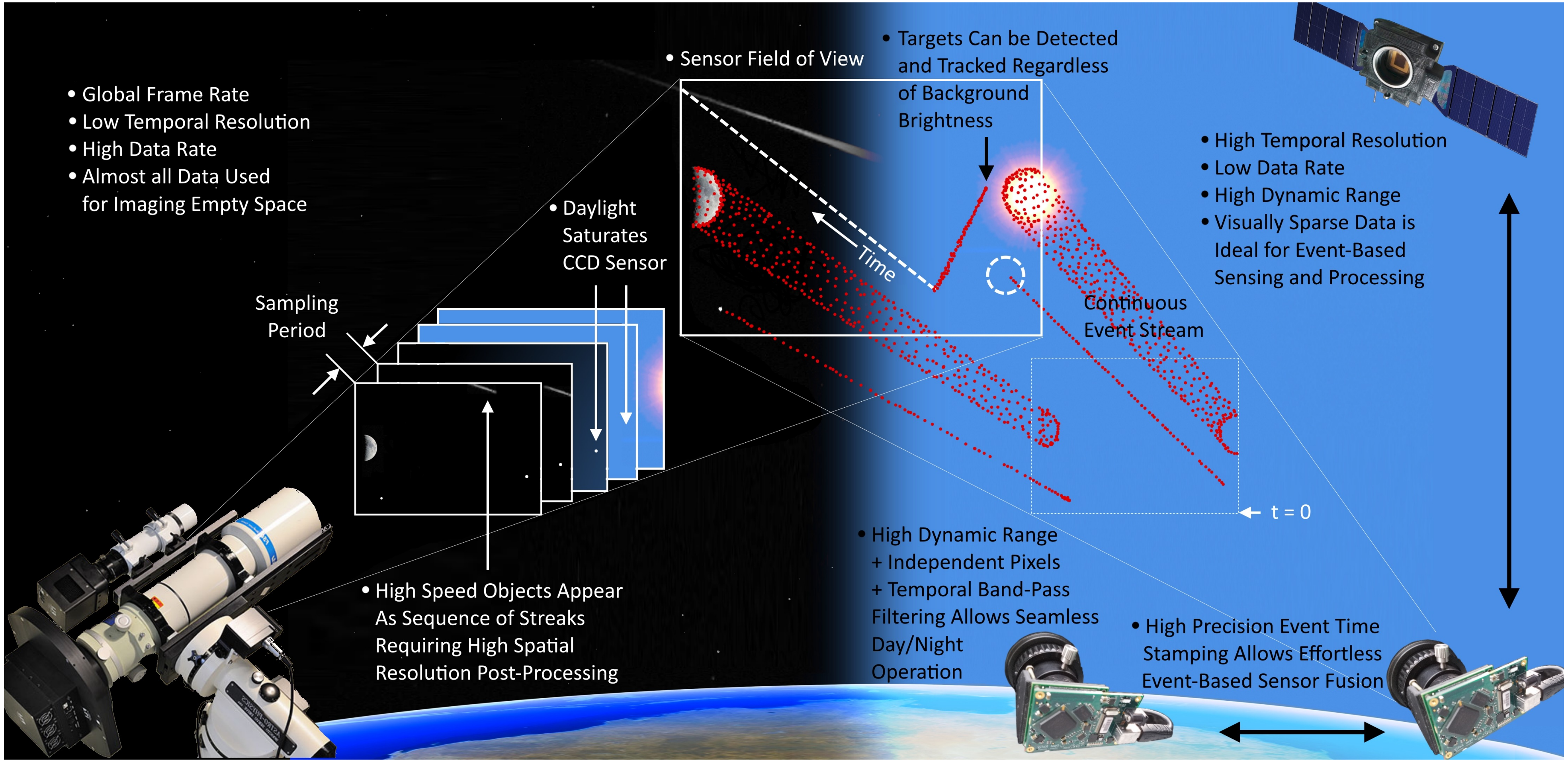

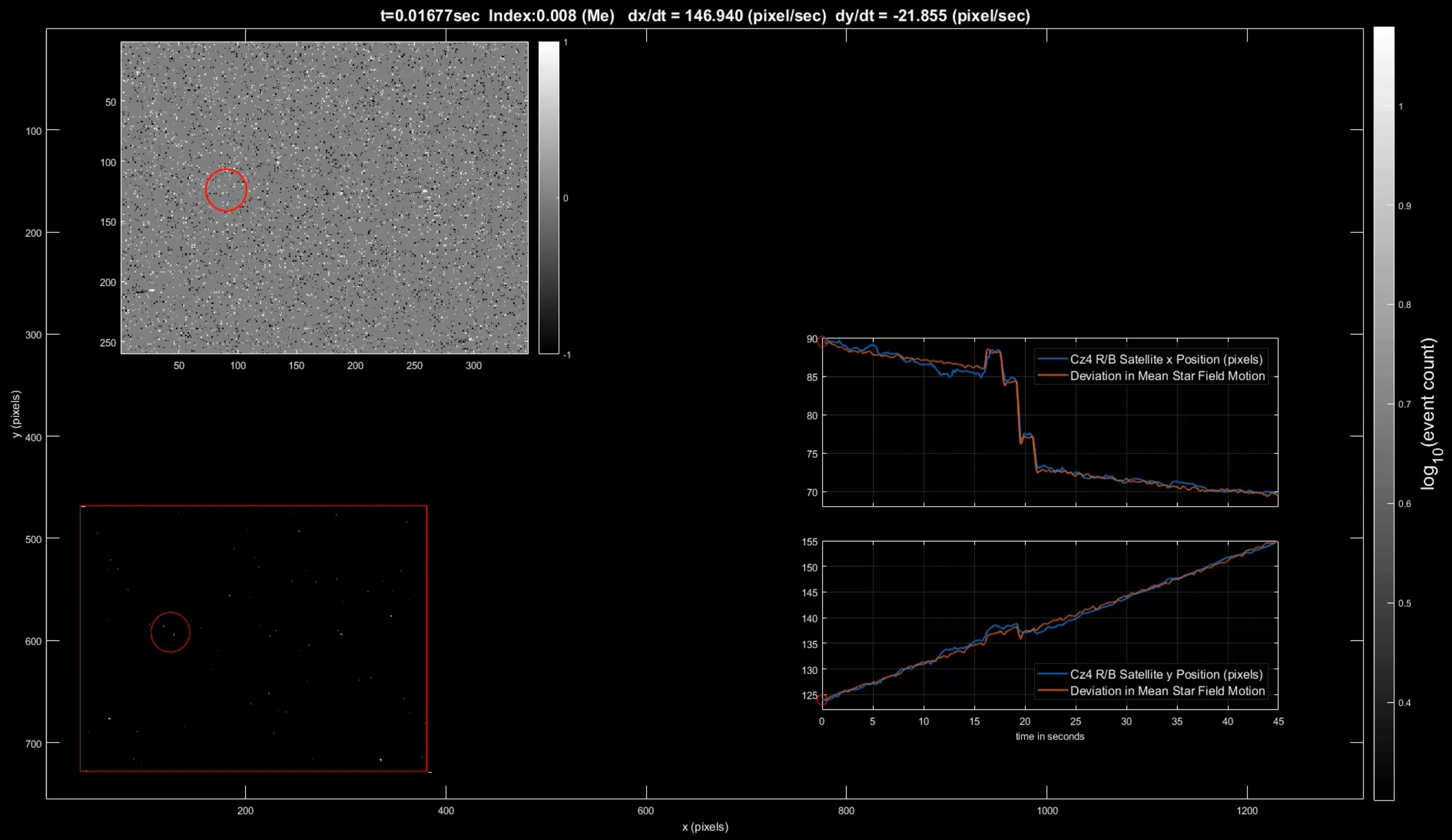

t=0.01677sec Index:0.008 (Me) dx/dt = 146.940 (pixel/sec) dy/dt = -21.855 (pixel/sec)
Cz4 R/B Satellite x Position (pixels)
Deviation in Mean Star Field Motion
Cz4 R/B Satellite y Position (pixels)
Deviation in Mean Star Field Motion
time in seconds
x (pixels)
y (pixels)
log10(event count)

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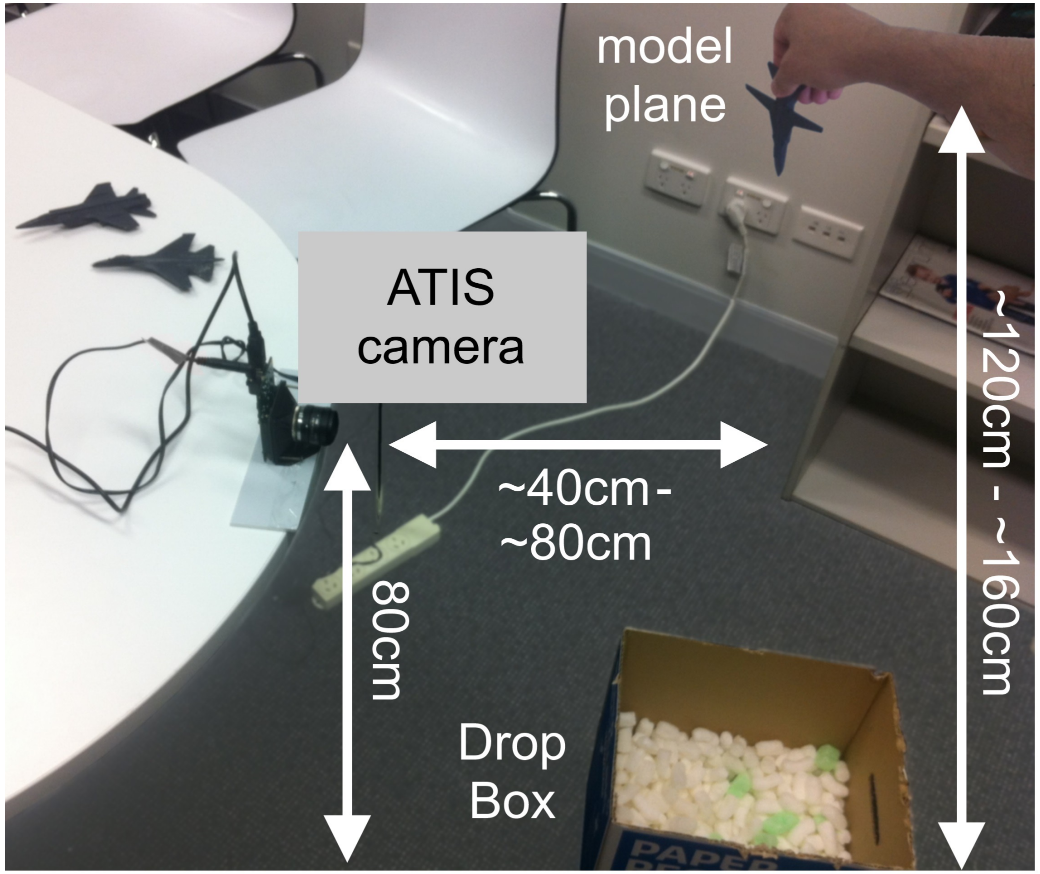
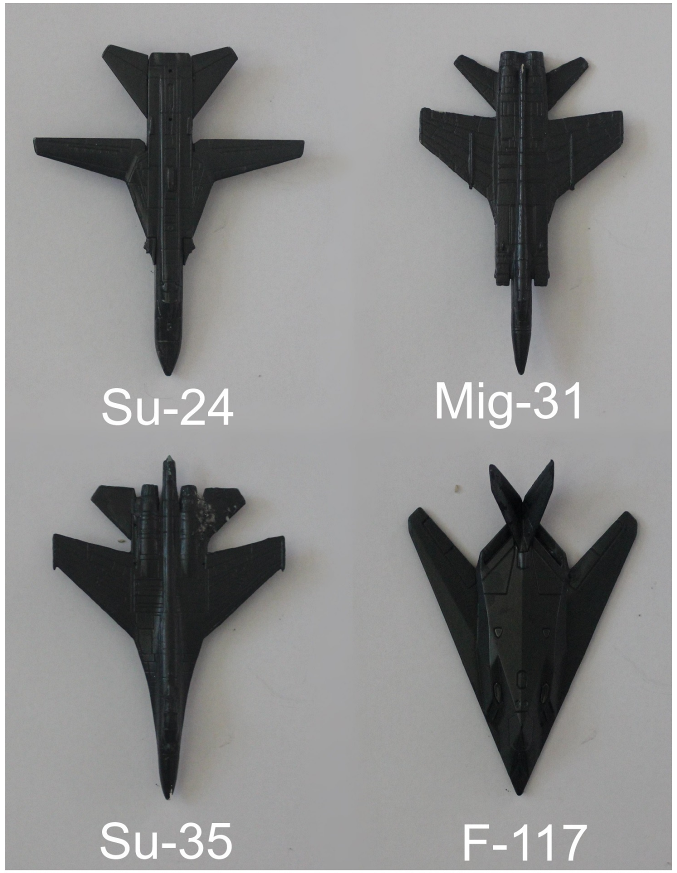
Event-based feature extraction using a plane dropping dataset

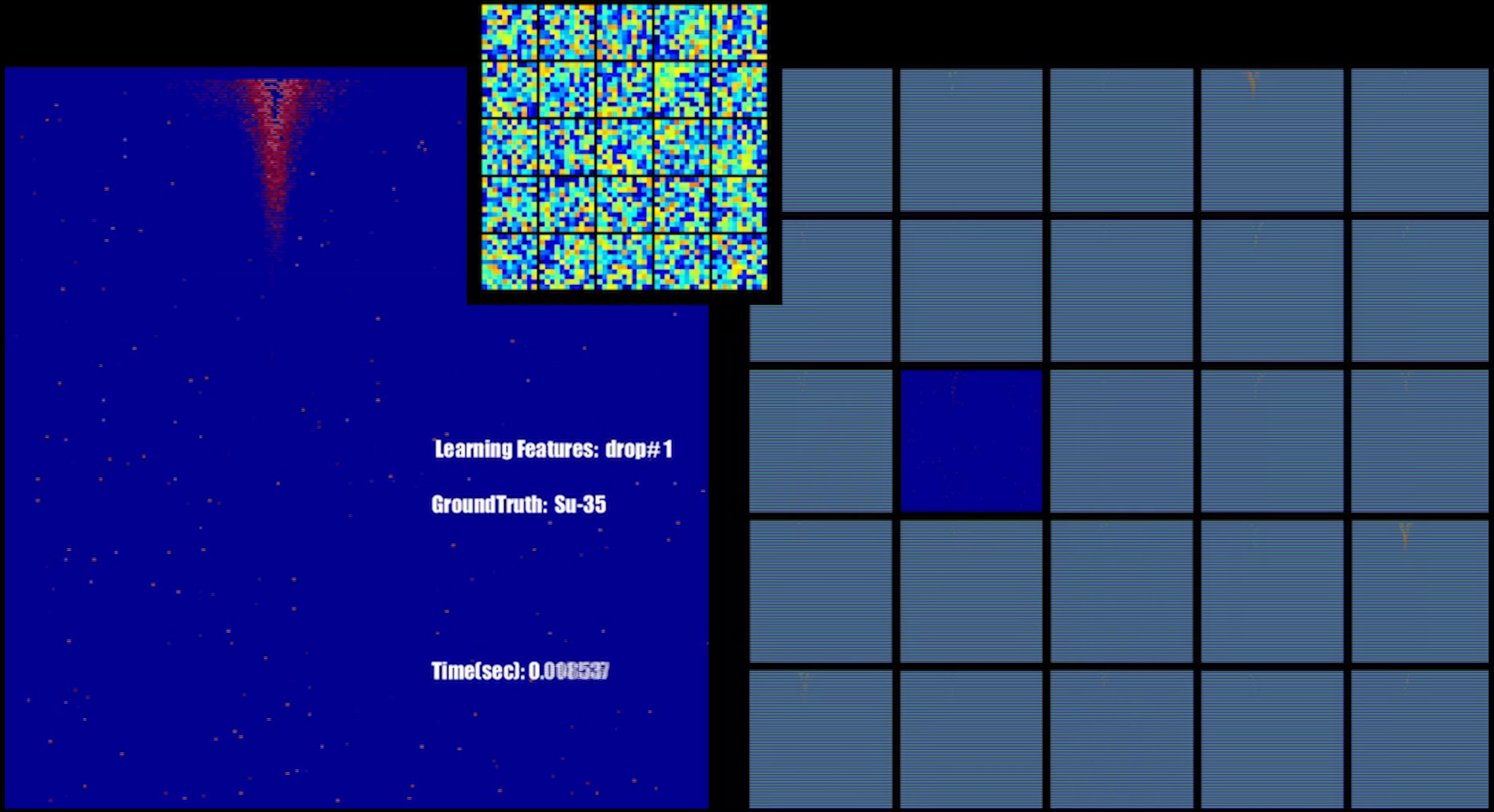


(a)



(b)

Event-based feature extraction using a plane dropping dataset



Whale watching

Event-based scene segregation

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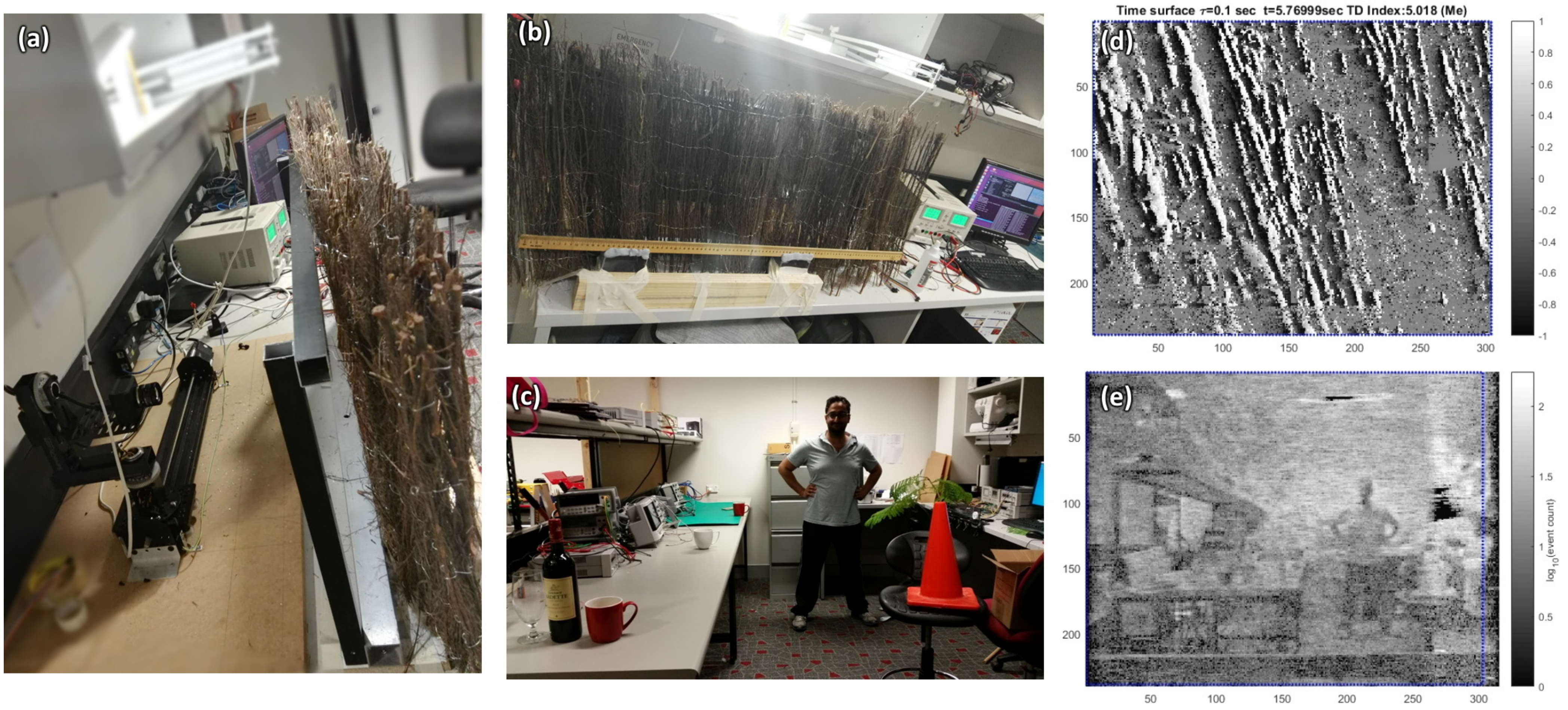
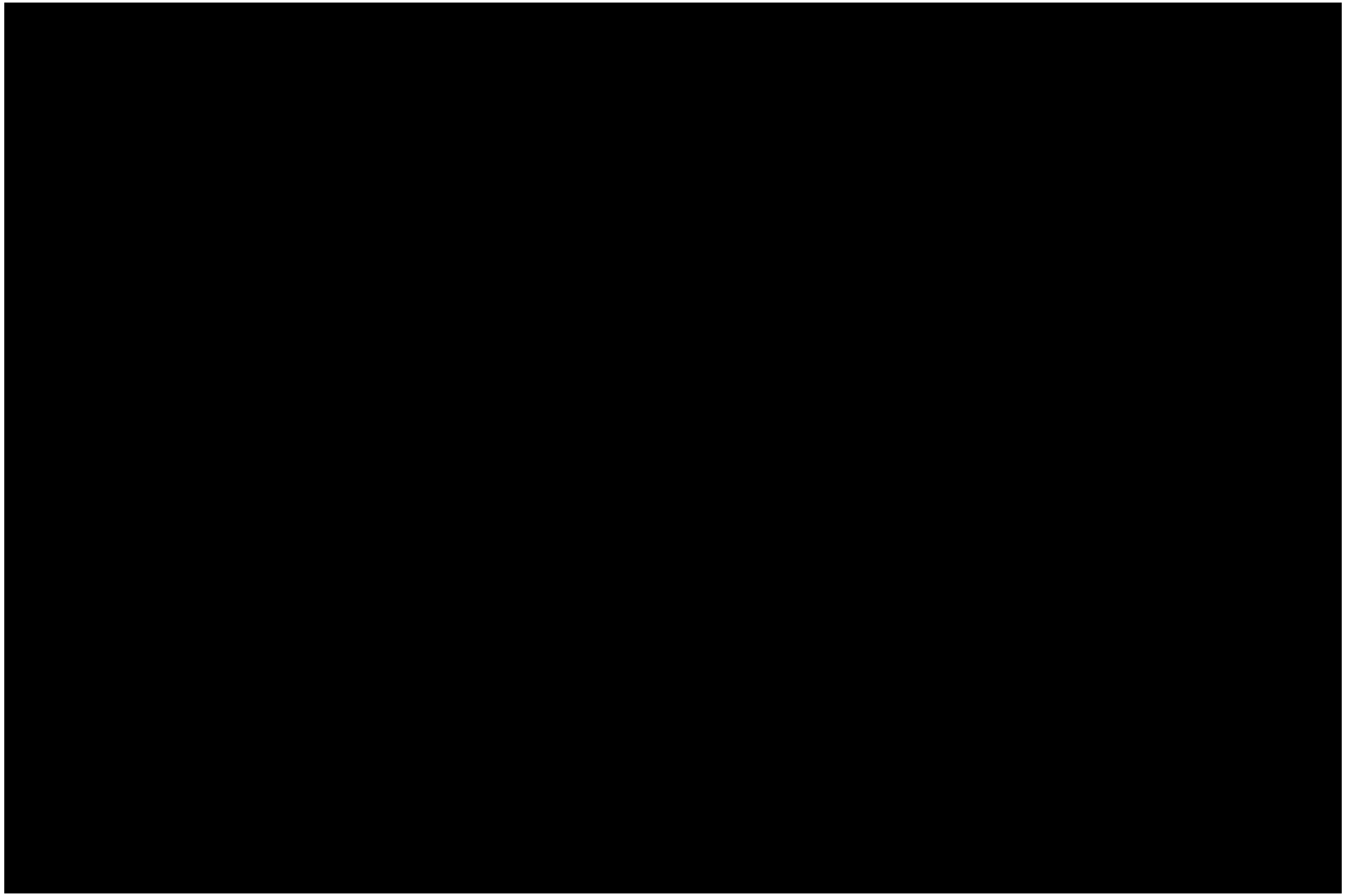


Event-based scene segregation



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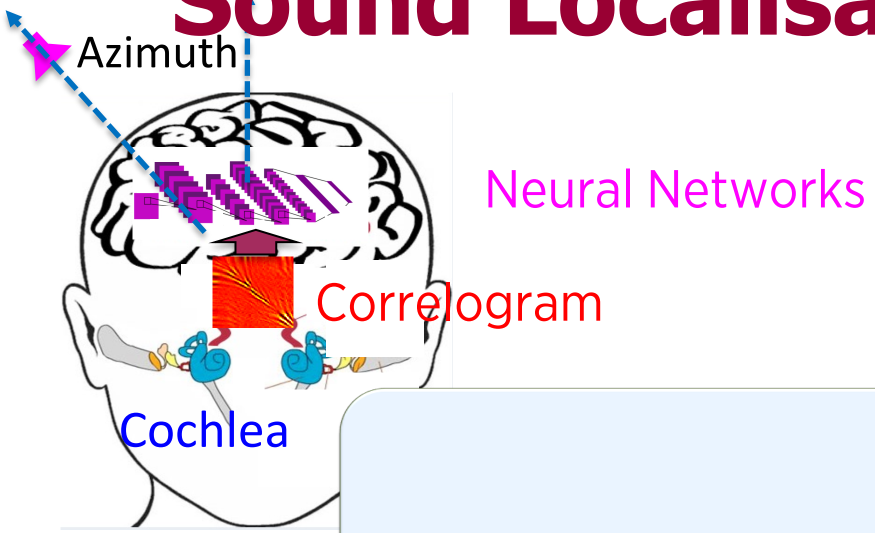
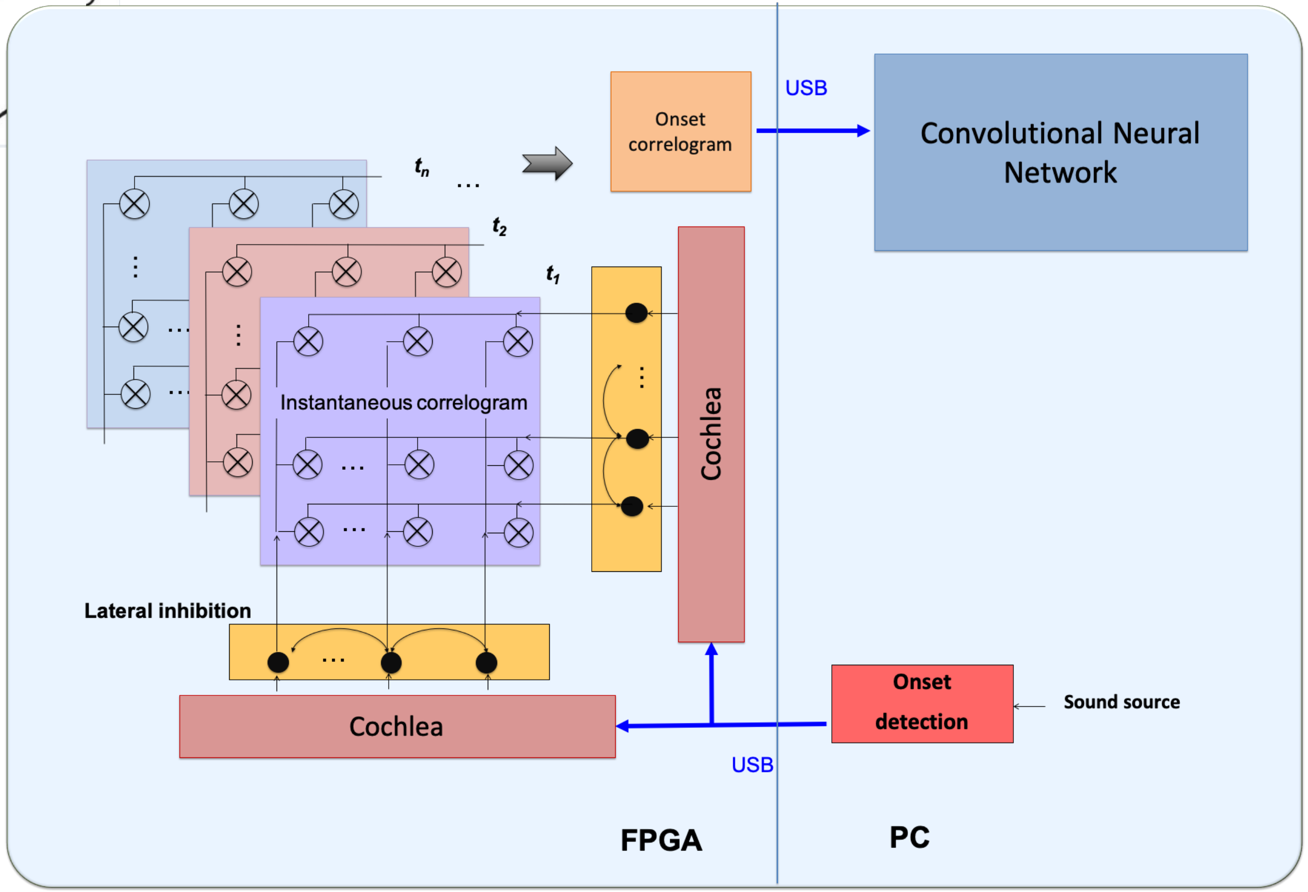
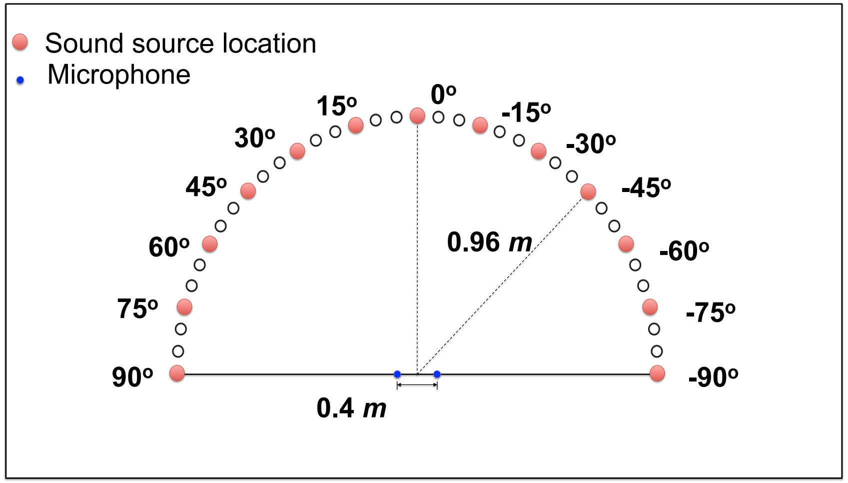
Sound Localisation in a reverberant room





Reverberant office recordings:
10 isolated spoken digits from Austalk
5 talkers



AusTalk (An audio-visual corpus of Australian English)
CNN: convolutional neural network

Sound Localisation in a reverberant room

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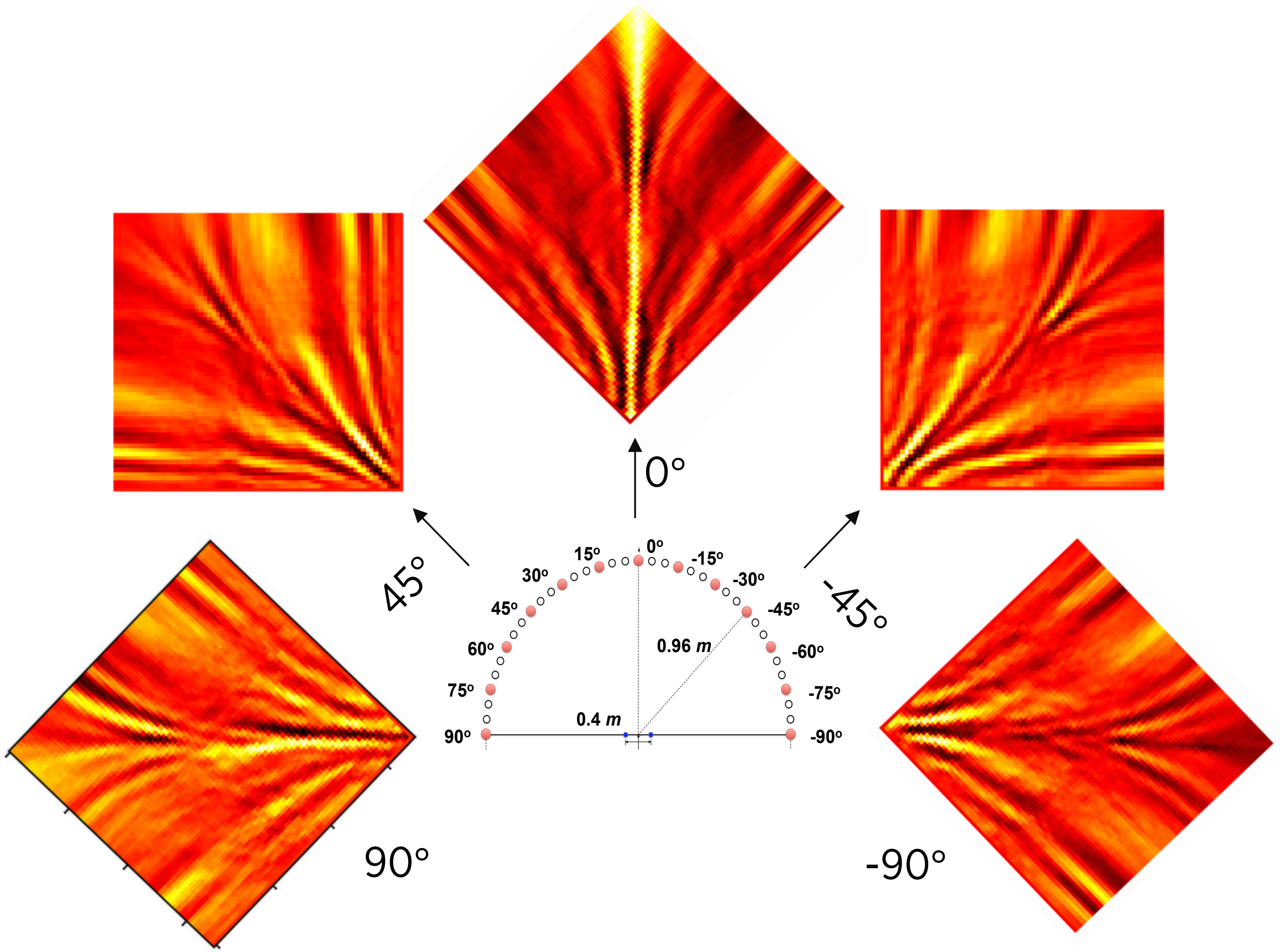
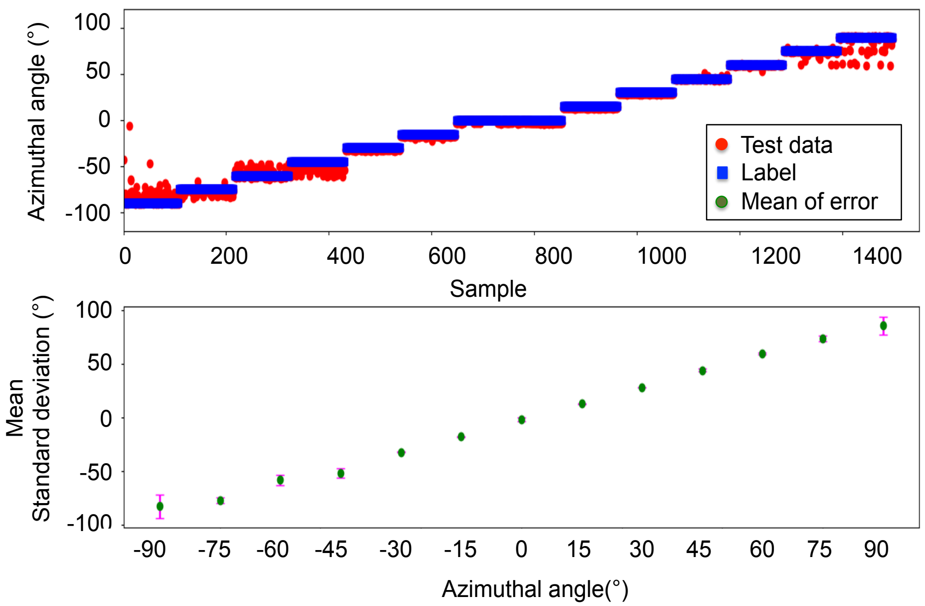
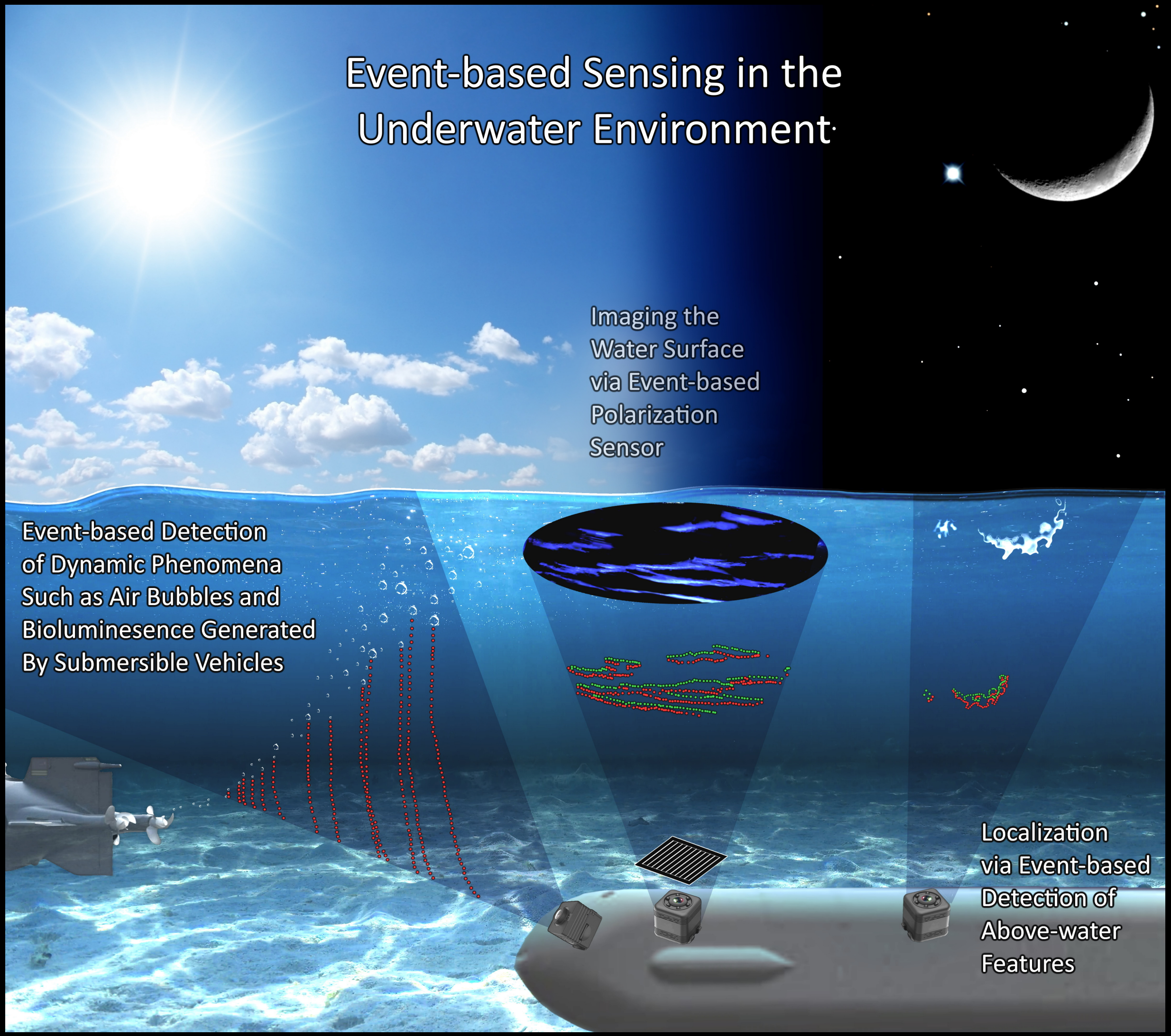


3-layer CNN regression




Event-based Sensing in the
Underwater Environment
Imaging the
Water Surface
via Event-based
Polarization
Sensor
Event-based Detection
of Dynamic Phenomena
Such as Air Bubbles and
Bioluminesence Generated
By Submersible Vehicles
Localization
via Event-based
Detection of
Above-water
Features

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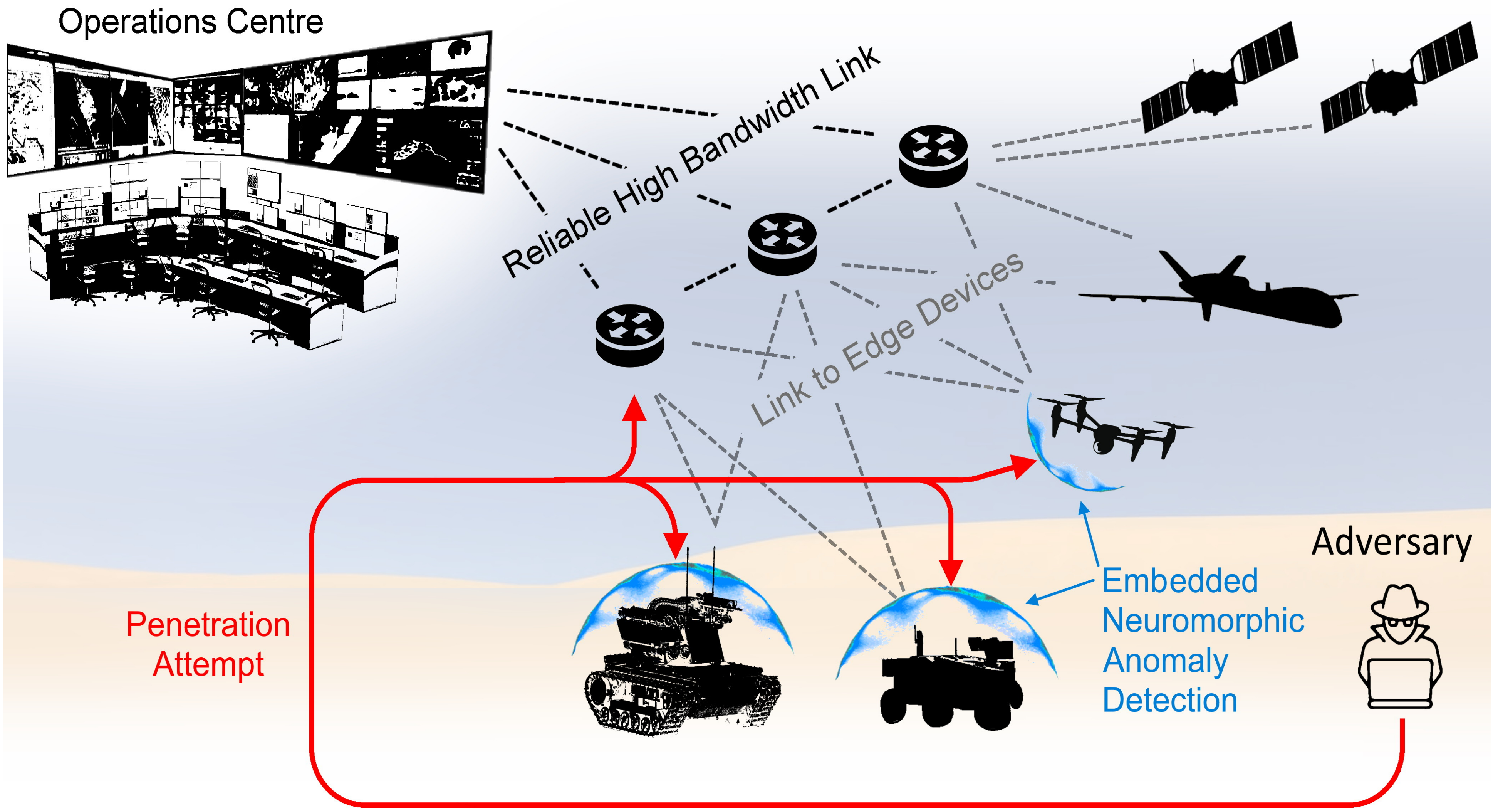

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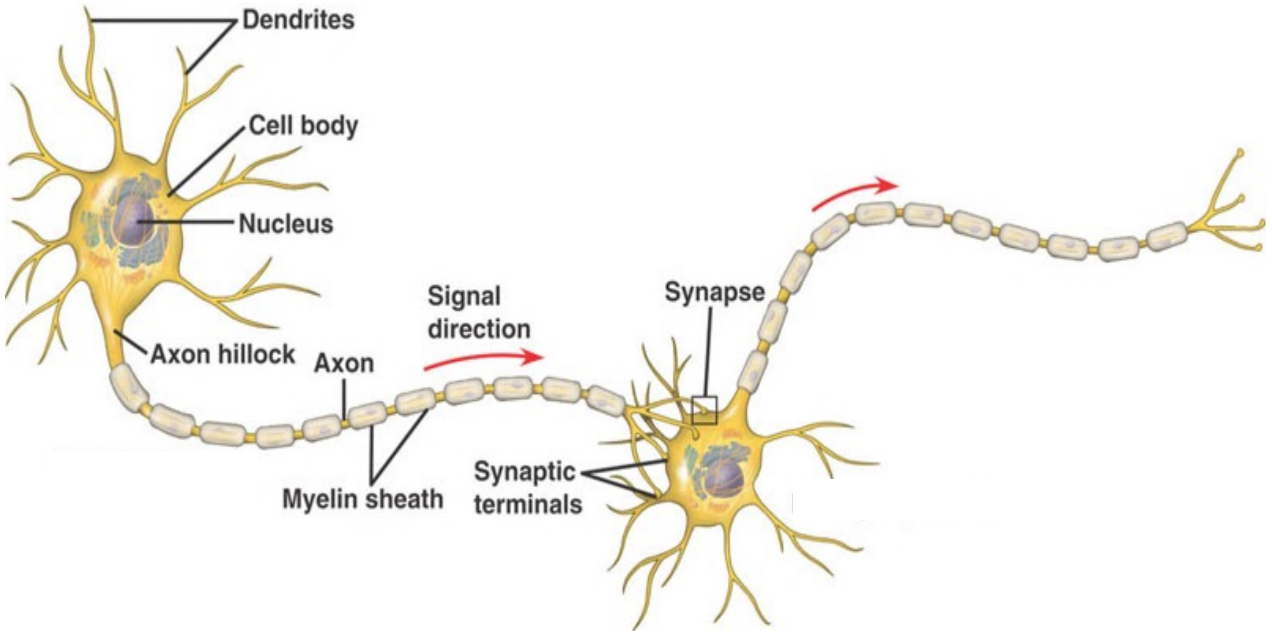
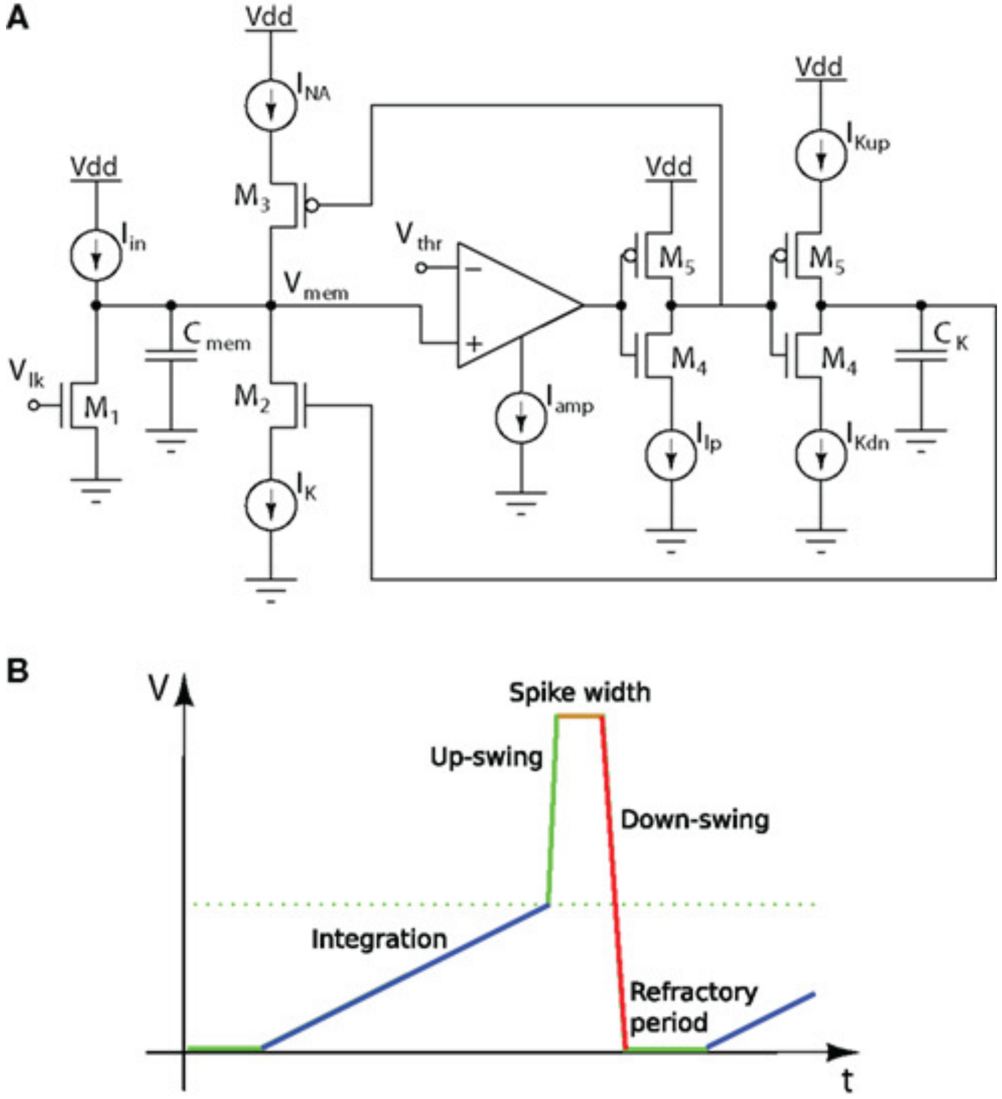
Modelling neurons in silicon

Neuron Model





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REVIEW article

Front. Neurosci., 31 May 2011 | https://doi.org/10.3389/fnins.2011.00073

Neuromorphic silicon neuron circuits

Giacomo Indiveri[1]*, Bernabé Linares-Barranco[2], Tara Julia Hamilton[3], André van Schaik[4], Ralph Etienne-Cummings[5], Tobi Delbruck[1], Shih-Chii Liu[1], Piotr Dudek[6], Philipp Häfliger[7], Sylvie Renaud[8], Johannes Schemmel[9], Gert Cauwenberghs[10], John Arthur[11], Kai Hynna[11], Fopefolu Folowosele[5], Sylvain Saighi[8], Teresa Serrano-Gotarredona[2], Jayawan Wijekoon[6], Yingxue Wang[12] and Kwabena Boahen[11]

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[4] School of Electrical and Information Engineering, University of Sydney, Sydney, NSW, Australia

[5] Whiting School of Engineering, Johns Hopkins University, Baltimore, MD, USA

[6] School of Electrical and Electronic Engineering, University of Manchester, Manchester, UK

[7] Department of Informatics, University of Oslo, Oslo, Norway

[8] Laboratoire de l'Intégration du Matériau au Système, Bordeaux University and IMS-CNRS Laboratory, Bordeaux, France

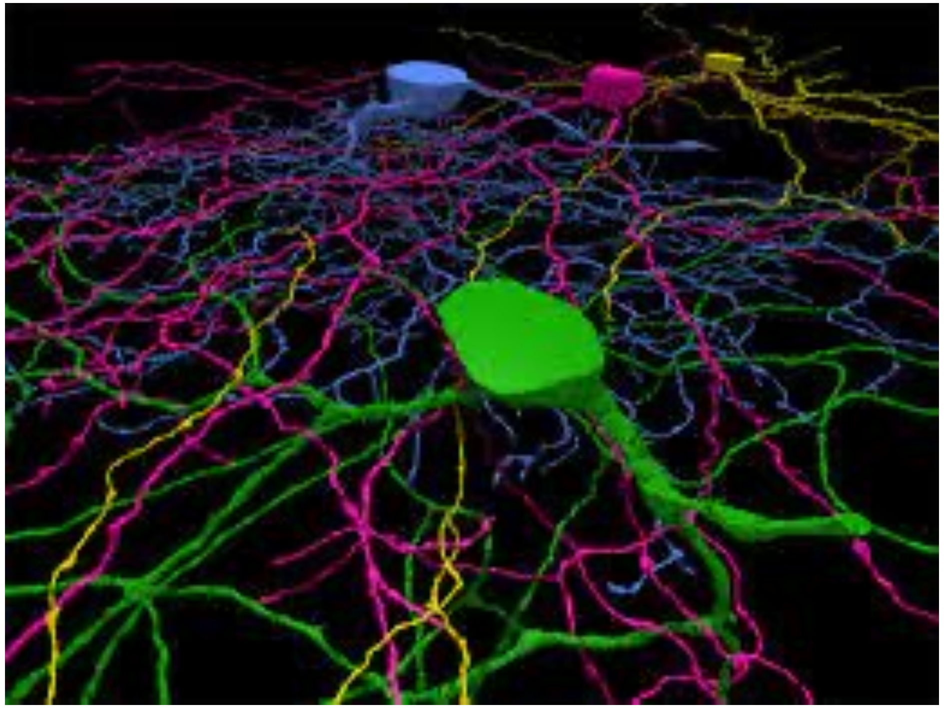
[9] Kirchhoff Institute for Physics, University of Heidelberg, Heidelberg, Germany

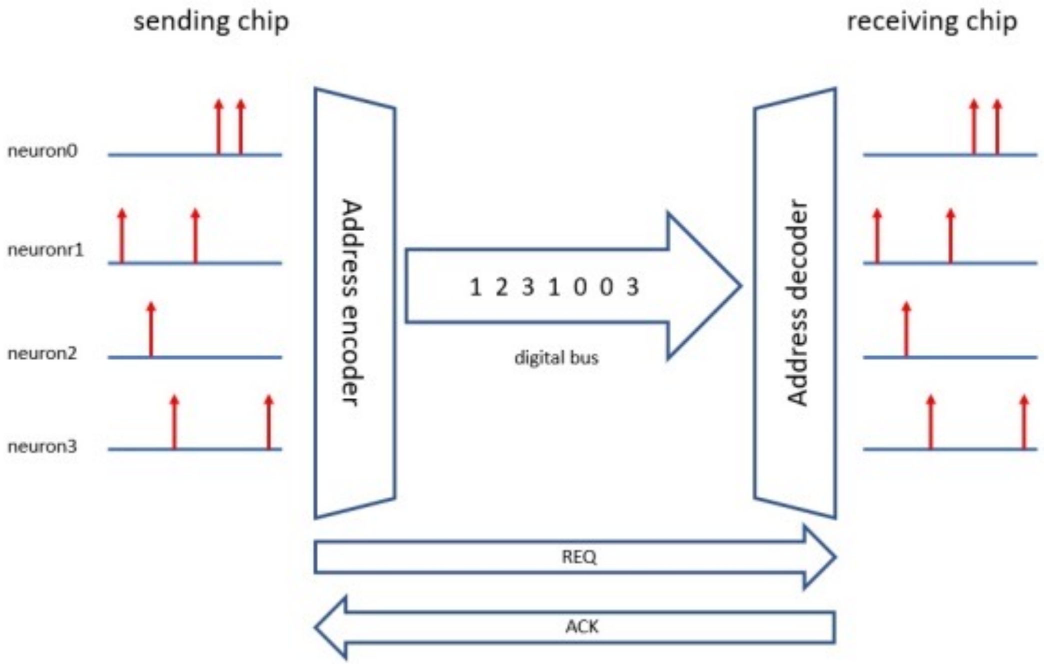
[10] Department of Bioengineering and Institute for Neural Computation, University of California San Diego, La Jolla, CA, USA

[11] Stanford Bioengineering, Stanford University, Stanford, CA, USA

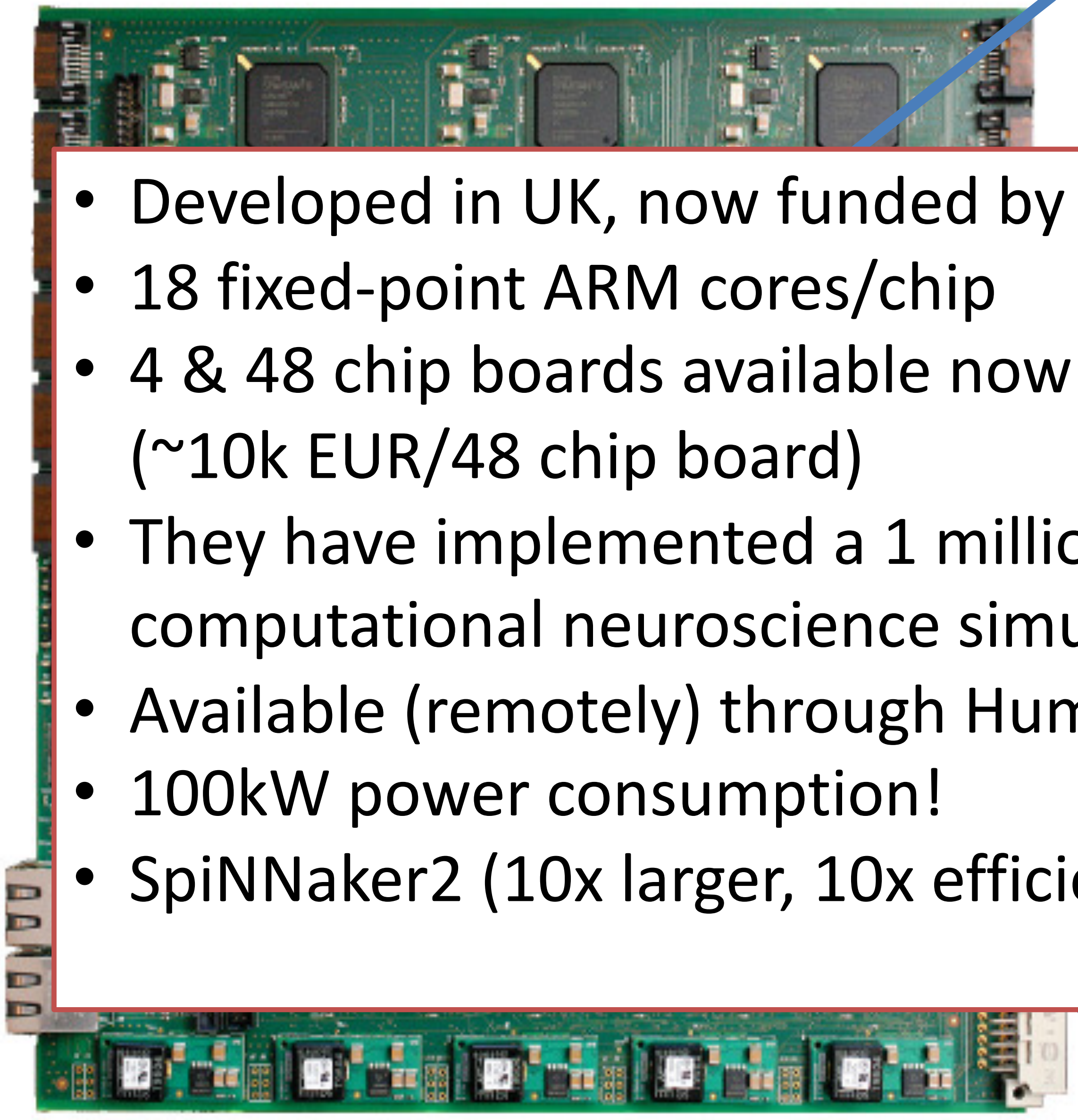
[12] Janelia Farm Research Campus, Howard Hughes Medical Institute, Ashburn, VA, USA

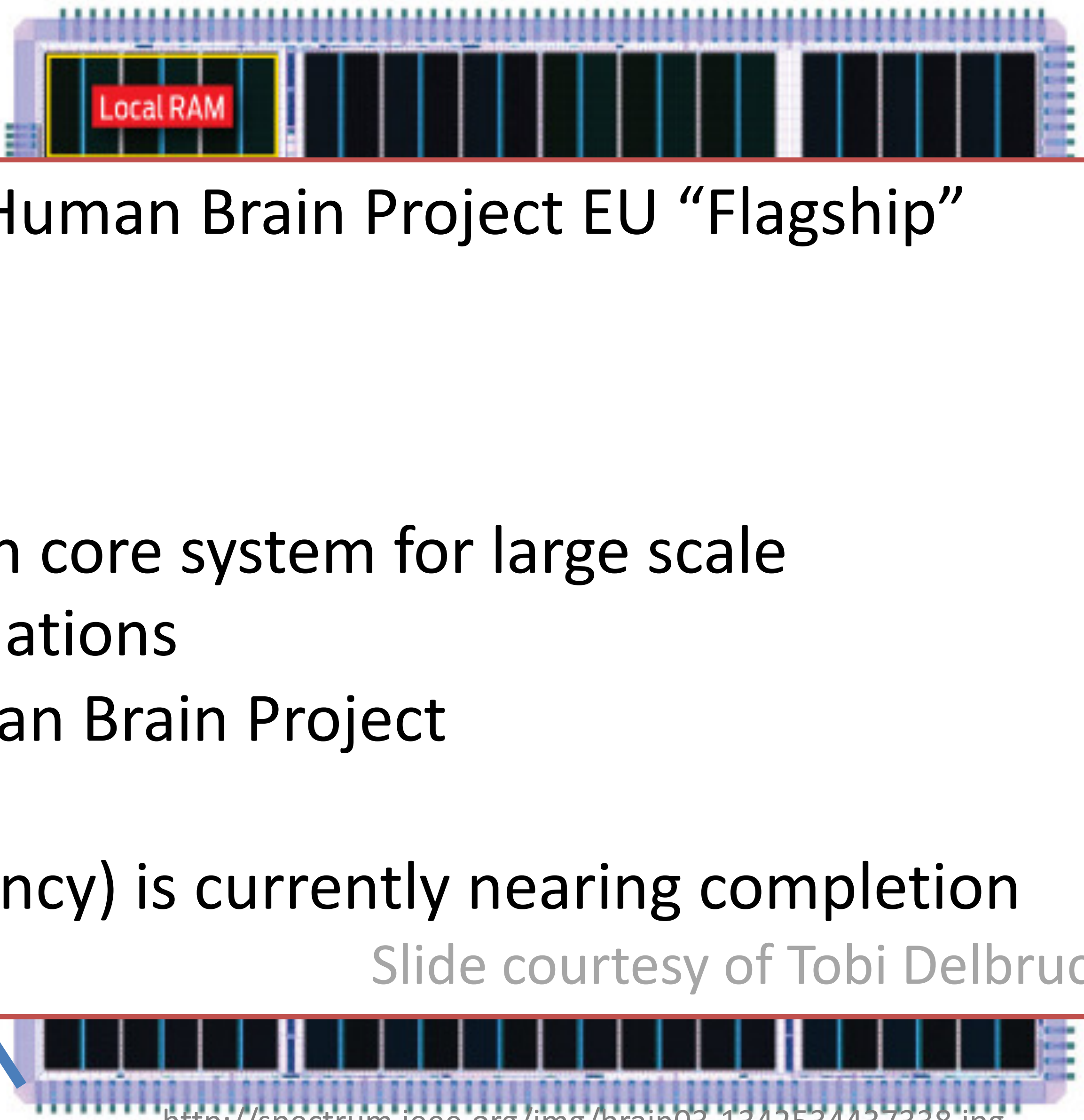
Neuron and interconnection





SpiNNaker – S Furber, Manchester

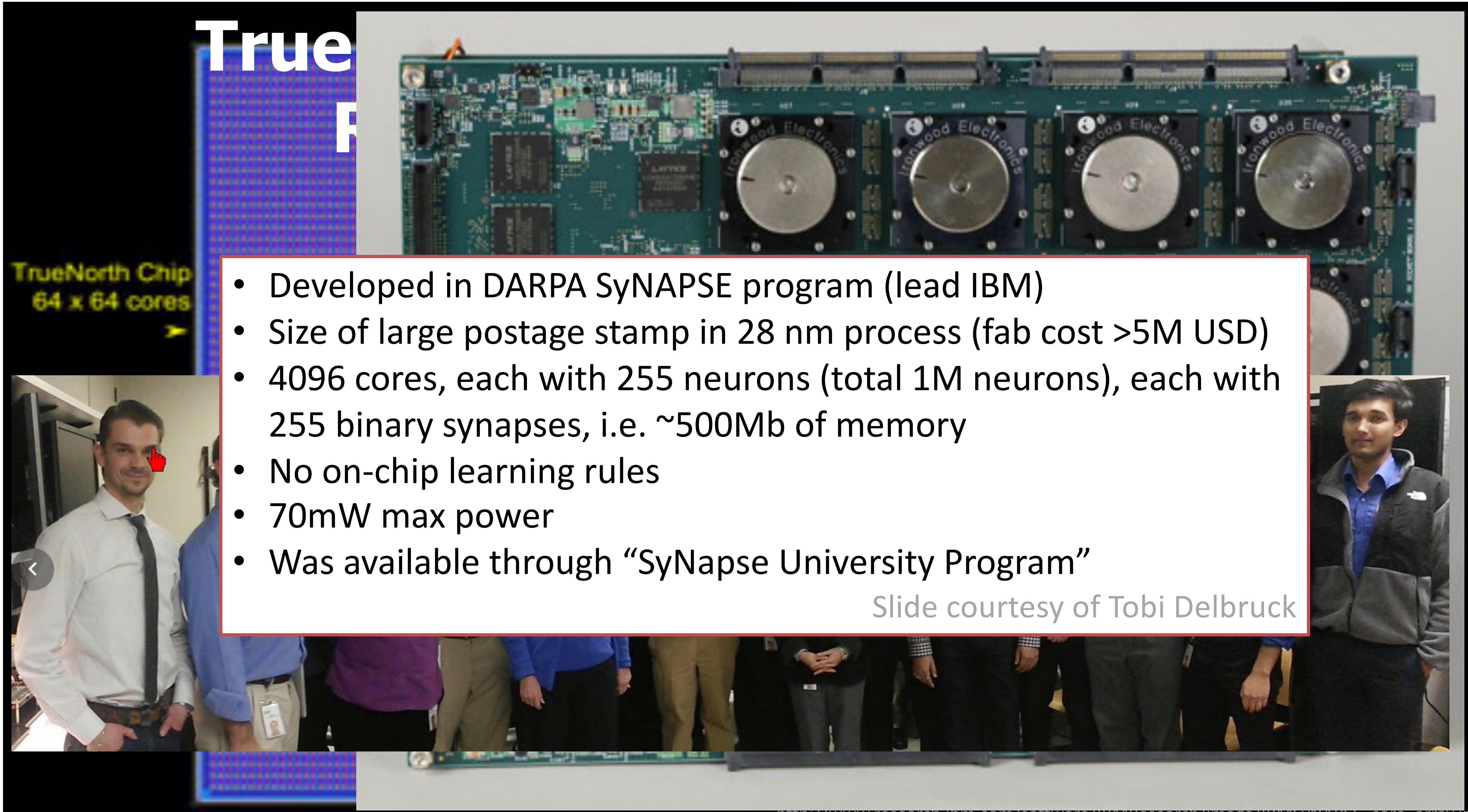




- Developed in UK, now funded by Human Brain Project EU “Flagship”
- 18 fixed-point ARM cores/chip
- 4 & 48 chip boards available now (~10k EUR/48 chip board)
- They have implemented a 1 million core system for large scale computational neuroscience simulations
- Available (remotely) through Human Brain Project
- 100kW power consumption!
- SpiNNaker2 (10x larger, 10x efficiency) is currently nearing completion

Slide courtesy of Tobi Delbruck

http://spectrum.ieee.org/img/brain03-1342534437338.jpg

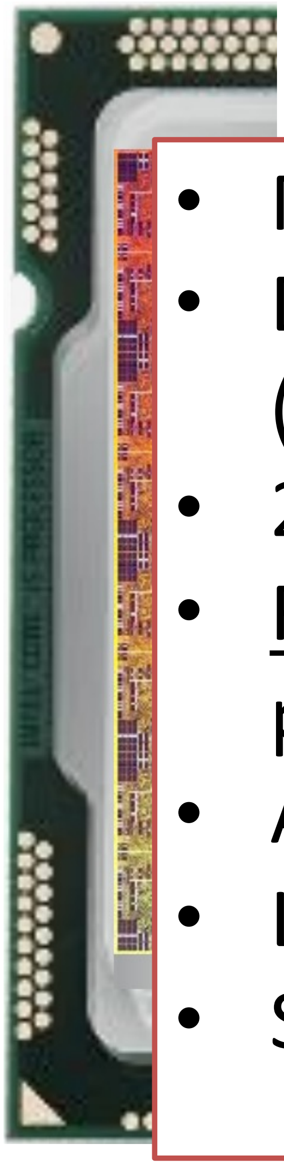


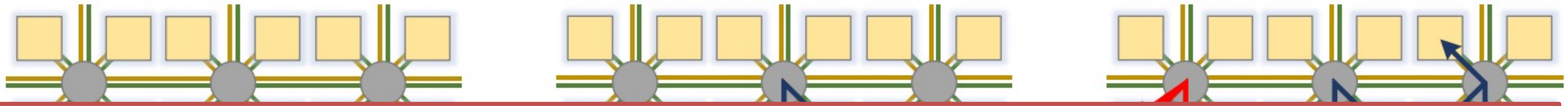
- Developed in DARPA SyNAPSE program (lead IBM)
- Size of large postage stamp in 28 nm process (fab cost >5M USD)
- 4096 cores, each with 255 neurons (total 1M neurons), each with 255 binary synapses, i.e. ~500Mb of memory
- No on-chip learning rules
- 70mW max power
- Was available through “SyNapse University Program”

Slide courtesy of Tobi Delbruck

http://www.research.ibm.com/software/IBMResearch/image/IBMSyNAPSE_core_array.jpg

Intel Loihi





- Multicore 8x16 64mm^2 digital SNN built in 14nm process
- Designed by experienced asynchronous digital design team (lead: Mike Davies)
- 2G transistors, max 127k neurons and 128M weights
- Features on-chip SNN learning with traces and various possible STDP-type rules
- Available via INRC with Intel
- Large board and USB stick implementation
- Similar power consumption to TrueNorth

Slide courtesy of Tobi Delbruck

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Questions?

Welcome

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International Centre for Neuromorphic Systems (ICNS)

https://www.westernsydney.edu.au/icns