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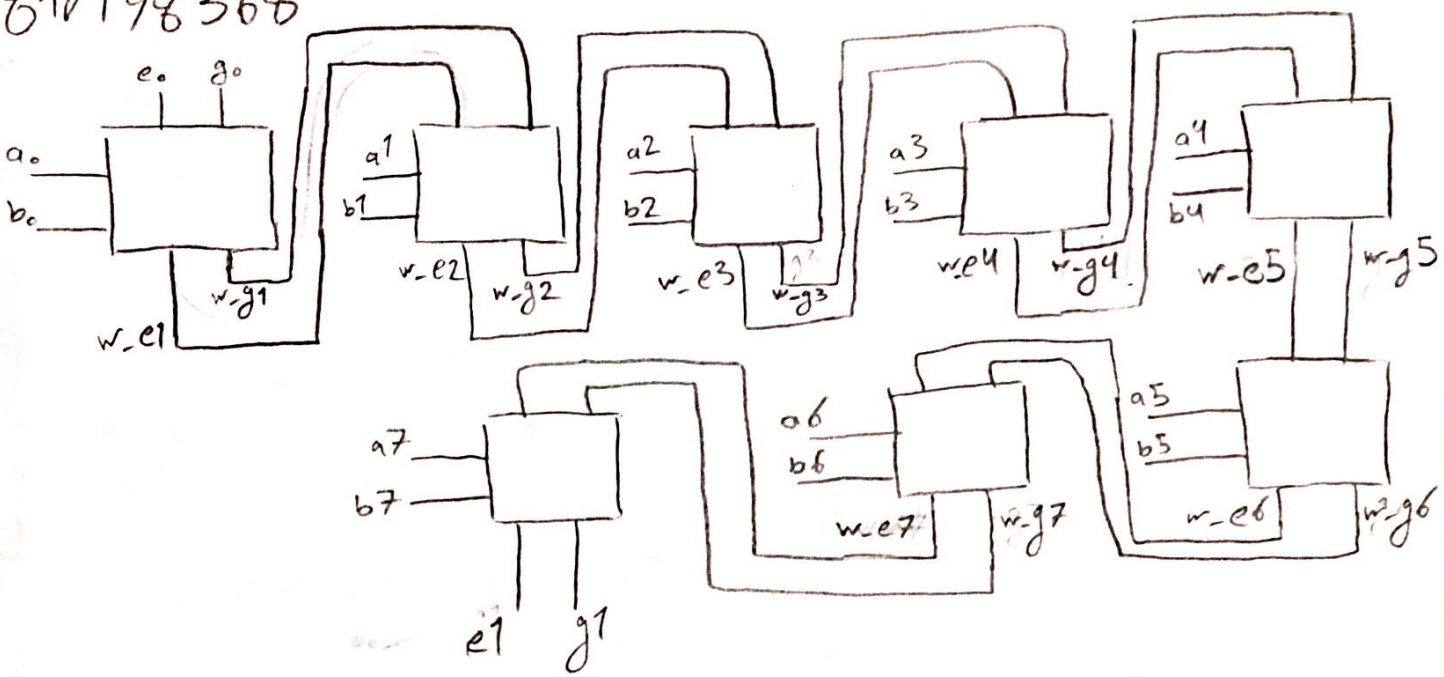
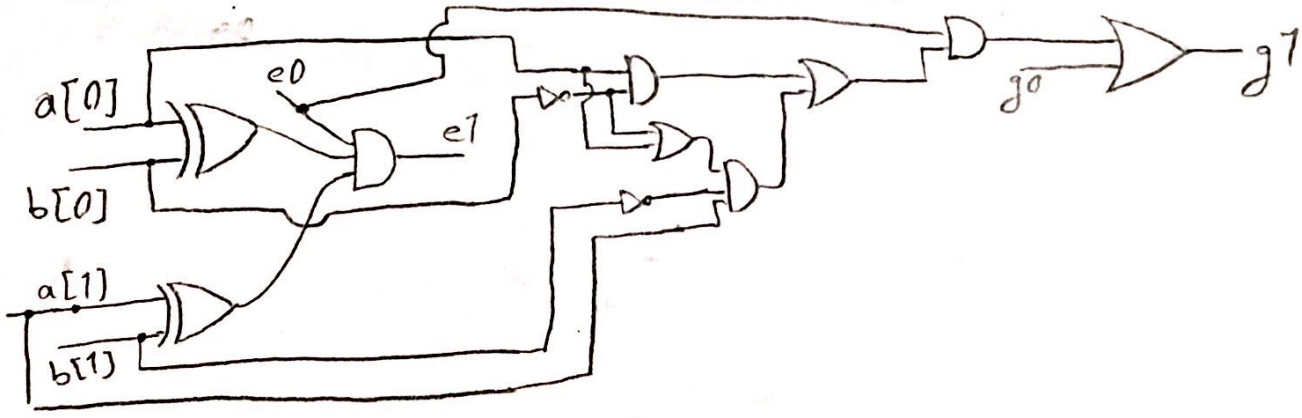
CA2



worst case delay to1 → 169

worst case delay to0 → 158



worst case delay to1: We start from g1, so the OR should go to1, the AND should go to1, the OR should go to1, the 3_input AND should go to1, the OR should go to1, the inverter should go to1.

$\Longrightarrow 19+13+19+17+19+5 = 92$

worst case delay to0: We start from g1, so the OR should go to0, the AND should go to0, the OR should go to0, the 3_input AND should go to0, the OR should go to0, the inverter should go to0.

$\Longrightarrow 17+17+17+22+17+7 = 97$

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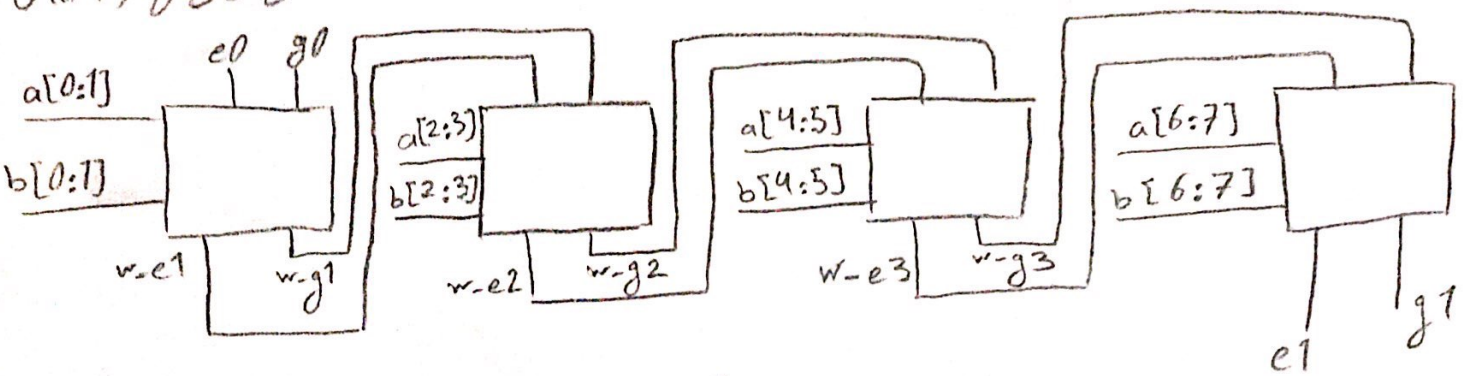
CA 2



worst case delay to1 ⟶ 368

worst case delay to0 ⟶ 388

Cons of TCS: Has more delay time in changing left bits.
Has more gates.
It can't be cascaded for odd bit numbers.
It need to be implement again.

Pros of TCS: Has less delay time in changing right bits.