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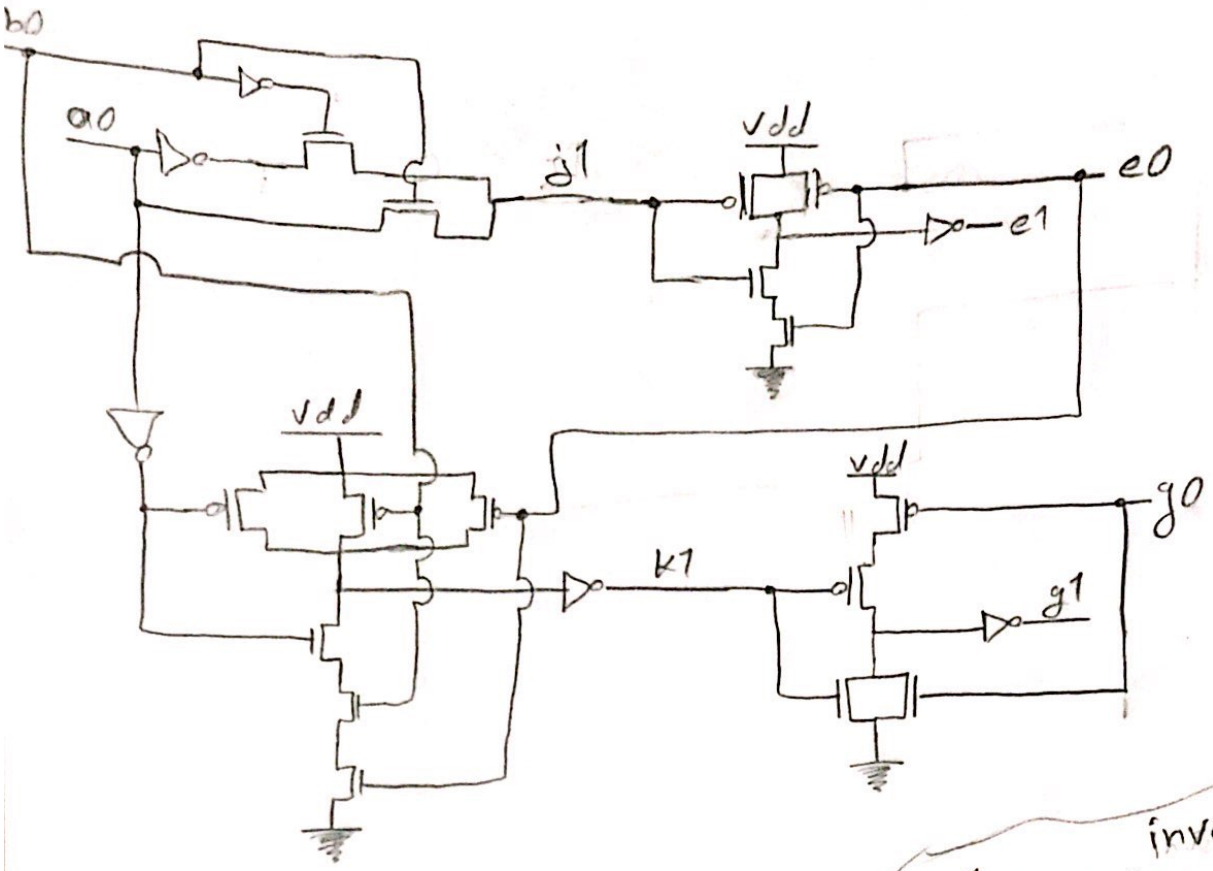

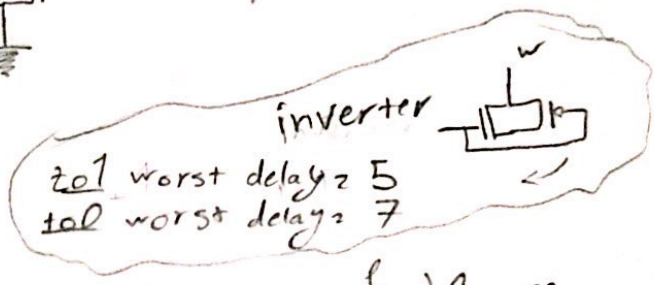

Worst case delay for e1:

to1: we start from a0=1, b0=1, e0=1 → in this way of b0 we have an inverter → inverter has 7ns daelay for to0, then we have a nmos → nmos has 5ns for to Z => 7+5 = 12
so far we have 12ns delay and we're in j1.
a0, b0, e0 started together so in 12ns delay of j1, e0 has done its job in 7ns, so e0 delay is not important. when j1 comes with 1, pmos should be Z → pmos has 7ns for to Z → 12+7 = 19
then at last we have inverter and its to1 → 19+5 = **24**

to0: we start from a0=0, b0=1, e0=0 → like the last one we have inverter and nmos in front of b0 → 12ns, and e0 did its job. so we are in j1 with the value of 0, and have a pmos that should go to1 or a nmos that should go to Z, both of them are 5ns 12+5=17, and we have an inverter that should go to0
17+7 = **24**

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worst case delay for g1:

to1: we start with a0=0, b0=1, e0=1, g0=1, we have inverter in front of a0 (we should go down from a0), so it has 5ns delay, but e0 in this 5ns has connected the nmos gate (it wants 4ns) and then b0 connects another nmos and then we have 4+4=8ns, so the inverter of a0 is not counted in delay, we have another nmos so → 8+4=12 and we have inverter to go to k1 → 12+5=17, in this time g0 done its job and so we have to2 for pmos (7ns) or to0 for nmos(4ns) infront of k1. → 17+7=24 and then another inverter → 24+5=29

to0: we start from a0=1, b0=0, e0=0, g0=0, like last one we don't need a0's inverter delay so we have three nmos that should go to2 → 3×5=15ns and one inverter to0 → 15+7=22 and g0 done its job in this time and we have to1 for pmos (5ns) or to2 for nmos(5ns) in front of k1 → 22+5=27 and at last we have inverter to0 → 27+7=34

Summary:

e1 → to1 = 24
↳ to0 = 24
⟹ BCS circuit worst case delay → to1 = 29
↳ to0 = 34

g1 → to1 = 29
↳ to0 = 34