UNIVERSITY OF TEHRAN

Electrical and Computer Engineering Department

Digital Logic Design ECE 367 / Digital System I ECE 894

Fall 1399

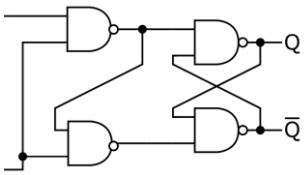
Computer Assignment 4

Basic Memory Structures, Latches and Flip-flops - Week 10

Name:	**Date:**
Username:	

In this assignment, you will be experimenting with latches and flip-flops and see their timing and functionality differences.

1. Generate a clocked D-latch with D and Clock inputs as shown in the following diagram. Describe this circuit in Verilog using NAND primitives.



2. Annotate the circuit of Part 1 with gate delays that are based on switch level delays of 4 NS for the nMOS and 6 NS for the pMOS transistors.
3. Simulate the circuit of Part 2 to verify its operation. For the start of simulation, the outputs begin with X values. You need to create a *D* and *Clk* signaling that will force the latch into a known and stable state. Exercise this circuit for cases that you think a glitch on output of a gate is possible. Show situations that this structure behaves as a latch, thus, has transparency.
4. Provide a reset (*rst*) input for the above latch that, when active, it will force the output to 0 and will keep the output at this value after *rst* is no longer active.
5. Form an 8-bit shift register using the above latch. From left to right (*i* to 0), the output of latch *i* connects to the D input of latch *i-1*. The D input of latch *i* is the *sIn* (serial input) of the shift register.
6. Simulate the circuit of Part 5 and explain why or why-not this circuit works as expected.
7. Build a D-type flip-flop using two of the above latches. Add an active high synchronous reset input to the flip-flop. Simulate this flip-flip and check its edge triggering behavior and the resetting mechanism that you inserted in the flip-flop.
8. Build an 8-bit register using the flip-flop of Part 7 in a **generate** statement.
   a. Write a testbench for this circuit and verify its clocking and resetting operations.
   b. Extend the testbench to include its shift operation.
9. Use an **always** statement to describe the circuit of Part 7. Verify its operation using a SystemVerilog testbench.
10. In a testbench compare simulations of the shift register built by putting gates together and the one with the **always** statement. Explain the differences.