دانشکده مهندسی کامپیوتر

طراحی کامپیوتری سیستم های دیجیتال

گزارش فاز آخر پروژه

استاد درس:

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علی صداقی

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موضوع:

MIPS Multi-cycle CPU

فایل‌های پروژه در پوشه های زیر موجود است:

- Phase1 (پروژه Xilinx)
- Final (پروژه نهایی Xilinx)
- Proteus (شماتیک در قالب پروتئوس)
- Waveform (اسکرین شات از خروجی تست)
- Resources (منابع استفاده شده در پروژه)

در ادامه این مستند گزارشی از طراحی شماتیک پروژه، نتایج خروجی و تست‌بنچ ها، منابع استفاده شده و ... داده می‌شود.

❖ **خروجی نهایی پروژه:**

پس از اتمام پیاده سازی یک برنامه به پردازنده داده شده تا نحوه عملکرد آن مشخص شود.

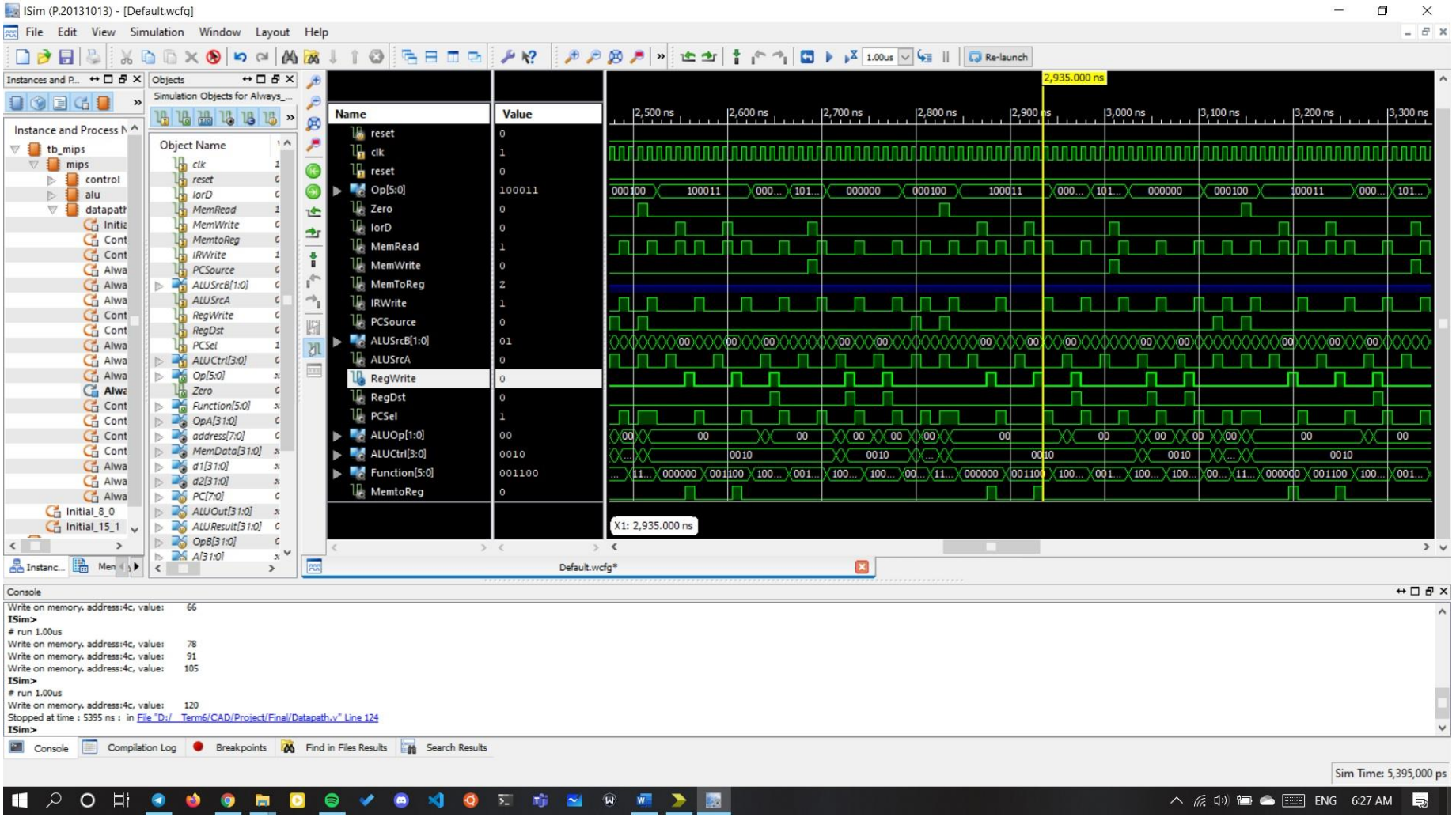
- پردازنده به کاملا به صورت Multi-cycle دستورات را اجرا می کند.

برنامه: کد اسمبلی یک Accumulator که اعداد ۱ تا ۱۵ را با هم جمع می کند.

نتایج:

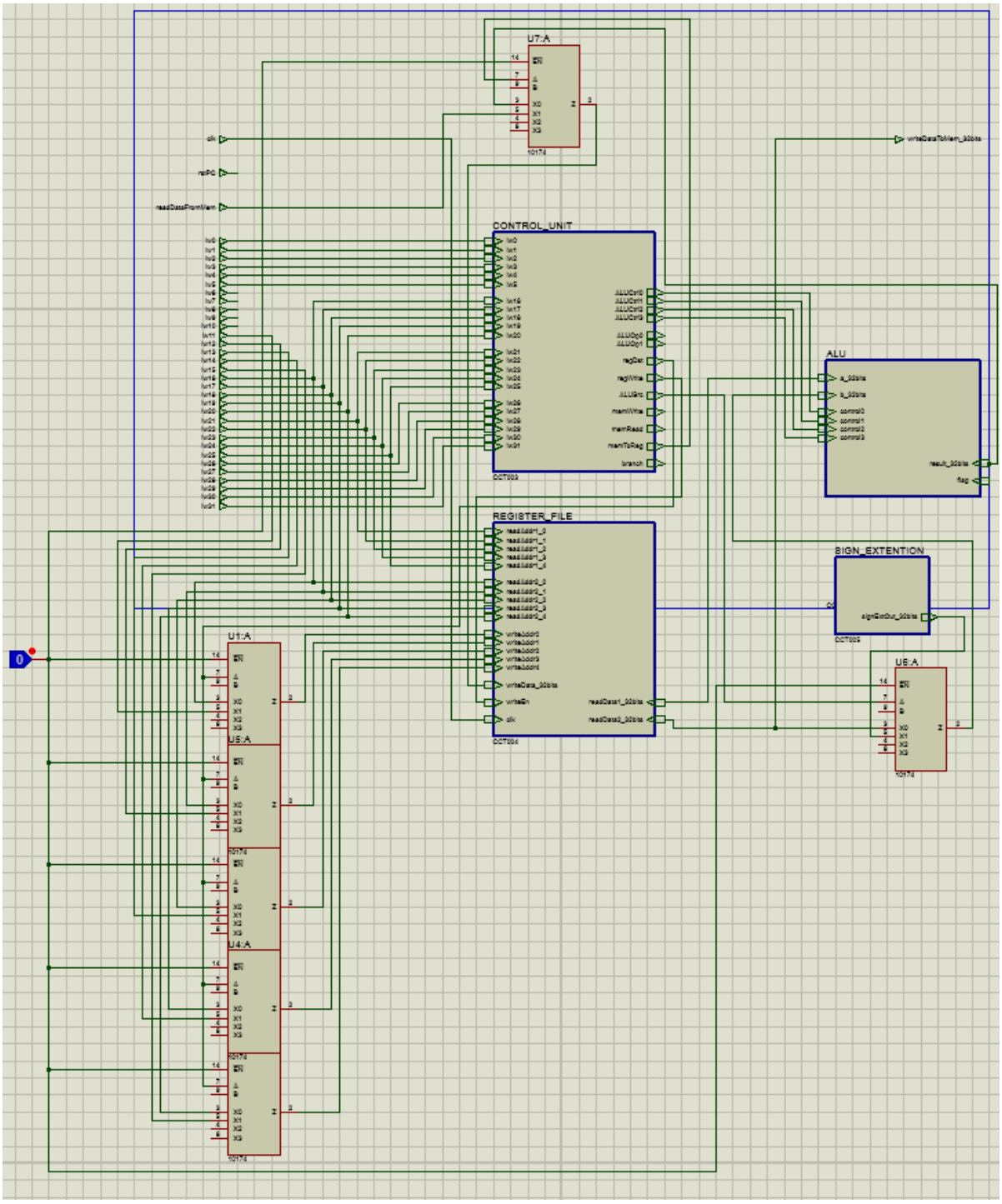
Console

```
ISim P.20131013 (signature 0x7708f090)
This is a Full version of ISim.
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
Write on memory. address:4c, value:      0
Write on memory. address:4c, value:      0
Write on memory. address:4c, value:      1
ISim>
# run 1.00us
Write on memory. address:4c, value:      3
Write on memory. address:4c, value:      6
Write on memory. address:4c, value:     10
ISim>
# run 1.00us
Write on memory. address:4c, value:     15
Write on memory. address:4c, value:     21
Write on memory. address:4c, value:     28
ISim>
# run 1.00us
Write on memory. address:4c, value:     36
Write on memory. address:4c, value:     45
Write on memory. address:4c, value:     55
Write on memory. address:4c, value:     66
ISim>
# run 1.00us
Write on memory. address:4c, value:     78
Write on memory. address:4c, value:     91
Write on memory. address:4c, value:    105
ISim>
# run 1.00us
Write on memory. address:4c, value:    120
Stopped at time : 5395 ns :  in File "D:/   Term6/CAD/Project/Final/Datapath.v" Line 124
ISim>
```



A: MIPS Datapath Testbench Figure

❖ **شماتیک:** تصاویر در پوشه Proteus نیز موجود می‌باشند.



❖ **نتایج فاز اول:** تصاویر در پوشه Waveform نیز موجود می‌باشند.

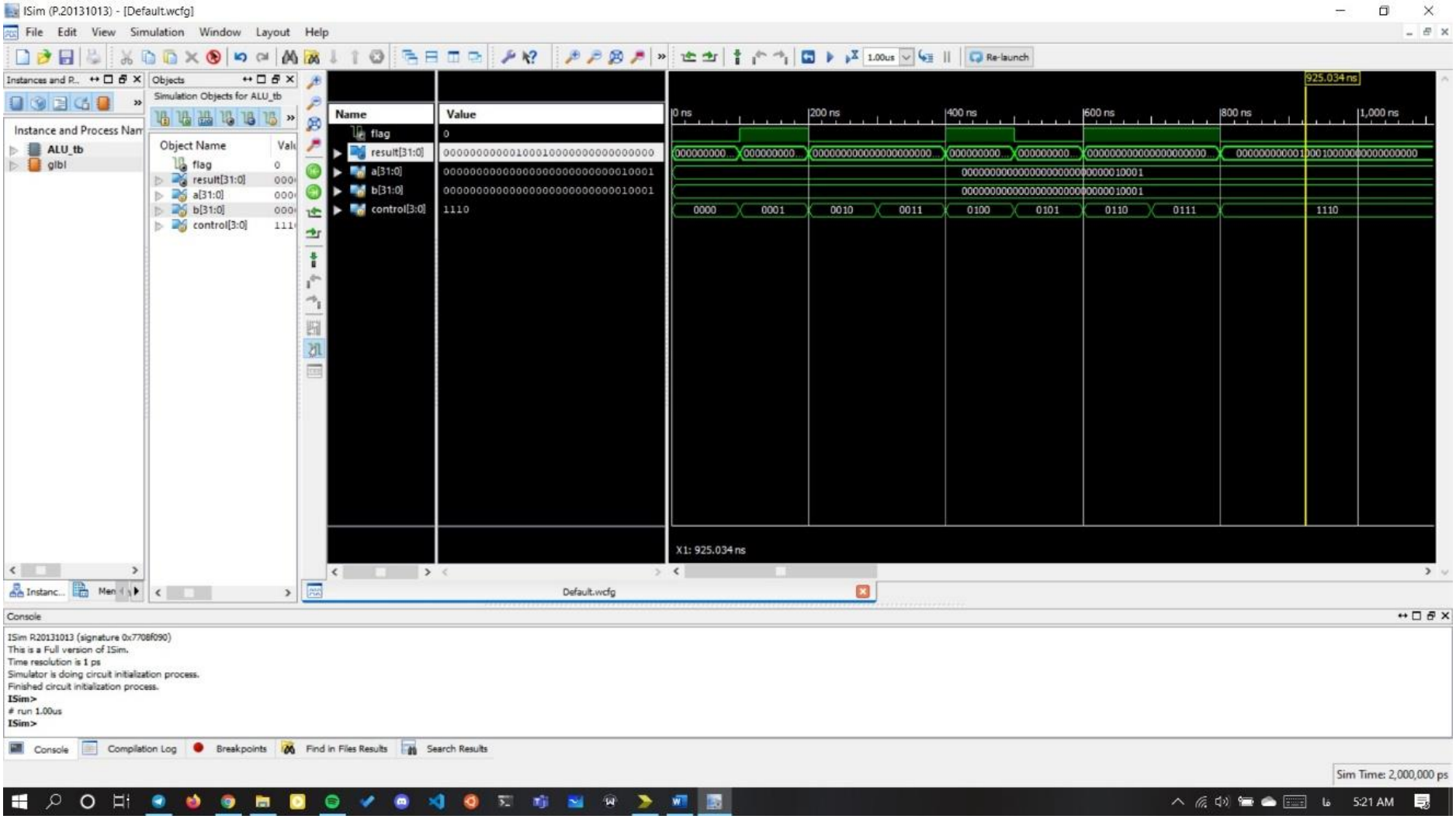


Figure B: ALU Testbench

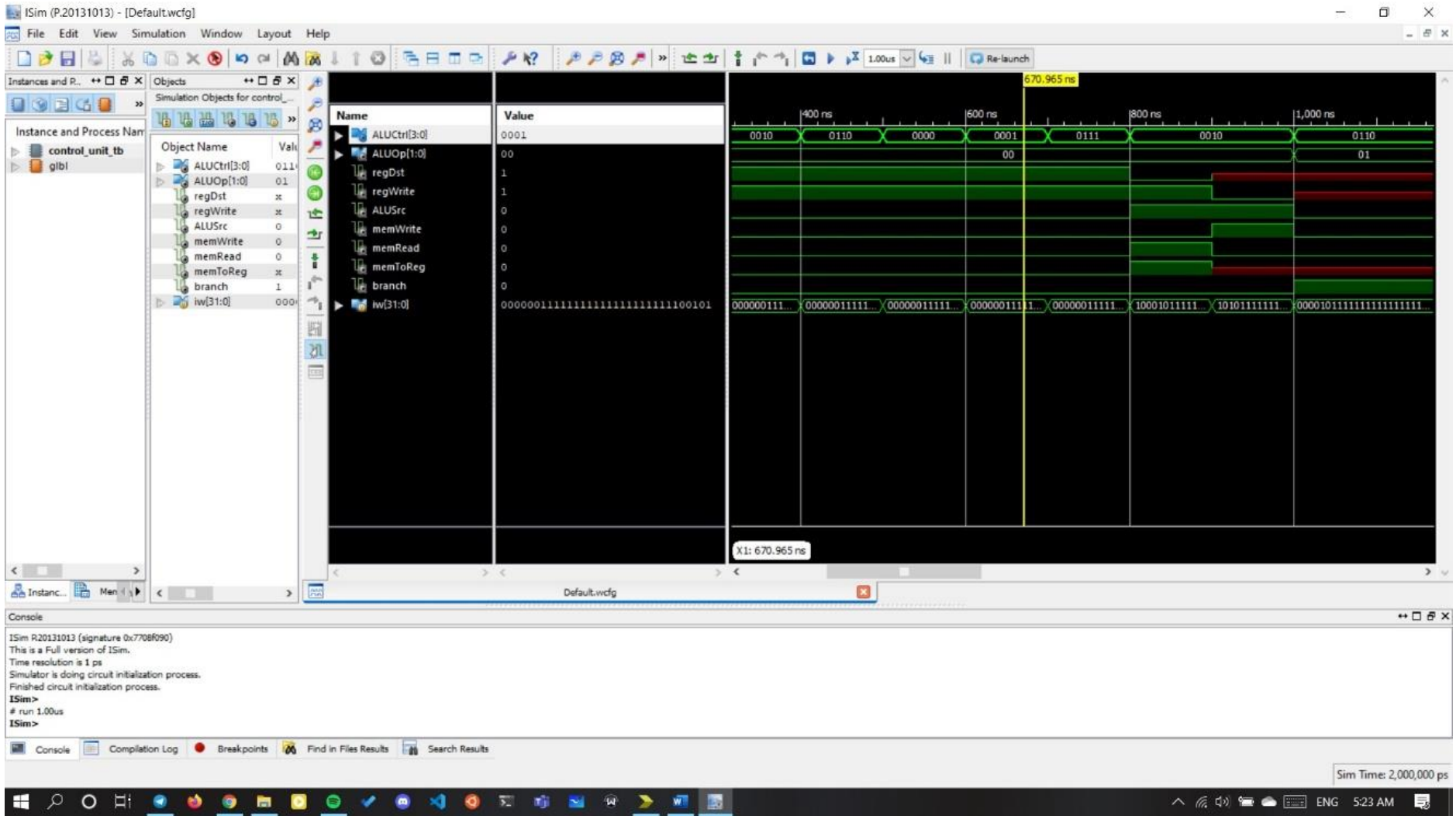


Figure C: Control Testbench

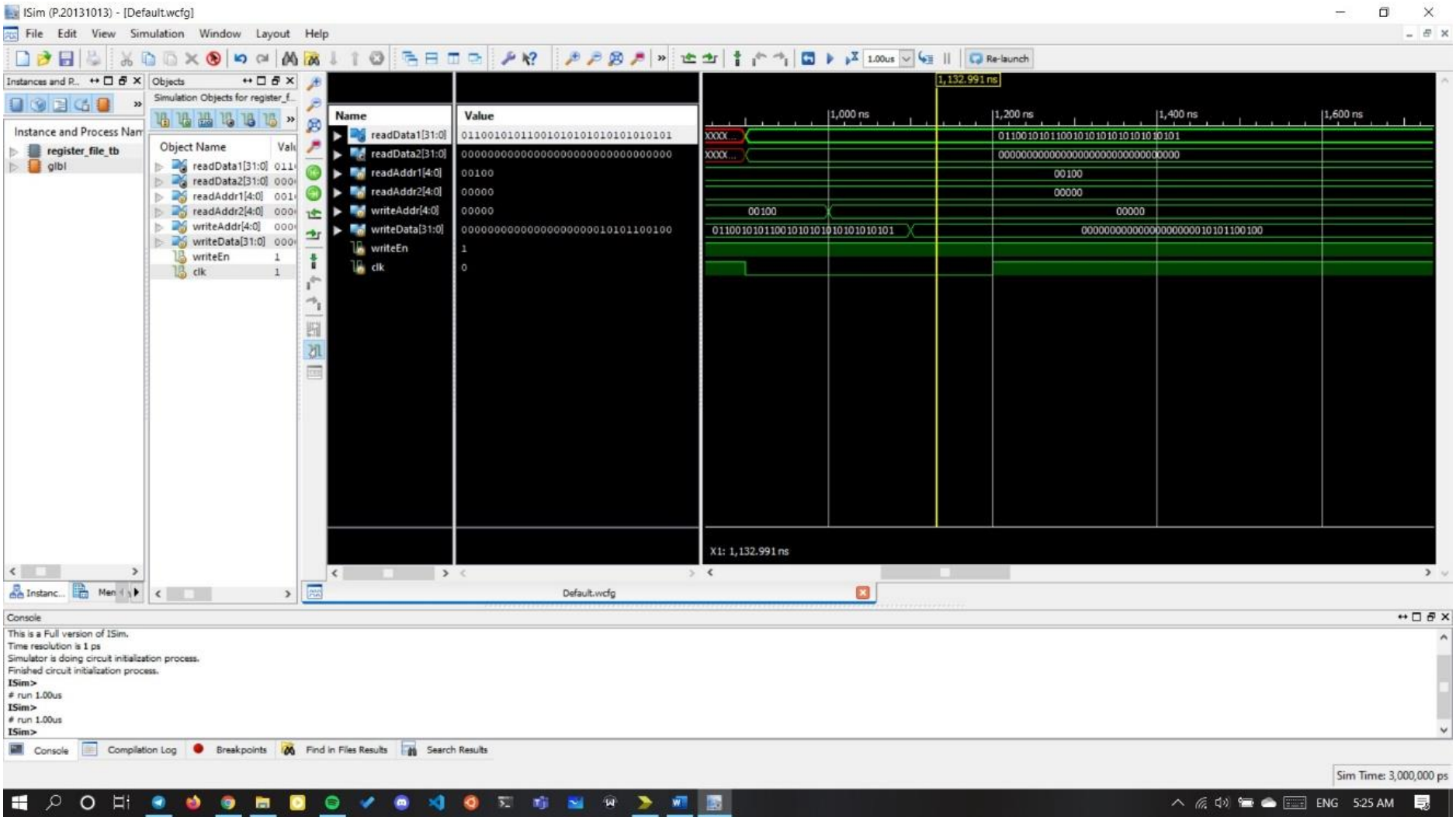
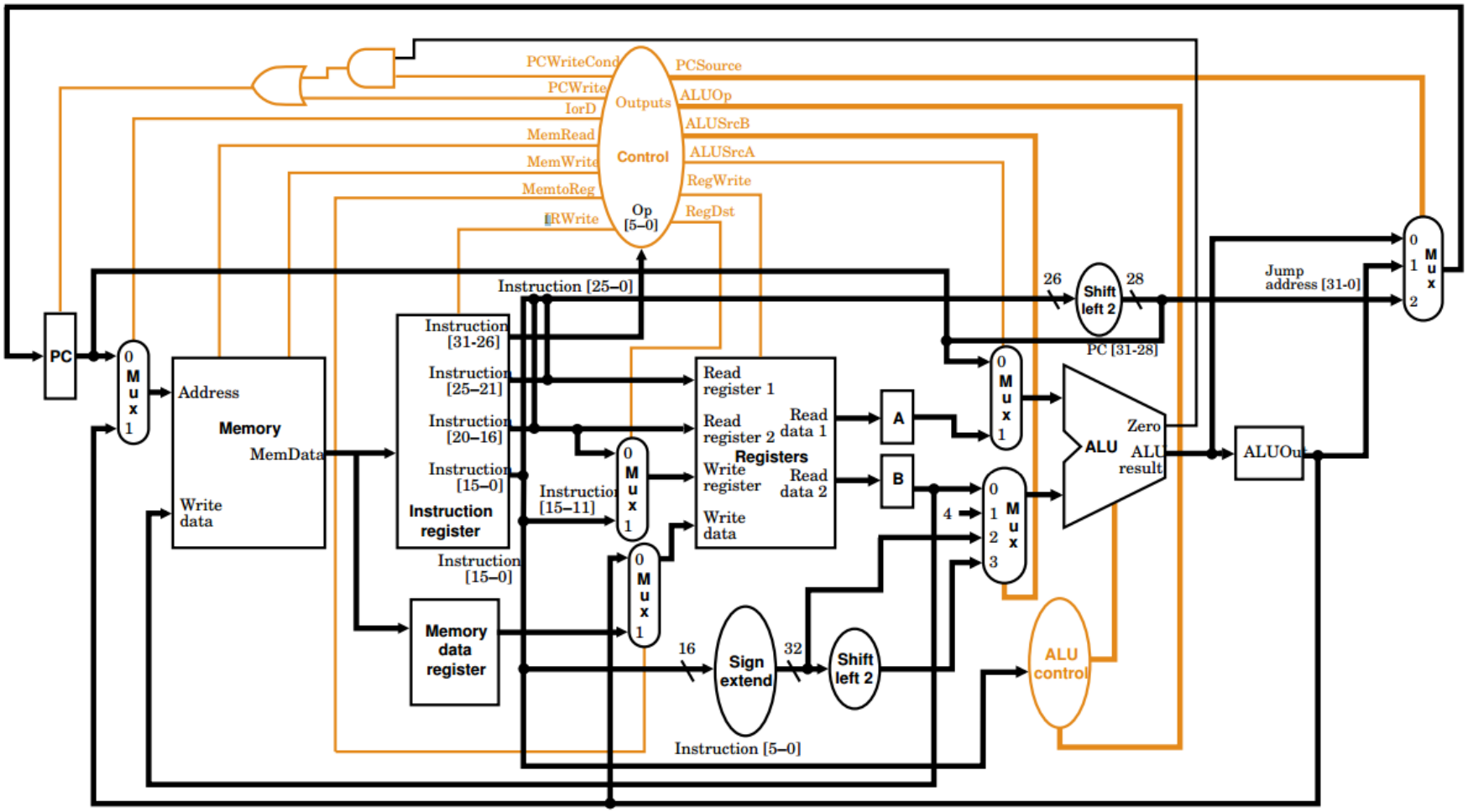


Figure D: Register File Testbench

Datapath در فاز دوم پروژه تست شده است.

❖ **منابع:**

- طراحی Datapath Multi-cycle:



- سیگنال های کنترلی:

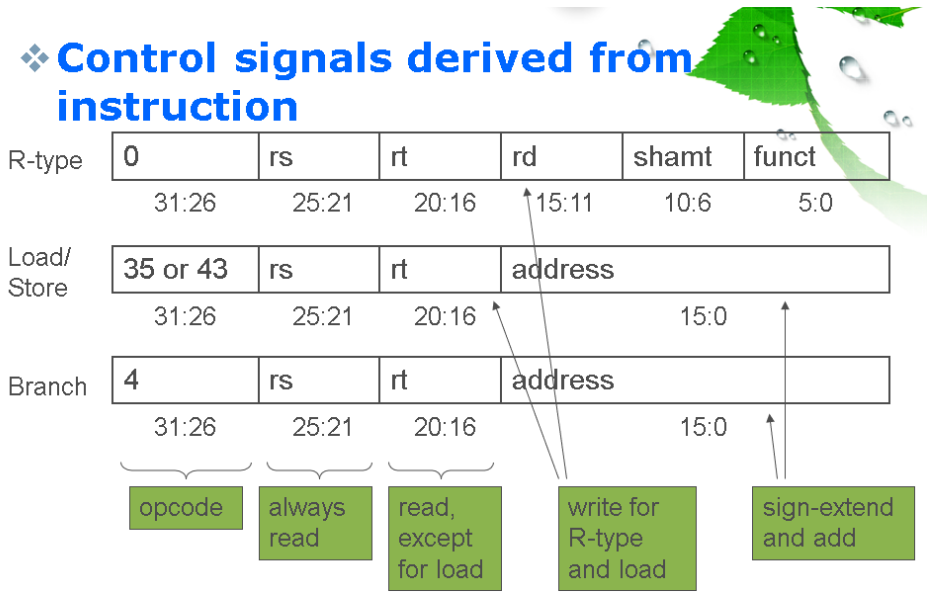
Actions of the 1-bit control signals

Signal name	Effect when deasserted	Effect when asserted
RegDst	The register file destination number for the Write register comes from the rt field.	The register file destination number for the Write register comes from the rd field.
RegWrite	None	The general-purpose register selected by the Write register number is written with the value of the Write data input.
ALUSrcA	The first ALU operand is the PC.	The first ALU operand comes from the A register.
MemRead	None	Content of memory at the location specified by the Address input is put on Memory data output.
MemWrite	None	Memory contents at the location specified by the Address input is replaced by value on Write data input.
MemtoReg	The value fed to the register file Write data input comes from ALUOut.	The value fed to the register file Write data input comes from the MDR.
IorD	The PC is used to supply the address to the memory unit.	ALUOut is used to supply the address to the memory unit.
IRWrite	None	The output of the memory is written into the IR.
PCWrite	None	The PC is written; the source is controlled by PCSource.
PCWriteCond	None	The PC is written if the Zero output from the ALU is also active.

Actions of the 2-bit control signals

Signal name	Value	Effect
ALUOp	00	The ALU performs an add operation.
	01	The ALU performs a subtract operation.
	10	The funct field of the instruction determines the ALU operation.
ALUSrcB	00	The second input to the ALU comes from the B register.
	01	The second input to the ALU is the constant 4.
	10	The second input to the ALU is the sign-extended, lower 16 bits of the IR.
	11	The second input to the ALU is the sign-extended, lower 16 bits of the IR shifted left 2 bits.
PCSource	00	Output of the ALU (PC + 4) is sent to the PC for writing.
	01	The contents of ALUOut (the branch target address) are sent to the PC for writing.
	10	The jump target address (IR[25–0] shifted left 2 bits and concatenated with PC + 4[31–28]) is sent to the PC for writing.

- ساختار Instruction:



Name	Format	Example					Comments
		3 bits	3 bits	3 bits	3 bits	4 bits	
add	R	0	2	3	1	0	add $1,$2,$3
sub	R	0	2	3	1	1	sub $1,$2,$3
and	R	0	2	3	1	2	and $1,$2,$3
or	R	0	2	3	1	3	or $1,$2,$3
slt	R	0	2	3	1	4	slt $1,$2,$3
jr	R	0	7	0	0	8	jr $7
lw	I	4	2	1	7		lw $1, 7 ($2)
sw	I	5	2	1	7		sw $1, 7 ($2)
beq	I	6	1	2	7		beq $1,$2, 7
addi	I	7	2	1	7		addi $1,$2, 7
j	J	2	500				j 1000
jal	J	3	500				jal 1000
slti	I	1	2	1	7		slti $1,$2, 7