Assignment

Objective: Design a Verilog module using state for a display adapter to retrieve and display an image following the XGA standard. The adapter must support a resolution of 1024x768 pixels at 60Hz and a color depth of 24 bits.

Requirements

1. **Image Storage**:
   - Use either FPGA BRAM or external SRAM (e.g., SRAM or SDRAM) to store pixel data for the image.
2. **Timing Control**:
   - Generate horizontal and vertical sync signals according to XGA specifications for 1024x768 at 60Hz.
   - Define parameters for sync pulse width, back porch, active pixel width, and front porch.
3. **Pixel Data Retrieval**:
   - Retrieve pixel data sequentially from memory based on the current pixel coordinates.
   - Implement logic to handle reading data in the correct order, considering the memory's interface timing.
4. **Display Output**:
   - Output the pixel data to an external display during the active display period.
   - Ensure that the output format matches the display requirements.

Detailed Specifications

- **Resolution**: 1024x768 pixels
- **Refresh Rate**: 60Hz
- **Color Depth**: 24 bits (RGB888)
- **Memory Size**: Sufficient to hold at least one image (e.g., for 1024x768, it requires 1024 * 768 * 3 bytes).
- **Sync Parameters** (for XGA):
  - Horizontal sync pulse width: 136 pixels
  - Horizontal back porch: 160 pixels
  - Horizontal front porch: 24 pixels
  - Vertical sync pulse width: 6 lines
  - Vertical back porch: 29 lines
  - Vertical front porch: 3 lines

Expected Outcomes

Students should deliver:

- A Verilog implementation of the display adapter, including:
  - Memory interface module

    - Display control logic
    - Sync signal generation
- Documentation explaining the design choices, XGA standard compliance, and how the memory is accessed.