
Blackrock
Neurotech

FPGA Prototype of W_ICONS Chip

Release v0.1.1

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DESCRIPTON:

1 FPGA Prototype 1

CHAPTER

ONE

FPGA PROTOTYPE

It prototypes the W_ICONs chip with the following changes and limitations: - Register file size is greatly reduced to integrate only 4 stimulation channels' parameters. - Analog macro is replaced with a synthesized analog macro to: - Imitates the recording behavior for all 64 channels

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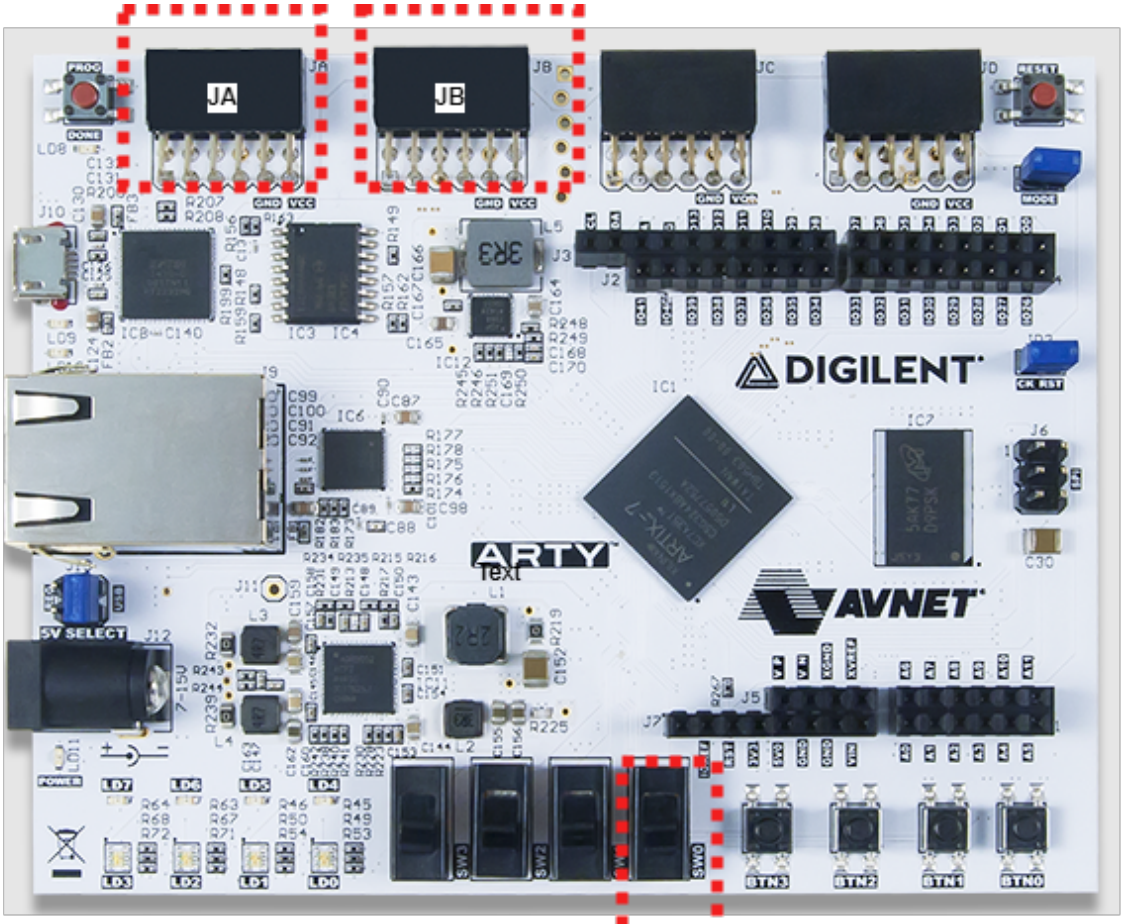
- each channel generates distinct constant values that can be easily recognizable.
  - Recording
    - `Ch0~31:    value= 18'h0720+ 2'b10 * idx; idx=0..31`
    - `Ch31~64:   value= 18'h0920+ 2'b10 * idx; idx=0..31`

  - Recording during the stimulation
    - `Ch0~3:     value= 18'h0320+ 2'b10 * idx; idx= 0..3`
    - `Ch31~64:   Not available;`
```

- No stimulation output can be observed but the logic for 4 channels is included.
- Author
  - Created by Ali Zeinolabedin on 02/09/2024.
  - Latest Update: 03/28/2024 by Ali Zeinolabedin

1.1 FPGA Architecture

- FPGA board: Arty A7 link
- Bit file is [here]/Cadence/w_icons/units/w_icons_top/fpga/vivado/export).
- Pin details:



SW0
External Reset:
Down: chip reset mode
Up: chip active mode

JB

			3	2	1

1: ERR_CRC
2: ERR_STIM
3: STIM_XEN

JA

6	5	4	3	2	1
12	11	10	9	8	7

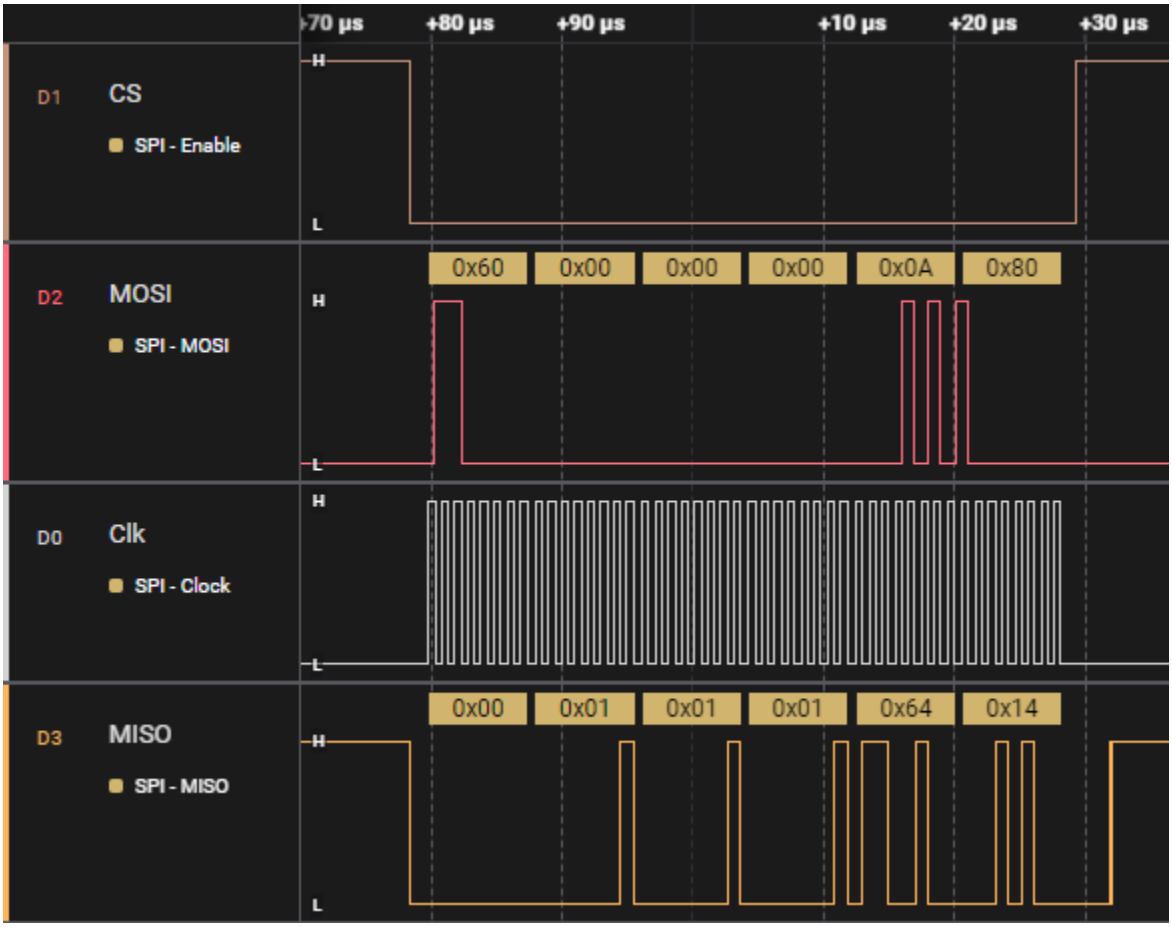
1: SPI_CLK
2: SPI_CS
3: SPI_MOSI
4: SPI_MISO
5: GND
6: VDD
7: ADC_EN
8: ADC1_OUT
9: ADC2_OUT
10: CLK_REC (33MHz, output)
11: GND
12: VDD

1.2 FPGA Prototype test

- The FPGA prototype is verified using the SPI cable (C232HM-DDHSL-0).
- A Python library is developed for testing W_ICONs chip. Here are the details.

1.3 Real measurement using FPGA prototype

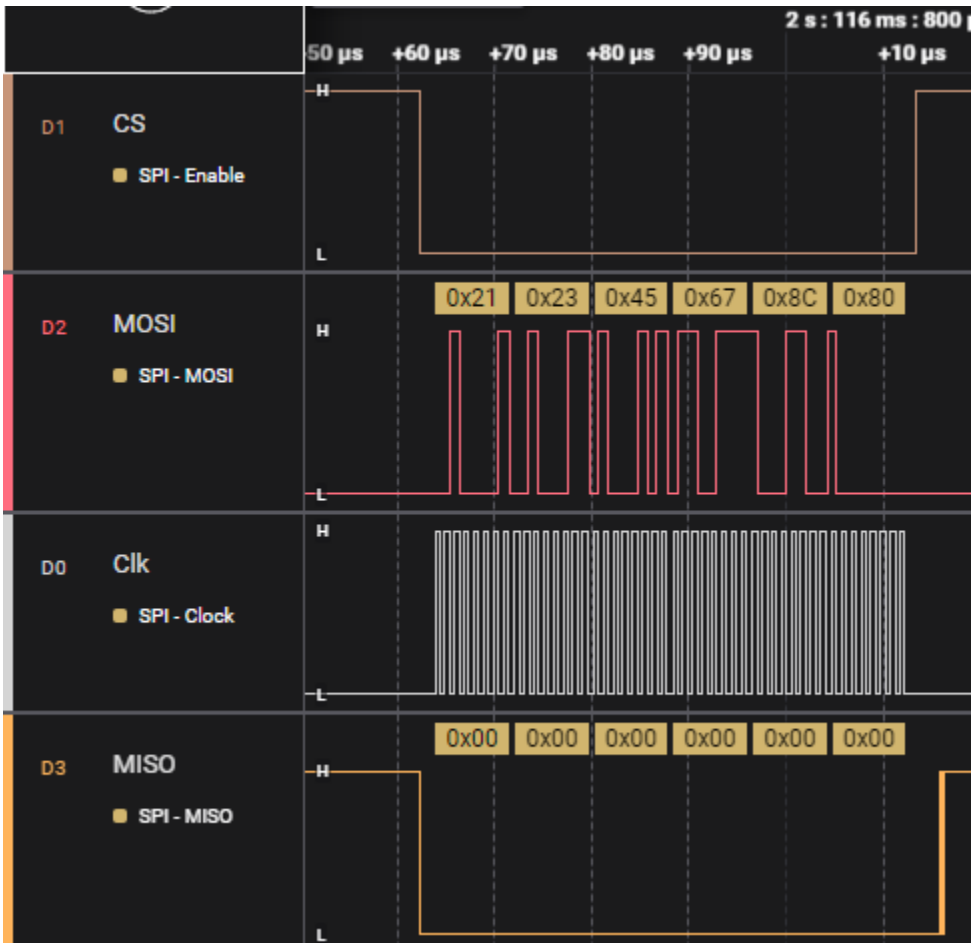
1.3.1 Reading Chip ID



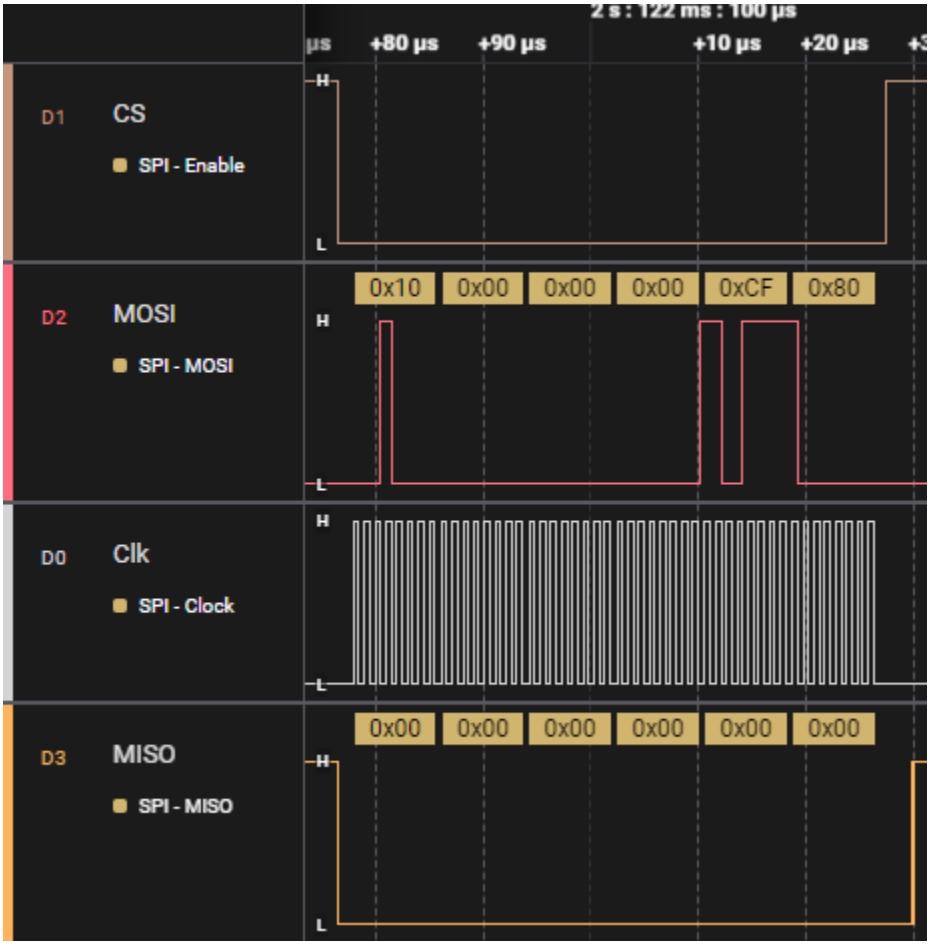
1.3.2 Write Data/Address

Write 0x12345678 to address 0xc and read it back

Write data (0x12345678)

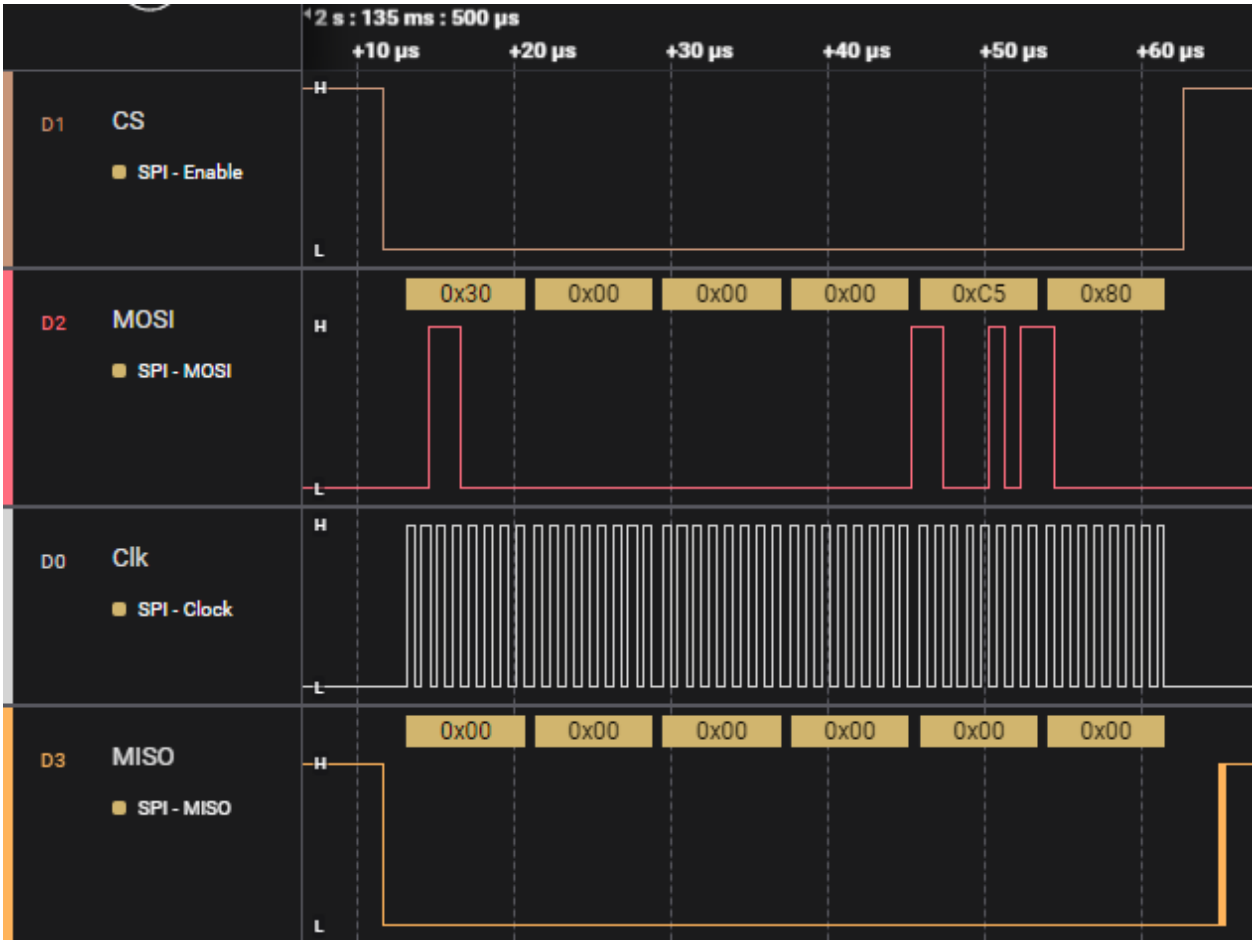


Write address (0xc):

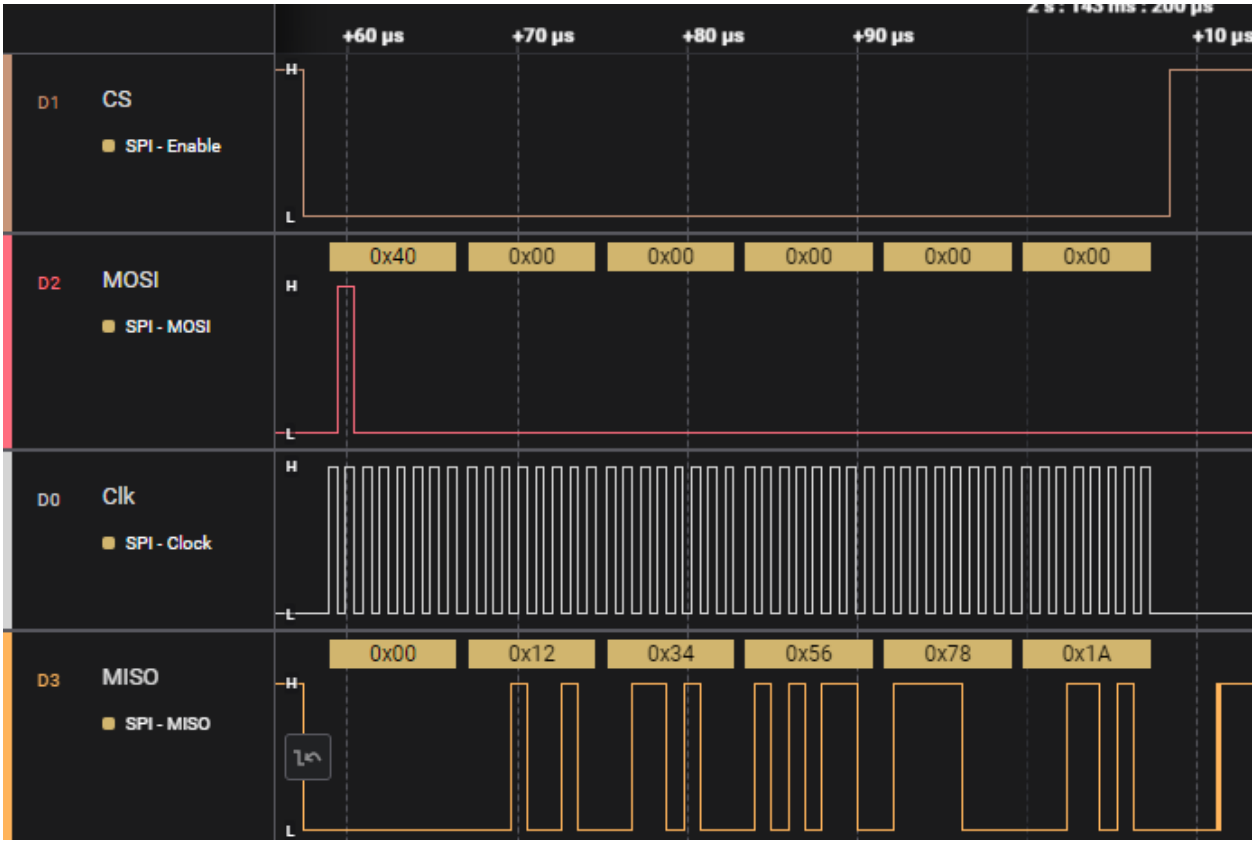


1.3.3 Read Data

Read address (0xc):

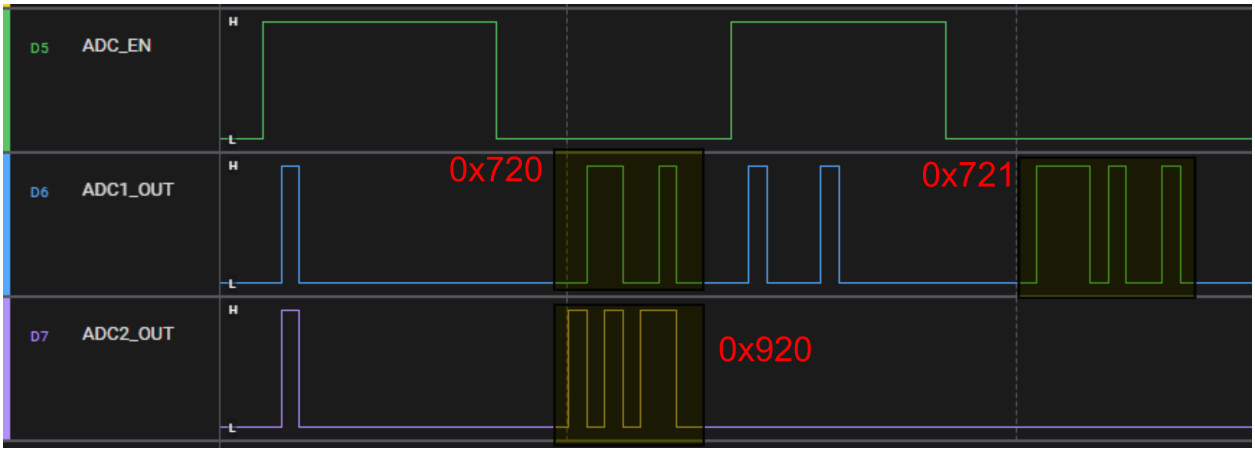


Read Data (0x12345678):



1.3.4 ADC Recording:

- Enable Ch0, Ch1, and Ch32
- Enable Recording



1.3.5 Recording during the simulation