پردازش سیگنال: انجام عملیات ریاضی روی سیگنال

Fixed-point

* Unsigned
* Signed

Floating-point

پیاده سازی عملگرهای جبری

* جمع کننده، ضرب کننده، تقسیم کننده، جذر، توابع مثلثاتی
* Sign & magnitude
* One’s complement
* Two’s complement

With two’s complement if we know the addition of many numbers does not have overflow, we do not need to be worried about internal overflow that may occur.

پیاده سازی در VHDL

* Unsigned
* Signed

use ieee.numeric\_std.all;

signal X: signed (7 downto 0) :=( others=>’0’);

نمایش اعداد اعشاری

* Floating-Point
* Fixed-Point

مفهوم یک عدد باینری، به تفسیری که از آن میشود بستگی دارد.

Quantization

Fixed-Point system does not have any standard.

Use s.m.n approach to show fixed-point numbers.

S: sign

M: number of integer digits

N: number of fraction digits

Fixed-point addition:

The number of fraction digits (N) of two numbers must be equal by appending zero in the right.

The number of integer digits (M) of two numbers must be equal by sign-extending the number with smaller M.

Fixed-point multiplication

(m1, n1)\*(m2, n2) => (m1+m2, n1+n2)

(s, m1, n1)\*(s, m2, n2) => (s, m1+m2+1, n1+n2)

Fixed-Point Quantization

Quantization noise (error)

Lesson2

(s, m, n) => (1, m+n+1, n) in Matlab

(s, 2, 8) => (1, 11, 8)

1. Create the model in Simulink application
2. Create Fixed-Point model
3. Compare floating-point output with fixed-point output and calculate quantization error

Quantization process

1. Quantizing out of system input signals
2. Quantizing in system input signals
3. Quantizing operands

DDS IP for creating sin waves in FPGA

Lesson 3

Filters & FFT

FIR and IIR Filters

Scaling

* Real scaling
* Virtual scaling