VHDL header:

Ieee library

Std\_logic\_1164

Use ieee.numeric\_std.all;

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| Library | LIBRARY library\_name;  USE library\_name.package\_name.package\_parts; |
| Entity | ENTITY entity\_name IS  PORT (  port\_name : signal\_mode signal\_type;  port\_name : signal\_mode signal\_type;  ...);  END entity\_name;  Mode: IN, OUT, INOUT, or BUFFER  ENTITY full\_adder IS  PORT (a, b, cin: IN BIT;  s, cout: OUT BIT);  END full\_adder; |
| Architecture | ARCHITECTURE architecture\_name OF entity\_name IS  [declarations]  BEGIN  (code)  END architecture\_name;  ARCHITECTURE dataflow OF full\_adder IS  BEGIN  s <= a XOR b XOR cin;  cout <= (a AND b) OR (a AND cin) OR  (b AND cin);  END dataflow; |
| Process | The PROCESS is executed every time a signal declared in its sensitivity list changes. |
| Data types | Package standard of library std: Defines **BIT, BOOLEAN, Natural, INTEGER, and REAL**  Package std\_logic\_1164 of library ieee: Defines **STD\_LOGIC and STD\_ULOGIC**  std\_logic\_arith of library ieee: Defines **SIGNED and UNSIGNED**  Packages std\_logic\_signed and std\_logic\_unsigned |
| User-Defined Data Types | TYPE integer IS RANGE -2147483647 TO +2147483647;  -- This is indeed the pre-defined type INTEGER.  TYPE natural IS RANGE 0 TO +2147483647;  -- This is indeed the pre-defined type NATURAL.  TYPE my\_integer IS RANGE -32 TO 32;  -- A user-defined subset of integers.  TYPE student\_grade IS RANGE 0 TO 100;  -- A user-defined subset of integers or naturals. |
| User-defined enumerated types | TYPE bit IS ('0', '1');  -- This is indeed the pre-defined type BIT  TYPE my\_logic IS ('0', '1', 'Z');  -- A user-defined subset of std\_logic.  TYPE bit\_vector IS ARRAY (NATURAL RANGE <>) OF BIT;  -- This is indeed the pre-defined type BIT\_VECTOR.  TYPE state IS (idle, forward, backward, stop);  -- An enumerated data type, typical of finite state machines.  TYPE color IS (red, green, blue, white);  -- Another enumerated data type. |
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| IF | IF (clk'EVENT AND clk='1') THEN q<=temp;  END IF; |