VHDL header:

Ieee library

Std\_logic\_1164

Use ieee.numeric\_std.all;

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| Library | LIBRARY library\_name;  USE library\_name.package\_name.package\_parts; |
| Entity | ENTITY entity\_name IS  PORT (  port\_name : signal\_mode signal\_type;  port\_name : signal\_mode signal\_type;  ...);  END entity\_name;  Mode: IN, OUT, INOUT, or BUFFER  ENTITY full\_adder IS  PORT (a, b, cin: IN BIT;  s, cout: OUT BIT);  END full\_adder; |
| Architecture | ARCHITECTURE architecture\_name OF entity\_name IS  [declarations]  BEGIN  (code)  END architecture\_name;  ARCHITECTURE dataflow OF full\_adder IS  BEGIN  s <= a XOR b XOR cin;  cout <= (a AND b) OR (a AND cin) OR  (b AND cin);  END dataflow; |
| Process | 12: The PROCESS is executed every time a signal declared in its sensitivity list changes. |
| Data types | Package standard of library std: Defines BIT, BOOLEAN, INTEGER, and REAL  Package std\_logic\_1164 of library ieee: Defines STD\_LOGIC and STD\_ULOGIC  std\_logic\_arith of library ieee: Defines SIGNED and UNSIGNED |
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