module tb();

reg clk;

reg rst;

//dump file

initial begin

$dumpfile("dump.vcd");

$dumpvars;

end

//simulation time

initial begin

#200;

$finish();

end

//clk

initial begin

clk=0;

#10;

clk=1;

end

//rst

initial begin

rst=1'b1;

#20;

rst=1'b0;

end

//another test

initial begin

$display("Hello, World");

end

endmodule

`timescale 1ns/1ps

// Code your testbench here

// or browse Examples

module tb();

reg clk100;

reg clk50;

reg clk25;

//dump file

initial begin

$dumpfile("dump.vcd");

$dumpvars;

end

initial begin

#200;

$finish();

end

initial begin

clk100=1'b0;

clk50=1'b0;

clk25=1'b0;

end

always #5 clk100 = ~clk100; //100MHz

always #10 clk50 = ~clk50;//50MHz

always #20 clk25 = ~clk25;//25MHz

//always @(a,b) //always\_comb, always\_ff, always\_latch

endmodule