Reza Nejati

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**TECHNICAL SKILLS**

* Proficiency in FPGA design tools, such as Xilinx’s Vivado, ISE, Quartus-II, ModelSim.
* Proficient in writing VHDL and Verilog code.
* Proficient in design and implement RTL logic, Block Level Simulation, FPGA Synthesis,

Writing Physical and Timing constraints (SDC).

* FPGA verification using VHDL / Verilog, System Verilog test benches, file IO and scripts, Write optimal timing constraints.
* Proficient in DSP modeling and hardware realization using FPGA.
* Proficiency in program Xilinx FPGA (Zynq 7000, Zynq UltraScale and Spartan).
* Experience with Intel FPGAs (MAX, Cyclone).
* Proficiency in FPGA Digital design interfacing to peripherals I2C, SPI, I2S, Ethernet, PCIe, ADC, DAC, RS-232/485, TCP/IP, UDP and CAN bus.
* Experience in using DDR memory controllers, AXI DMA, Scatter-Gather DMA, and FIFO.
* Experience to work with RF ADC RF DAC and RF transceiver (ad9361, ad9739).
* Familiar to work with Keras, CNN and Neural Network implementing inside the FPGA using DPU (Vivado, Petalinux, Vitis AI) and hls4ml.
* Experience in AXI interface and PS-PL communication, Linux PS-PL solution.
* Proficiency in fixed-point DSP blocks.
* Experience with Digital Signal Processing operations and optimization: FIR, IIR, CIC FFT, NCOs, DPLLs, Up/Down sampling, multi rate signal processing, convolution, PWM, CORDIC.
* Knowledge of PCB design using Altium Designer (Schematic design, Part Creation, impedance control “Polar Si8000”, differential pairs).
* Experience selecting and integrating image sensors (CMOS, MIPI-CSI, LVDS, and USB) and display (VGA, HDMI, DVI, MIPI-DSI) to FPGA.
* Knowledge of video standards (YUV, RGB, YUV420).
* Experience in interfacing high frequency LVDS ADC and DAC and SPI ADC to FPGA.
* Experience with JTAG programing and debugging, Xilinx ILA, and Chipscope.
* Experience in developing Xilinx HLS kernels using C++.
* Proficiency in use of ARM STM32 microcontroller (RTOS, Motion Control, Keil IDE)
* Knowledge on real-time embedded (Zynq, Microblaze, STM32, PIC and 8051).
* Proficiency with MATLAB and Simulink (HDL Coder, Xilinx System Generator for DSP).
* Proficiency in using Linux OS, customize Linux using PetaLinux.
* Experience in embedded software design for Arm cores on Xilinx SDX.
* Experience in design image processing hardware accelerator using HLS, OpenCV.
* Fluency in the C / C++, Python and Makefile systems (make, CMake).
* Proficiency in motor control system design (Steeper motor, BLDC, induction machine).
* Familiar with TCL scripting language.
* Proficiency in Model Based design techniques using Matlab / Simulink.
* Experience in programing of AVR, PIC, Arduino, Raspberry and BeagleBone.
* Proficiency in the use of lab equipment such as Oscilloscope, Logic analyzers, power supplies.

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**WORK EXPERIENCE**

* **Research and Development Engineer,** January 2022 to present  
  **SAMM Teknologi, Istanbul, Turkey.**

**Responsibilities**

* Interfacing the ad9361 transceiver to the Kintex FPGA.
* Building the hardware platform for using the DPU, Create Linux platform in the Petalinux in the Zynq FPGA.
* **FPGA Engineer,** September 2018 to November 2021  
  **Simut Co, Tehran, Iran.**

**Responsibilities**

* Design and develop RTL code for use in ultrasonic signal processing, interfacing LVDS ADC, SPI ADC and sonar Pulser to FPGA, writing the DSP code using VHDL and HLS.
* Writing the test bench for test and verify the FPGA code using MATLAB.
* Customize Linux using Petalinux.
* **FPGA Engineer,** April 2015 to September 2018  
  **Novinilya Co, Isfahan, Iran.**

**Responsibilities**

* Interfacing image sensor to FPGA, Implementing Computer Vision algorithms into the FPGA, creating hardware image co-processor using Vivado HLS, Mapping image processing algorithms to hardware (FPGA, Sitara SoC), researching cost and size effectiveness of image processing solution in hardware. Developing Linux using Petalinux.

**TEACHING AND RESEARCH EXPERIENCE**

* **Lecturer of Electrical Engineering (Full time) ,**2006 to 2015

Islamic Azad University Majlesi Branch, Isfahan, Iran.

**Responsibilities**

* Teaching course: Microcomputers, Fuzzy Controller, Neural Network,

Linear Control Systems Lab, Electrical Machine Lab, Distribution System.

Head of Research center in embedded system and DSP Engineering.

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EDUCATION

* Master’s Degree in Electrical Engineering Islamic Azad university Najaf Abad Branch, Isfahan, Iran, September 2004 to September 2006.

Thesis: Design and Simulation of Adaptive Neuro-Fuzzy Stabilizer in Multi

Machine Power System.

* Bachelor’s Degree in Electrical Engineering Islamic Azad University Khomni Shahr Branch, Isfahan, Iran, and September 1997 to July 2002.

Senior Project: Experimental Design of Self Tuning Inverter using

8051 Microcontroller.

**LANGUAG**

* Proficiency in English TOEFL IBT 85, October 2020.

**Certifications**

* Efficient implementation of DSP algorithm on FPGA, Iran Science and Technology University, April, 2014.

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**References**

* **Mohammad Eghbali Ghahyazi, Manager Digital Radio Functions at Ericsson**

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