AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH
Faculty of Engineering

Laboratory Report Cover Sheet

Students must complete all details except the faculty use part.

Please submit all reports to your subject supervisor or the office of the concerned faculty.

Laboratory Title: Study of Jfet and Mosfet characteristics
Experiment Number: 8 Due Date: 29-11-22 Semester: Fall
Subject Code: EEE 2109 Subject Name: Electronic device Lab Section: C
Course Instructor: Dr. Mohammad Shidujaman Degree Program: BSc EEE

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Title: Study of Jfet and monfet characterization

Introduction: The most common transistor types are the metal Oxide semiconductor field effect transistors and the bipolar junction transistors. BJTs based circuits dominated the electronics market in 1960s and 1970s. Nowdays most electronic circuits, particularly integrated circuits are made of monfets. The bjt are mainly used for specific applications like analog circuits high speed circuits or power electronics. There are two main difference

between bjt and fets. The first in that fets are charge-controlled devices while bjts are current controlled devices. The second difference in that the input impedence of the fets in very high while that of bjt is low. As for the fet transistors, there are two types; the junction field effect transistor and metal oxide field effect transistor. The combination of n type and p type mosfets allow for the realization of the complementary metal oxide semiconductor technology.

Theory and Methodology:

Transistor is a kind of current control device and its generating current includes electron flow and hole flow. The transistor is therefore referred to as bipolar junction transistor. Fet is unipolar device in which the current of n channel fet is formed by electron flow and the current of p channel is formed by electron flow. fet is a kind of voltage-control device. fet can also perform the function that general transistors do with the only exception that the bias

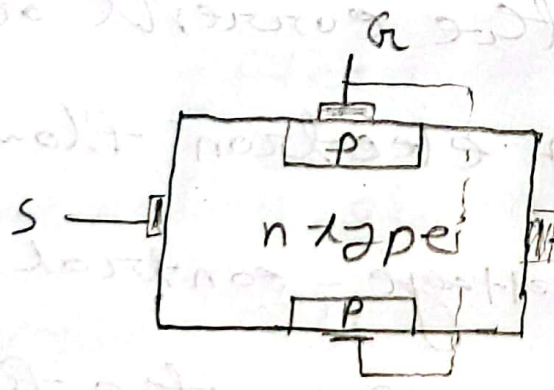
conditions and characteristics.

The characteristics of fet is listed as follows:

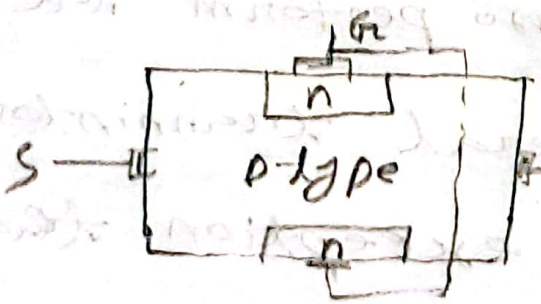
2) fet has very high input impedence

2) When fet is used as switch there is no offset voltage.

3) During operation the thermal stability of fet is higher than that of bjt

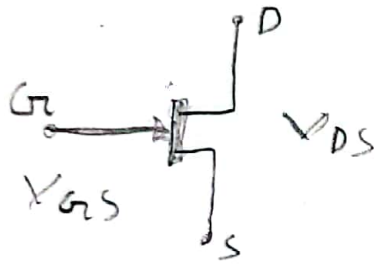


a) n-channel

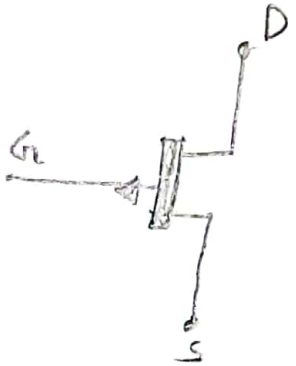


b) p-channel

The internal structure of jfet is shown in figure 1. The n channel jfet is formed by diffusing one pair of p-type region into a slab of n-type material.

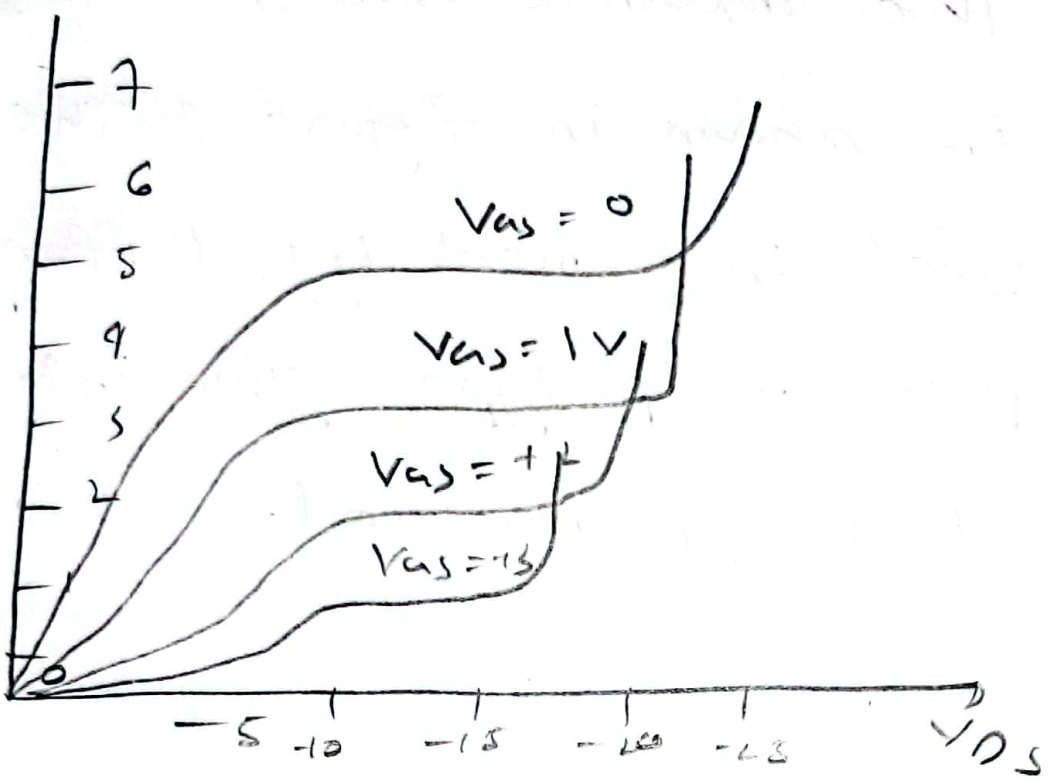


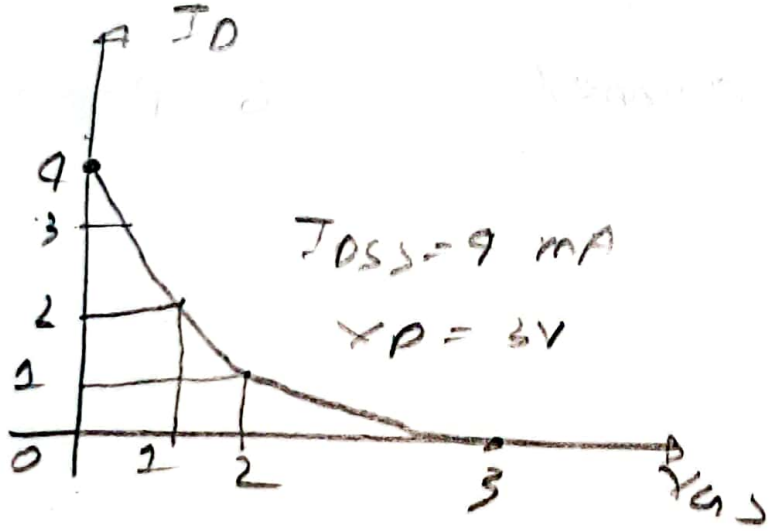
a) n-channel



b) p-channel

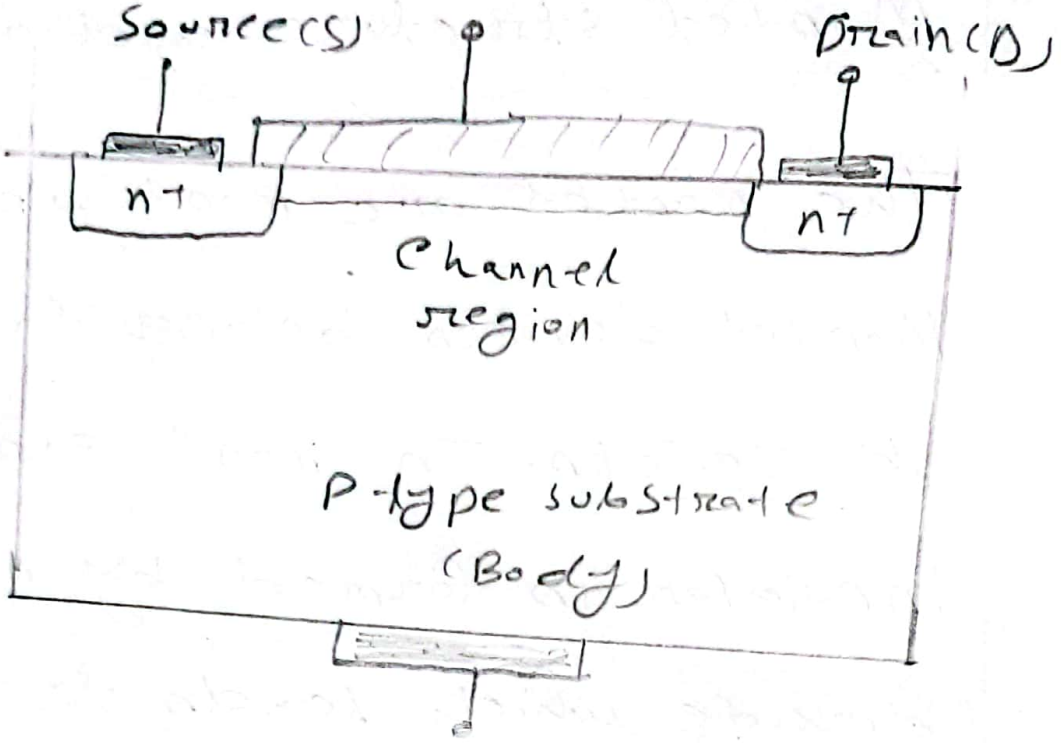
The p-channel jfet is constructed in the same manner as the n-channel device of but with a reversal of the p and n type materials.


7
6
5
4
3
2
1
0
$V_{GS} = 0$
$V_{GS} = -1V$
$V_{GS} = -2$
$V_{GS} = -3$
-5
-10
-15
-20
-25
V_{DS}

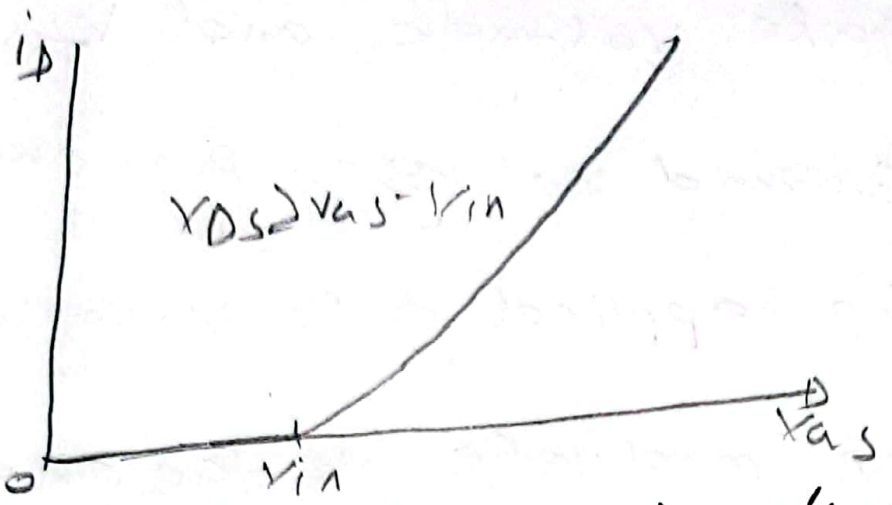

I_D
4
3
2
1
0
1
2
3
V_{GS}
$I_{DSS} = 9$ mA
$V_P = -3V$

Monfet structure and operation:

The monfet are most widely fetn. Monfet devices belong to the group of Igfetn. In most cases the insulator is formed by silicon dioxide which leads to the term monfetn. Monfet like all other igfets has three terminal which are called gate (G), Drain (D) and source (S). There are four type of monfet. The type depends wheter the channel between the drain and source is an electron current or a hole current.

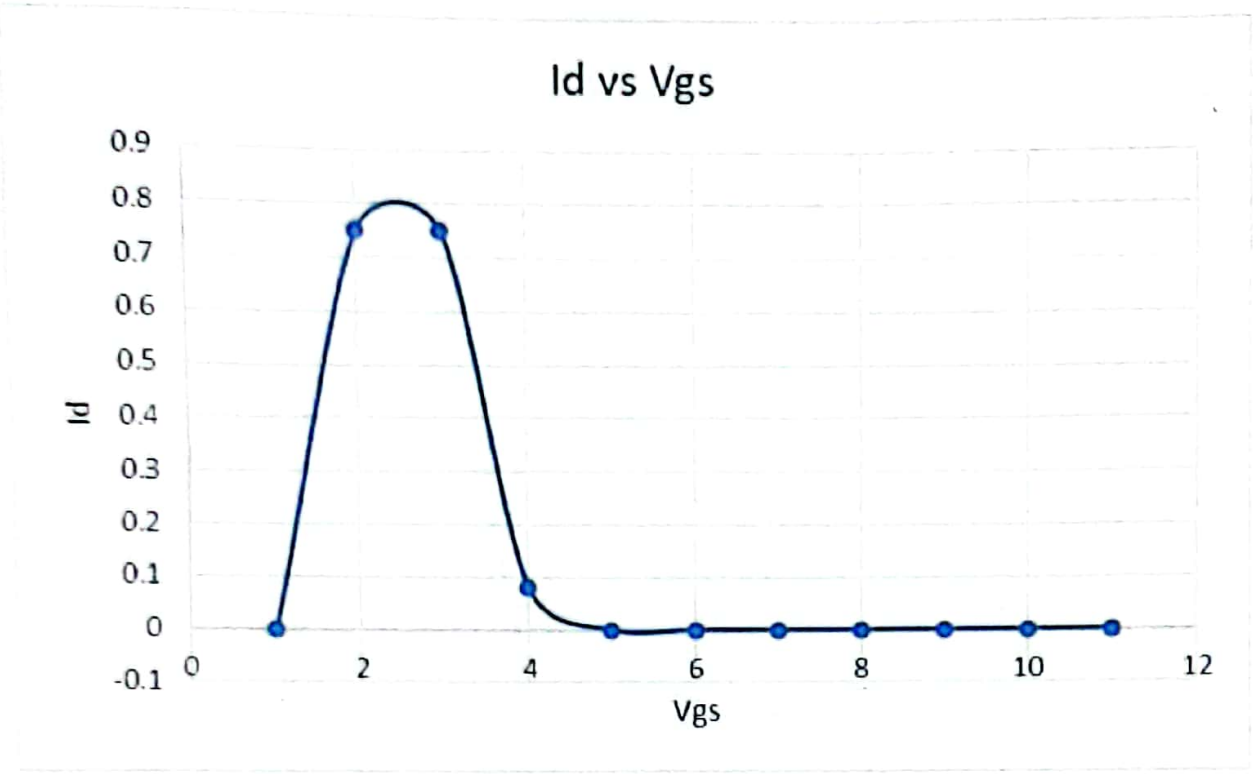


From the region of substrate under the gate due to the positive voltage applied to the gate The holes are pushed away down wards into the substrate leaving behind a depletion region. At the same time the positive gate voltage attracts into the channel region.

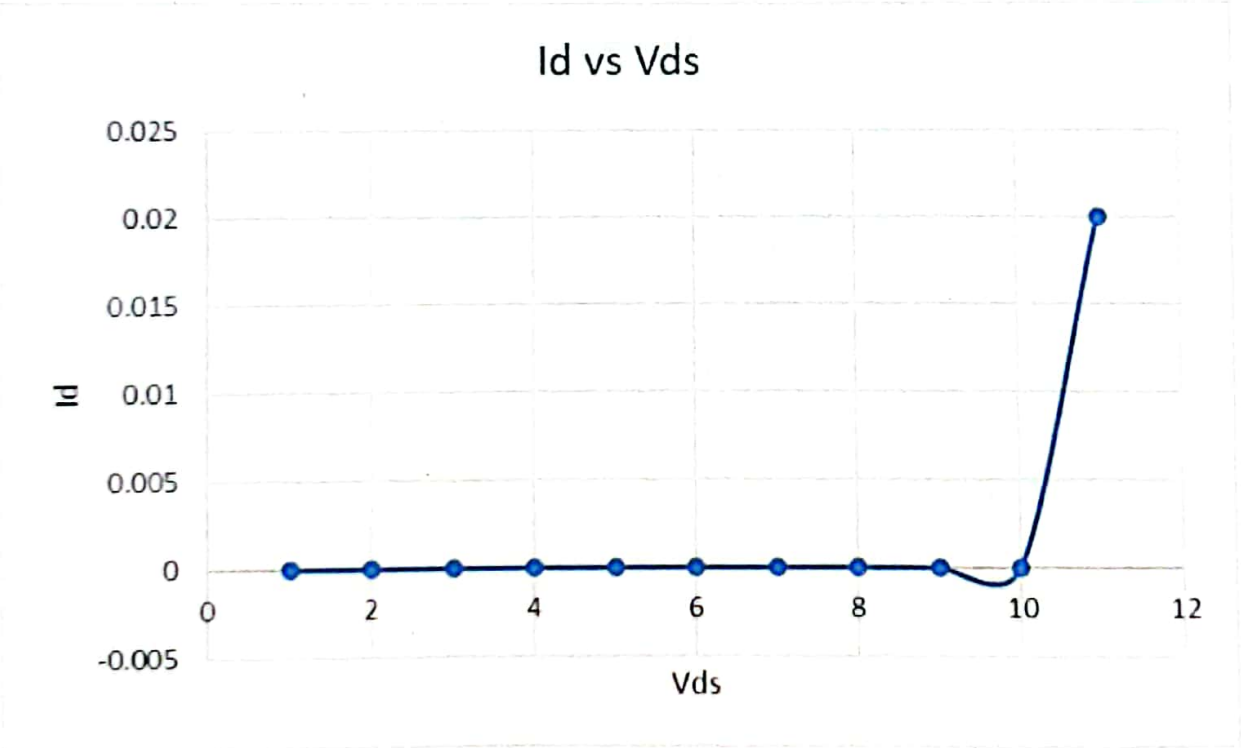


The induced n region thus forms the channel for current flow from drain to source. The channel is only a few nanometers wide. Nevertheless the entire current transport occur in the channel between drain and source. So in order for current the current to flow from drain to source the condition should be satisfied is $v_{GS} > V_{TN}$, where V_{GS} is the

gate voltage and V_{th} is the threshold voltage. By changing the applied gate voltage we can modulate of the channel. Such kinds of Mos transistors are realized by the physical implanatation of an n-type region between the drain and source.



For table 1



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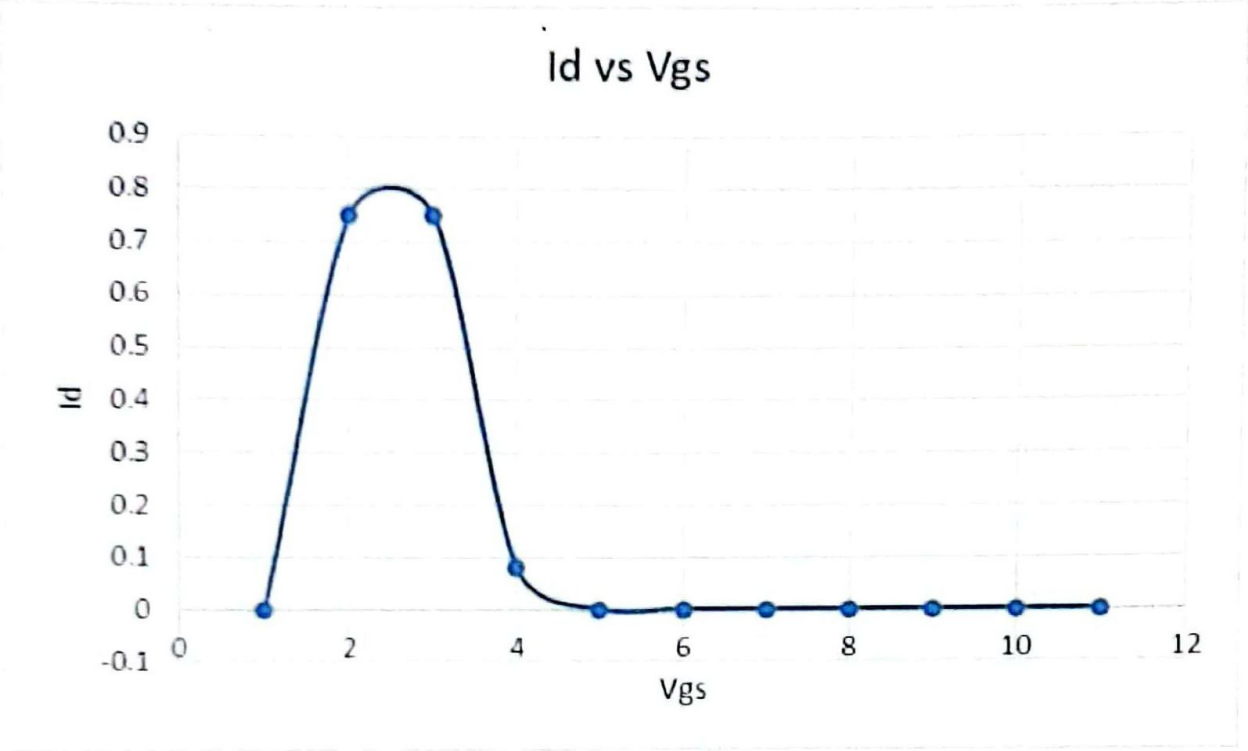
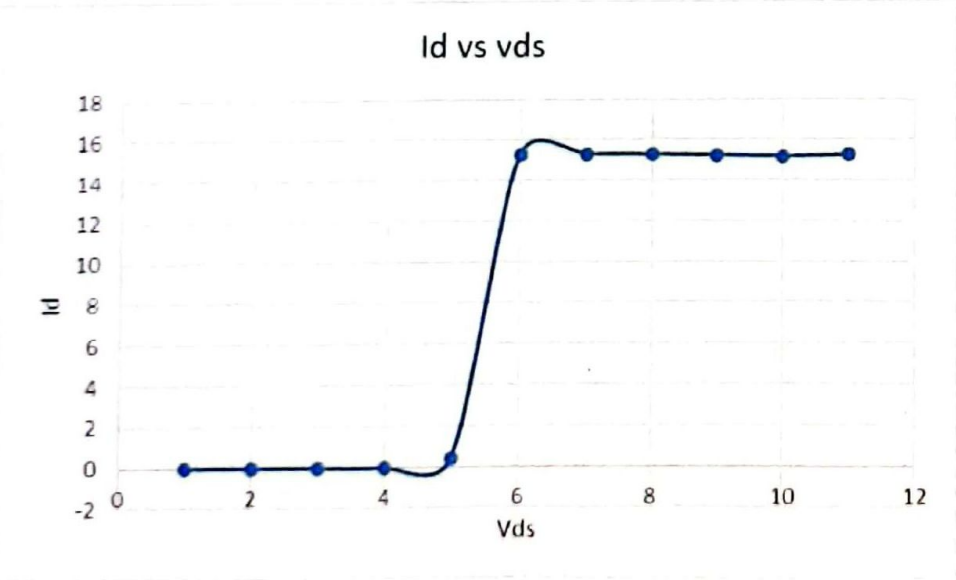
~~For table 2~~

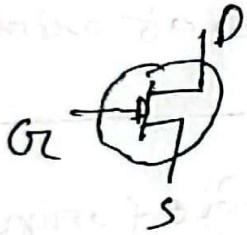


For table 3

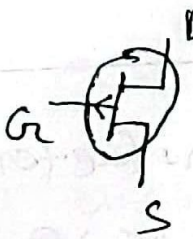


For table - 4

3. Jfet stands for junction field effect transistor. The jfet is a three terminal semiconductor device and the terminals are source, drain, gate. Jfet has a channel between source and drain.



N-channel fet



P-channel fet

Mosfet stands for metal oxide semiconductor field effect transistor.

Jfet	Mosfet
Jfet operates only in depletion mode	Mosfet can be operated in both mode
Jfet has a gate terminal which is not insulated from the channel	The gate terminal of the mosfet is not insulated from thin layer of oxide
The manufacturing process of jfet is simpler	Manufacturing of mosfet is complex
For jfet gate current is more	For mosfet gate current is less
Jfet is used in low noise applications	Mosfet is used in high noise application

2. Biasing Methods make the transistor circuit active, saturation region. cutoff region.

Active region is also called Linear region. This region lies between saturation and cutoff. This is the region where the mosfet works. cutoff region is the region where mosfet operate in the off region. for turning this we need to apply the voltage above the threshold voltage

Conclusion:-

The characteristics of jfet and mosfet is defined by a plotting a curve between the drain current and drain voltage. The transfer characteristics was defined by observing different values of drain current with variation in gate-source voltage.