AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH
Faculty of Engineering

Laboratory Report Cover Sheet

Students must complete all details except the faculty use part.

Please submit all reports to your subject supervisor or the office of the concerned faculty.

Laboratory Title: Study of Inverter Circuit using MOSFET and DJT
Experiment Number: 9 Due Date: 6-Dec-22 Semester: Fall 2022-23
Subject Code: EEE 2104 Subject Name: Electronic Devices (LAB) Section: C
Course Instructor: Dr. Mohammad Shidujaman Degree Program: Bsc EEE

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Faculty comments_____

Abstract: This experiment gives an excellent practical realization of the RTL inverter, NMOS inverter, and CMOS Inverter. At first a CMOS Inverter will be designed, simulated and understood in the pre-lab sec. then all kind of Inverter circuits mentioned above will be designed on the project board in the laboratory and analysed the theoritical concepts and the practical results.

Introduction: The objective of this experiment is to observe - RTL inverter, NMOS inverter and CMOS inverter.

Theory and Methodology: RTL is a large step beyond DL. Basically, RTL replaces the diode switch with a transistor switch. If a +5V signal is applied to the base of the transistor, the transistor turns fully on and grounds the output signal. If the input is grounded, the transistor turns off and the output signal rises to +5 volts. In this

way, the transistor inverts the logic sense of the signal, but also it ensures that the output voltage will always be a valid logic level under all circumstance. Because of this, RTL circuits can be cascaded indefinitely, where DL circuits can not be cascaded reliably at all.

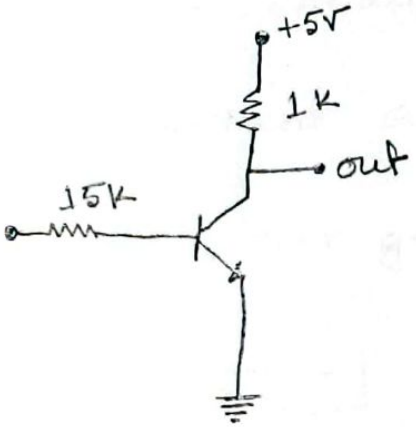

Fig: N-MOS Inverter.

N-MOS Inverter: An inverter can be designed with a single NMOS and a resistor. In case of NMOS inverter two NMOS are used where one is used as a load and another one as used for inverting the input. The load transistor must have a high and the switching transistor have a low resistance.

CMOS Inverter: The two MOSFETs are designed to have matching characteristics. Thus, they are complementary to each other. when off, their resistance is effectively infinite; when on, their channel resistance is about 200 ohm. Since the gate is essentially an open circuit it draws no current, and the output voltage will be equal to either ground.

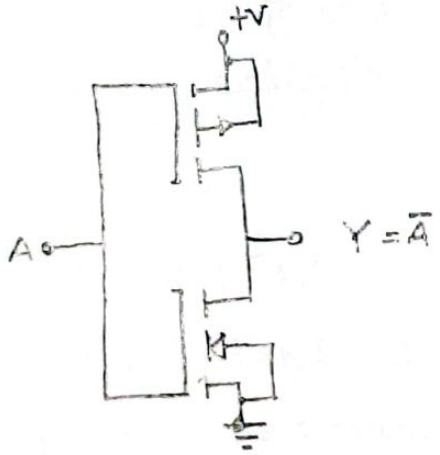

Fig: CMOS inverter.

when input A is grounded, the N-channel MOSFET is forward biased, so it has a channel enhanced within it selb. This channel has a resistance of about 200 ohm, connecting the output line to the +V supply. This pulls the

output upto +V. When input A is at +V, the P-channel MOSFET and N-channel MOSFET is on, thus pulling ~~out~~ the output down to ground. Thus, this circuit has correctly performs logic inversion, and at the same time provides active pull-up and pull-down, according to the output state.

Apparatus:

1) DC Power Supply [1]
2) Power Supply Cable [2]
3) Multimeter [1]
4) Project Board [1]
5) For RTL Inverter [1]
5) 1k and 15k Resistance [1]
6) 2N4124 NPN Silicon transistor, or equivalent [1]
7) DMM [1]

For CMOS Inverter [1]

10) IRF 9540: enhancement type p-channel MOSFET [1]
11) IRF 540: enhancement type n-channel MOSFET [1]

Precautions: Have your instructor check all your components and connections after you done settings up the circuit and make sure only enough voltage to turn on the chip, otherwise it may get damaged.

Experimental Procedure:

1. Construct the circuit as shown in figure
2. Use multimeter to take the readings.

RTL Inverter	Vin	V_c	V_{BE}	I_B	I_c
A = 0	0 V	2.6V	2.6 V	0	2.7
A = 1	4.43V	.048 V	0.698V	.46 mA	2.6

Table-1: RTL Inverter circuit Parameter

NMOS Inverter	Vin	V_D	V_{DS}	I_D
A = 0	5.1	1.7V	1.7 V	1.9 mA
A = 1	3.5	.005 V	0.028mV	0

Table-2: NMOS Inverter Circuit Parameter.

CMOS Inverter	MOSFET Type	V_{in}	V_D	V_{DS}	I_D
A=0	PMOS	5V	5	0	5.1mA
	NMOS	-0.3V	5	5	5.1 mA
A=1	PMOS	5V	0	5	0
	NMOS	5V	0	0	0

Questions for report writting:

RTL: advantages:- The primary advantages of RTL was that it used a minimum number of transistor, thats makes RTL low cost from another.

NMOS: Advantages:-

1. Very low power dissipation.
2. Power supply can be varried.
3. Large fan out Capability.

Disadvantage:-

1. Speed of operation are lowest due to High Capability.
2. Large propagation delay per gate.

CMOS: Advantages:-

1. Extreamly large fan-out Capability.
2. lower power dissipation.
3. Lower propagation delay than nmos.

Dis advantages:-

1. Increased Cost due to additional processing.

Discussion and Conclusion: Interpret the data an determine the extent to which the experiment was successful in complying with the goal that was initially set.

Refferences:

1. AIUB ED lab manual.
2. A.S. Serda, K.C Smith, A D, Microelectronic Circuits, Oxford press (1998)
3. J.K Keown, ORCAD Pspice. and Circuit Analys prentice Hall press (2001)