AMERICAN INTERNATIONAL UNIVERSITY BANGLADESH
Faculty of Engineering

Laboratory Report Cover Sheet

Students must complete all details except the faculty use part.

Please submit all reports to your subject supervisor or the office of the concerned faculty.

Laboratory Title: Bipola Junction Transistor (BJT) study of single stage Transistor common Emitter
Experiment Number: 07 Due Date: 22/11/22 Semester: Fall 2022-23
Subject Code: EEE____ Subject Name: Electronic Device Lab Section: "C"
Course Instructor: Dr. Mohammad Siddiqaman. Degree Program: BSc. EEE / BSc. CSE

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Group Number (if applicable): 07 ☐ Individual Submission ☑ Group Submission

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Faculty comments _____

Title: Bipolar Junction Transistor (BJT): Study of single stage transistor Amplifier.

Introduction: The aim of the ac analysis is to determine the voltage amplification (A_V), current amplification (A_I), input impedance (Z_i), output impedance (Z_o), and the phase relation between the input voltage (V_i) and the output voltage (V_o). After performing the dc analysis, we will now calculate the small signal parameters depending on the model being used, draw the small signal equivalent circuit and then perform the ac analysis.

The main objectives of this experiment are to –

1. Trace the circuit diagram of a single stage transistor Amplifier;
2. Measure Beta (β) of the transistor with multimeter.

3. Measure the Q-point.
4. Measure the maximum signal that can be amplified with the amplifier without any distortion.
5. Measure the maximum voltage gain of the amplifier at 1 KHz.
6. Measure the voltage gain of the amplifier at different values of load resistance.

Theoretical Background: The analysis is done assuming that the signal frequency is sufficiently high. Subsequently it can be assumed that all the coupling capacitors (C_E) act as perfect short circuit. Such a frequency is said to be in the mid band of the amplifier.
The hybrid-π model and T-model can be valid only for small signals. The general forms of these models are shown in the following figures 1 and 2.

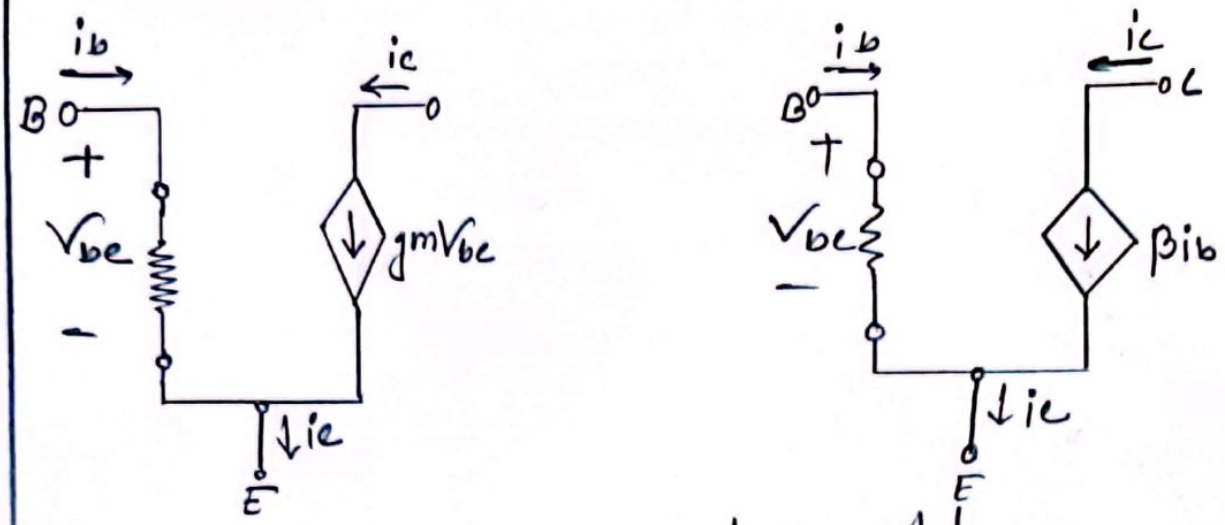

Fig: 1 The Hybrid π-model

Where, Transconductance

$$g_m = \frac{I_C}{V_T} \quad \text{and} \quad V_T = \frac{KT}{q}$$

Common emitter input resistance

$$r_\pi = \frac{\beta}{g_m}$$

Common base input resistance.

$$r_e = \frac{\alpha}{g_m}$$

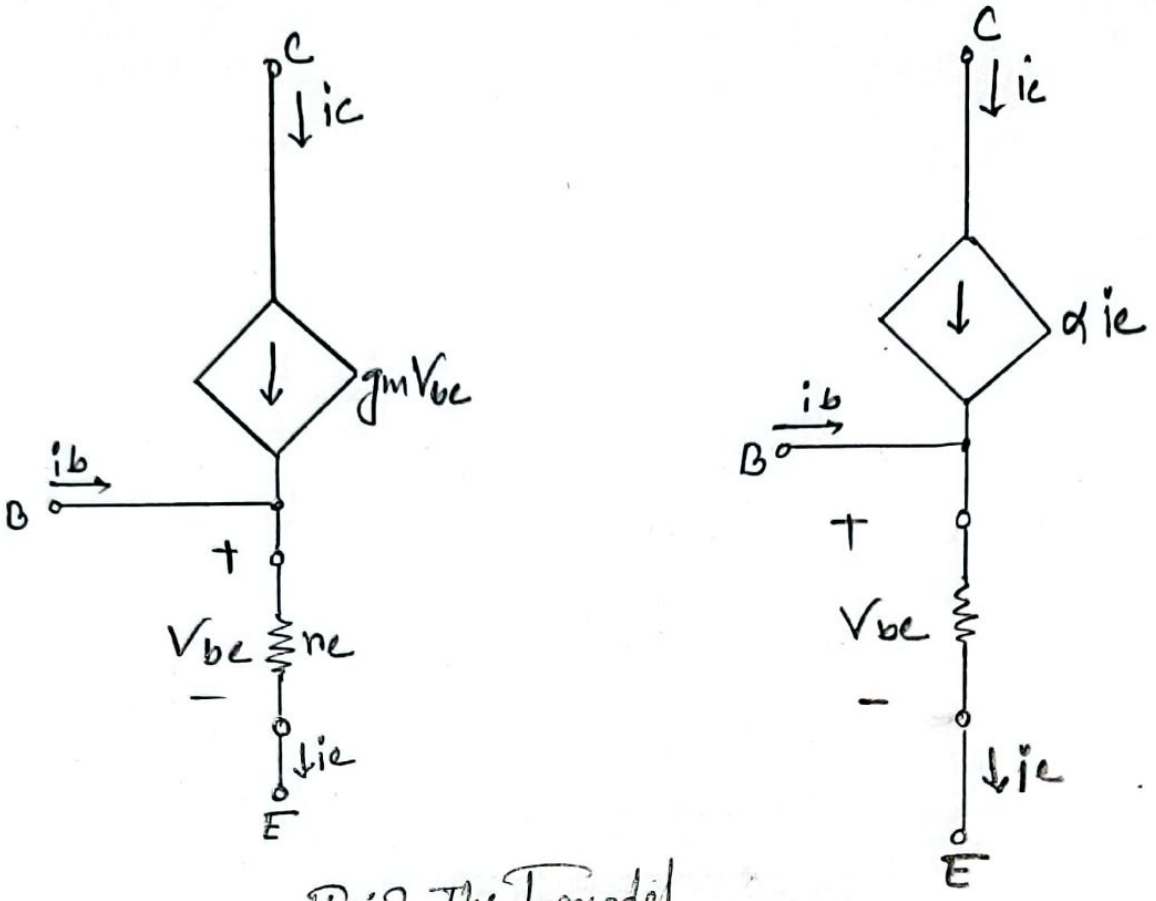

Fig:2 The T-model

Since in this experiment we will mainly concentrate on single stage amplifier where most widely used single transistor amplifierr in common emitter configuration is shown in the figure below.

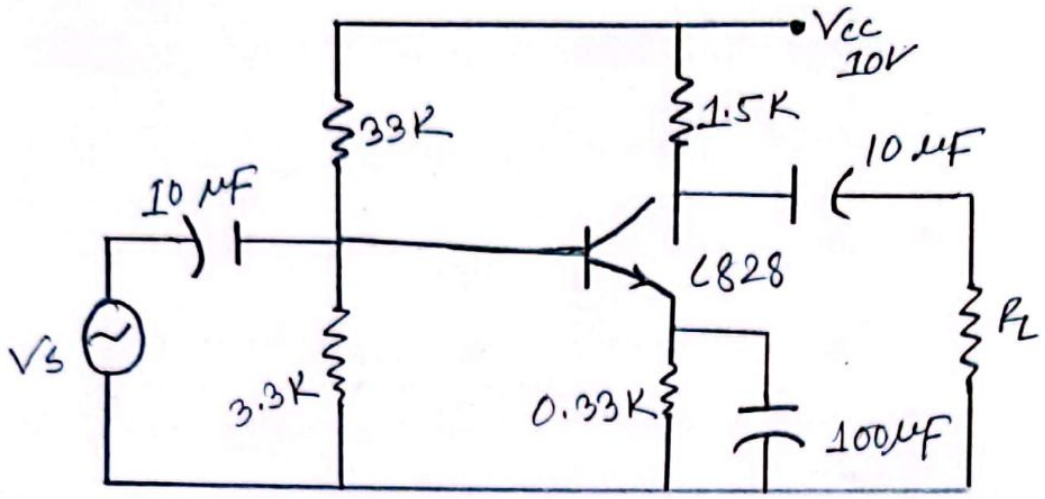

Fig: 3 Single Stage CE Amplifier.

Apparatus:

NO	Apparatus	Quantity
1.	Transistor (C828)	1
2.	33K, 10K, 4.7K, 1K, 3.3K, 1.5K, 330Ω	1 for each Resistor
3.	Project Board	1
4.	Cathode Ray Oscilloscope (CRO)	1
5.	Multimeter	1
6.	Signal Generator	1
7.	100 μF Capacitor	1
8.	Probes	2
9.	Power supply cable	2

Precaution: Transistors are sensitive to be damaged by electrical overloads, heat, humidity and radiation. Damage of this nature often occurs by applying the inconnect polarity voltage to the collector circuit or excessive voltage to the input circuit One of the most frequent causes of damage to a transistor is the electrostatic discharge from the human body when the device is handled.

Experimental Procedure:

1. Measure β of the transistor with multimeter.
2. Calculate Dc operating point of the transistor circuit.
3. Implement the circuit as shown in the figure.
4. Measure the operating point with the help of table:1 and compare with your calculate value.

5. Feed ac signal of 1 KHz at the input and observe the input and output on the CRO.

6. Increase the input signal till the output wave shape starts getting distorted. Measure this input signal. This is the maximum input signal that the amplifier can amplify without any distortion.

7. Now feed an ac signal that is less than the maximum signal handling capacity of the amplifier. Fix the input signal frequency at 1 KHz, Draw the input and output voltage wave shape and calculate gain.

8. Connect different load resistors and find the voltage gain of the amplifier for each.

Observations:

1. Q-point of the amplifier:

V_{cc}	V_c	$V_{cc}-V_c$	$I_c = (V_{cc}-V_c)/R_c$	V_{cc}
10 V	8.69V	1.29V	4.93 mA	8.40V

2. Maximum signal that can be handled by the amplifier without introducing distortion = 50 V and Operating frequency = 50KHz.

3. Voltage Gain of the Amplifier:

Load resistor	Input Voltage	Output voltage	Gain
1K	410 mV	3V	1.31 V
4.7K	410 mV	4.26 V	10.39 V
10K	410 mV	4.88 V	11.91 V
100K	410 mV	4.78 V	11.65 V

Calculation:

$$IC = (Vcc - Vc)/Rc$$

$$= 8.607$$

$$\text{Gain} = \frac{\text{Output}}{\text{Input}}$$

Simulation and Measurement:

Table 1:

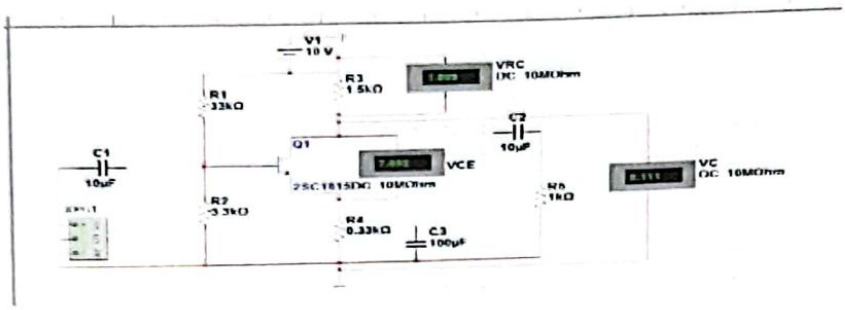

Fig: 4

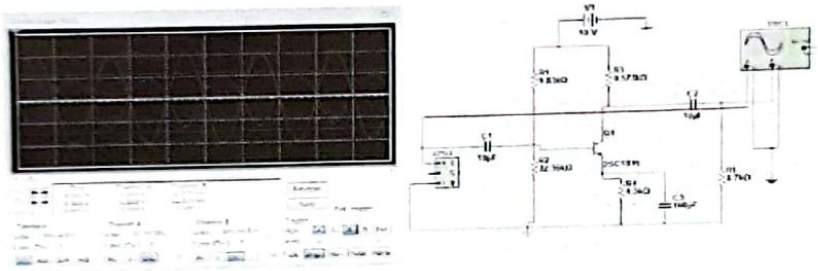

Fig: 5

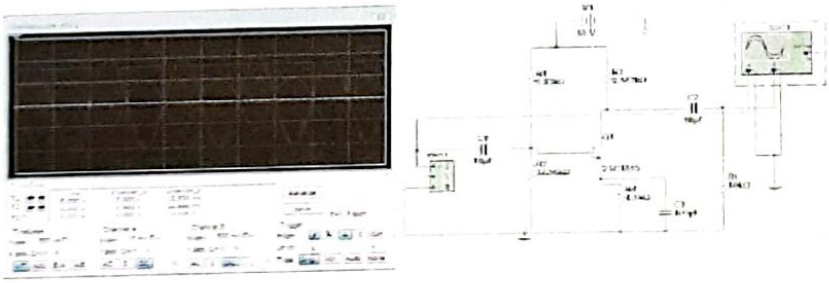

Fig: 6

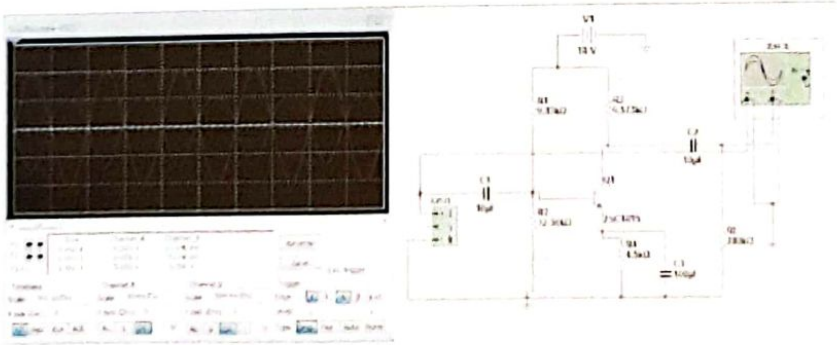

Fig: 7

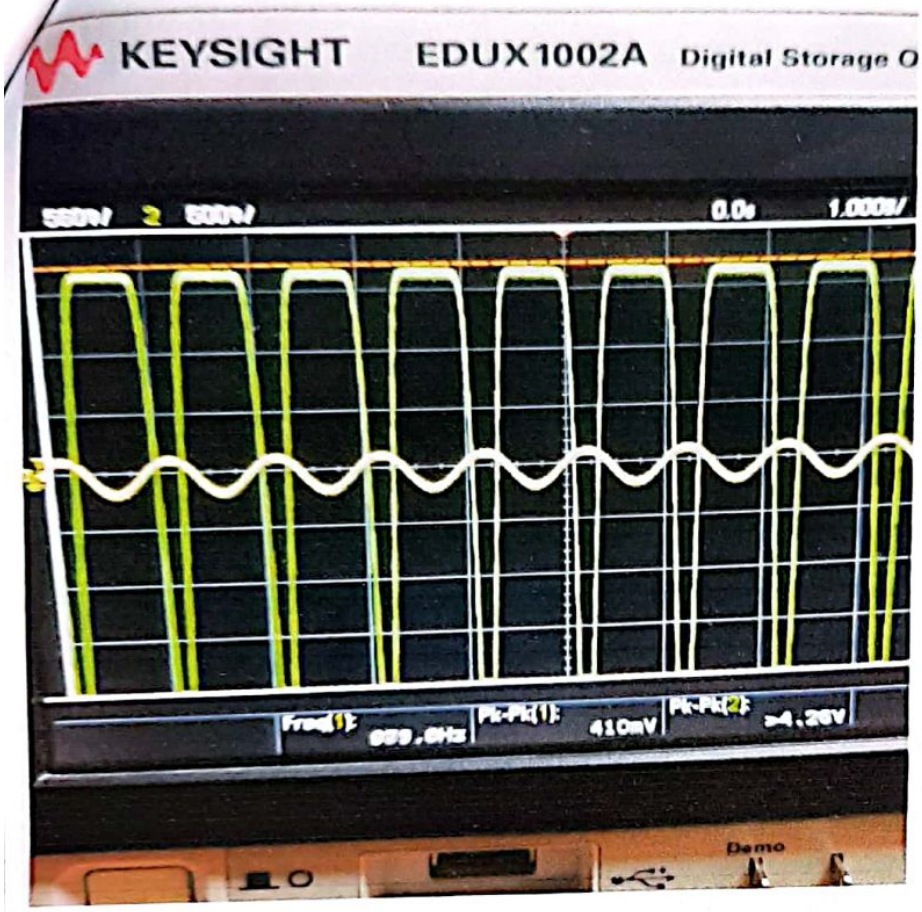

Fig: single stage CE Amplifierr wave

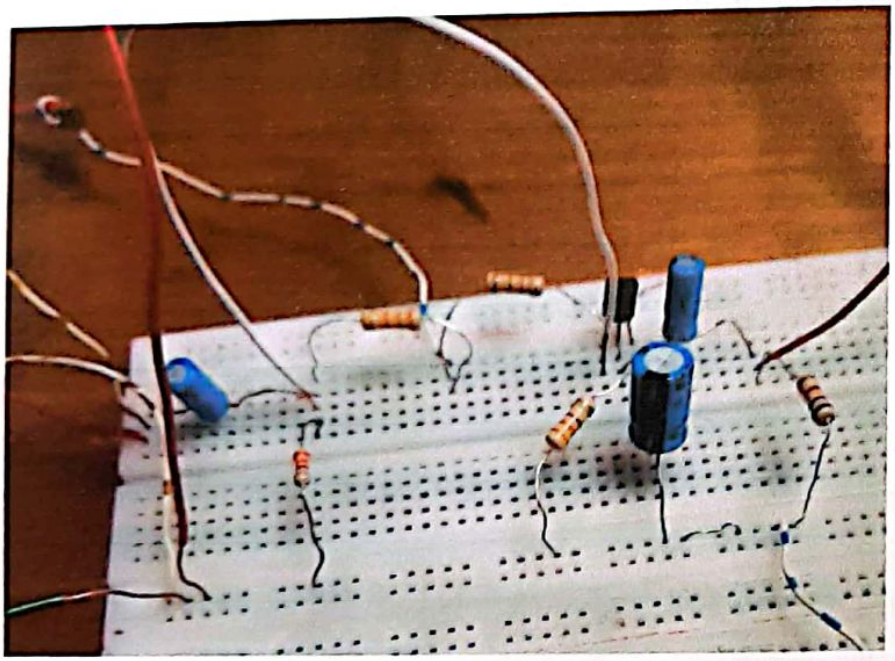

Fig: single stage CE Amplifier

Discussion:

1. The dc power source needs to be switched off while changing the transistors.
2. The trainer board needs to be checked if working properly.
3. The circuit was connected properly and was also checked before taking the readings

References:

1. American International University-Bangladesh (AIUB) Electronic Devices Lab manual.
2. A.S. Sedra, K.C. Smith, "Microelectronic Circuits" Oxford University Press (1998).
3. J. Keown, ORCAD PSpice and circuit Analysis Prentice Hall Press (2001)
4. P. Horowitz, W. Hill, "The Art of Electronics," Cambridge University press (1989)