Digital Logic Design :

Lecture 7

Perform the following Logic operation using only NAND gates :

$$F = A(B + CD) + B\bar{C}$$

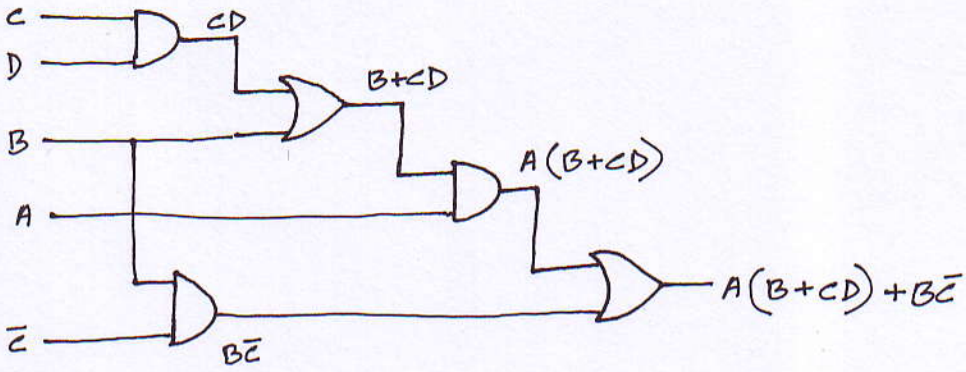
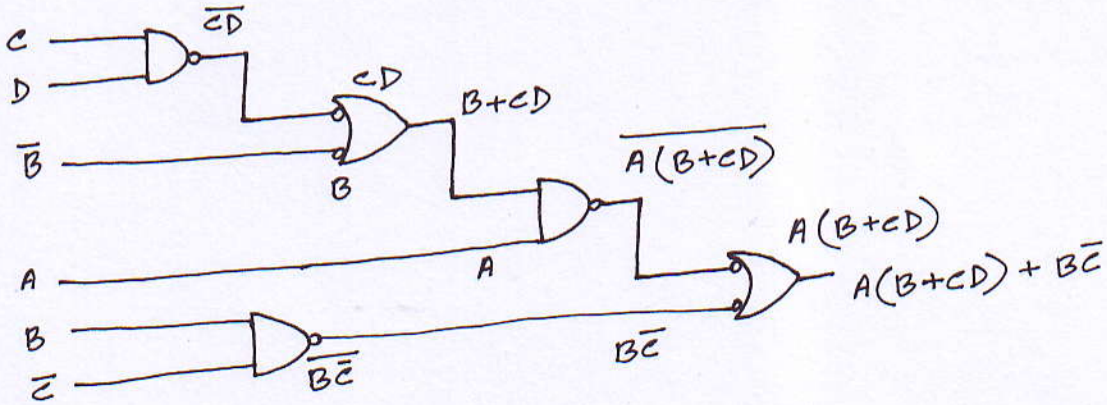


Fig : AND/OR implementation



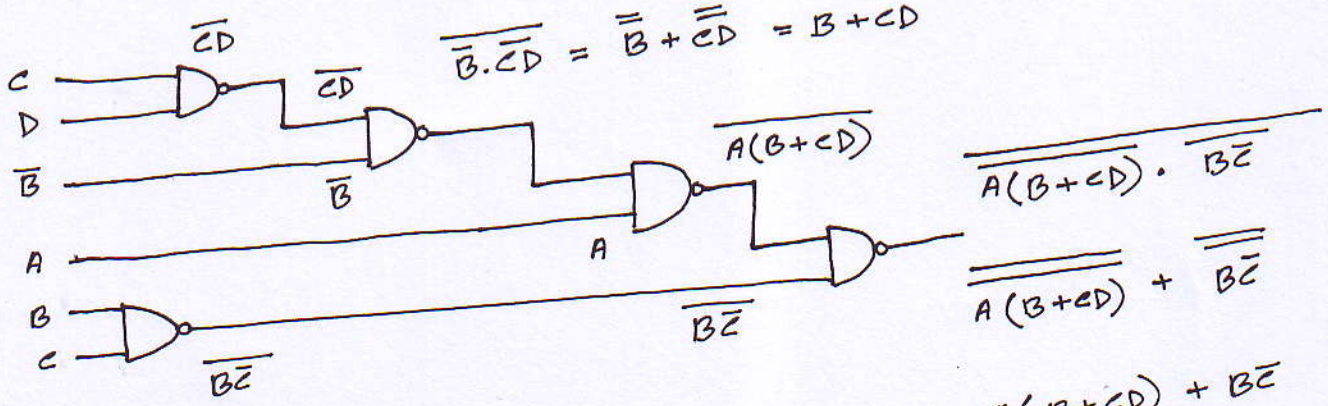
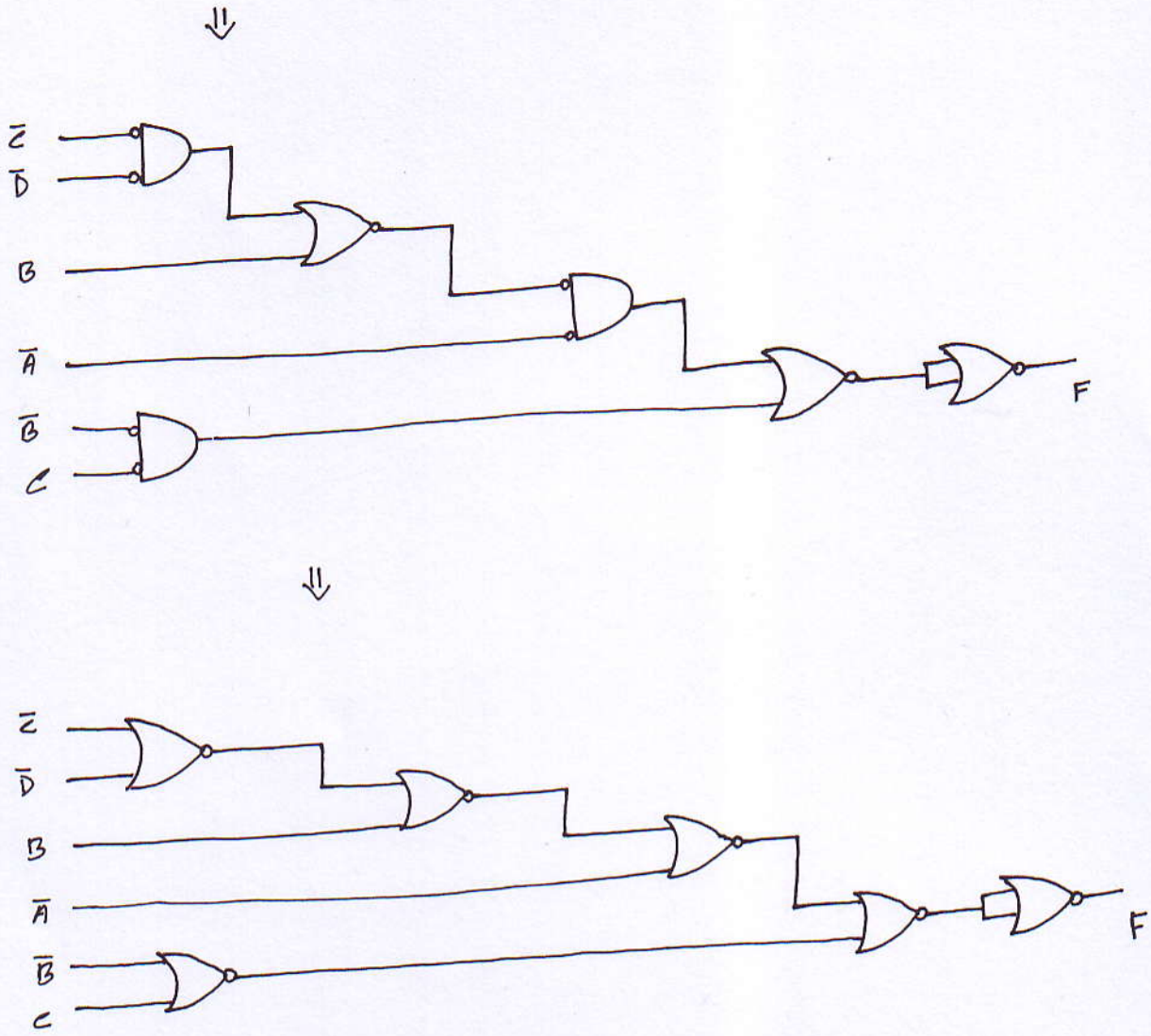
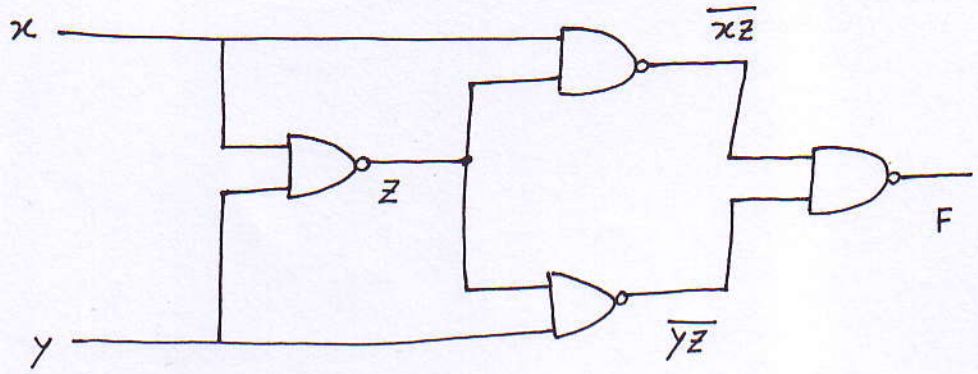


Fig : NAND implementation

Using only NOR gates



Determine the truth table for the following cht :



x	Y	$z = \overline{xy}$	$\overline{xz}$	$\overline{yz}$	F
0	0	1	1	1	0
0	1	1	1	0	1
1	0	1	0	1	1
1	1	0	1	1	0

$\therefore$ $F = x \oplus Y$

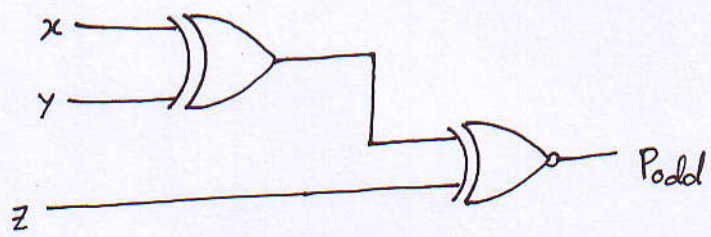
Parity Bit : A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message including the parity bit, is transmitted and then checked at the receiving end for errors. An error is detected if the checked parity does not corresponds to the one transmitted. The circuit that generates the parity bit in the transmitter is called the parity generator. The circuit that checks the parity in the receiver in the receiver is called

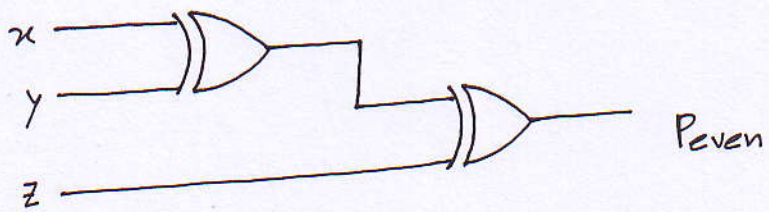
Odd parity generation / Even parity generation

Three bit message x	y	z	Odd parity generated P_{odd}	Even parity generated P_{even}
0	0	0	1	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	0	1

$$P_{odd} = x \oplus y \odot z$$

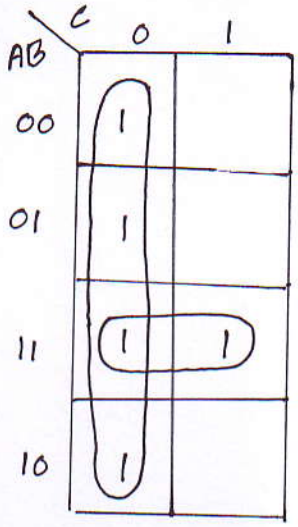
$$P_{even} = x \oplus y \oplus z$$



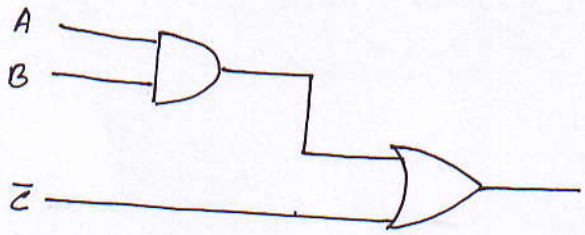


Implement a logic circuit for the following truth table with minimum gates :

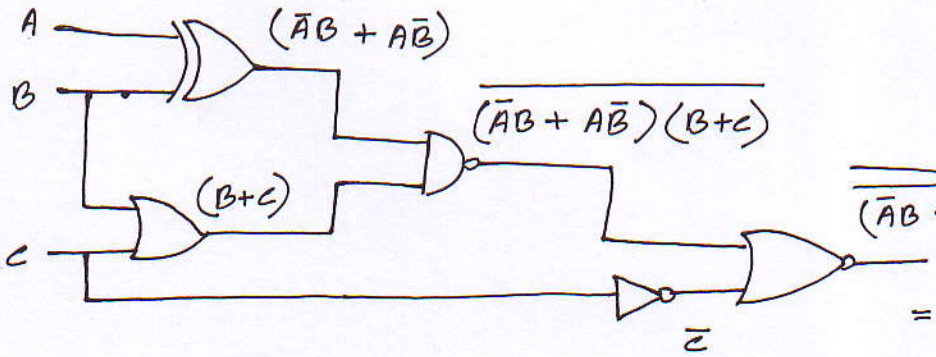
Inputs			Output
A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1



$\therefore X = \bar{C} + AB$



form a truth table for the following logic circuit



$$\overline{(\bar{A}B + A\bar{B})(B+C) + \bar{C}}$$

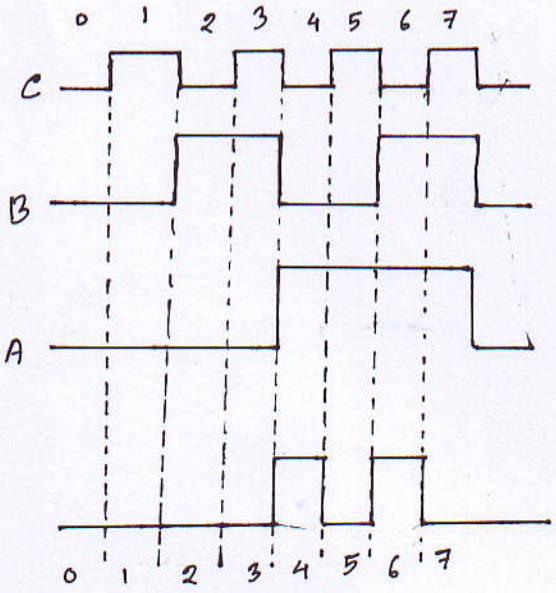
$$= \overline{\overline{(A \oplus B)(B+C)} \cdot \bar{C}}$$

$$= (A \oplus B)(B+C) \cdot C$$

$$F = \overline{(\overline{A\bar{B} + \bar{A}B})(B+C) + \bar{C}}$$

Truth table :

Inputs A B C	A ⊕ B	Output F
0 0 0	0	0
0 0 1	0	0
0 1 0	1	0
0 1 1	1	1
1 0 0	1	0
1 0 1	1	1
1 1 0	0	0
1 1 1	0	0



Draw the timing diagram for the output variable (F) of the circuit described above when the timing diagram for input variables A, B and C are as below,