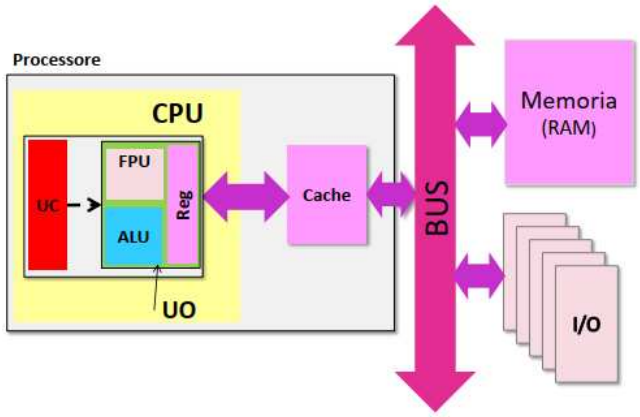
Summary of Computer Architecture (07CJJM – CS)

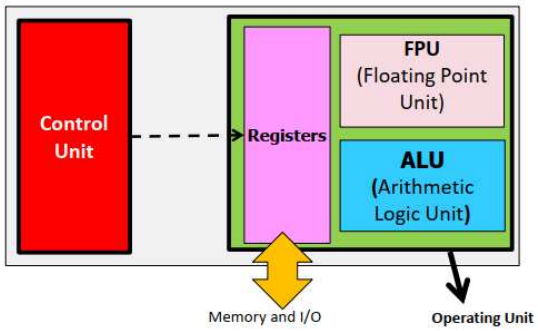
1. Overview



- **Input/Output (I/O) devices**
  Enable the interaction of the computer with the external world, by means of synchronized digital signals.
  - **Input**: From the external world to the system
    Examples: Keyboard, Mouse, Microphone, etc.
  - **Output**: From the system to the external world
    Examples: Monitor, Printer, Loudspeakers, etc.

2. Central Processing Unit

- It performs all the required elaborations (arithmetic, logic, graphic...).
- It is composed by:
  Control Unit
  Registers
  Flags
  ALU/FPU



- **Control Unit**
  It is the computer heart:
  - According to the provided program...
  - And the state of all the units...
  - Schedules the operations to be executed...
  - And issues the corresponding instructions

  Main elements

  - Program Counter
  - Instruction Register
  - Control Logic

- **Registers**
  - Local memory elements used for storing data temporally (ex.Partial results).
    - Small number (8...128)
    - word dimension (8...64 bit)

- **Flags**
  - State indicator of the ALU operation result
  - single bit (0=false, 1=true)
  - usually grouped into a register
  - Most common flags:
    - Z (zero) V (overflow)
    - CY (carry) N (negative)

- **ALU & FPU**
  Usually composed by combinational circuits
  - **ALU (Arithmetic-Logic Unit)**
    It performs all integer computations (arithmetic and logic)
  - **FPU (Floating Poiunt Unit)**
    It performs all floating point computations

- **The Clock**
  All the computers have a timing element (namely clock) generating atemporal reference common for all the elements that are part of theelaborating system.

- **Instruction Timing**
  A machine-cycle is the time interval where the basic operation is executed and it is an integer multiple value of the clock period.
  The execution requires an integer number of machine cycle variable according to the kind of instruction.

3. Memory

- It stores data and instructions that the computer needs to execute.
- Features:
  - Addressing
  - Parallelism
  - Access (sequential or random)

- **Addressing**
  Memory is organized in cells (minimum directly accessible unit).
  An address (number) is assigned to each cell for uniquely identifying it.

- **Parallelism**
  - Each memory cell contains a fixed quantity of bit:
  - Same for all the cells (of a certain memory unit)
  - Accessible with a unique instruction
  - It is a multiple of a byte
  - At least 1 byte (typically a word for the main memory supporting the OU)

- **Internal Memory**
  - Inside the computer
  - Solid state (chip)
  - Usually volatile

- Fast (nanoseconds, 10-9s)
- Limited quantity (some GB)
- Not removable
- Expensive (0.1 € / MB)

- **External Memory**
  - External to the computer
  - Sometime removable
  - Not electronic (e.g., magnetic, optical)
  - Permanent
  - Slow (milliseconds, 10-3 s)
  - Large quantity (some TB)
  - Cheap (0.1 € / GB)

4. Interconnections (BUS)

- Bus features
  - A single data is transported at time
  - frequency = n. data transported at in a second
  - Width = n. di bit composing a single data
  - If not properly dimensioned, it could be a bottleneck

- Bus Types
  - A single bus is composed of the following buses:
    - Data Bus (DBus)
    - Address Bus (ABus)
    - Control Bus (Cbus)