# Design accelerator for system based on NOIS II

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**Nowadays, one of the most commonly used applications in image processing is the use of filters, which are crucial for more detailed image analysis. Among the types of filters frequently applied in image processing are Gaussian filters, minimum filters, maximum filters, high-pass filters, low-pass filters, and band-pass filters. In this report, we focus on an edge detection filter that detects horizontal and vertical edges, which will be examined further.**

### Introduction

The Nios II processor is a 32-bit soft-core processor designed by Altera for FPGA platforms. This processor is highly flexible and can be configured and customized to meet the needs of specific designs, and additional instructions or custom hardware units can be added as needed. In this report, changes have been made to the hardware unit, turning it into an Accelerator, which operates alongside the Nios II processor.

### Exercise Description

In feature extraction, one of the critical steps is edge detection. In classic feature extraction, after noise reduction and image normalization, the two-dimensional gradient of the image is calculated, which reflects the rate of change in the color domain. This method is often implemented using the Sobel filter , which is one of the primary filters used for edge detection. This has been implemented in this report using the VHDL hardware description language, and we will explore the results of this implementation.

### Design of the Master, Slave, and Accelerator

In this step, the Accelerator is connected to the previous system through the Avalon Bus, which allows communication between the Master and Slave modules and the Accelerator. The design of the Accelerator and its integration into the system is shown in Figure 1.

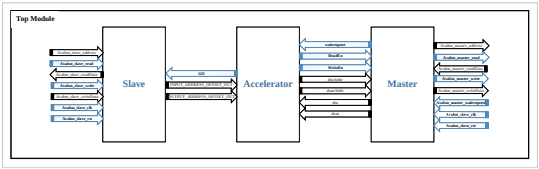


**Figure 1:** *Figure 1*

### System Design in Qsys

After designing the accelerator in VHDL, it is necessary to transfer this module into the Qsys environment for integration with the system. In Qsys, it is important to ensure that signals are properly configured as either Signed or Unsigned, depending on their use. Small adjustments are required to ensure proper synthesis of the designed system.

### Building the System

The system must be built and tested using the Nios II Software Build Tools for Eclipse. In this step, we generate the BSP (Board Support Package) and write a program to interact with the accelerator. This program reads image data from memory, sends it to the accelerator for processing, and retrieves the processed data.

### Conclusion

The designed accelerator was successfully integrated into the system and was able to process image data using the edge detection filter. The results from the testbench demonstrate that the system operates as expected, with the processed image data correctly written back to memory after filtering. Further improvements could include optimizing the accelerator for speed and adding additional filters.

## References

[Alipour Fraydani, 2024] Alipour Fraydani, A. (2024). Homework on Methodology and automatic design algorithms of digital systems, University of Tehran. *Unpublished Manuscript*, Department of Electrical Engineering, University of Tehran.