HOMEWORK #3
MLP Implementation By VHDL

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In this homework we try to implemented MLP by VHDL. in this project we design Datapath and Controller for every Neuron.

VHDL, Datapath, Controller, State Diagram

I. INTRODUCTION

In this homework first we want describe Dathapath and Controller of Single Neuron in next step connected them to hidden layer, in output compare them and identify classes of iris (Setosa, Versicolor, Virginica).

II. DATAPATH AND CONTROLLER

A. *Datapath*

Figure 2.1 show datapath of single neuron

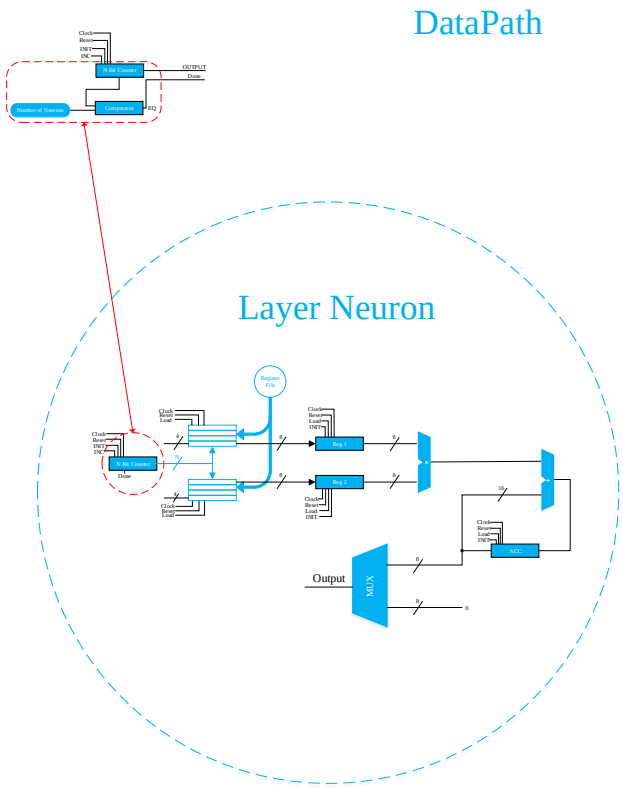

Figure II:I

Datapath has two register file for store inputs and weights, next one we have two register that we called Partial register that every data that need to process goes there next one data multiply and add with bias, first one bias initial in Accumulator and after than that add with before data. Output multiplexer describe ReLu function.

B. *Controller*

In this level describe a Controller Figure 2.2 shown the controller of single neuron.

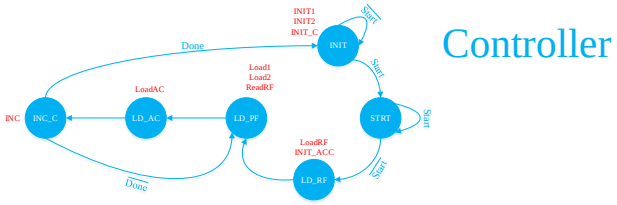

Figure II:II

Controller start with Start signal, this signal have to on and off for start control, next state load data to register files and Accumulator initial with bias data first one, after than load data to Partial registers and load to Accumulator after than, increment counter if neuron doing itself duty controller issued Done, else load new value to partial register.

Counter provide address for register files, architeture of it shown in Figure 3.1

```
OUTPUT   <= MyFile(to_integer(AddRead)) WHEN (ReadEn = '1') ELSE (others=>'Z');

process(Clock, Reset)
begin
   if (Reset = '1') then
      MyFile <= (others=>(others=>'0'));
   elsif (Clock = '1' AND Clock'event) then
      if (Load = '1') then
         MyFile(0)   <= INPUT_0;
         MyFile(1)   <= INPUT_1;
         MyFile(2)   <= INPUT_2;
         MyFile(3)   <= INPUT_3;
         MyFile(4)   <= INPUT_4;
         MyFile(5)   <= INPUT_5;
         MyFile(6)   <= INPUT_6;
         MyFile(7)   <= INPUT_7;
         MyFile(8)   <= INPUT_8;
         MyFile(9)   <= INPUT_9;
      end if;
   end if;
end process;
```

Figure II:III

Figure 3.2 show Address counter that addressed register files.

```
OUTPUT   <= MyFile(to_integer(AddRead)) WHEN (ReadEn = '1') ELSE (others=>'Z');

process(Clock, Reset)
begin
   if (Reset = '1') then
      MyFile <= (others=>(others=>'0'));
   elsif (Clock = '1' AND Clock'event) then
      if (Load = '1') then
         MyFile(0)   <= INPUT_0;
         MyFile(1)   <= INPUT_1;
         MyFile(2)   <= INPUT_2;
         MyFile(3)   <= INPUT_3;
         MyFile(4)   <= INPUT_4;
         MyFile(5)   <= INPUT_5;
         MyFile(6)   <= INPUT_6;
         MyFile(7)   <= INPUT_7;
         MyFile(8)   <= INPUT_8;
         MyFile(9)   <= INPUT_9;
      end if;
   end if;
end process;
```

Figure II:IV

Partial registers shown in Figure 3.2 this registers stored values for process.

```
OUTPUT   <= OUTPUT_Inst;

process(Clock, Reset)
begin
   if (Reset = '1') then
      OUTPUT_Inst <= (others=>'0');
   elsif (Clock = '1' AND Clock'event) then
      if (Load = '1') then
         OUTPUT_Inst <= INPUT;
      end if;
      if (INIT = '1') then
         OUTPUT_Inst <= (others=>'0');
      end if;
   end if;
end process;
```

Figure II:III

Figure 3.4 shown datapath that synthesizer arrived that our describe from VHDL.

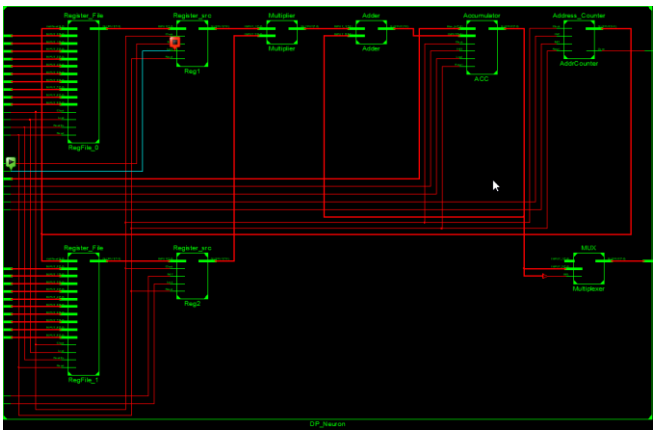

Figure II:IV

Figure II:V

III. RESULTS

Examples shows in Figure 3.1, 3.2, 3.3, 3.4 .

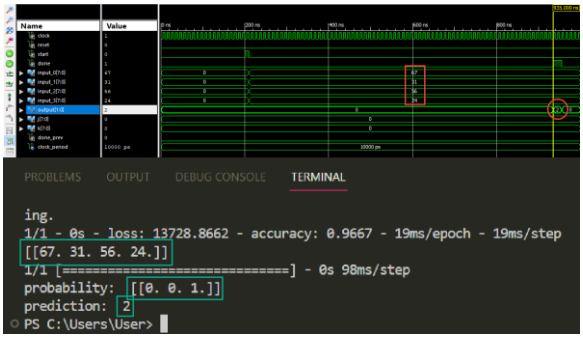

Figure III:I

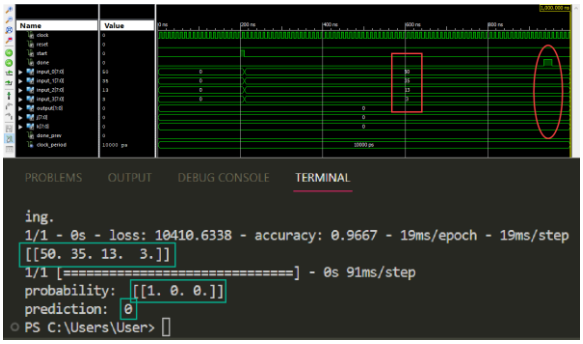

Figure III:II

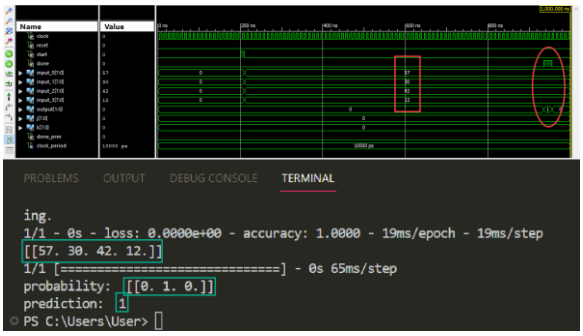

Figure III:III

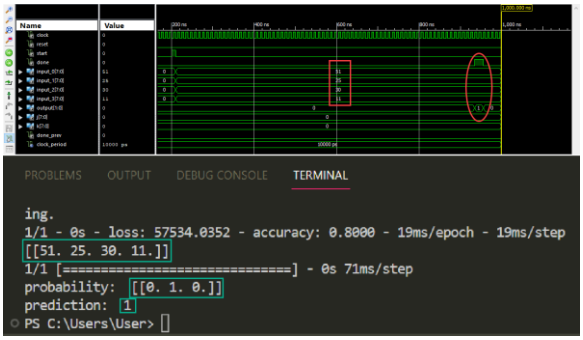

Figure III:IV

Resolution of this algorithm shown in Figure 3.5.

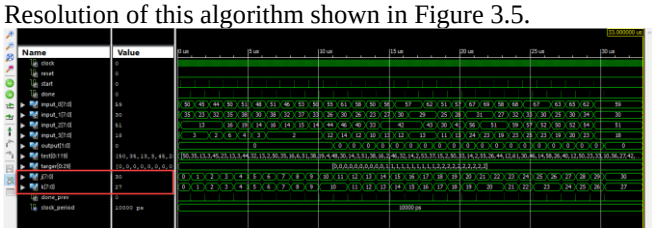

Figure III:V

As you can see resolution is 0.9 (27/30) that this resolution for test data received.

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