A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference

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***Abstract*—A voltage reference circuit operating with all transistors biased in weak inversion, providing a mean reference voltage of 257.5 mV, has been fabricated in 0.18 μm CMOS technology. The reference voltage can be approximated by the difference of transistor threshold voltages at room temperature. Accurate subthreshold design allows the circuit to work at room temperature with supply voltages down to 0.45 V and an average current consumption of 5.8 nA. Measurements performed over a set of 40 samples showed an average temperature coefficient of 165 ppm/°C with a standard deviation of 100 ppm/°C, in a temperature range from 0 to 125 °C. The mean line sensitivity is $\approx$0.44%/V, for supply voltages ranging from 0.45 to 1.8 V. The power supply rejection ratio measured at 30 Hz and simulated at 10 MHz is lower than -40 dB and -12 dB, respectively. The active area of the circuit is $\approx$0.043 mm^2.**

***Index Terms*—Voltage reference, subthreshold circuit, ultra-low power, temperature compensation, CMOS analog design.**

I. Introduction

SUBTHRESHOLD circuits are becoming increasingly popular in low-power low-voltage design. Thanks to the power savings offered, they are particularly attractive in portable scenarios, such as wearable medical devices [1] or passive RFIDs, where energy optimization is of the utmost importance. Moreover, self-powered energy-harvesting systems [2], used to provide power for applications like wireless microsensors and biomedical implants, also employ subthreshold operation to reduce energy consumption. Those power requirements are mostly met by means of supply voltage reduction allowed by subthreshold operation. However, devices biased in subthreshold are much more sensitive to temperature variations and to process variability, in particular to threshold voltage dispersion. This is therefore a challenge for the designer to devise and employ circuit compensation techniques.

Manuscript received April 29, 2010; revised October 25, 2010; accepted October 27, 2010. Date of publication December 20, 2010; date of current version January 28, 2011. This paper was approved by Associate Editor Lucien Breems. This work was supported in part by the Consiglio Regionale della Calabria under the project *Programma di stages per i migliori giovani laureati della Calabria:* L.R. n. 08/2007, art. 3 L.R. n. 26/2004.

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Digital Object Identifier 10.1109/JSSC.2010.2092997

Voltage references are broadly used in analog and digital systems to generate a DC voltage independent of Process, supply Voltage and Temperature (PVT) variations. The most common solution for on-chip integration is the Bandgap Voltage Reference (BGR), which can be implemented in standard CMOS technology exploiting parasitic vertical BJTs. Conventional BGRs generate a nearly temperature independent reference, of about 1.25 V, and therefore they require a higher supply voltage, which might not meet the low-voltage constraints for low-power applications. However, several solutions, exploiting the BGR principle, have been implemented that ensure sub-1V operation [3]. In [4]–[6] the reference voltage is lowered by means of resistive subdivision. As an alternative approach, floating gate structures have been used to realize high precision programmable voltage references, as in the case of [7], where subthreshold operation allowed a minimum power consumption of 1.35 μW. Most often forward biased PN-junctions of BGRs are substituted with MOSFETs biased in the subthreshold region [8]–[10]. Thus, a supply voltage $(V_{\rm DD})$ of 0.6 V and a power consumption of 9 μW are achieved. Other solutions have been implemented in standard CMOS technology, without exploiting the traditional BGR principle [11]–[15]. Subthreshold operation allowed sub-1 μW power consumption [12]–[15] and sub-1V operation [14], [15].

In this work, subthreshold operation is exploited to minimize both the power consumption and the supply voltage. A new CMOS voltage reference configuration, based on a temperature compensation technique derived from the subthreshold regime of operation, is described. Within the circuit, n-channel MOSFETs with two different threshold voltages are present and the reference voltage value can be approximated, in last analysis, to the difference of those two threshold voltages at room temperature. Measurements on silicon confirm that the proposed configuration allows minimum power consumption about one order of magnitude lower than the best solutions found in the literature. Among the compared circuits, the proposed configuration is characterized by the lowest supply voltage.

This paper is organized as follows: in Sections II and III the principle of operation of the proposed voltage reference and the circuit configuration realized are described in detail; dynamic range and power consumption considerations are discussed in Section IV; in Section V measurement results are shown and compared with low-power low-voltage competitors.

II. Operating Principle

A voltage reference can be simply represented by a current source and a diode connected NMOS, as shown in Fig. 1. Such a structure has been adopted in [14], where the load nMOS works

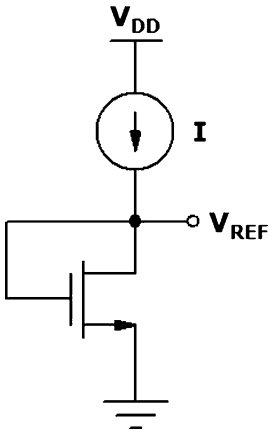

Fig. 1. Scheme of principle of a simple voltage reference.

in the saturation region providing a temperature compensated reference voltage ($V_{\rm REF}$) higher than its threshold voltage ($V_{\rm th}$) at room temperature.

In this work we exploited the subthreshold operation of the load transistor, in order to obtain $V_{\rm REF} < V_{\rm th}$ and, consequently, to further reduce the supply voltage of the overall voltage reference circuit. It is worth noting that biasing the load nMOS in subthreshold region in [14] would not allow temperature compensation, consequently even the current source solution adopted in this work is different from the one used in [14].

Investigating the subthreshold behaviour of the load, a formula for the injected current, compensating the reference voltage dependence on temperature, can be obtained. The $I-V$ characteristics of an nMOS operating in subthreshold region is given by

$$I_D = S\mu V_T^2 \exp\left(\frac{V_{\rm GS}-V_{\rm th}}{mV_T}\right)\left[1-\exp\left(-\frac{V_{\rm DS}}{V_T}\right)\right] \quad (1)$$

where $S = (W/L)C_{\rm OX}$ (W/L is the transistor aspect ratio and $C_{\rm OX}$ is the gate oxide capacitance per unit area), μ is the electron mobility, $V_T = k_B\,T/q$ is the thermal voltage (k_B is the Boltzmann constant, q the elementary charge and T the absolute temperature), $V_{\rm th}$ is the MOSFET threshold voltage, m the subthreshold slope parameter, $V_{\rm GS}$ and $V_{\rm DS}$ are the gate-to-source and the drain-to-source voltages, respectively. From (1), for $V_{\rm DS} \geq 4V_T$, I_D becomes almost independent of $V_{\rm DS}$, thus $V_{\rm REF}$ can be approximated by

$$V_{\rm REF} = V_{\rm GS} = V_{\rm th} + mV_T \ln\left(\frac{I_D}{S\mu V_T^2}\right). \quad (2)$$

Let us note that, at a first approximation, $V_T(T), V_{\rm th}(T)$ and $\mu(T)$ introduce dependence on temperature. As shown in (3), it is usually assumed that $V_{\rm th}$ decreases linearly with temperature [16]:

$$V_{\rm th} = V_{\rm th}(T_0) + (k_{t1} + k_{t2}V_{\rm BS})(T/T_0 - 1) \quad (3)$$

where $V_{\rm th}(T_0)$ is the threshold voltage at the reference temperature ($T_0 \cong 300.15°{\rm K}$), $V_{\rm BS}$ is the body-to-source voltage of the transistor. Temperature coefficients k_{t1} and k_{t2} have negative values.

In order to have a temperature compensated output reference voltage, the following condition must be satisfied:

$$\frac{\partial V_{\rm REF}}{\partial T} = 0. \quad (4)$$

Based on (2), a simple solution of (4) can be obtained by generating the current I_D with the following temperature dependence:

$$I_D(T) = \alpha\mu T^2 \quad (5)$$

Therefore, imposing (4) a value for a (constant with temperature) can be found. Substituting it in (2) and remembering that $V_{\rm BS} = 0$ V in the scheme of Fig. 1, the reference voltage becomes

$$V_{\rm REF} = V_{\rm th}(T_0) + |k_{t1}|. \quad (6)$$

However, the above solution does not ensure subthreshold operation for the active load.

For this reason, more detailed analysis has to be done, considering for the current source the more general form $I(T) = \alpha\mu T^2 f(T)$. Substituting it in (2), the condition (4) becomes a differential equation in $f(T)$:

$$\frac{\partial V_{\rm REF}}{\partial T} = \frac{k_{t1}}{T_0} + m\frac{k_B}{q}\ln\left(\frac{\alpha}{S\,(k_B/q)^2}\right) + m\frac{k_B}{q}\left\{\ln\left(f\left(T\right)\right) + \frac{T}{f\left(T\right)}\frac{\partial}{\partial T}\left(f\left(T\right)\right)\right\} = 0. \quad (7)$$

In order to achieve temperature compensation the term in curly brackets in (7) should be constant with temperature. A possible solution for $f(T)$ could be simply a constant, but this would lead to the case found in (5). Another solution, which can ensure subthreshold operation, can be written as

$$I_D(T) = \alpha\mu T^2 \exp\left(\frac{AT+B}{CT}\right) \quad (8)$$

where A, B and C are constant with temperature. This solution has been chosen since it was easy to generate with a subthreshold MOSFETs based current reference, as will be clear in the next section. It is worth noting that the current reference used in [14] does not allow implementing (8), therefore, in that case, it is not possible to compensate temperature effects by biasing the load in subthreshold regime. Substituting (8) in (2), from (4) an expression for a can be found which leads to the temperature-compensated reference voltage

$$V_{\rm REF\_OPT} = V_{\rm th}(T_0) + |k_{t1}| + m\frac{k_B}{q}\frac{B}{C}. \quad (9)$$

In this case, if the term B/C is negative, differently from (6), the load transistor can work in subthreshold region. In the next section we will show how to implement a circuit configuration like the one in Fig. 1, based on the proposed operating principle.

III. Electrical Configuration

The architecture of the proposed voltage reference is illustrated in Fig. 2. The self-biased current source has no resistors and works with all MOSFETs in the subthreshold region. It generates the current to be injected in the load transistor ($\rm M_{10}$)

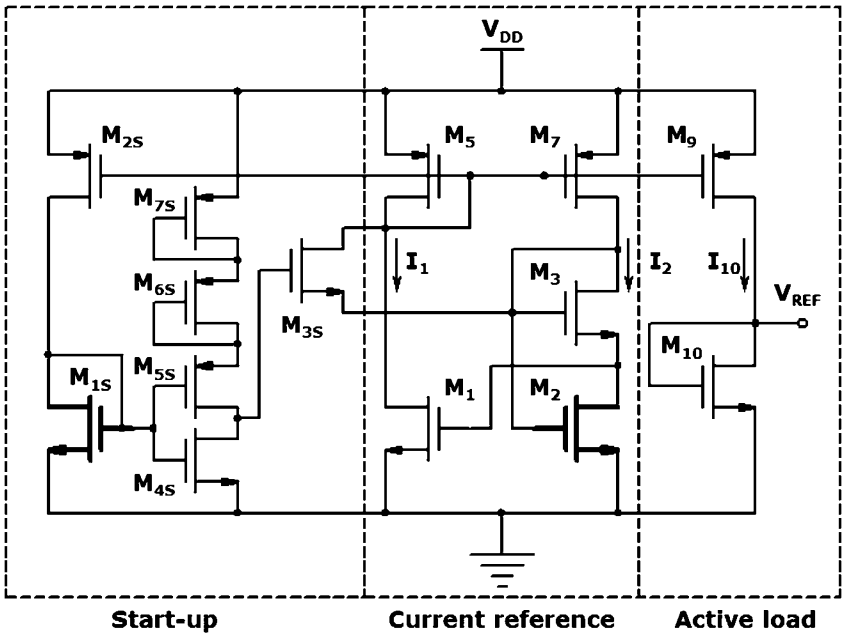

Fig. 2. Proposed CMOS voltage reference circuit.

TABLE I
PROCESS PARAMETERS

Technology	UMC 0.18-μm CMOS process.		
	Voltage range	**V_{th}-NMOS**	**V_{th}-PMOS**
SVT-MOSFET	0 V ≤V_{GS}, V_{DS}, $\|V_{BS}\|$≤ 1.8 V	0.320 V	-0.456 V
HVT-MOSFET	0 V ≤V_{GS}, V_{DS}, $\|V_{BS}\|$≤ 3.3 V	0.600 V	-0.720 V

TABLE II
TRANSISTOR SIZES OF THE CURRENT REFERENCE AND THE ACTIVE LOAD

Transistor	**Value (*W/L*)**
M_1	8 μm / 50 μm
M_2	100 μm / 24 μm = (50 μm / 24 μm) × 2
M_3	2 μm / 2 μm
M_5	68 μm / 50 μm = (17 μm / 50 μm) × 4
M_7	52 μm / 50 μm = (26 μm / 50 μm) × 2
M_9	97 μm / 29 μm = (48.5 μm / 29 μm) × 2
M_{10}	1.5 μm / 50 μm

branch. A start-up circuit has been added as a precautionary measure to ensure bias in the desired state.

Table I summarizes information about the technology chosen to implement the proposed circuit. In particular, the table contains the allowed voltage ranges and the threshold voltage values of both Standard $\mathrm{V_{th}}$ (SVT) and High $\mathrm{V_{th}}$ (HVT) MOSFET models.

Table II shows the size of transistors in the current reference and in the active load.

A. Current Reference

The purpose of the current generator in Fig. 2 is to provide a current, as independent as possible of supply voltage variations, which compensates temperature effects on V_{REF}.

A current in the form (8) can be obtained taking into account a linear combination of nMOS V_{GS} voltages in the subthreshold region. Among the possible solutions for the current reference we chose a self-biased configuration where only three subthreshold operated NMOSs, $\mathrm{M_{1–3}}$, perform such V_{GS} combination, giving

$$V_{\mathrm{GS2}} = V_{\mathrm{GS1}} + V_{\mathrm{GS3}}. \tag{10}$$

In the current reference, PMOSFETs $\mathrm{M_5}$ and $\mathrm{M_7}$ form a subthreshold current mirror providing ratioed currents $I_2/I_1 = (W/L)_7/(W/L)_5 = a$. All the transistors in the proposed solution are SVT-MOSFETs, except for $\mathrm{M_2}$ and $\mathrm{M_{1S}}$, which are HVT-MOSFETs. In order to ensure subthreshold operation for the whole current source, for $\mathrm{M_2}$ a high V_{th} device was chosen. Using (2), (9) becomes

$$m_2 V_T \ln\left(\frac{I_2}{S_2\mu_2 V_T^2}\right) = \Delta V_{\mathrm{th}} + m_3 V_T \ln\left(\frac{I_2}{S_3\mu_3 V_T^2}\right) + m_1 V_T \ln\left(\frac{I_1}{S_1\mu_1 V_T^2}\right) \tag{11}$$

where $\Delta V_{\mathrm{th}} = V_{\mathrm{th1}} + V_{\mathrm{th3}} - V_{\mathrm{th2}}$. Assuming that electron mobilities in (11) are identical ($\mu \approx \mu_1 \approx \mu_2 \approx \mu_3$) and using $I_2 = aI_1$, the current flowing in the left branch of the current generator can be evaluated from (11) as

$$I_1 = Q^{1/\Sigma_m} \mu V_T^2 \exp\left(-\frac{\Delta V_{\mathrm{th}}}{V_T \Sigma_m}\right) \tag{12}$$

where $Q = a^{m_2-m_3}(S_3^{m_3}S_1^{m_1}/S_2^{m_2})$ and $\Sigma_m = m_1 + m_3 - m_2$. Considering the $V_{\rm th}$ thermal behaviour shown in (3), it can be concluded that the subthreshold current reference architecture in Fig. 2 generates a current in the form (8).

The stability of $V_{\rm REF}$ with $V_{\rm DD}$ variations mainly depends on the current generator's insensitivity to supply voltage variations. This characteristic is achieved by means of the self-biased current source architecture, where the high impedance elements per branch ($\rm M_7$ and $\rm M_1$) are capable of absorbing supply voltage variations leaving their current almost unchanged [17].

Significant improvement of the reference voltage line sensitivity and the power supply rejection ratio (PSRR) can be obtained by using an additional current mirror, in the self biased current reference circuit [12]. The use of additional current mirrors in the current generator, which add transistors in stack increasing the minimum achievable $V_{\rm DD}$, were avoided.

B. Active Load

The generated current is then mirrored into a diode connected transistor through $\rm M_9$. The current mirror gain can be expressed as $I_{10}/I_1 = (W/L)_9/(W/L)_5 = c$. Therefore, with $\rm M_{10}$ working in the subthreshold region, the reference voltage becomes, from (2) and (12),

$$V_{\rm REF} = V_{\rm th10} + m_{10}V_T \ln\left\{Q^{1/\Sigma_m}\frac{c}{S_{10}}\right\} - \frac{m_{10}}{\Sigma_m}\Delta V_{\rm th}. \quad (13)$$

The temperature dependence of the reference voltage is firmly related to the thermal behaviour of V_T and $V_{\rm th}$. According to the linear approximation made in (3), setting $\partial V_{\rm REF}/\partial T = 0$, a value of $(W/L)_{10}$ for temperature compensation can be extracted as

$$\left(\frac{W}{L}\right)_{\rm 10OPT} = \frac{Q^{1/\Sigma_m}c/C_{\rm OX10}}{\exp\left\{\frac{q}{k_BT_0}\left[\frac{1}{\Sigma_m}(K + k_{t2,3}V_{\rm BS3}) - \frac{k_{t1,10}}{m_{10}}\right]\right\}} \quad (14)$$

where $K = k_{t1,1} + k_{t1,3} - k_{t1,2}$ ($k_{t1,i}$ and $k_{t2,i}$ are the threshold voltage temperature coefficients of the i-th transistor).

Hence, satisfying (13), $V_{\rm REF}$ becomes

$$\begin{aligned} V_{\rm REF\_OPT} &= V_{\rm th10}(T_0) + |k_{t1,10}| + \frac{m_{10}}{\Sigma_m}(V_{\rm th2}(T_0) + |k_{t1,2}|) \\ &\quad - \left[\frac{m_{10}}{\Sigma_m}(V_{\rm th1}(T_0) + V_{\rm th3}(T_0) \right. \\ &\quad \left. + |k_{t1,1}| + |k_{t1,3}| + |k_{t2,3}|V_{\rm BS3})\right]. \end{aligned} \quad (15)$$

The term indicated in square brackets ensures subthreshold operation of $\rm M_{10}$.

As is clear from (15), the reference voltage value only depends on process parameters. A simpler expression for $V_{\rm REF\_OPT}$ can be obtained considering that, as usual, the m parameters of different NMOSFETs biased in the subthreshold region have similar values (then $m_{10}/\Sigma_m \approx 1$) and $k_{t1,1} \approx k_{t1,2} \approx k_{t1,3} \approx k_{t1,10}$. Therefore, the reference voltage value can be approximated to the threshold voltage difference between an HVT-NMOS ($V_{\rm th2}$) and an SVT-NMOS ($V_{\rm th1}$ or $V_{\rm th3}$). For the technology chosen this difference is enough for the subthreshold operation of $\rm M_{10}$ and, consequently, it is possible to exploit the temperature compensation theory developed in the first section. The mean reference voltage measured is 257.5 mV, about 23 mV lower than the roughly predicted value. This difference is mainly due to the increase of the threshold voltage of $\rm M_3$ caused by both body effect and the effect of lateral pocket implants ($\rm M_3$ has a medium channel length of 2 μm).

The active load aspect ratio, for temperature compensation, predicted by (14), for the chosen technology, neglecting the body effect on $\rm M_3$, is 0.0273, while the one chosen after circuit simulation for temperature coefficient optimization, is $(W/L)_{10} = 1.5\ \mu{\rm m}/50\ \mu{\rm m} = 0.030$. The good agreement confirms the validity of the proposed theoretical approach for subthreshold temperature compensation.

IV. Design Considerations

A. Dimensioning for Minimum Current Consumption

The minimum current consumption is not limited by the operating region of transistors inside the proposed configuration. Thanks to subthreshold operation, all $|V_{\rm GS}|$ values are smaller than the absolute value of MOSFET threshold voltages. Recalling (2), it can be stated that, in principle, there is no lower limit for the current supplied in the subthreshold voltage reference of Fig. 2. Nevertheless, the proposed temperature compensation technique imposes a lower bound for the generated current, as explained in the following.

The total current drawn from the power supply, neglecting the current flowing in the start-up circuit, can be expressed as the sum of the currents injected into the current source and the active load branches:

$$I_{\rm DD} = I_1(1 + a + c) = I_1 B. \quad (16)$$

From (12) and (14), we can rewrite $I_{\rm DD}$ as

$$I_{\rm DD} = \frac{A}{E}\frac{B}{c}\left(\frac{W}{L}\right)_{\rm 10OPT} \quad (17)$$

wherein with A and E we indicate the process and temperature dependent parameters found in (12) and (14), respectively:

$$\begin{aligned} A &= \mu V_T^2 \exp\left(-\frac{\Delta V_{\rm th}}{V_T\Sigma_m}\right) \\ \frac{1}{E} &= C_{\rm OX10}\exp\left\{\frac{q}{k_BT_0}\left[\frac{1}{\Sigma_m}(K + k_{t2,3}V_{\rm BS3}) - \frac{k_{t1,10}}{m_{10}}\right]\right\}. \end{aligned} \quad (18)$$

The remaining terms in (17) only rely on MOSFET aspect ratios. In order to reduce the power consumption, while compensating temperature effects on the reference voltage, the load aspect ratio resulting from (12) should not exceed the minimum derivable for the technology chosen: $W_{\rm MIN}/L_{\rm MAX}$. Moreover, to further reduce $I_{\rm DD}$, the term B has to be minimized (from (16), $B_{\rm MIN} \sim 1$), whereas the current mirror gain c has to be maximized (i.e., $c_{\rm MAX} = (W_{\rm MAX}/L_{\rm MIN})/(W_{\rm MIN}/L_{\rm MAX})$).

B. Minimum Supply Voltage

Considering the voltage reference configuration in Fig. 2, the supply voltage will redistribute as a sum of a $V_{\rm DS}$ and a $V_{\rm GS}$ in the branches of both current reference and active load. Although subthreshold operation does not limit the minimum $V_{\rm GS}$ achievable, in order to generate a current and hence a reference voltage, as independent as possible of $V_{\rm DD}$ variations, the high impedance transistors (i.e., $\rm M_1$, $\rm M_7$ and $\rm M_9$) should absorb at least a $V_{\rm DS} \sim 4V_T$. The maximum working temperature of the proposed circuit is 125°C, therefore, the minimum $V_{\rm DS}$ value able to ensure proper operation, even at that temperature, becomes $4V_T = 137$ mV. Consequently, by generating a current (12) so that, in each branch, $V_{\rm GS} \ll 4V_T$, a minimum supply voltage of $4V_T$ can be achieved with a similar voltage reference architecture regardless of the process technology chosen.

Nevertheless, in our specific case, the gate-to-source voltage of $\rm M_{10}$, obtained for temperature compensation, is process dependent and its value cannot be minimized. So, the minimum $V_{\rm DD}$, ensuring a $|V_{\rm DS}| > 4V_T$ for $\rm M_9$, will be

$$V_{\rm DDMIN} \geq V_{\rm REF\_OPT} + 4V_T. \tag{19}$$

Since the mean reference voltage measured is 257.5 mV, it follows that $V_{\rm DDMIN}$, for the subthreshold circuit configuration in Fig. 2, will be equal or higher than 395 mV, considering the thermal voltage value at the maximum operating temperature. Obviously, the higher $V_{\rm DDMIN}$, the more accurate the approximation done in (2) for $\rm M_9$ and, as a consequence, the smaller the circuit line sensitivity.

From measurements, proper operation was observed with $V_{\rm DD} \geq 450$ mV, which is the smallest obtained so far for voltage reference circuits.

C. Sensitivity to Supply Voltage Variations

A common parameter used for the evaluation of the reference voltage sensitivity to $V_{\rm DD}$ variations is the line sensitivity. It is defined as $\rm LS = (\Delta V_{REF}/\Delta V_{DD})/V_{REF}(\%)$, where $\Delta V_{\rm DD}$ is the $V_{\rm DD}$ range of operation ($1.8\ \rm V - 0.45\ V = 1.35\ V$ for the proposed circuit), $\Delta V_{\rm REF}$ is the absolute variation of the reference voltage, in the $V_{\rm DD}$ range considered, and $V_{\rm REF}$ stands for the mean output value. The line sensitivity optimization starts from the minimization of $\Delta V_{\rm REF}$. From Figs. 1 and 2, it is clear that it can be easily translated in the minimization of I_{10} variations.

Neglecting the effect of the term in square brackets in (1) (i.e., considering a $V_{\rm DS} \geq 4V_T$), we can rewrite the subthreshold drain current, highlighting the $V_{\rm DS}$ dependence:

$$I_D = I_0 \exp\left(\frac{V_{\rm GS}}{mV_T}\right) \exp\left(\frac{\lambda_D V_{\rm DS}}{mV_T}\right) \tag{20}$$

in which I_0 summarizes the product between the aspect ratio and the process and temperature parameters found in (1) and λ_D is the drain-induced barrier lowering (DIBL) factor [18]. Subthreshold operated MOSFETs do not suffer from channel length modulation, therefore, for $V_{\rm DS} \geq 4V_T$, I_D will depend on $V_{\rm DS}$ only because of the DIBL effect. As is well known, the DIBL effect significantly decreases with increasing channel length.

The $\Delta V_{\rm DD}$ will cause a $\Delta V_{\rm DS} = V_{\rm DSMAX} - V_{\rm DSMIN}$ on the high impedance transistor in the branch. Assuming constant $V_{\rm GS}$, the resulting I_D variation will be characterized by a maximum to minimum ratio $I_{\rm DMAX}/I_{\rm DMIN} = \exp(\lambda_D \Delta V_{\rm DS}/mV_T)$. Recalling (2), the $\Delta V_{\rm REF}$ owing to $V_{\rm DD}$ variations can be written as

$$\begin{aligned}\Delta V_{\rm REF} &= m_{10} V_T \ln\left(\frac{I_{\rm DMAX}}{I_{\rm DMIN}}\right) \\ &= \frac{m_{10}}{m^*}\lambda_D \Delta V_{\rm DS} \approx \lambda_D \Delta V_{\rm DS}\end{aligned} \tag{21}$$

where m^* is the subthreshold slope factor of the high impedance transistor.

Therefore, the line sensitivity can be rewritten as

$$\rm LS \approx \frac{\lambda_D}{V_{REF}} \frac{\Delta V_{DS}}{\Delta V_{DD}}\% \approx \frac{\lambda_D}{V_{REF}}\%. \tag{22}$$

As expected, for line sensitivity minimization, the high impedance transistors in the proposed configuration (i.e., $\rm M_1$, $\rm M_7$, $\rm M_9$) should be as long as possible, in order to improve the stability of the generated current and, therefore, the one of $V_{\rm REF}$.

The result found in (22) not only gives a quick evaluation of the expected line sensitivity of the proposed voltage reference configuration, but can also be extended to every voltage reference architecture operated in subthreshold region, where only one high impedance transistor per branch is present. Such architectures are very common in ultra low voltage solutions, where the reduction of transistor stacks helps in lowering the minimum $V_{\rm DD}$ achievable. In [14], where a two-transistor stack per each branch is present, a minimum $V_{\rm DD}$ of 0.9 V was attained.

The DIBL factor was measured for a pMOS of the same channel length as $\rm M_9$, the transistor that absorbs $V_{\rm DD}$ variations in the active load branch, obtaining a λ_D of about 0.001. From (21), therefore, the expected LS is 0.388%/V, only 13% different from the measured mean line sensitivity, due mostly to the subthreshold slope factor difference between pMOS and NMOS, which we assumed equal in (21).

D. Process Variations

The generated voltage (15) is a linear combination of threshold voltages parameters. As usually happens in low-power CMOS integrated voltage [12]–[15], the reference voltage is process dependent. Thus, neglecting matching errors in (14), the accuracy of the output voltage is mainly due to the accuracy of threshold voltages of transistors $\rm M_1$, $\rm M_3$, $\rm M_2$, $\rm M_{10}$. Process variations are generally distinguished in WIthin Die (WID or intra-die) variations and Die to Die (D2D or inter-die) variations [12]. The first type of variations causes mismatch between transistors of the same chip and influences the relative accuracy of transistor parameters. Careful layout techniques [19] and large transistor W/L [20], can help to reduce those effects. D2D variations, instead, influence the absolute accuracy of transistor parameters and their effects are not compensated in the proposed configuration.

Threshold voltage measurements over a set of forty SVT-NMOSs, with a W/L of 12 μm/50 μm, were performed. Each transistor belongs to a different die and is placed within the same

voltage reference dies. The average and the standard deviation values obtained are 318.5 mV and 6.7 mV, respectively. Expressing $V_{\mathrm{REF\_OPT}}$ as the threshold voltage difference between an HVT-NMOS and an SVT-NMOS, the standard deviation of $V_{\mathrm{REF\_OPT}}(\sigma_{\mathrm{VREF}})$ can be approximated with

$$\sigma_{\mathrm{VREF}} = \sqrt{\sigma_{\mathrm{HVT}}^2 + \sigma_{\mathrm{SVT}}^2} \tag{23}$$

where σ_{HVT} and σ_{SVT} are the V_{th} standard deviations of an HVT-NMOS and an SVT-NMOS, respectively. In (23) has been implicitly assumed that the variation processes of the two V_{th} s are independent, i.e., their covariance is zero. Moreover, assuming that $\sigma_{\mathrm{HVT}} = \sigma_{\mathrm{SVT}} = \sigma_{V_{\mathrm{th}}}$, it is easy to evaluate the standard deviation of the voltage reference as

$$\sigma_{\mathrm{VREF}} \approx \sqrt{2}\sigma_{V_{\mathrm{th}}}. \tag{24}$$

The σ_{VREF} obtained from (24) is 9.5 mV, only 0.5 mV lower than the measured one. This testifies that the main contributor to the voltage reference inaccuracies are the nMOS threshold voltage variations.

On the other hand, since the threshold voltage dependence of temperature, $\partial V_{\mathrm{th}}/\partial T$ has small dependence on process variations, as demonstrated in [12], even the temperature coefficient of the reference voltage will benefit from a similar behaviour with process variations.

V. Measurement Results

A set of 40 prototype chips, from three separate runs, were successfully implemented in UMC 0.18-μm, 1.8 V/3.3 V, CMOS process. The circuit photo and the corresponding layout are shown in Fig. 3(a) and (b), respectively. The occupied chip area is only $\approx$0.0430 mm^2, thanks mainly to the reduced number of transistors in the core of the circuit (current reference and active load subsections).

Wafer-level DC measurements have been performed using a Cascade SUMMIT 11861B prober equipped with a Temptronic chuck temperature controller and a Keithley 4200-SCS semiconductor parameter analyzer.

In this section, measurement results of a chip with typical behaviour are discussed and compared with best performing low-power low-voltage solutions found in the literature, subsequently a statistical analysis of the performance, regarding the 40 samples fabricated, is presented. As a typical performance chip, the one with the median temperature coefficient (TC) was chosen, since it is, commonly, the most critical figure of merit for voltage reference circuits. However, as will be clear from statistical analysis, those typical results are very close to the average ones.

In Fig. 4, the $V_{\mathrm{REF}} - V_{\mathrm{DD}}$ characteristic at room temperature is reported. The circuit starts working properly with $V_{\mathrm{DD}} = 0.45$ V. In the supply voltage range from 0.45 V to 1.8 V a mean reference voltage of 263.5 mV is generated. In this supply voltage range, the output voltage changes at most by 1.6 mV, thus leading to a line sensitivity of 0.440%/V.

The current consumption changes slightly with V_{DD}, at room temperature it varies from 7.0 nA to 7.9 nA in the supply voltage range under consideration. Therefore, under the above-mentioned operating conditions, the minimum power

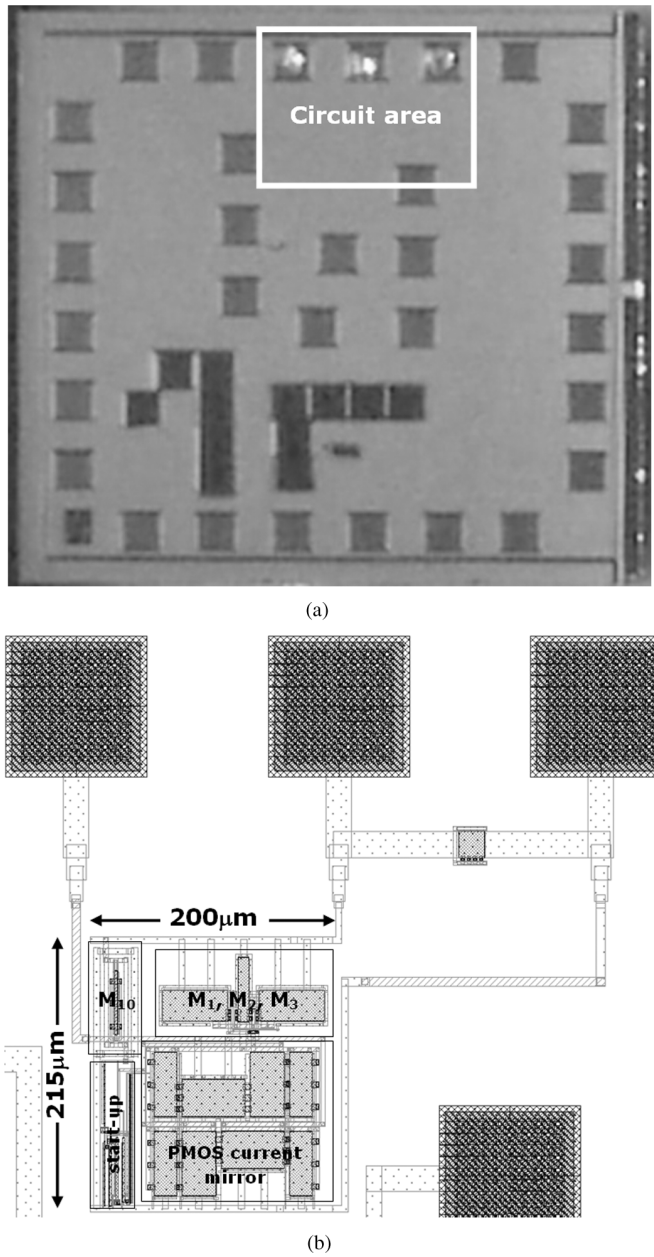

Fig. 3. (a) Chip photo. (b) Layout of the proposed CMOS voltage reference circuit.

consumption is just 3.2 nW. In Fig. 5(a) the measured values of the current drawn from the power supply, in the temperature range between 0°C and 125°C, are shown. The supply current increases with temperature according to (12), reaching 36.0 nA at $V_{\mathrm{DD}} = 0.45$ V@125°C, and 40.8 nA at $V_{\mathrm{DD}} = 1.8$ V @125°C.

The reference voltage dependence on temperature is shown in Fig. 5(b). Averaging the V_{REF} variation on the V_{DD} range considered, it results $\approx$4.7 mV, leading to an average TC of 142 ppm/°C. From Fig. 5(b), it is clear that the TC is quite independent of V_{DD}.

The measured and simulated PSRR values at room temperature, at minimum supply voltage, are illustrated in Fig. 6. Because of the very high value of the output impedance of the circuit, PSRR measurements have been performed by connecting

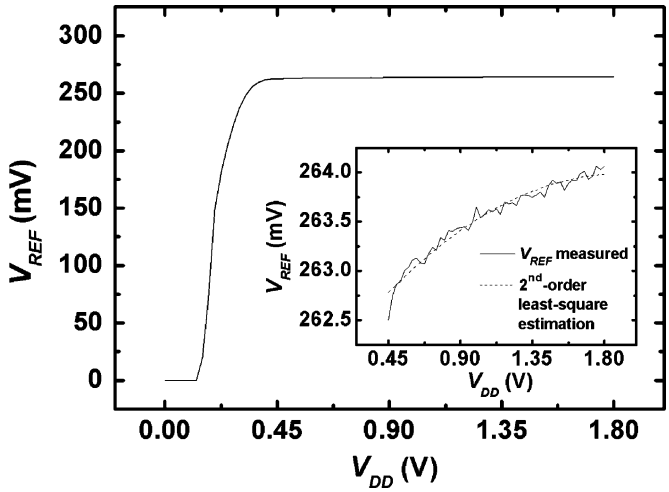

Fig. 4. Measured output voltage as a function of power supply at room temperature and zoom in the $V_{\rm DD}$ operating range.

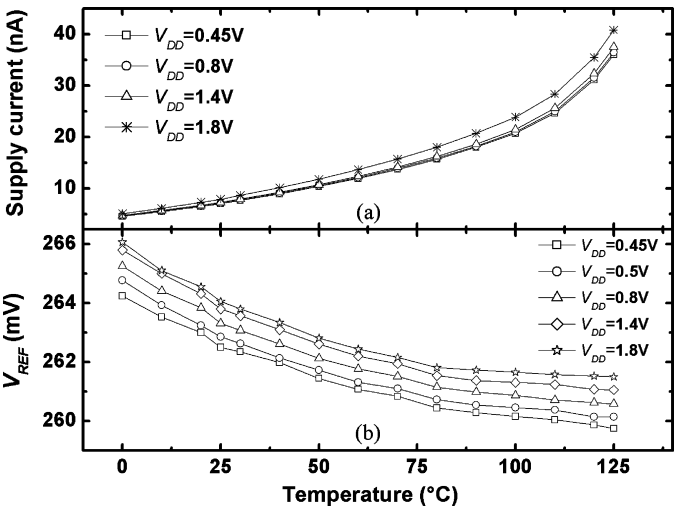

Fig. 5. (a) Supply current versus temperature for different supply voltages. (b) Temperature dependence of the generated reference voltage for different supply voltages.

the voltage reference output to a CMOS operational amplifier (TLC2201). Indeed, from post-layout simulations, the evaluated output impedance $(Z_{\rm OUT})$ is 55 $\rm M\Omega//0.3$ pF, higher than typical input impedance of commercial oscilloscope probes. The opamp input capacitance $(C_{\rm IN})$ is about 20 pF (considering packaged amplifiers, generally, $C_{\rm IN}$ does not go below 10 pF) and forms a low-pass filter with $Z_{\rm OUT}$ having a -3 dB frequency of 144 Hz. For this reason, the high output impedance of the circuit did not allow an accurate measurement of the PSRR for frequencies above 30 Hz. However, from Fig. 6, it is clear that the simulation results are in good agreement with the measurements obtained.

The measured equivalent output noise amplitude, without filtering capacitors, is shown in Fig. 7. At 10 Hz its value is 2.3 $\mu\rm V/\sqrt{Hz}$ and the root mean square voltage noise, measured in a bandwidth from 0.1 Hz to 10 Hz, is 22.0 μV.

It is clear that the designed circuit can only drive high impedance loads such as the capacitive loads offered by

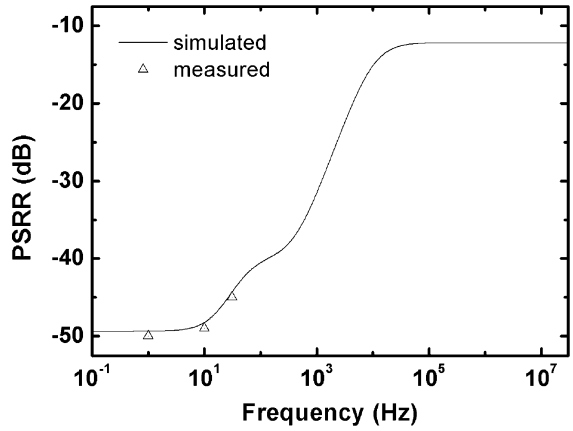

Fig. 6. PSRR at room temperature, for $V_{\rm DD} = 0.45$ V.

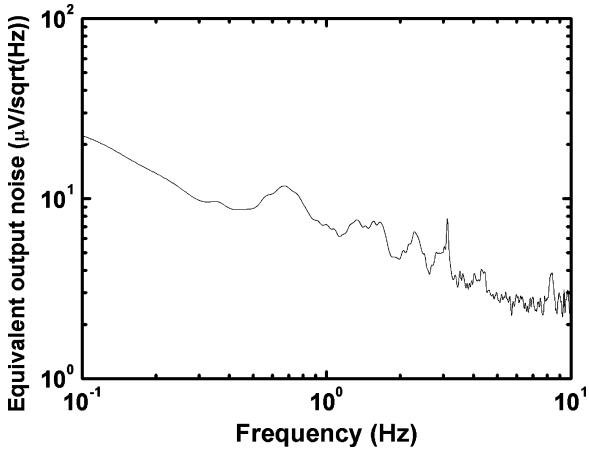

Fig. 7. Measured equivalent output noise $(\rm V/\sqrt{Hz})$ from 0.1 Hz to 10 Hz.

MOSFET-based comparators or buffers. Most often voltage references do not drive directly loads, as in the case of voltage supply circuits [21].

Table III summarizes the measurement results of the typical performance chip and compares them with the best low voltage, low power voltage references found in literature, implemented in standard CMOS process. From the comparison it results that the proposed configuration achieves the lowest supply voltage and current dissipation, thus leading to at least a $10\times$ reduction in power consumption with respect to the other proposed solutions. Moreover, those results are obtained while preserving competitive line sensitivity, temperature coefficient, PSRR and area occupation.

Measurements were carried out on a set of 40 samples. In Table IV, a brief summary of the statistical analysis results, reporting most relevant figures of merit, is given. In particular mean (μ) and standard deviation (σ) values of the temperature coefficient $(\rm TC_{AVG})$, the line sensitivity (LS), the power consumption at $V_{\rm DD} = 0.45$ V $(P_{\rm DISS})$ and the reference voltage $(V_{\rm REF})$ at room temperature were reported. $\rm TC_{AVG}$ and $V_{\rm REF}$ refer to the averaged values on the $V_{\rm DD}$ range considered. In Fig. 8 the distributions of these parameters are shown. To our knowledge, detailed statistical information about key performance indicators like TC, LS or power consumption, are not given in works concerning low power voltage references. For

TABLE III
COMPARISON WITH LOW-VOLTAGE LOW-POWER CMOS VOLTAGE REFERENCES

	Proposed configuration	*Ref. [14]*	*Ref. [15]*	*Ref. [8]*	*Ref. [12]*	*Ref. [13]*	*Ref. [11]*
Technology	0.18μm CMOS	0.35μm CMOS	0.18μm CMOS	0.18μm CMOS	0.35μm CMOS	0.35μm CMOS	0.6μm CMOS
Supply voltage (V)	**0.45 to 2**	**0.9 to 4**	**0.6 to 2.3**	**0.85 to 2.5**	**1.4 to 3**	**1.1 to 4**	**1.4 to 3**
Supply current (μA) @ room temperature	**0.007@0.45V 0.008@1.8V**	**0.040@0.9V 0.055@4V**	**<0.040@0.7V** –	**3.882@0.85V average**	**0.2143@1.4 -**	**~0.021@1.1V ~0.024@4V**	**<9.7**
V_{REF} (mV)	263.5	670	~220	221	745±25	96.6±4.0 vers-1 108.9±3.1 vers-2	309.3±19.26
TC (ppm/°C)	142	10	127	194	7	11.4 – [-20:80] , vers-1	36.9
T range(°C)	[0:125]	[0:80]	[-20:100]	[-20:120]	[-20:80]	9.2 – [-20:80] , vers-2	[0:100]
Line Sensitivity (%/V)	0.440	0.270	~2.730	0.905	0.002	0.090 , vers-1 0.170 , vers-2	0.083
PSRR (dB)	V_{DD}=0.45V	V_{DD}=0.9V	-	-	V_{DD}=2V	V_{DD}=3V	V_{DD}=1.4V
Low freq [≤100Hz]	-45.0	-47	-41	-	-45	<-60	-47
High freq [≥10MHz]	(-12.2 sim.)	-40	-	-	~ -22@10kHz	<-40	-20
Die area (mm^2)	0.0430	0.0450	0.0040	0.0238	0.0550	0.0189 , vers-1 0.0193 , vers-2	0.0550

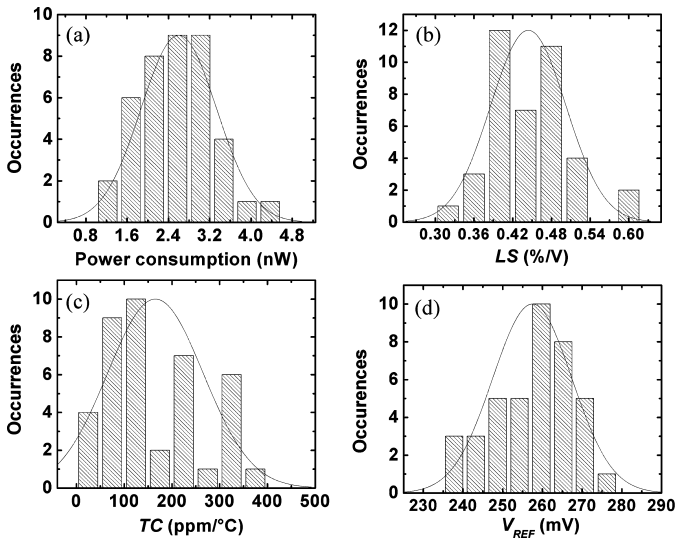

Fig. 8. Distributions of the most relevant figures of merit for the 40 measured samples: (a) Power consumption @25°C and $V_{\rm DD} = 0.45$ V. (b) Line sensitivity @25°C. (c) Temperature coefficient. (d) Generated voltage reference @25°C.

TABLE IV
STATISTICAL ANALYSIS OF PERFORMANCE

Number of samples	40 from three separate runs	
	μ	σ
TC_{AVG} (ppm/°C)	165	100
LS (%/V) @ 25°C	0.444	0.058
P_{diss} (nW) @ 0.45V & 25°C	2.6	0.7
V_{REF} (mV) @ 25°C	257.5	10.0

this reason it was not possible to compare the statistical results in detail.

The mean power consumption at the minimum $V_{\rm DD}$ and at room temperature is 2.6 nW and it remains lower than 5 nW in the worst case (see Fig. 8(a)). However, even in that case, the proposed circuit continues to achieve the lowest power consumption, considering that the best low power solutions reported in literature do not go below 23 nW [13].

The line sensitivity distribution, in the $V_{\rm DD}$ range from 0.45 V to 1.8 V, is shown in Fig. 8(b) and the mean value is 0.444%/V. It varies from a minimum value of 0.329%/V to a maximum value of 0.606%/V.

The best $\rm TC_{AVG}$ is 39 ppm/°C, which means an average variation of the output voltage of 1.2 mV in the temperature range from 0°C to 125°C. The worst $\rm TC_{AVG}$ (357 ppm/°C), instead, gives an average variation of about 12 mV. From Fig. 8(c) it is evident that the TC is the quantity with the largest dispersion, indeed, the coefficient of variation σ/μ is $\approx$61%. The temperature coefficient is a very sensitive parameter, in [6] a 4-bit trimming network is used to optimize it, by changing resistor values after fabrication.

Fig. 8(d) shows the distribution of $V_{\rm REF}$ at room temperature. The σ/μ is 3.9%, such spread in reference voltage is higher in the proposed circuit than when using BGRs, e.g., in [22] the σ/μ is around 1.5%. However, the proposed solution exhibits a power consumption and a minimum supply voltage significantly lower compared to bandgap-like circuits.

VI. CONCLUSION

An ultra low voltage, extremely low power voltage reference circuit fabricated in the UMC 0.18-μm CMOS process, is presented. The circuit works with all transistors in subthreshold operation, thus allowing a remarkable reduction of minimum supply voltage and power consumption. In this sense, the proposed solution represents a significant advance in low power low voltage reference circuit design: the power dissipation is only 2.6 nW, which is about one order of magnitude lower than that of the best results found in the literature, and the minimum supply voltage for correct operation falls to 0.45 V. In addition, a temperature compensation technique and a simple model for line sensitivity prediction in subthreshold-operated voltage reference circuits is presented and demonstrated. The extremely low power and low voltage features of the proposed circuit make

it very attractive for ultra low power battery-operated electronic applications.

ACKNOWLEDGMENT

The authors wish to thank S. Pierro and G. Staino for technical support.

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