INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. (2013)
Published online in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.1950

A sub-1 V nanopower temperature-compensated sub-threshold CMOS voltage reference with 0.065%/V line sensitivity

Luca Magnelli[1], Felice Crupi[2,*,†], Pasquale Corsonello[2] and Giuseppe Iannaccone[3]

[1]*Danube Mobile Communications Engineering GmbH & Co KG, Intel Mobile Communications, Freistädter Straße 400, 4040, Linz, Austria*
[2]*Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica, University of Calabria, Via P. Bucci 42C, 87036, Rende, Italy*
[3]*Dipartimento di Ingegneria dell'Informazione, University of Pisa, Via G. Caruso 16, 56122, Pisa, Italy*

ABSTRACT

We present the design of a nanopower sub-threshold CMOS voltage reference and the measurements performed over a set of more than 70 samples fabricated in 0.18 μm CMOS technology. The circuit provides a temperature-compensated reference voltage of 259 mV with an extremely low line sensitivity of only 0.065% at the price of a less effective temperature compensation. The voltage reference properly works with a supply voltage down to 0.6 V and with a power dissipation of only 22.3 nW. Very similar performance has been obtained with and without the inclusion of the start-up circuit. Copyright © 2013 John Wiley & Sons, Ltd.

Received 23 January 2013; Revised 16 July 2013; Accepted 3 August 2013

KEY WORDS: voltage reference; subthreshold CMOS; low voltage; low power

1. INTRODUCTION

Ultra-low-power, low-voltage design requirements are crucial in emerging applications such as portable medical devices, microsensor nodes and passive RFIDs. For such portable systems, power consumption reduction becomes essential to extend the battery lifetime and/or the communication range. This leads to a strong demand for circuit building blocks operating with low supply voltages and low power consumption. Among them, voltage reference circuits are ubiquitous; they are broadly used in analog and digital systems to generate a DC voltage independent of process, supply voltage and temperature variations [1–7]. Recently, we proposed a temperature compensated sub-threshold CMOS voltage reference which operates with a supply voltage down to 0.45 V and with a power dissipation of only 2.6 nW [1]. In this work, we propose an alternative configuration of sub-threshold nanopower CMOS voltage reference by introducing a cascode-like current-mirroring scheme in the current reference in order to remarkably improve the line sensitivity (LS) with a suboptimal temperature compensation.

2. PROPOSED VOLTAGE REFERENCE

The circuit topology of the proposed voltage reference with start-up is shown in Figure 1. As in the case of [1], all transistors are biased in the sub-threshold region.

*Correspondence to: F. Crupi, Dipartimento di Ingegneria Informatica, Modellistica, Elettronica e Sistemistica, University of Calabria, Via P. Bucci 42C, 87036, Rende, Italy.
†E-mail: felice.crupi@unical.it

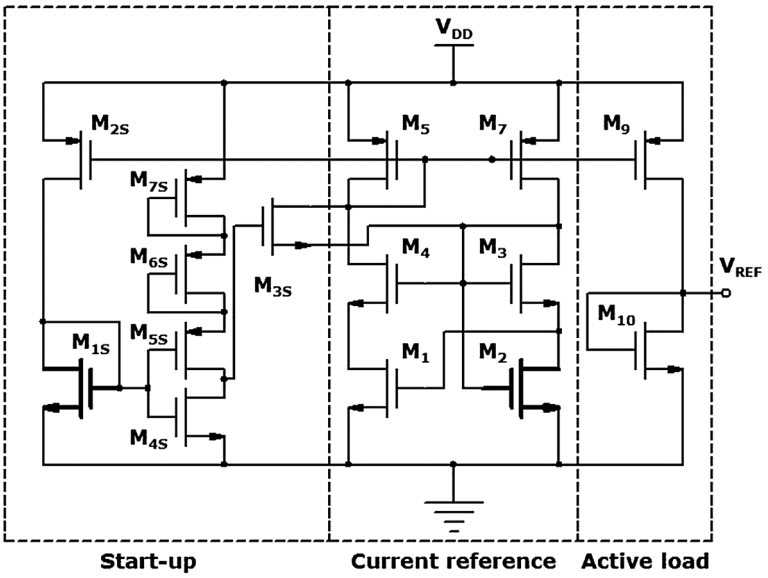

Figure 1. Schematics of the proposed voltage reference.

The current reference section generates the current via M_{1-3}, that – mirrored in the active load (M_{10}) – will compensate the temperature effects on the generated reference voltage, V_{REF}. Within the current reference architecture, V_{GS2} can be expressed as the sum of V_{GS1} and V_{GS3}. Therefore, as explained in [1], the generated current can be expressed as,

$$I_D(T) = \alpha\mu T^2 \exp\left(\frac{AT + B}{CT}\right) \tag{1}$$

where T is the absolute temperature, μ is the electron mobility and A, B and C are independent of temperature. The current generated according to Eq. 1 is injected in the M_{10} thus obtaining a temperature-compensated voltage reference [1]. Indeed, considering that M_2 is a high threshold voltage, NMOS and $M_{1,3,10}$ are standard threshold voltage transistors, the output reference voltage is

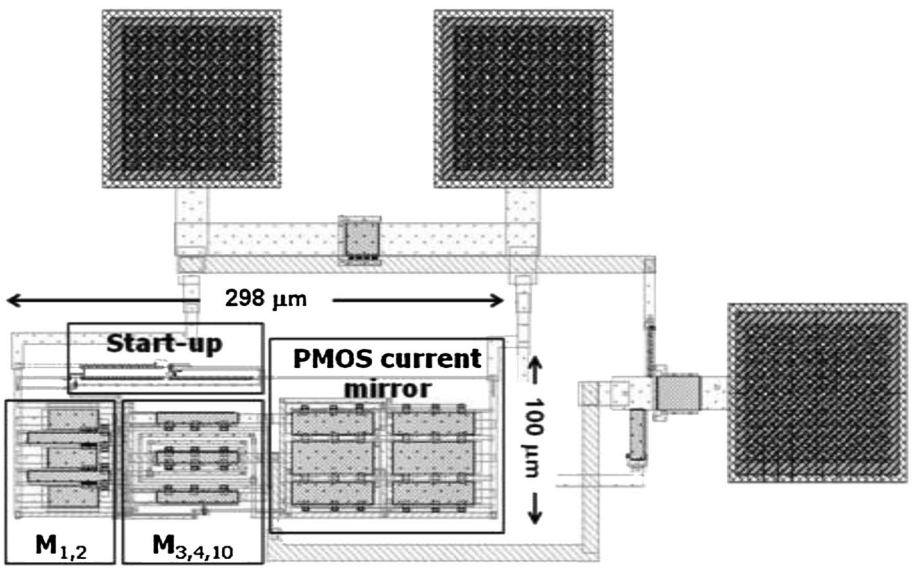

Figure 2. Layout of the proposed voltage reference.

DOI: 10.1002/cta

approximately equal to the difference between the threshold voltages of the high voltage and standard threshold voltage nMOSFETs. A more detailed analysis about the temperature compensation concept can be found in [1], where the mentioned temperature compensation theory is discussed.

In the present circuit, the introduction of a cascode-like current-mirroring scheme in the self-biased current reference is key to improve line sensitivity. In particular, M_4 acts as a cascode device, thus shielding M_1 from V_{DD} variations. In the previous configuration [1], the drain current of M_1 can vary according to V_{DD} variations, because of DIBL effect, while in the present configuration, the I_{D1} variation is significantly reduced thanks to the additional cascode device M_4. Clearly, the reduced sensitivity of the reference current to the power supply variations decreases the overall LS of the voltage reference. This improvement comes at the cost of the additional voltage headroom consumed by M_4.

3. MEASUREMENT RESULTS

The proposed voltage reference with and without the start-up section has been fabricated in UMC 0.18 μm CMOS process. The circuit layout with start-up circuit is shown in Figure 2. The occupied chip

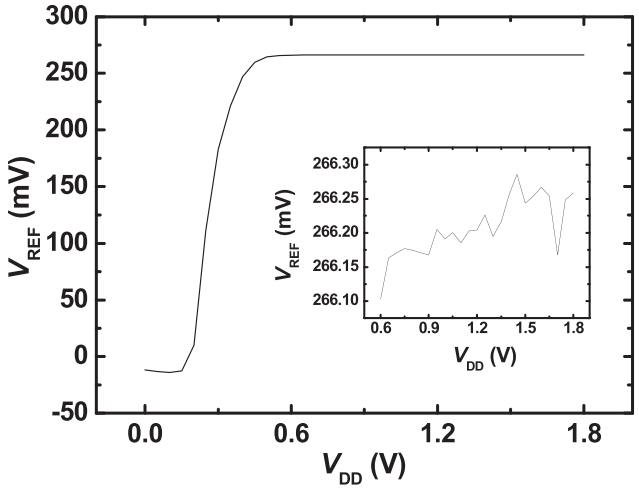

Figure 3. Measured output voltage as a function of power supply at room temperature and zoom in the V_{DD} operating range.

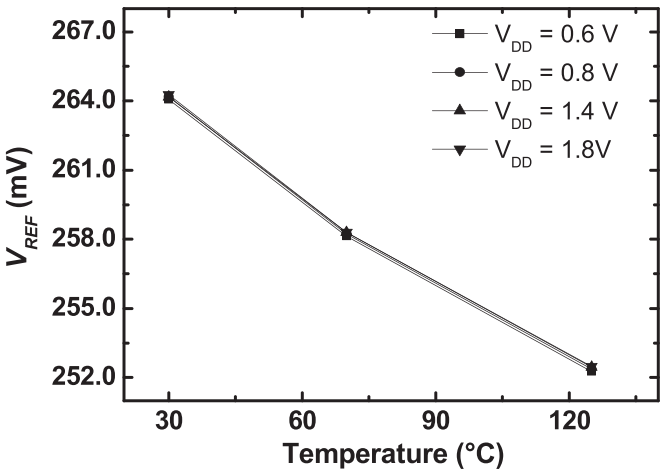

Figure 4. Measured reference voltage as a function of temperature for several voltage supply levels.

DOI: 10.1002/cta

Table I. Comparison with low-voltage nanopower CMOS voltage references.

	This work	[1]	[2], version 1	[3]	[4]	[5]	[6] Simulations	[7]
Technology	0.18 µm	0.18 µm	0.35 µm	0.35 µm	0.18 µm	0.18 µm	0.18 µm	0.35 µm
V_{DD} *(V)*	0.7	0.45 to 2	1.1 to 4	0.9 to 4	0.6 to 2.3	1 to 2.5	0.85 to -	1.4 to 3
I_{supply} *(nA)*	37@0.6 V	7@0.45 V	~21@1.1 V	40@0.9 V	<40@0.7 V	46@1 V	6@0.85 V	214@1.4 V
	37@1.8 V	8@1.8 V	~24@4 V	55@4 V	–	–	–	–
V_{REF} *(mV)*	259.0	263.5	96.6±4.0	670	~220	548	650	745±25
TC (ppm/°C)	462 [0:125]	142 [0:125]	11.4 [−20:80]	10 [0:80]	127 [−20:100]	30 [−30:150]	37 [−10:160]	7 [−20:80]
T range(°C)								
LS (%/V)	0.065	0.440	0.090	0.270	~2.730	–	0.31	0.002
PSRR (dB)	V_{DD}=0.6 V	V_{DD}=0.45 V	V_{DD}=3 V	V_{DD}=0.9 V	–	V_{DD}=1 V	–	V_{DD}=2 V
Low freq [≤100Hz]	(−44.0 sim.)	−45.0	<−60	−47	−41	−54@100Hz	−65	−45
High freq [≥10MHz]	(−40.3 sim.)	(−12.2 sim.)	<−40	−40	–	–	–	~ −22@10kHz
Area (mm^2)	0.0298	0.0430	0.0189	0.0450	0.0040	0.0036	–	0.0550

DOI: 10.1002/cta

Table II. Statistical analysis of the proposed voltage reference with and without the start-up circuit.

Configuration	*With start-up*		*Without start-up*	
Number of samples	37		35	
	μ	σ	μ	σ
TC_{AVG} *(ppm/°C)*	462	134	463	141
LS (%/V) @ 25°C	0.065	0.041	0.070	0.047
P_{diss} *(nW) @ 0.25°C*	22.3	5.4	21.9	5.3
V_{REF} *(mV) @ 25°C*	259	9.8	258.3	9.8

area is 0.0298 mm^2. As shown in Figure 3 for a typical sample, in the V_{DD} range [0.6;1.8] V, V_{REF} varies just a few tenths of millivolts, thus leading to an LS of 0.065%/V. Notwithstanding, adding a transistor in the stack of the left branch of the current reference increases the V_{DDmin} from 0.45 V to 0.6 V. The temperature coefficient (TC) of the proposed configuration is 462 ppm/°C, around three times higher than in the case of [1]. In Figure 4, the V_{REF} dependency on temperature for a typical sample is shown. In order to understand the temperature behavior, process corner simulations of the post layout circuit configuration were performed before fabrication. Nevertheless, they showed a worst case TC of only 32 ppm/°C. A possible reason for the observed difference may be the inaccuracy of the employed BSIM3v3.2 models in capturing the temperature behavior in the sub-threshold region. A comparison with the best previous sub-1-μW CMOS voltage references is reported in Table I. The comparison with [1–6] indicates that the proposed voltage reference achieves the lowest LS (in [6] no LS measurements are mentioned). In terms of power dissipation, it only consumes more than [1] and the simulated circuit in [6]. From a comparison with our previous configuration [1], it follows that the introduction of the cascode transistor in the current reference architecture was successful in terms of LS; it has been improved by a factor 10× with the new solution.

Among sub-1-μW voltage references, [7] exhibits a LS lower than the proposed solution, but at the cost of a higher V_{DDmin} and a power consumption overhead of more than one order of magnitude. Table II summarizes the measurement results, providing mean and standard deviation values of the most relevant figures of merit with and without the start-up circuit. Similar performance has been obtained in both cases, thus implying that the inclusion of a well-designed start-up circuit does not appreciably degrade the performance of the voltage reference. It is worth noting that in 35 samples without the start-up circuit, we never observed the DC operating point of zero current. This observation suggests that the start-up circuit could be removed thus reducing the occupied chip area. The area occupied by proposed circuit decreases from 0.0298 mm^2 to around 0.0200 mm^2 if the startup circuit is removed.

4. CONCLUSION

We presented a nanopower sub-threshold CMOS voltage reference fabricated with 0.18 μm CMOS process. The reference voltage can be approximated by the difference of transistor threshold voltages. The circuit exhibits an extremely low LS of only 0.065% at the price of a relatively high TC of 462 ppm/°C. The voltage reference properly works with a supply voltage down to 0.6 V and with a power dissipation of only 22.3 nW. No appreciable differences have been observed between the behaviours of circuits with and without start-up block.

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DOI: 10.1002/cta