# MIDDLE EAST TECHNICAL UNIVERSITY

EE 414

Introduction to Analog Integrated Circuits

Term Project Final Report

**An Adjustable Voltage Regulator in 180 nm CMOS Technology**

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# A. Introduction

In this term-project for analog IC Design course, we are required to design an adjustable voltage regulator in 180 nm CMOS technology. For this project, we have designed a circuit which provides regulated and adjustable voltage at the output. The circuit contains supply input, ground, adjust, and output pins. After designing the circuit we have implemented, simulated and verified its operation. At the last step we have drawn its layout in 180 nm technology. In this report, detailed quantitative work related to the design specifications, design procedure, simulation results and layout of the circuit will be given.

# B. Project Description

## 1. GENERAL SPECIFICATIONS:

In this term project we are required to design an adjustable voltage regulator in a 180 nm CMOS technology. We are also required to satisfy some specifications for the regulator. First of all output voltage is required to be programmed with adjust input and external resistors between 1.2 V and $0.9xV_{IN}$. Other specifications can be listed as follows:

| | |
|---|---|
| Input voltage ($V_{IN}$) range | 1.3 V-3.3 V |
| Maximum power dissipation (no load condition) | <1 µW |
| Minimum resistive load | 200 kΩ |
| Output voltage change with temperature between -40°C and 85°C | <10mV |
| Output voltage change with input between 1.3 V-3.3 V (Line Regulation) | <5mV |
| Output voltage change between full load (200 kΩ) and no load conditions (Load Regulation) | <1mV |

**Figure 1 -** Specifications of the adjustable voltage regulator.

## 2. DESIGN PROCEDURE and QUANTITATIVE WORKS:

In order to satisfy all the specifications, our first step was to obtain a reference voltage with desired characteristics. Reference voltage needs to be completely independent from temperature and supply variations to provide a reference to our adjustable regulator circuit at any temperature and with any supply voltage.

Having obtained such a reference voltage we focused on designing an op-amp which also needs to perform its operations with input voltage of 1.3 Volts, and needs to be able to drive a load of 200k resistance.

### *a. Voltage Reference Circuit Design Procedure*

During the last weeks of the semester we researched among lots of papers related to ultra-low power voltage reference circuits. We tried circuits that we experienced in the class, even if their voltage characteristics were promising; their power dissipation was quite high compared to our specs. Therefore we tried optimizing a few circuit structures that we found from literature, and explained in our preliminary report, in detailed [1], [2], [3], [4], [5]. And we obtained the best results with the circuit that was described in [3], whose figure is given below. (**Figure 2**)

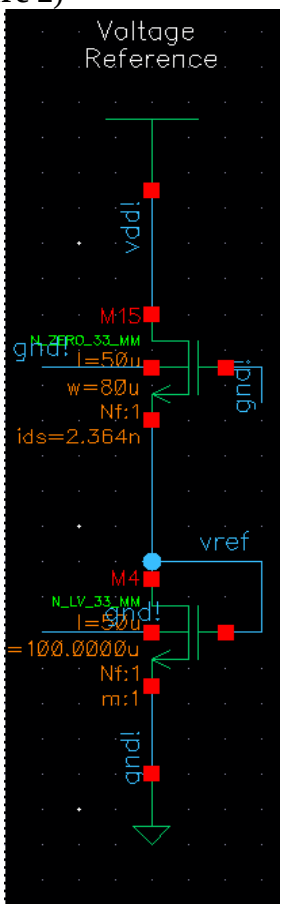


**Figure 2**

Here, note that the upper transistor is a ZERO nMOS (depletion type) to ensure that circuit is open with only ground connections. In other words, to obtain good quality voltage reference, we utilized GND which is perfect at any condition.

$$I_{sub} = \mu C_{ox} \frac{W}{L}(m-1)V_T^{\,2} \exp\left(\frac{V_{gs}-V_{TH}}{mV_T}\right)\left(1-\exp\left(\frac{-V_{ds}}{V_T}\right)\right)$$

$$I = \mu_1 C_{ox1} \frac{W_1}{L_1}(m_1-1)V_T^{\,2} \exp\left(\frac{0-V_{ref}-V_{TH1}}{m_1 V_T}\right)$$

$$= \mu_2 C_{ox2} \frac{W_2}{L_2}(m_2-1)V_T^{\,2} \exp\left(\frac{V_{ref}-V_{TH2}}{m_2 V_T}\right)$$

$$V_{ref} = \frac{m_1 m_2}{m_1+m_2}(V_{TH2}-V_{TH1}) + \frac{m_1 m_2}{m_1+m_2} V_T \ln\left(\frac{\mu_1 C_{ox1} W_1 L_2}{\mu_2 C_{ox2} W_2 L_1}\right)$$

Considering these equations and out trials we found out that keeping ‘L’ values large helps us to improve channel length modulation effect (line regulation is affected by that) and also power consumption.

Thus setting the given structure with (80u/50u) ZERO nMOS and (100u/50u) LV nMOS, we obtained a reference voltage at 99mV with line regulation of 0.5mV and temperature variation of 0.1 mV within the given intervals.

*b.* *<u>Operational Amplifier Circuit Design Procedure</u>*

In order to ensure that our circuit can be driven by 1.3 Volts and can provide enough gain, and can drive load of 200 kilo ohms, we constructed the following circuit in **Figure 3**. Here on the upper side, there is a self-biasing circuitry and inputs are handled with 2 ZERO nMOS’s. This circuit requires no biasing current since ZERO nMOS’ are always open and their current is limited by their W/L ratios. Actually, at the beginning we designed the circuit with biasing currents at the bottom, however during simulation phase, we found out that without that stage the current is still the same and acceptable for our purposes. At the output stage we utilized a basic common-drain amplifier to provide load driving capability to our op-amp.

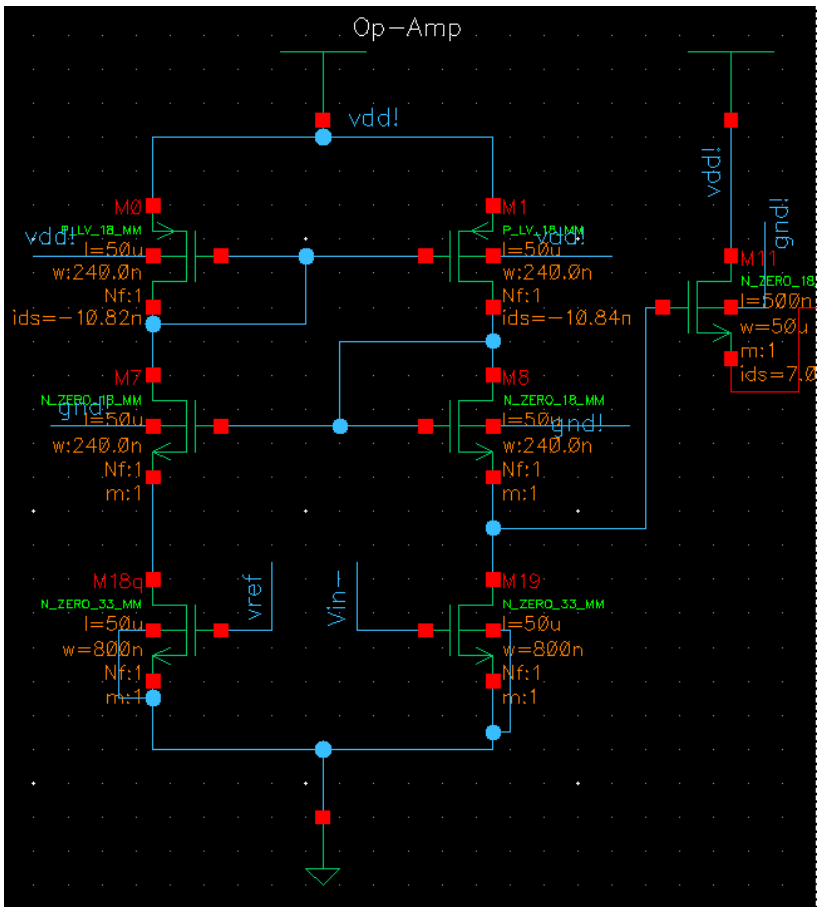


**Figure 3**

For this op-amp gain is around $g_{m19}(r_{o19}//r_{o1})$ and resistance seen from output is $(1/g_{m11})$; during the simulation phase starting from these equations we designed our circuit and found the following values for W/Ls.

## 3. SIMULATION RESULTS:

We have completed our schematic design and found optimal parameters after doing some simulations. Our design includes 9 transistors, 2 of which is used for voltage reference and 7 of which is used for op-amp. The view of the schematic is shown in **Figure 4.**

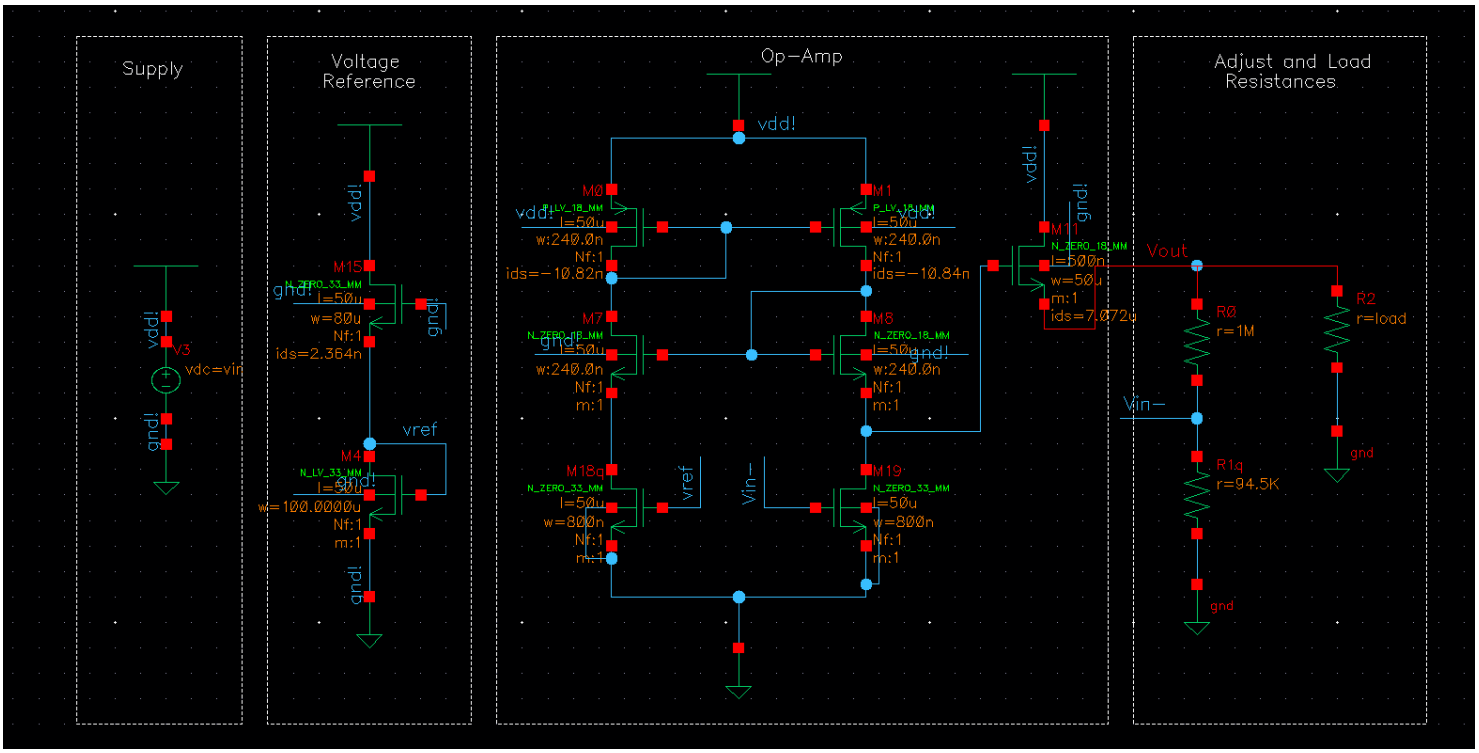


**Figure 4**– Schematic view

We have simulated this circuit and saw that we were satisfying the specifications given in the project description. While doing simulations, we have swept both temperature and input voltage in order to see both temperature dependence and supply dependence at the same time. We have also swept the load by adjusting its value as 200 kΩ (full load) and 100 GΩ (~no load) and got 2 different output voltage values for 2 different loads each time sweeping for temperature and supply. Options that we have set during simulations are shown in **Figure 5.**

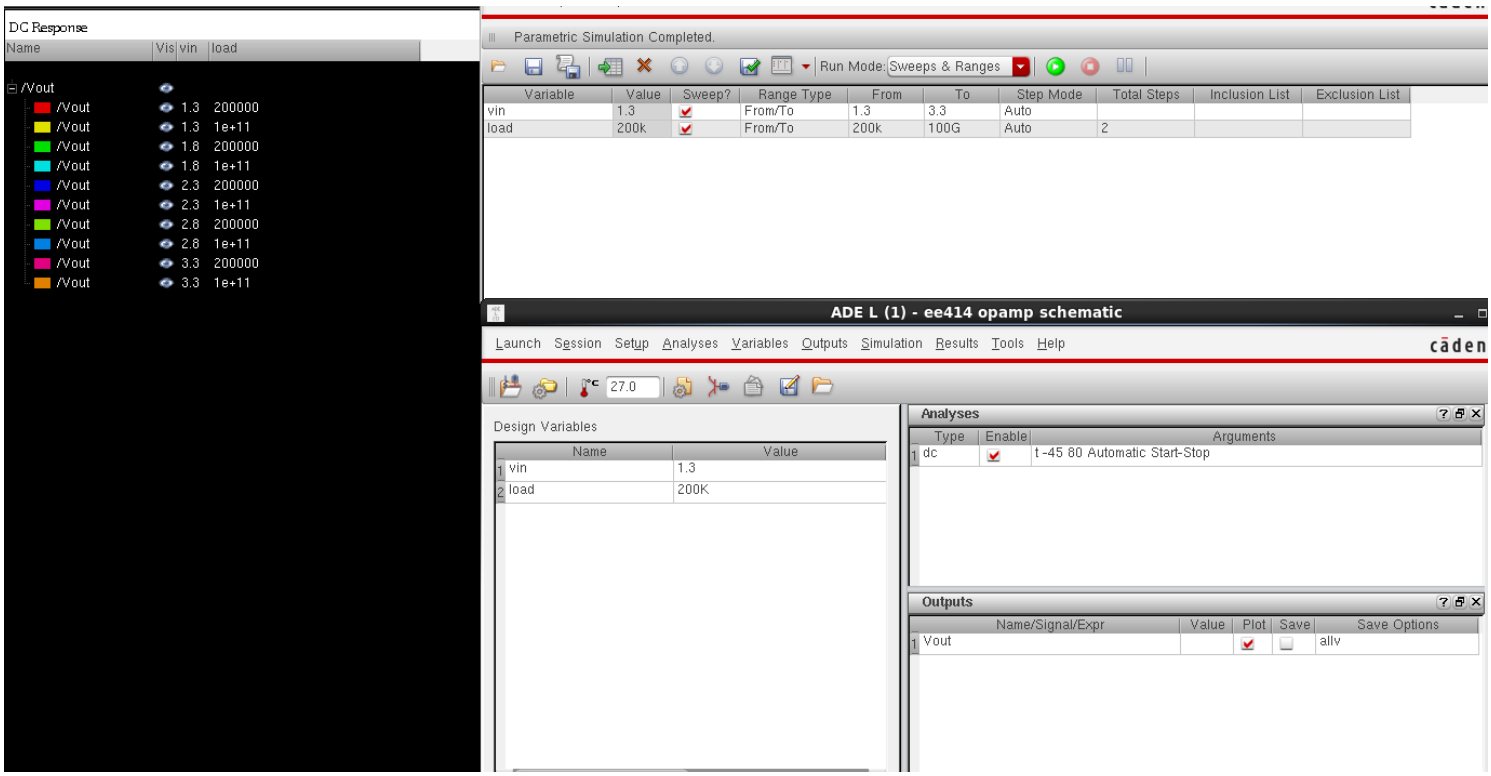


**Figure 5** –Simulation Options

After adjusting the settings of the simulation as described above, we have run the simulation. The results are shown in **Figure 6.** In the graph, 2 adjacent lines represent 2 different output voltage values for 2 different load conditions (e.g. orange and pink). Moreover, 5 adjacent groups of lines represent 5 different output voltages for 5 different input voltages (e.g. orange-pink and blue-green).

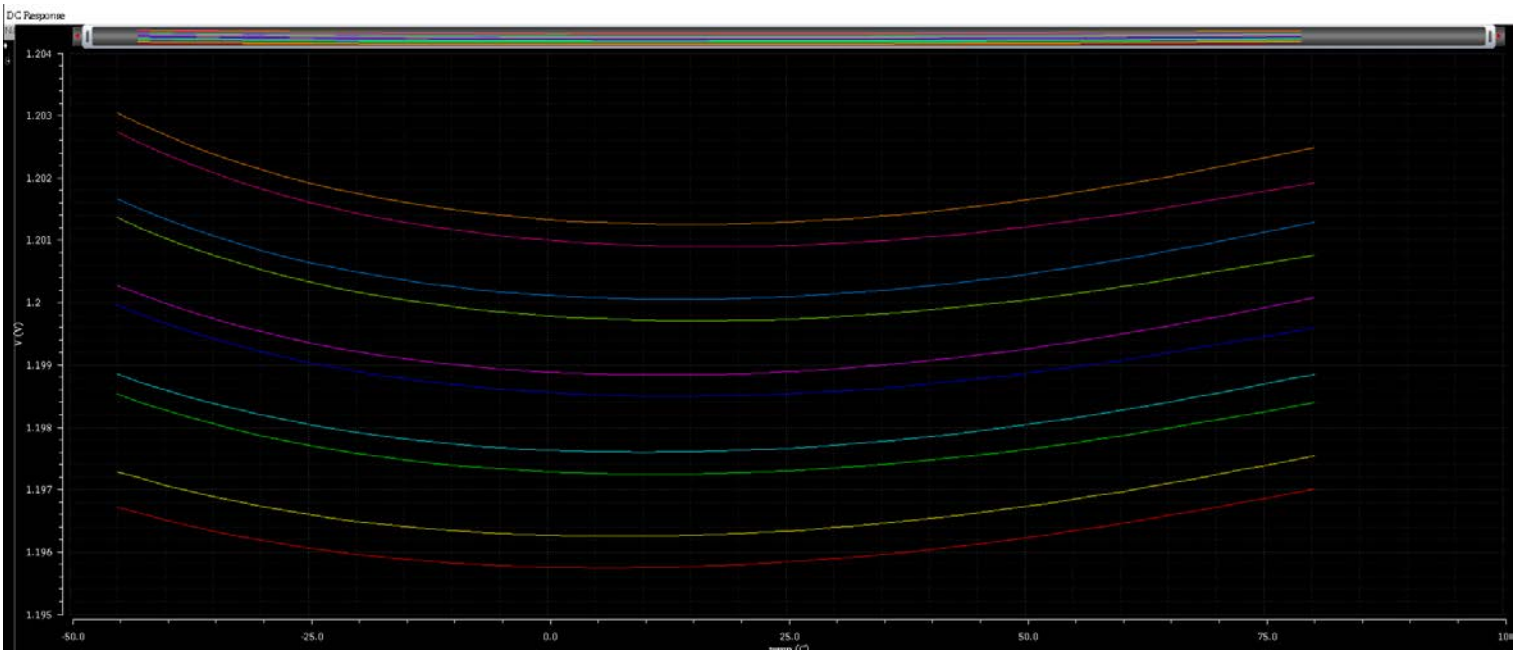


**Figure 6** – Simulation Results

**Note:** We have adjusted the output voltage as 1.2 V while doing all of the simulations because it is the best voltage point that satisfies all of the specifications. If one wants to change the output voltage between 1.2 and 3.3 V, he/she has to play with the adjust resistors. However, we do not guarantee that all of the specifications are satisfied for output voltages different than 1.2 V.

One can investigate all of the specifications just by looking the graph above. However, we have put cursor points and cursor lines in order for specifications to be understood more easily. The results for temperature dependence are shown in **Figure 7.**

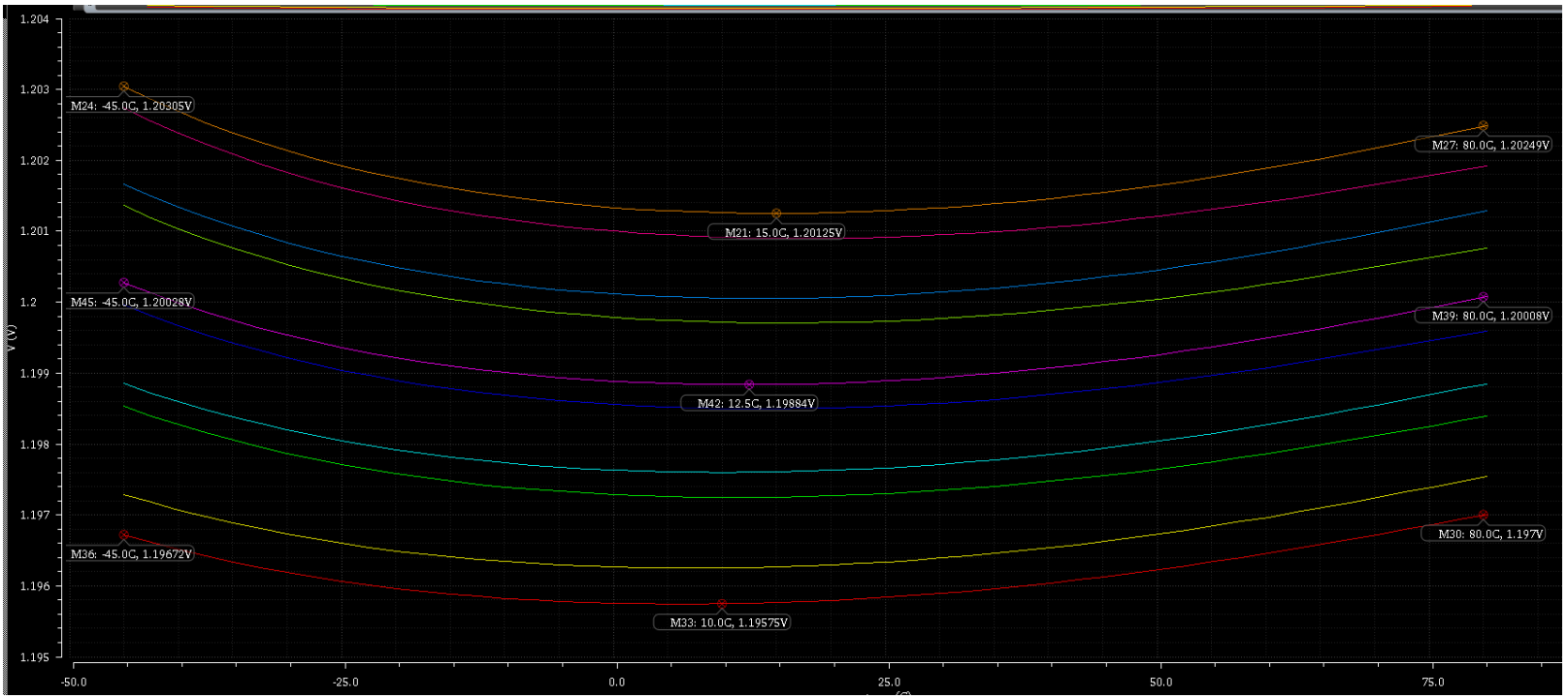


**Figure 7** – Temperature Dependence

The interpretations of **Figure 7** can be seen in **Table 1.**

| | **Vout Change between -45°C and 15°C** | **Vout Change between 15°C and 80°C** | **Vout Change between -45°C and 80°C** | **Minimum Vout Change** | **Maximum Vout Change** |
|---|---|---|---|---|---|
| **Vin = 3.3 V** | 1.8 mV | 1.3 mV | 0.5 mV | 0.5 mV | 1.8 mV |
| **Vin = 2.3 V** | 1.4 mV | 1.3 mV | 0.1 mV | 0.1 mV | 1.4 mV |
| **Vin = 1.3 V** | 1 mV | 1.3 mV | 0.3 mV | 0.3 mV | 1.3 mV |

**Table 1** – Temperature Dependence

Design specifications say that maximum output voltage change with temperatures between -45°C and 80°C should be 10 mV. Therefore; we do not only satisfy the temperature dependence specification, but we are also so far away from the limit, as our worst case is 1.8 mV.

The results for line regulation and load regulation are shown in **Figure 8.**

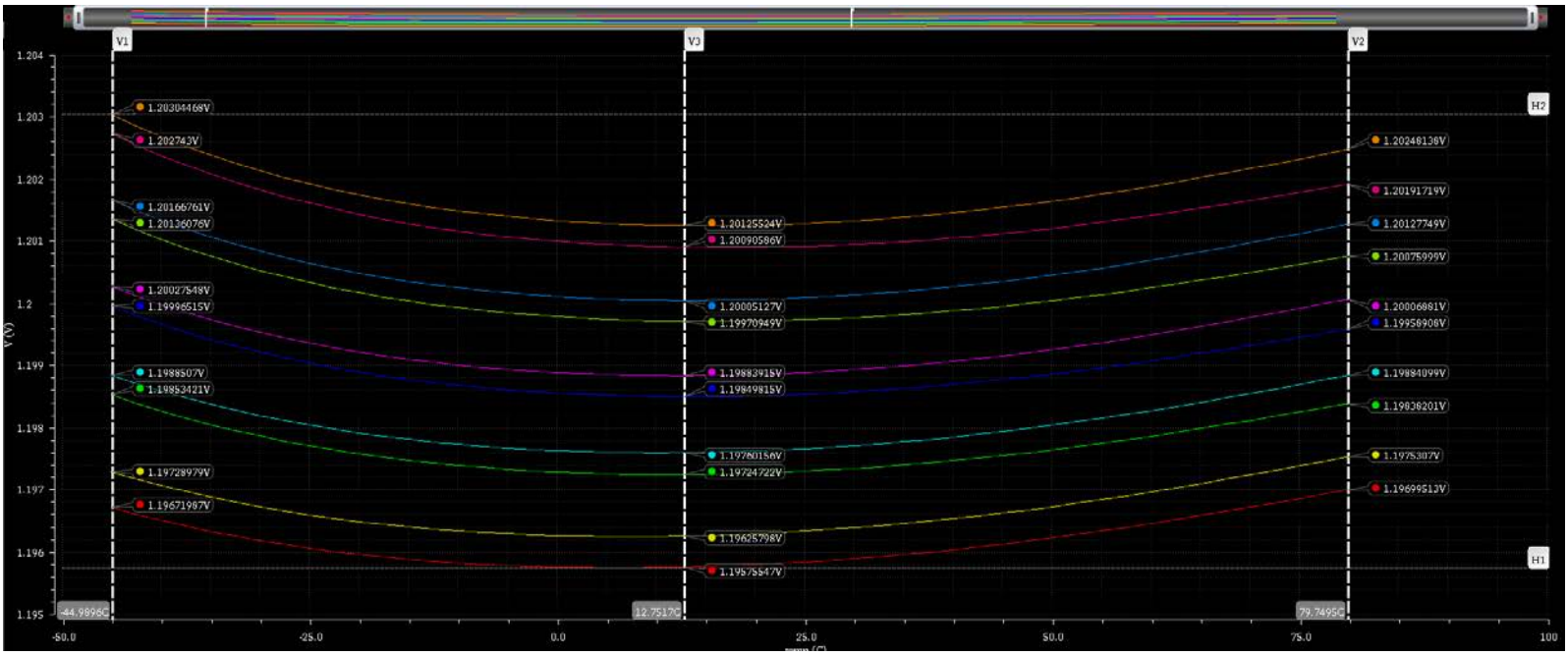


**Figure 8**– Line and Load Regulation

The representations of the lines on the graph are given in **Table 2.**

| (5 Groups from bottom to top) | Full Load (200 kΩ) | No Load (100 GΩ) |
|---|---|---|
| **Vin = 1.3 V** | ----- Red | ----- Yellow |
| **Vin = 1.8 V** | ----- Dark Green | ----- Light Blue |
| **Vin = 2.3 V** | ----- Dark Blue | ----- Purple |
| **Vin = 2.8 V** | ----- Light Green | ----- Blue |
| **Vin = 3.3 V** | ----- Pink | ----- Orange |

**Table 2** – Representation of Lines

Line regulations for full load and no load conditions do not have significant difference. Therefore, we do not need to consider full load and no load conditions separately for line

regulation calculations. One of them is sufficient. The interpretations of **Figure 8** about line regulation are given in **Table 3.** Line regulation is calculated by taking the difference of output voltages corresponding to input voltages of 1.3 V and 3.3 V.

| | **Temp. = -45°C** | **Temp. = 12.8°C** | **Temp. = 80°C** | **Typical Line Regulation** | **Maximum Line Regulation** |
|---|---|---|---|---|---|
| **Line Regulation** | 5.7 mV | 5 mV | 5 mV | 5 mV | 5.7 mV |

**Table 3** – Line Regulation

According to the design specifications, maximum line regulation should be 5 mV. Our design satisfies this requirement unless the temperature is too low. However, we are still on the verge of line regulation limit.

Another parameter that can be understood the graph above is load regulation. As one can see from the graph, load regulation does not vary significantly with temperature. Therefore, we selected anoptimal temperature (12.8°C) while calculating load regulation. The interpretations of **Figure 8** about load regulation are given in **Table 4.**

| | **Vin = 1.3 V** | **Vin = 1.8 V** | **Vin = 2.3 V** | **Vin = 2.8 V** | **Vin = 3.3 V** | **Typical Load Regulation** | **Maximum Load Regulation** |
|---|---|---|---|---|---|---|---|
| **Load Regulation** | 0.5 mV | 0.4 mV | 0.3 mV | 0.3 mV | 0.3 mV | 0.3 mV | 0.5 mV |

**Table 4** – Load Regulation

Design specifications say that maximum load regulation should be 1 mV. So, we satisfy the load regulation specification and we are also far from the limit.

Then, one more specification remains. That is power consumption. We have calculated the power consumption of our circuit by adding the currents drawn from transistors. The corresponding current values can be seen in **Figure 4.** Then, the maximum power consumption can be calculated when supply voltage is at 3.3 V, as follows;

$$I_{ds,M15} = 2.36\ nA$$

$$I_{sd,M0} = 10.82\ nA$$

$$I_{sd,M1} = 10.84\ nA$$

$$Power\ Consumption = (I_{ds,M15} + I_{sd,M0} + I_{sd,M1})\ (V_{dd})$$

$$= (2.36\ nA + 10.82\ nA + 10.84\ nA)\ (3.3\ V)$$

$$= 79.26\ nW$$

In the design specifications, maximum power dissipation should be less than 1 uW. Therefore, our 79.26 nW power dissipation value is a very good result. This is due to the fact that we focused on how to design the circuit with the least number of transistors, and also we tried to keep their L values as large as possible. This power dissipation is a result of using total of 9 transistors. (Note that, power dissipated on the adjust resistances are not included since adjust part is external and can be set by changing resistances)

In addition to all of these specifications, the output voltage of the design is required to be adjusted between 1.2 V and 0.9*Vin by playing with the adjust resistors. For this purpose, we have simulated our circuit one more time and saw that the output voltage can be programmed between the specified values. The results for supply voltage of 3.3 V can be seen in **Figure 9.**

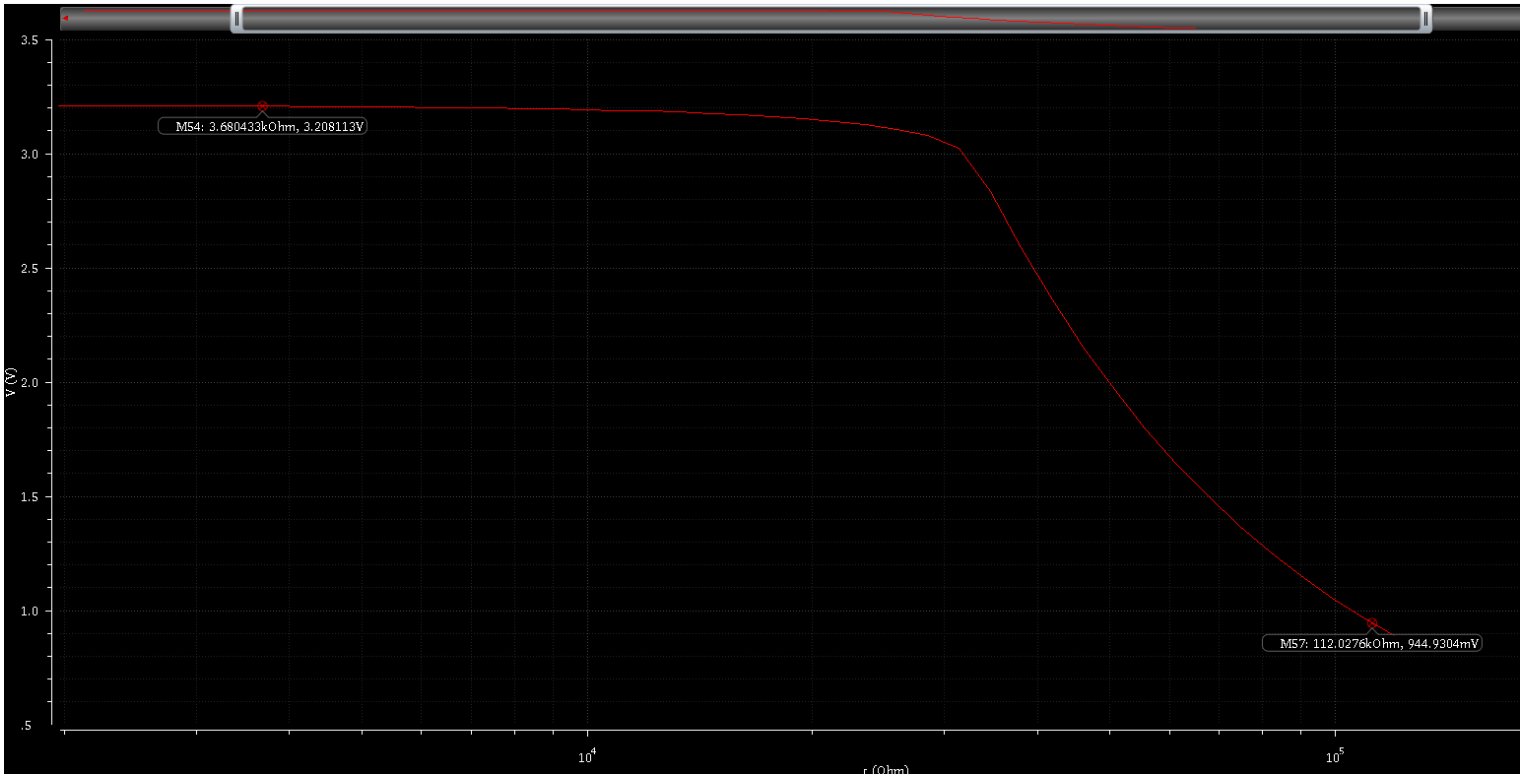


**Figure 9**– Adjusting the Output Voltage

On the graph above, one of the adjust resistors is swept in a wide range and the output voltage is drawn. One can see from the graph that the output voltage can be adjusted between 945 mV and 3.21 V. Since the maximum value of 0.9*Vin is (0.9)*(3.3 V) =2.97 V, this specification is satisfied in our design. Furthermore, if we keep going increasing the value of the resistance of the adjust resistor on the graph, we can also reach lower values up to ~800 mV either.

This is the last simulation we have implemented. In this way, we have proven that our design meets all of the requirements given in the design specifications.

*Design Summary:*

| Property | Specification | Typical Value | Worst Case |
|---|---|---|---|
| Line Regulation | 5 mV | 5 mV | 5.7 mV (@ T=-45 C) |
| Load Regulation | 1 mV | 0.3 mV | 0.5 mV (@ Vin=1.3 V) |
| Temperature Compensations | 10 mV | 1.4 mV | 1.8 mV (@ Vin=3.3 V) |
| Power Consumption | 1 uW | < 80 nW | 80 nW (@ Vin=3.3V) |
| Output Swing | 1.2V – 0.9 * Vin | 0.9 V - 0.97 * Vin | Satisfied |
| Supply Voltage | 1.3 V – 3.3 V | Starts working at **0.9 V**(But line regulation could get worse) | Satisfied |

**Table 5** – Design Summary

## 4. LAYOUT

After verifying the operation of our circuit, we went on to draw the layout of it. While drawing the layout, we have used readymade drawings for the transistor cells. We have placed them at proper positions and made the connections between them. We have also put the substrates of nMOS and pMOS transistors. Moreover, we have put n-well for pMOS transistors since we are using n-well process technology in our design. We have completed drawing the layout by taking the design rules into account. The view of the layout is given in **Figure 10.**

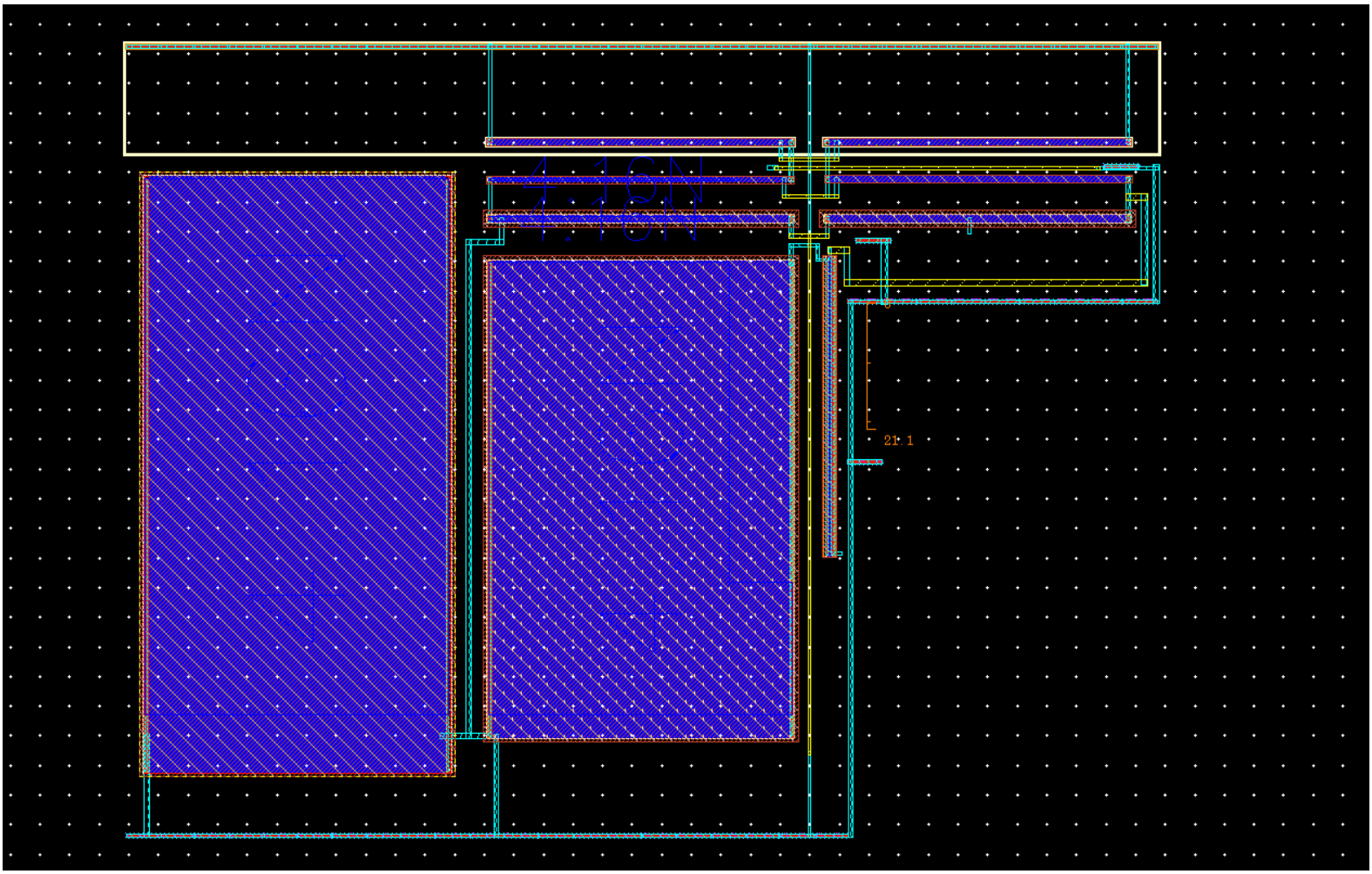


**Figure 10**– Layout View

After drawing the layout, we have done a DRC check in order to see whether there was any error due to violating the design rules or not. DRC gave us some errors and all of the errors are due to the same reason. The maximum distance between the transistors and their bulk region should be 20 um, but we were violating this rule. The output of DRC is shown in **Figure 11.**

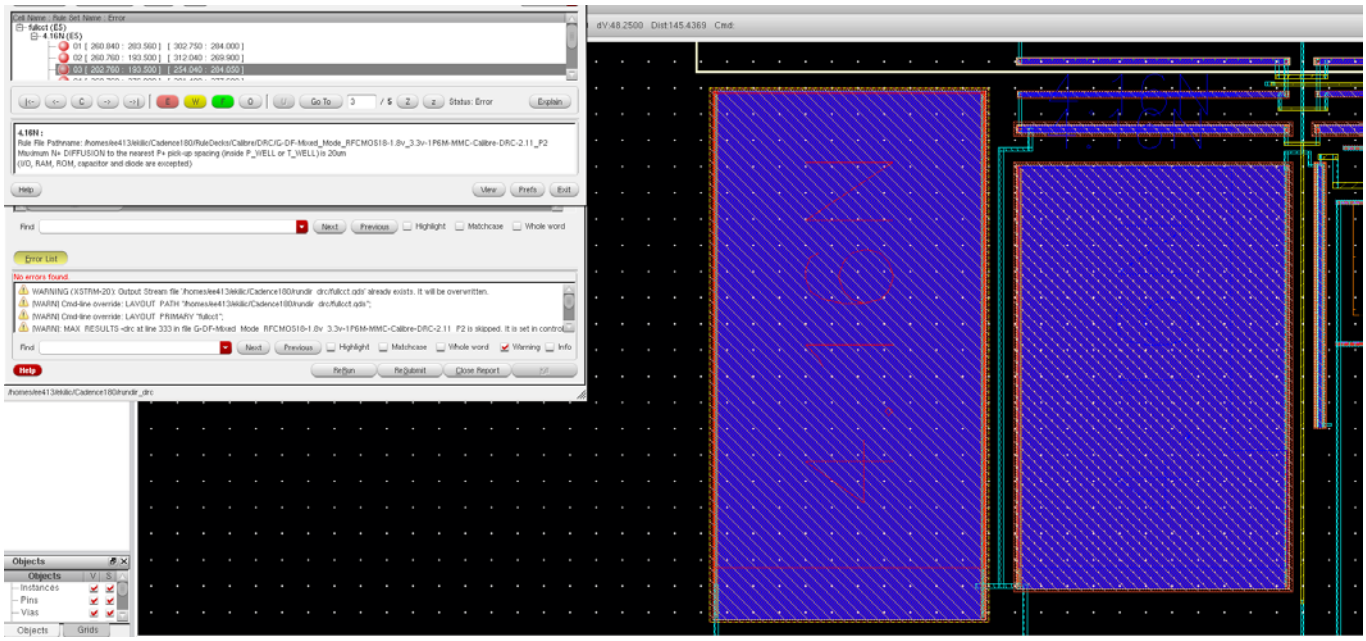

**Figure 11** – The Output of DRC

Since we were using 2 big transistors in our design (100x100um$^2$ and 80x100um$^2$), there were no other way except putting the bulk regions of those transistors into their active regions in order to obey the rules. We tried putting the bulk regions into active regions, but we got another error that time. Cadence did not allow us to do that. Therefore, we had to rearrange our design. We thought that if we increased the finger number of those transistors and decrease their width sizes without changing their characteristics, we might be able to draw the layout without any error. For this purpose, we rearranged the schematic of the design without affecting the simulation results. The view of the schematic for the voltage regulator is given in **Figure 12.**

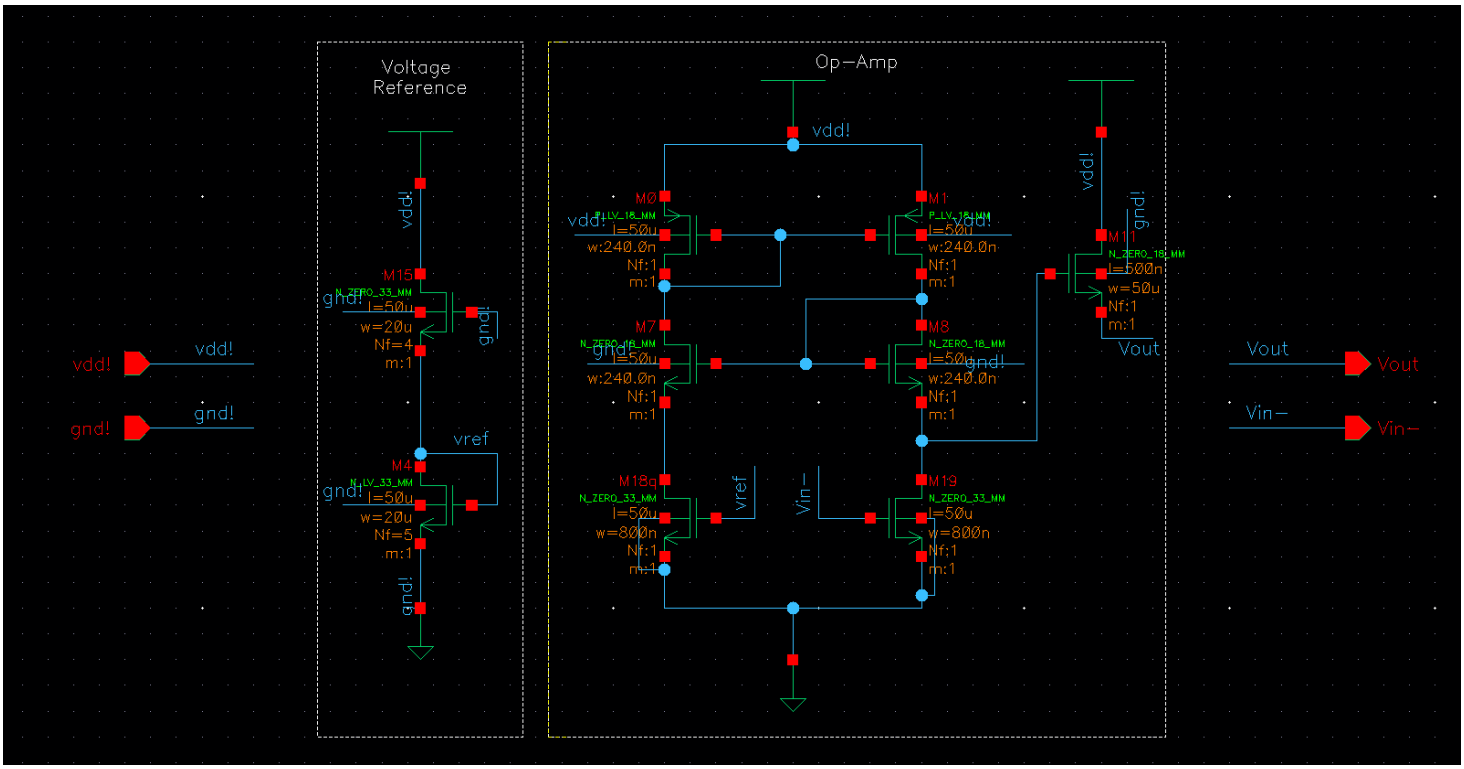


**Figure 12**– Schematic View of the Voltage Regulator

After that, we attained corresponding finger numbers in the layout and redrew it. We also put pin names and corresponding labels to vdd, gnd, Vin- and Vout. The final view of the layout is shown in **Figure 13.**

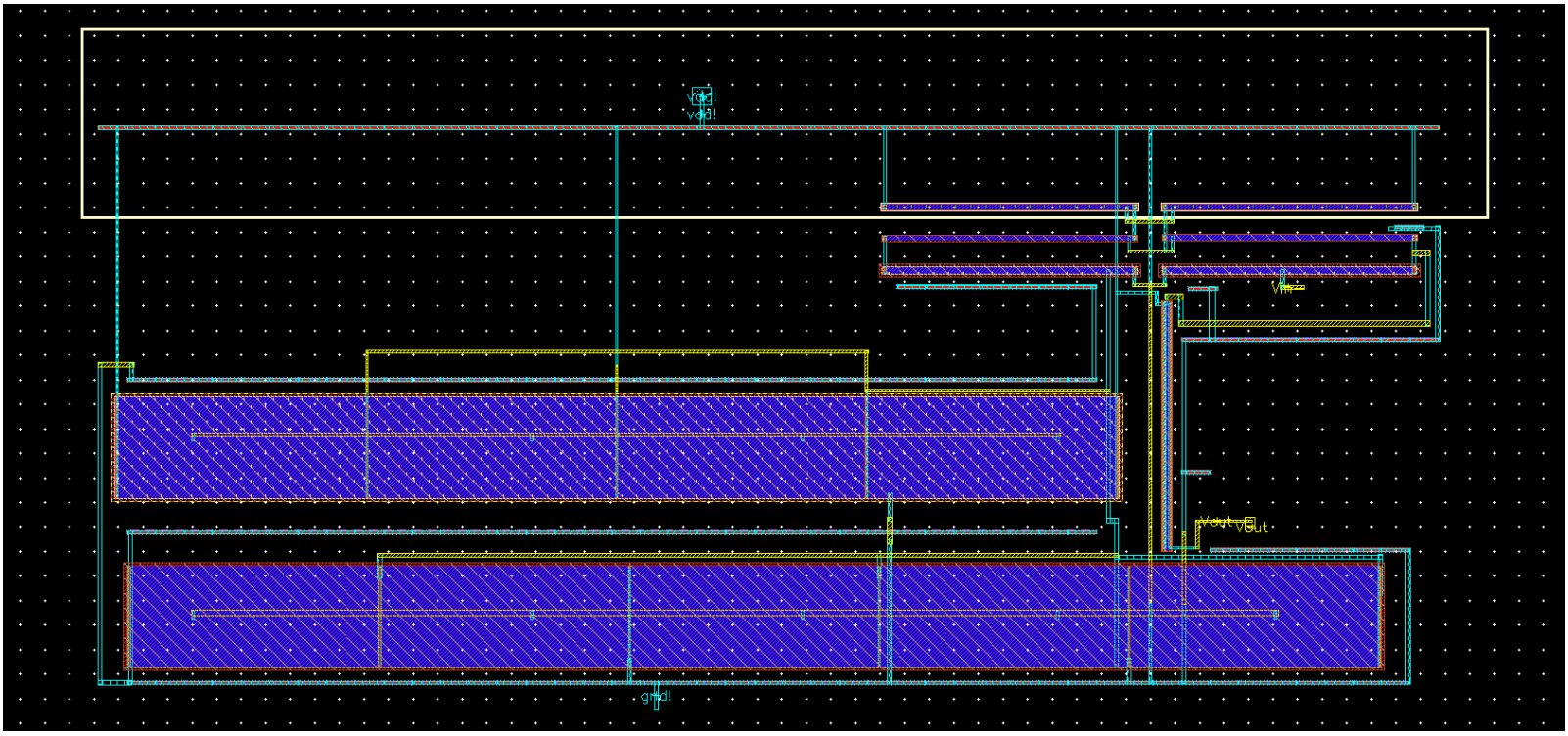


**Figure 13**– The Final View of the Layout

After completing the layout, we have done DRC again. At that time, we saw that there were no errors left in our layout. The results of DRC are shown in **Figure 14.**


**Figure 14**– Results of DRC

After DRC, we had to do an LVS check in order to see whether schematic and layout were matching or not. We have done LVS check and after a few minor corrections saw that schematic and layout matched. The results are shown in **Figure 15, Figure 16** and **Figure 17.**

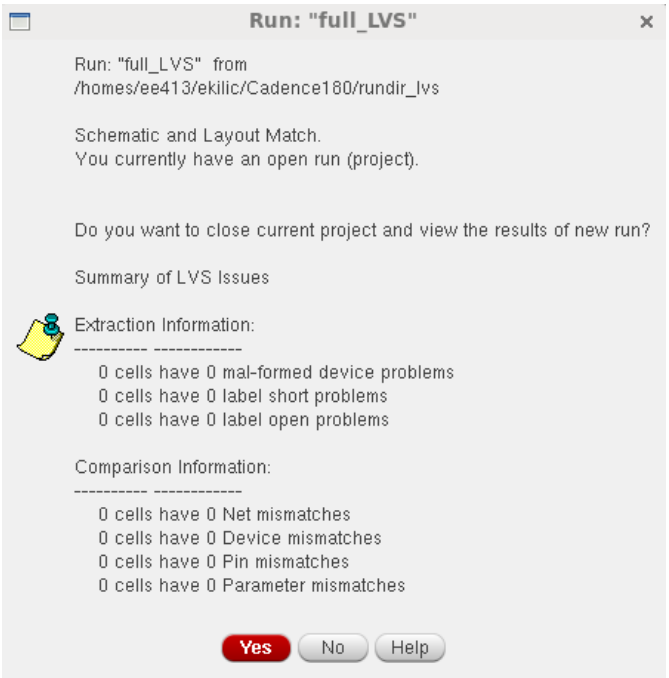


**Figure 15**

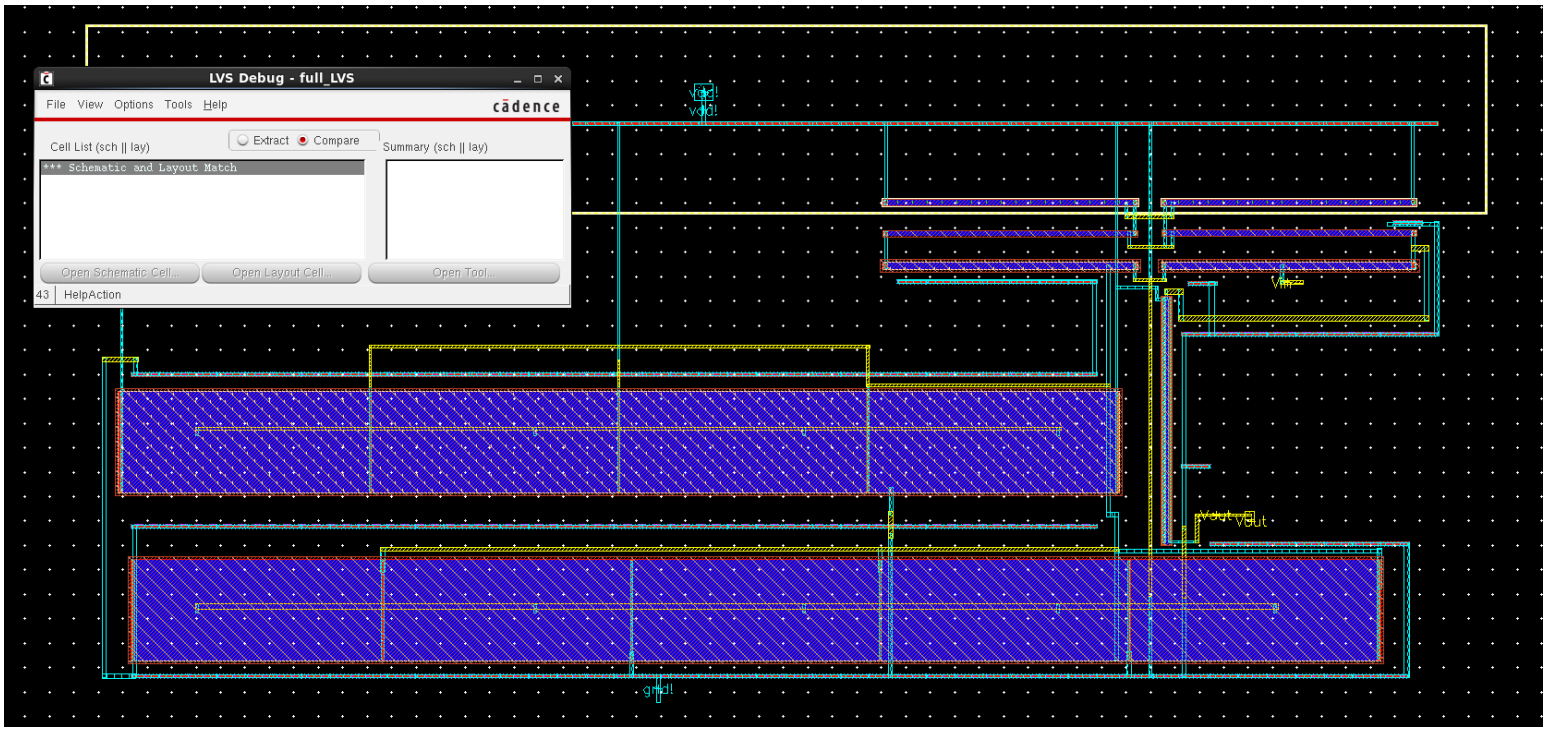


**Figure 16**

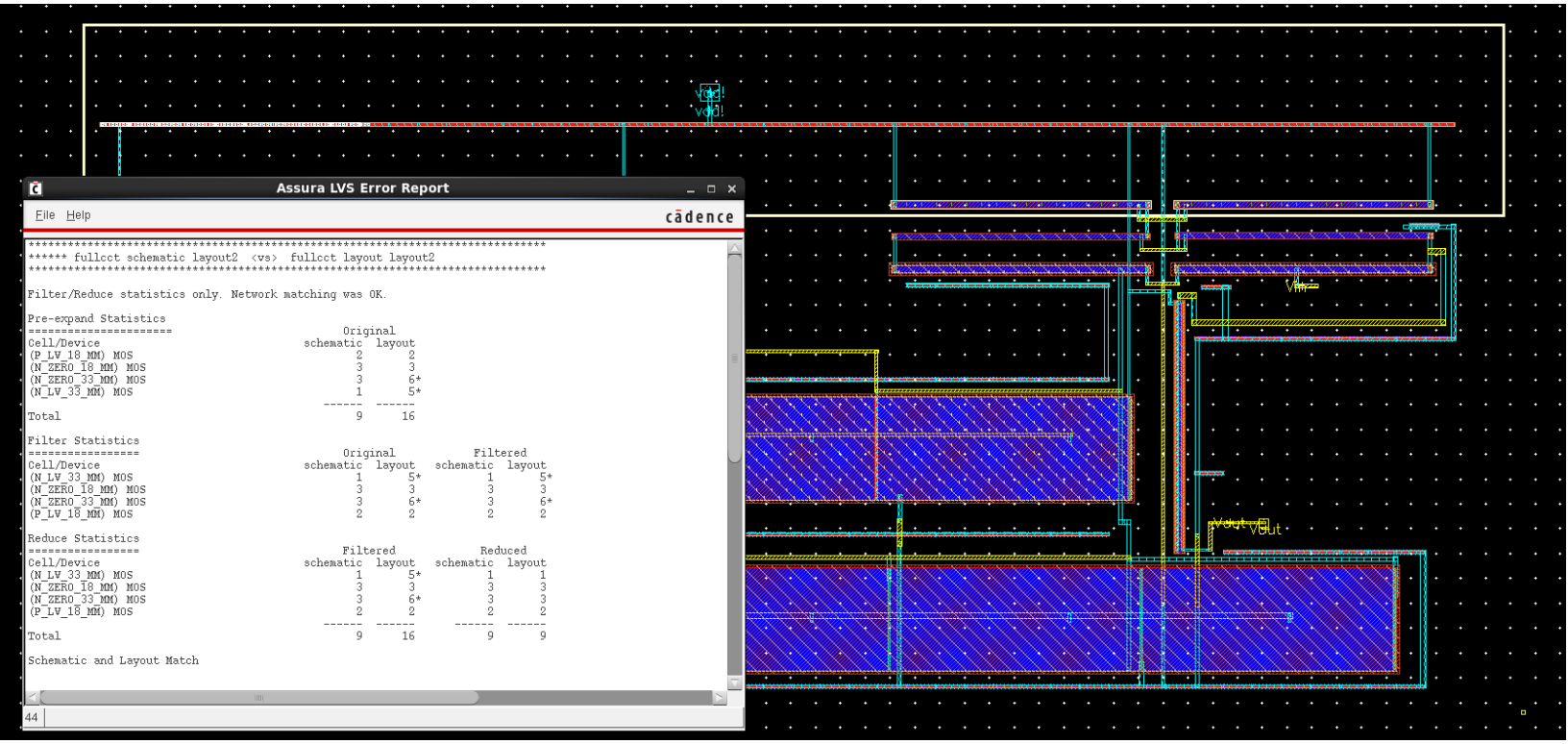


**Figure 17**

As one can see from the results above, schematic and layout of our layout matched. In this way, we have proven that out layout is properly drawn. This was the last thing to be done in the design; therefore, our job has finished here. The symbolic view of the voltage regulator is given in **Figure 18.**

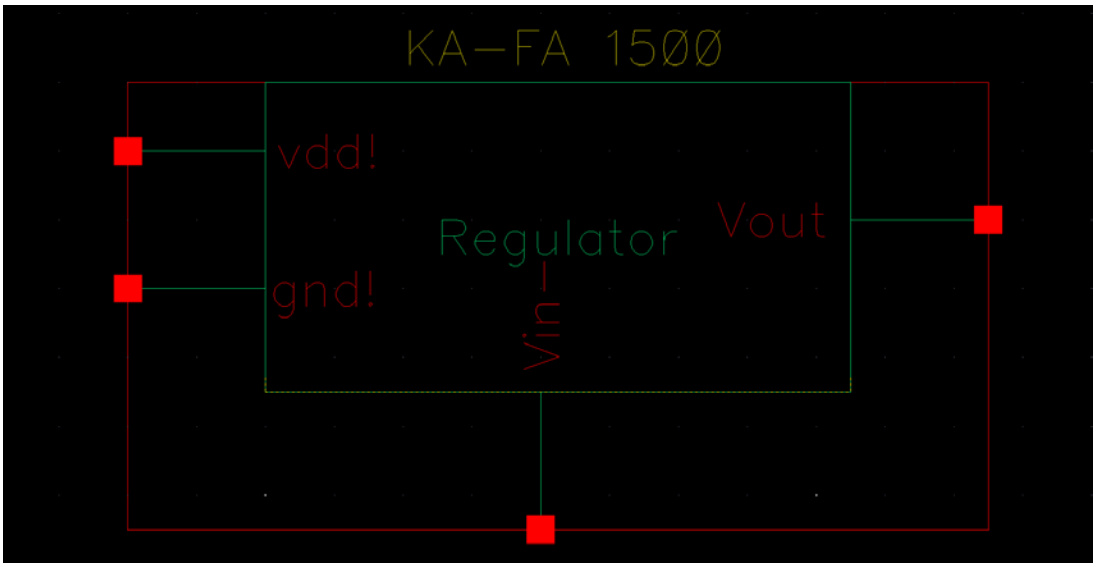


**Figure 18**– Symbol of the Voltage Regulator

## C. Conclusion

In this project for EE 414 Analog IC Design course, we have designed, implemented, verified, and simulated an adjustable voltage regulator in 180 nm CMOS technology. It can be easily said that, we designed a successful circuit which performs all the given specifications. As it can be seen from the simulation results section and **Table 5**, our circuit is within all the specs except that its line regulation is at the edge of the spec (it is between 5 and 5.7 mV whereas given specification was 5mV).

During the project, we read and investigated a lot especially for the voltage regulator part, thus our design process was quite instructive in terms of cutting-edge research in these topics, and we learnt a lot. We also got familiar with 180 nm CMOS technology and experienced its properties.

In this report, all design steps, schematic implementation, layout drawings, and DRC & LVS results are presented.

## D. References


[1] De Vita, Giuseppe, and Giuseppe Iannaccone. "A sub-1-V, 10 ppm/° C, nanopower voltage reference generator." *Solid-State Circuits, IEEE Journal of* 42.7 (2007): 1536-1542.

[2] Qu, Zihua, et al. "A sub-0.6 V, 34.8 nW, 4.6 ppm/° C CMOS voltage reference using subthreshold and body effect techniques." *Microelectronics & Electronics, 2009. PrimeAsia 2009. Asia Pacific Conference on Postgraduate Research in*. IEEE, 2009.

[3] Seok, Mingoo, et al. "A 0.5 V 2.2 PW 2-transistor voltage reference." *Custom Integrated Circuits Conference, 2009. CICC'09. IEEE*. IEEE, 2009.

[4] Ueno, Ken, et al. "A 300 nW, 15 ppm/C, 20 ppm/V CMOS voltage reference circuit consisting of subthreshold MOSFETs." *Solid-State Circuits, IEEE Journal of* 44.7 (2009): 2047-2054.

[5] Gungor, A.C., and Kilic E. “EE 414 Term Project Preliminary Report”