A 0.3-μW, 7 ppm/℃ CMOS Voltage Reference Circuit for On-Chip Process Monitoring in Analog Circuits

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***Abstract*— A CMOS voltage reference circuit for on-chip process compensation in analog circuits has been developed in 0.35-μm CMOS process. The circuit generates a reference voltage based on threshold voltage of a MOSFET at absolute zero temperature. Theoretical analyses and experimental results showed that the circuit generates a quite stable reference voltage of 745 mV on average. The temperature coefficient and line sensitivity of the circuit were 7 ppm/℃ and 0.002%/V, respectively. The circuit consists of subthreshold MOSFETs with a low-power dissipation of 0.3 μW or less. By utilizing the nature of the reference voltage, which changes with the process conditions of threshold voltage in each LSI chip, the circuit can be used as an elementary circuit block for on-chip process compensation systems.**

I. Introduction

Progress in CMOS technology by device and voltage scaling has made it possible to integrate large scale analog and digital circuit systems for high performance and low power dissipation on a single chip. On the other hand, process variations in an LSI chip have become a significant issue in state-of-the-art CMOS technology. This is because process variations cause degradation of circuit performance and low fabrication yield in low power circuits. Therefore, it is becoming highly important for LSI designers to compensate for process variations. In CMOS process parameters, variation of threshold voltage of a MOSFET is one of the serious problems because threshold voltage has a significant impact on its drain current.

The variation of threshold voltage can be classified broadly into two categories: within-die (WID) (intra-die) variation and die-to-die (D2D) (inter-die) variation [1], [2]. The former affects the relative accuracy of transistors placed closely within a chip, and can be reduced in analog circuits by using large-sized transistors [3] and careful layout techniques [4]. However, the latter affects the absolute accuracy of the chip and could not be compensated in conventional circuit techniques. Therefore, a design method providing sufficient circuit performance even at the worst case corners is required. As a result, it has not been possible to optimize the performance, power dissipation, operating frequency, and area overhead of LSIs.

To solve these problems, in this paper, we propose a CMOS voltage reference circuit to monitor the D2D variation of threshold voltage. The circuit generates a voltage based on the threshold voltage of a MOSFET in an LSI chip. Because the output voltage changes with the process conditions of threshold voltage in each LSI chip, the circuit can be used as an elementary circuit block for on-chip process compensation systems. The following sections describe this reference circuit.

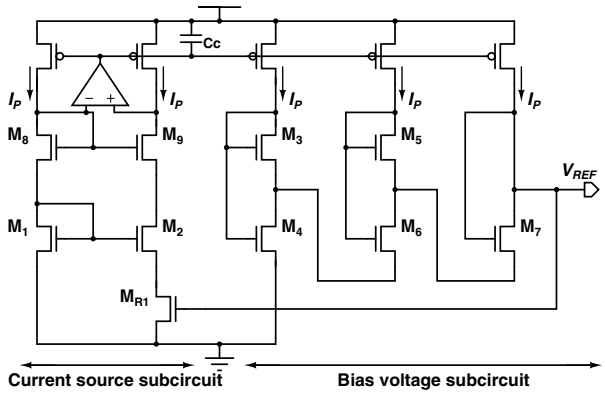

Fig. 1. Schematic of the proposed voltage reference circuit.

II. Circuit Configuration

Figure 1 shows voltage reference circuit we proposed. The circuit consists of a current source subcircuit, a bias-voltage subcircuit, and an operational amplifier. The current source subcircuit is based on a β multiplier self-biasing circuit and uses a MOS resistor M_{R1} instead of an ordinary passive resistor. The bias-voltage subcircuit accepts the current through pMOS current mirrors and generates the reference voltage. The bias-voltage subcircuit consists of a diode-connected transistor (M_4) and two differential pairs (M_3-M_6, M_5-M_7), and is based on the translinear principle. We operate all MOSFETs in the subthreshold region except for MOS resistor M_{R1}, which is operated in the strong-inversion and deep triode region. An operational amplifier and nMOS current mirror (M_8, M_9) are used to improve the power supply rejection ratio (PSRR) and line sensitivity of the circuit.

The circuit generates negative and positive temperature dependent voltages and combines these voltages to produce a reference voltage with a zero temperature coefficient. The following sections describe the circuit operation in detail.

A. Operation Principle

The subthreshold MOS current I_D can be expressed as

$$I_D = KI_0 \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right), \quad (1)$$

where K is the aspect ratio (=W/L) of transistors, $I_0 (= \beta(\eta - 1)V_T^2)$ is the process-dependent parameter, $V_T (= k_B T/q)$ is the thermal voltage, V_{TH} is the threshold voltage of a MOSFET, and η is the subthreshold slope factor [5]. In the circuit in

Fig.1, the current flowing in the circuit I_P is determined by the ratio of M_1 and M_2 and the resistance of MOS resistor M_{R1}, and is given by

$$I_P = \beta(V_{REF} - V_{TH})\eta V_T \ln(K_2/K_1), \quad (2)$$

where β is the current gain factor.

In the bias-voltage subcircuit, gate-source voltages of transistors (V_{GS3} through V_{GS7}) form a closed loop with the reference voltage V_{REF}, so we find that

$$\begin{aligned} V_{REF} &= V_{GS4} - V_{GS3} + V_{GS6} - V_{GS5} + V_{GS7} \\ &= V_{GS4} + \eta V_T \ln\left(\frac{2K_3K_5}{K_6K_7}\right) \\ &= V_{TH} + \eta V_T \ln\left(\frac{3I_P}{K_4I_0}\right) + \eta V_T \ln\left(\frac{2K_3K_5}{K_6K_7}\right). \end{aligned} \quad (3)$$

The reference voltage can be expressed by the sum of gate-source voltage V_{GS4} and thermal voltage V_T scaled by the transistor sizes. Because these voltages have negative and positive temperature dependence, respectively, a constant voltage reference circuit with little temperature dependence can be constructed by adjusting the size of the transistors. Note that the threshold voltages of transistors in source-coupled pairs (M_3-M_6, M_5-M_7) are canceled each other by source-coupled circuit configuration.

B. Temperature Dependence

The temperature dependence of the threshold voltage can be given by

$$V_{TH} = V_{TH0} - \kappa T, \quad (4)$$

where V_{TH0} is the threshold voltage at absolute zero, and κ is the temperature coefficient of the threshold voltage [6]. From Eqs. (2) and (4), the output voltage in Eq. (3) can be rewritten as

$$\begin{aligned} V_{REF} &= V_{TH0} - \kappa T \\ &\quad + \eta V_T \ln\left\{\frac{6\eta K_{R1}K_3K_5(V_{REF}-V_{TH})}{K_4K_6K_7(\eta-1)V_T}\ln\left(\frac{K_2}{K_1}\right)\right\}. \end{aligned} \quad (5)$$

The temperature coefficient of the reference voltage V_{REF} in Eq. (5) is given by

$$\begin{aligned} \frac{dV_{REF}}{dT} &= -\kappa + \frac{\eta k_B}{q}\ln\left\{\frac{6\eta K_{R1}K_3K_5(V_{REF}-V_{TH})}{K_4K_6K_7(\eta-1)V_T}\ln\left(\frac{K_2}{K_1}\right)\right\} \\ &\quad + \eta V_T\left\{\frac{1}{V_{REF}-V_{TH}}\left(\frac{dV_{REF}}{dT}+\kappa\right)-\frac{1}{T}\right\}. \end{aligned} \quad (6)$$

On the condition where $V_{REF} - V_{TH0} \ll \kappa T$ and $\eta V_T \ll \kappa T$, the temperature coefficient of the reference voltage V_{REF} in Eq. (6) is rewritten as

$$\frac{dV_{REF}}{dT} = -\kappa + \frac{\eta k_B}{q}\ln\left\{\frac{6q\eta\kappa}{k_B(\eta-1)}\frac{K_{R1}K_3K_5}{K_4K_6K_7}\ln\left(\frac{K_2}{K_1}\right)\right\}. \quad (7)$$

Therefore, the condition for a zero temperature coefficient can be given by

$$-\kappa + \frac{\eta k_B}{q}\ln\left\{\frac{6q\eta\kappa}{k_B(\eta-1)}\frac{K_{R1}K_3K_5}{K_4K_6K_7}\ln\left(\frac{K_2}{K_1}\right)\right\} = 0. \quad (8)$$

By setting the aspect ratios K in accordance with Eq. (8), a constant reference voltage of a zero temperature coefficient can be obtained. From Eqs. (5) and (8), the output voltage V_{REF} is given by

$$V_{REF} = V_{TH0}. \quad (9)$$

Therefore, the circuit generates the threshold voltage of MOSFET at absolute zero temperature.

C. Temperature stability of the reference voltage V_{REF}

As discussed in previous sections, the circuit generates a reference voltage with little temperature dependence. However, because the output voltage refers to the threshold voltage of a MOSFET at absolute zero temperature, it is assumed that process variations have a significant impact on the output voltage. Temperature characteristics of the reference voltage depend on both the temperature coefficient of the threshold voltage κ and the aspect ratios of transistors K, as shown in Eq. (7). Therefore, the temperature coefficient of threshold voltage κ is the key parameter for temperature independent operation. The following discusses the temperature stability of κ with process variation.

The physical expression of threshold voltage in Eq. (4) can be expressed as

$$V_{TH} = -\frac{E_g}{2q} + \psi_B + \frac{\sqrt{4\varepsilon_{si}qN_A\psi_B}}{C_{OX}}, \quad \psi_B = V_T \ln\left(\frac{N_A}{n_i}\right), \quad (10)$$

where ψ_B is the difference between fermi level and intrinsic level, ε_{si} is the silicon permittivity, N_A is the channel doping concentration, n_i is the intrinsic carrier density, and E_g is the bandgap energy of silicon [5]. From Eq. (10), the temperature coefficient of the threshold voltage $\left(\frac{dV_{TH}}{dT} = \kappa\right)$ is given by

$$\frac{dV_{TH}}{dT} = -(2\eta-1)\frac{k_B}{q}\left\{\ln\left(\frac{\sqrt{N_cN_v}}{N_A}\right)+\frac{3}{2}\right\}+\frac{\eta-1}{q}\frac{dE_g}{dT}, \quad (11)$$

where N_c and N_v are the effective densities of states in the conduction and valence bands, respectively. From Eqs. (10) and (11), we find that the threshold voltage V_{TH} and the temperature coefficient of the threshold voltage κ depend on the channel doping concentration N_A. The temperature coefficient of the threshold voltage contains N_A as a process variation parameter, but the effect of the variation on the temperature coefficient κ can be ignored because N_A is contained in a logarithmic function.

To verify the effect of the process variations on the threshold voltage and the temperature coefficient of the threshold voltage, Eqs. (10) and (11) were calculated considering 0.35-μm CMOS parameters. Figure 2 shows a plot of the calculated threshold voltage V_{TH} and the temperature coefficient of threshold voltage κ as a function of the channel doping concentration N_A. In the doping concentration around 2×10^{17} cm^{-3}, which is the typical concentration in the CMOS process we used, the threshold voltage of a MOSFET changes significantly, about $\pm20\%$, with N_A, while the temperature coefficient of the threshold voltage changes little, about $\pm2\%$. This is because doping concentration N_A in Eq. (11) is

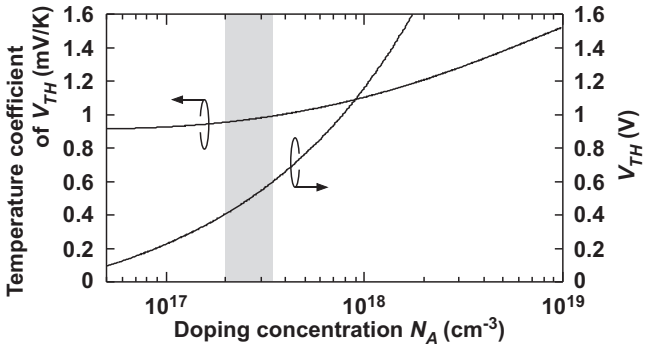

Fig. 2. Calculated TC of threshold voltage $(dV_{TH}/dT = \kappa)$ (left axis) and threshold voltage (V_{TH}) (right axis) as a function of channel doping concentration (N_A).

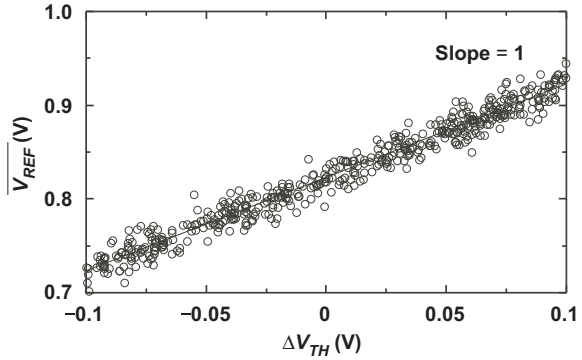

Fig. 3. Scatter plot of the output voltage as a function of D2D threshold voltage variation ΔV_{TH} from 500-point Monte Carlo simulations. The output voltage shows a linear dependence on threshold voltage $\left(\Delta\overline{V_{REF}}/\Delta V_{TH} \approx 1\right)$.

contained in a logarithmic function. Therefore, the variation of N_A is compressed, and the temperature coefficient of the threshold voltage κ has little process dependence. By setting the aspect ratios K in Eq. (8), a constant voltage of a zero temperature coefficient can be obtained.

III. Simulation Results

We confirmed the operation of the circuit by a SPICE simulation with a set of 0.35-μm standard CMOS parameters and a 1.5-V power supply. To verify the stability of the circuit operation with process variations, Monte Carlo analysis assuming both D2D variations (uniform distribution: –0.1 V $< \Delta V_{TH} <$ 0.1 V) and WID mismatch variations (Gaussian distribution: $3\sigma_{V_{TH}}$) in all MOSFETs were considered.

Figure 3 shows the scatter plot of the average output voltage $\overline{V_{REF}}$ in the temperature range of –20 to 80℃ as a function of the D2D variation in threshold voltage ΔV_{TH}. The output voltage shows a linear dependence on the variation of threshold voltage, because the circuit monitors the threshold voltage of MOSFET as shown in Eq. (9). Figure 4 shows the distribution of average output voltage $\overline{V_{REF}}$. The average voltage $\overline{V_{REF}}$ was about 828 mV in this simulations. The coefficient of variation (σ/μ) in 500 runs, which include D2D and WID variations, was 7%.

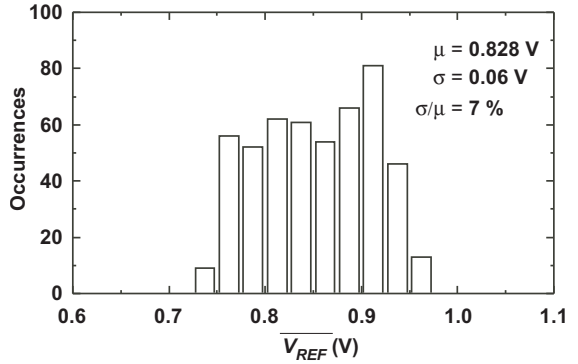

Fig. 4. Distribution of the output voltage with 500-point Monte Carlo simulations assuming both D2D and WID variations.

IV. Experimental Results

We fabricated a prototype chip with a 0.35-μm, 2-poly, 4-metal standard CMOS process. Figure 5 shows a chip micrograph of our prototype chip. The chip area was 0.052 mm^2(=200 μm $\times$ 260 μm). Figure 6 shows measured output voltage V_{REF} as a function of temperature from –20 to 80℃ with different power supply V_{DD}: 1.4, 1.5, 2, 2.5, and 3 V. An almost constant output voltage can be obtained. The average output voltage was about 745 mV. The temperature variation and temperature coefficient were 0.48 mV and 7 ppm/℃, respectively. Figure 7 shows output voltage V_{REF} as a function of power supply from 0 to 3 V at room temperature. The circuit operated correctly with more than 1.4 V power supply. The line sensitivity was 0.002%/V in the supply range of 1.4 to 3 V. A constant reference voltage with little temperature and power supply dependence can be

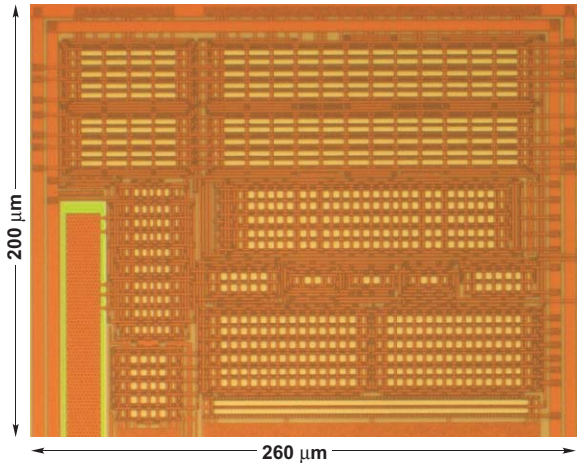

Fig. 5. Chip micrograph.

obtained. The current I_P was extremely low, about 36 nA at room temperature, and the maximum current I_P was 39 nA at 80℃. The total power dissipation of the circuit was 0.3 μW at a 1.5-V power supply and at room temperature.

Table I summarizes the performance of the proposed circuits and compares the performance of reported CMOS voltage

TABLE I

COMPARISON OF REPORTED CMOS VOLTAGE REFERENCE CIRCUITS

	This work	De Vita [7]	Leung [8]	Giustolisi [9]	Huang [10]
Process	0.35-μm, CMOS	0.35-μm, CMOS	0.6-μm, CMOS	1.2-μm, CMOS	0.18-μm, CMOS
Temperature range	–20 - 80℃	0 - 80℃	0 - 100℃	–25 - 125℃	20 - 120℃
V_{DD}	1.4 - 3 V	0.9 - 4 V	1.4 - 3 V	1.2 V	0.85 - 2.5 V
V_{REF}	745 mV	670 mV	309.3 mV	295 mV	221 mV
Power	0.3 μW(@1.5 V) Room temp.	0.036 μW(@0.9 V) Room temp.	29.1 μW(@3 V) Max. temp	4.3 μW(@1.2 V) N.A.	3.3 μW(@0.85 V) Average
TC	7 ppm/℃	10 ppm/℃	36.9 ppm/℃	119 ppm/℃	271 ppm/℃
Line sensitivity	0.002%/V	0.27%/V	0.08%/V	N.A.	0.9%/V
Chip area	0.052 mm^2	0.045 mm^2	0.055 mm^2	0.23 mm^2	0.0238 mm^2

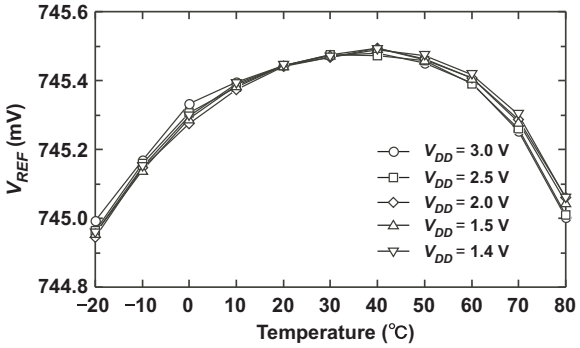

Fig. 6. Measured results of the output voltage V_{REF} as a function of temperature with different power supply.

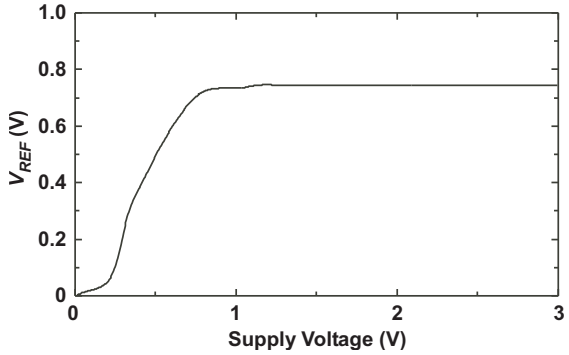

Fig. 7. Measured results of the output voltage V_{REF} as a function of power supply.

reference circuits [7]-[10]. The proposed voltage reference circuit shows the best temperature coefficient and line sensitivity performance compared to the other CMOS voltage reference circuits.

The simulation and measurement results have showed that the effect of the WID mismatch variation can be made small, but that the effect of the D2D process variation of threshold voltage directly affects the output voltage. Therefore, the absolute value of the output voltage changes significantly with process variations. In general, the change in reference voltage is fatal in LSI systems. However, we assume the reference voltage of the circuit as a D2D process variation signal in each LSI chip and, by using the on-chip signal, the reference voltage circuit can be used as an elementary circuit block for on-chip compensation systems such as a robust reference current generator, slew rate compensation techniques in analog buffers, frequency compensation in VCO, and so on.

V. CONCLUSION

A CMOS voltage reference circuit to monitor the process variation in each LSI chip was developed. A prototype chip with a 0.35-μm CMOS process was fabricated and its operation was demonstrated in this paper. The temperature coefficient and line sensitivity were 7 ppm/℃ and 0.002%/V, respectively. The power consumption was extremely low, about 0.3 μW. Because the output voltage changes with the process conditions of threshold voltage in each LSI chip, the circuit can be used as an elementary circuit block for on-chip process compensation systems. The output voltage of the proposed circuit enables us to monitor the D2D variation of each LSI chip.

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