A Sub-1-V, 10 ppm/°C, Nanopower Voltage Reference Generator

Giuseppe De Vita and Giuseppe Iannaccone, *Member, IEEE*

***Abstract*—An extreme low power voltage reference generator operating with a supply voltage ranging from 0.9 to 4 V has been implemented in AMS 0.35-μm CMOS process. The maximum supply current measured at the maximum supply voltage and at 80 °C is 70 nA. A temperature coefficient of 10 ppm/°C is achieved as the combined effect of *1)* a perfect suppression of the temperature dependence of mobility; *2)* the compensation of the channel length modulation effect on the temperature coefficient; and *3)* the absence of the body effect. The power supply rejection ratio without any filtering capacitor at 100 Hz and 10 MHz is lower than −53 and −42 dB, respectively. The occupied chip area is 0.045 mm^2.**

***Index Terms*—CMOS voltage reference, low power, temperature compensation.**

I. Introduction

LOW voltage and extreme low power are essential design requirements for circuits and systems to be deployed in a pervasive electronics scenario, where battery replacement can be very costly or where other energy-scavenging techniques are used. The growing interest for such types of applications drives a robust demand for circuit building blocks operating with low supply voltage and sub-microwatt power. Among them, voltage reference generators are ubiquitous: they are used in almost all analog and digital systems to generate a DC voltage independent of the supply voltage and of temperature variations. In order to ensure compatibility with the rest of the system, they are preferentially implemented with a standard CMOS process. Common solutions entail the use of a bandgap voltage reference, which can be implemented in any standard CMOS technology by exploiting the parasitic vertical BJTs [1], [2]. Bandgap voltage references typically provide a voltage around 1.25 V and therefore require a higher supply voltage. Such constraint can be overcome by using resistive subdivision methods [2] that allow us to reduce the reference voltage, enabling sub-1-V operation.

Other voltage references are based on the availability of transistors with two different threshold voltages in the same CMOS technology. Such feature can be obtained by using a selective channel implant [3], [4], by using different materials for the gate stack [5], or by doping differently the polysilicon gates [6]. Such solutions cannot be implemented in a standard CMOS technology because they require additional fabrication steps.

Other types of voltage references, implemented with a standard CMOS technology, are based on a weighted difference between the gate-source voltages of two MOS transistors [7]–[9] but they cannot usually operate in the sub-1-V regime. Design solutions of this type typically compensate the temperature dependence of the mobility only at the reference temperature, thereby providing a degraded temperature coefficient when the circuit is not at the reference temperature [1], [2], [7], [8]. Moreover, they use one or more resistors, which largely increase the area occupation on silicon.

In this paper, we present a CMOS voltage reference, which exploits the MOS characteristics in the saturation and in the subthreshold regions, able to operate with a supply voltage lower than 1 V and with power consumption lower than 100 nW. The proposed design achieves a complete cancellation of the effects of the temperature dependence of carrier mobility for any temperature. Also, channel-length modulation and body effect are compensated, providing very good temperature compensation.

II. Overview Of CMOS-Based Voltage Reference Circuits

A simplified circuit of a conventional voltage reference generator based on the difference between the gate-source voltages of two MOS transistors is shown in Fig. 1(a) [9]. Both transistors work in the saturation region. The *I–V* characteristic of an nMOS transistor in weak and moderate inversion can be well approximated by the parabolic expression:

$$I_D = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{th})^2(1 + \lambda V_{DS}) \tag{1}$$

where μ is the electron mobility in the channel, C_{ox} is the oxide capacitance per unit area, V_{th} is the threshold voltage, λ is the channel length modulation coefficient, and W and L are the channel width and length, respectively. By using (1) and neglecting the channel length modulation effect ($\lambda = 0$), the reference voltage V_{REF} has the expression shown below [9]:

$$V_{REF} = V_{GS2} - V_{GS1} = V_{th2} - V_{th1} + \sqrt{2I}\left(\sqrt{\frac{1}{k_2}} - \sqrt{\frac{1}{k_1}}\right) \tag{2}$$

where the current I is indicated in Fig. 1(a), subscript i associates any quantity to transistor M_i, and $k_i \equiv \mu C_{ox}(W_i/L_i)$. To reduce the dependence of V_{REF} on the temperature via I and the parameters k_i (through the mobility), a low bias current is used so that $V_{REF} \cong V_{th2} - V_{th1}$. We also need a multiple

Manuscript received October 31, 2006; revised March 1, 2007. This work was supported by the Fondazione Cassa di Risparmio di Pisa.

G. De Vita was with the Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa, I-56122 Pisa, Italy. He is now with Marvell Semiconductor, 27100 Pavia, Italy (e-mail: giuseppe.devita@iet.unipi.it).

G. Iannaccone is with the Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università di Pisa, I-56122 Pisa, Italy (e-mail: g.iannaccone@iet.unipi.it).

Digital Object Identifier 10.1109/JSSC.2007.899077

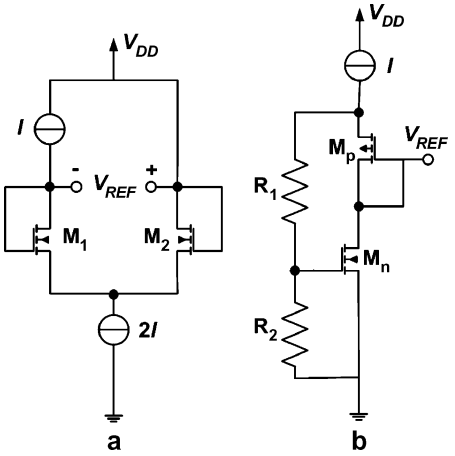

Fig. 1. (a) Simplified circuit of a conventional voltage reference based on the difference between the gate-source voltages of two MOS transistors. (b) Simplified circuit of the voltage reference proposed in [8].

threshold voltage process and good process control to make the temperature coefficients of the two V_{th} as close as possible.

Another design based on the difference between the gate-source voltages of two MOS transistors has been presented in [8] and requires a standard CMOS process. A simplified circuit of such design is shown in Fig. 1(b). The current I, shown in Fig. 1(b), is a PTAT current. By using (1) with $\lambda = 0$, the expression of the reference voltage is

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) V_{GSn} - |V_{GSp}| \tag{3}$$

where R_1 and R_2 are the resistances shown in Fig. 1(b), and V_{GSn} and V_{GSp} are the gate-source voltages of $\mathrm{M_n}$ and $\mathrm{M_p}$, respectively. As shown in [8], the resistance ratio is chosen in order to compensate the temperature dependence of the threshold voltage while the ratios W_i/L_i are chosen in order to compensate the mobility temperature dependence *only at* the reference temperature. As a consequence, notwithstanding the advantage of using a standard CMOS process, the temperature coefficient rapidly degrades when the temperature departs from the reference temperature. A measured temperature coefficient of 36.9 ppm/°C is achieved [8]. Furthermore, the minimum supply voltage is still larger than 1.4 V.

A simplified circuit of a voltage reference, based on a difference between the gate-source voltages of two MOS transistors, that allows us a perfect suppression of the temperature dependence of the mobility is shown in Fig. 2(a) [10]. The current I in Fig. 2(a) is properly generated so that the temperature dependence of the mobility is completely suppressed. Since all transistors in Fig. 2(a) work in the saturation region, by using (1) with $\lambda = 0$, the expression of the reference voltage is

$$\begin{aligned} V_{REF} &= \left(1 + \frac{R_1}{R_2}\right) V_{GS2} - V_{GS1} \\ &= \frac{R_1}{R_2} V_{th} + \sqrt{2I}\left[\left(1 + \frac{R_1}{R_2}\right)\frac{1}{\sqrt{k_2}} - \frac{1}{\sqrt{k_1}}\right] \end{aligned} \tag{4}$$

where I is the bias current of $\mathrm{M_1}$ and $\mathrm{M_2}$. As is clear from (4), the current I must be proportional to $\mu(T)T^2$ in order to compensate for both the temperature dependence of mobility

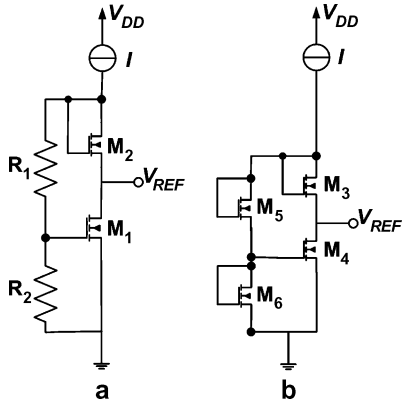

Fig. 2. (a) Simplified circuit of the voltage reference proposed in [10]. (b) Simplified circuit of the voltage reference proposed in [11].

and the negative linear temperature dependence of V_{th}. From (4) one can obtain the ratio R_1/R_2 that provides zero temperature coefficient at any temperature.

Unfortunately, in such design the temperature coefficient degrades due to non-ideal effects, i.e., channel length modulation and body effect. An experimental temperature coefficient of 25 ppm/°C is achieved.

A design solution that provides both a complete suppression of the temperature dependence of mobility and a compensation of non-ideal effects is illustrated in Fig. 2(b) [11]. Since all transistors work in the saturation region, by using (1) with $\lambda = 0$, the expression of the reference voltage is

$$V_{REF} = V_{th} + \left[\frac{1}{\sqrt{k_4}}\left(1 + \sqrt{\frac{W_6/L_6}{W_5/L_5}}\right) - \frac{1}{\sqrt{k_3}}\right]\sqrt{2I}. \tag{5}$$

Again, by generating I [now indicated in Fig. 2(b)] proportional to $\mu(T)T^2$, one can obtain the ratio $(W_6/L_6)/(W_5/L_5)$ that provides zero temperature coefficient of V_{REF} in (5) at all temperatures. If we now consider also the channel length modulation effect, if the previous first-order condition is satisfied, the temperature coefficient of the reference voltage is

$$\frac{\partial}{\partial T} V_{REF} \cong \frac{\lambda}{4} K_{t1}(2V_{th} - V_{REF}) \tag{6}$$

where K_{t1} is the BSIM3v3 threshold voltage temperature coefficient. As is clear from (6), in order to achieve a zero temperature coefficient, the reference voltage must be set to twice the threshold voltage.

If we consider the body effect, the threshold voltage of a MOS transistor can be written as follows:

$$V_{th} = V_{th0} + \gamma\sqrt{\phi_f - V_{BS}} \tag{7}$$

where γ is a process constant, φ_f is the surface potential of the MOS transistor, V_{th0} is the threshold voltage for $V_{BS} = 0$, and V_{BS} is the bulk-source voltage. If the first-order condition for a zero temperature coefficient is satisfied, the temperature coefficient of the reference voltage is

$$\frac{\partial}{\partial T} V_{REF} \cong \frac{\gamma}{2}\frac{\partial \phi_f}{\partial T}\left(\frac{1}{\sqrt{\phi_f - V_{BS5}}} - \frac{1}{\sqrt{\phi_f - V_{BS3}}}\right). \tag{8}$$

In order to achieve a zero temperature coefficient, it is sufficient to ensure that the source terminals of M_3 and M_5 are at the same voltage. In conclusion, thanks to the topology used in [11], channel-length modulation and body effects can be compensated, leading to a very good temperature coefficient of 10 ppm/°C. Unfortunately, the minimum supply voltage is still quite high, that is, larger than 1.5 V, and thus it is not suitable for low-voltage applications.

III. Operating Principle of the Proposed Voltage Reference Generator

In this paper, we present a CMOS voltage reference with a minimum supply voltage smaller than 1 V, really enabling low-voltage operation, and which still provides a very good temperature coefficient thanks to a complete suppression of the temperature dependence of mobility and to the compensation of non-ideal effects.

Let us consider the active load of the proposed reference voltage generator, shown in Fig. 3. Assuming that all transistors of the active load work in the saturation region, the output reference voltage would be given by

$$V_{REF} = V_{th10} + \sqrt{\frac{2I_0}{k_{10}}} \tag{9}$$

where I_0 is the bias current of M_{10}. As is evident from (9), the temperature coefficient of the output reference voltage consists of a first component due to the temperature dependence of the threshold voltage and a second component due to the temperature dependence of mobility and of the bias current. Since k_{10} is proportional to mobility, a bias current proportional to mobility would completely suppress the effect of the temperature dependence of mobility on the output reference voltage.

As a first approximation, we can assume that the threshold voltage of an nMOS transistor linearly decreases with temperature, as shown below:

$$V_{th}(T) = V_{th}(T_0) - K_{t1}(T - T_0) \tag{10}$$

where T is the absolute temperature and T_0 is the absolute temperature at which K_{t1} is evaluated. As a consequence, in order to achieve the temperature compensation with a perfect cancellation of the temperature dependence of mobility at *any* temperature, we need a bias current proportional to mobility and to the temperature squared, that is, $I_0 \propto \mu(T)T^2$. We have found a solution to generate such a current based on MOS transistors operating in the saturation and the subthreshold regions, as will be explained in the next section.

IV. Circuit Description

The proposed voltage reference generator is shown in Fig. 3. A circuit formed by transistors numbered from M_1 to M_8 generates a current I_0 as independent as possible of the supply voltage V_{DD}. Such current is then injected into the diode-connected nMOS transistor M_{10}. The temperature dependence of I_0 is compensated by the temperature dependence of the gate-source voltage of M_{10}, generating a temperature-compensated reference voltage V_{REF}.

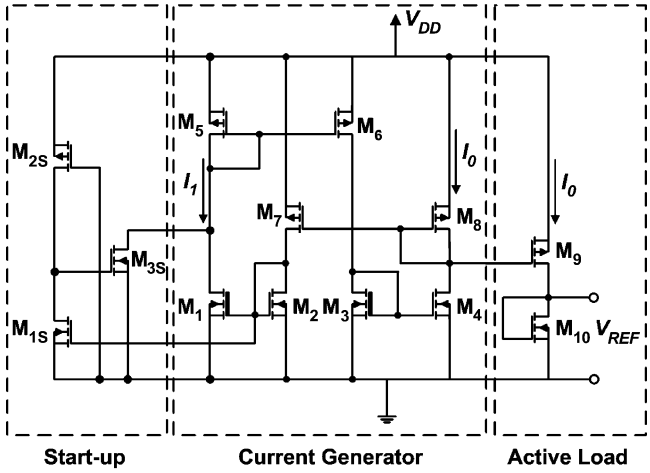

Fig. 3. Proposed voltage reference circuit.

A. Current Generator Circuit

The core of the current generator circuit is represented by transistors M_1–M_4, which determine the value of the current I_0, whereas transistors M_5 and M_6 impose equal current I_1 in M_1 and M_3 and transistors M_7 and M_8 impose equal current I_0 in M_2 and M_4. Transistors M_1 and M_3 (indicated in Fig. 3 with a symbol having a thicker line for the gate) are 5-V nMOS transistors with a threshold voltage of 0.7 V; all the other transistors are 3.3-V MOS transistors with a threshold voltage of 0.498 V and −0.75 V for nMOS and pMOS, respectively. The two different threshold voltages allow us to bias M_1 and M_3 in the subthreshold region and, at the same time, to bias M_2 and M_4 in the saturation region. Such behavior is achieved by setting the gate-source voltages of M_1, M_2 and M_3, M_4 to a value between 0.498 V and 0.7 V. The *I–V* characteristics of an nMOS transistor that operates in the saturation and the subthreshold regions can be approximated by (1) and (10), respectively.

$$I_D = \mu C_{ox} V_T^2 \frac{W}{L} \exp\left(\frac{V_{GS} - V_{th}}{mV_T}\right)\left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{11}$$

where V_T is the thermal voltage and m is the subthreshold slope parameter. In the following, the integer subscript i will be added to quantities referred to transistor M_i. The gate-source voltages of M_1 and M_2 (M_3 and M_4) are identical and can be extracted from (1) and (10) by considering M_1 and M_3 in subthreshold with drain current I_1 and M_2 and M_4 in saturation with a drain current I_0. Then, by enforcing $V_{GS1} = V_{GS2}$ and $V_{GS3} = V_{GS4}$, we have

$$V_{th1} + mV_T \ln\left(\frac{I_1}{\mu C_{ox} V_T^2 W_1/L_1}\right) = V_{th2} + \sqrt{\frac{2I_0}{\mu C_{ox} W_2/L_2}} \tag{12}$$

$$V_{th3} + mV_T \ln\left(\frac{I_1}{\mu C_{ox} V_T^2 W_3/L_3}\right) = V_{th4} + \sqrt{\frac{2I_0}{\mu C_{ox} W_4/L_4}} \tag{13}$$

where we have neglected channel length modulation ($\lambda = 0$) and have set the term between square brackets in (10) to unity. Obviously, since the source terminals of all nMOS transistors are grounded, the body effect plays no role and $V_{th1} = V_{th3}$ and $V_{th2} = V_{th4}$. By subtracting (12) from (13), we can extract the expression of the current I_0:

$$I_0 = \frac{\mu C_{ox} W_4/L_4}{2(N-1)^2} m^2 V_T^2 \ln^2\left(\frac{W_3/L_3}{W_1/L_1}\right) \tag{14}$$

where we have defined $N \equiv \sqrt{(W_4/L_4)/(W_2/L_2)}$.

B. Active Load

The active load consists of a diode-connected nMOS transistor, M_{10}. The current previously generated, given by (14), is then injected into the diode-connected transistor M_{10}, in order to generate a temperature-compensated reference voltage. M_{10} operates in the saturation region and then by using (1) and (14), we can derive the output voltage V_{REF}:

$$V_{REF} = V_{th10} + \frac{mV_T}{N-1}\sqrt{\frac{W_4/L_4}{W_{10}/L_{10}}} \ln\left(\frac{W_3/L_3}{W_1/L_1}\right). \tag{15}$$

The proposed configuration of the voltage reference generator allows us to generate the current I_0 with no resistors, as opposed to what is done in similar circuits [2], [8]. This is particularly important in the case of an ultra-low-power voltage reference generator because a very large resistance would be necessary to generate a very small current I_0 (some tens of nA). As a consequence, the proposed circuit topology allows us to drastically reduce the area occupation on the chip, as will be evident from comparison with the literature.

Since the reference voltage generator has two stable states, corresponding to the current given by (14) and to zero current, a start-up circuit (formed by M_{1S}–M_{3S}) is used to ensure that the former stable state is achieved.

V. Design Considerations

A. Channel Length Modulation Effect

Transistors M_2, M_3, M_5, M_8, and M_{10} are diode-connected, and therefore almost all the variation of the supply voltage drops on the drain-source voltages of transistors M_6, M_7, M_9 of the current mirrors, and on the drain-source voltages of transistors M_1, M_4. As a consequence, in order to drastically reduce the channel length modulation effect, the channel length of all the transistors in the current mirrors and of M_4 must be quite large, and the drain-source voltage of M_1, which operates in the subthreshold region, must be larger than $4V_T$ so that the V_{DS} dependence of the current in (10) becomes negligible.

B. Dimensioning for Minimum Power Consumption

The minimum power consumption of the proposed voltage reference generator and then the minimum acceptable value of the bias current I_0 is imposed by M_2, M_4, and M_{10}, which must operate in the saturation region. By assuming that $W_4/L_4 > W_2/L_2$, if M_4 operates in the saturation region with $V_{GS4} > V_{th4}$, then M2, which has the same drain current, will work in the saturation region as well. In such condition, the minimum current I_0 can be evaluated by imposing that M_4 operates in the saturation region with $V_{GS4} = V_{th4}$. The minimum currents $I_{0\,\min}$ and $I_{1\,\min}$ have thus the following expressions:

$$I_{0\,\min} = \frac{\mu C_{ox} W_2/L_2}{2} m^2 V_T^2 \ln^2\left(\frac{W_3/L_3}{W_1/L_1}\right) \tag{16}$$

$$I_{1\,\min} = \mu C_{ox} V_T^2 (W_3/L_3) \exp\left(-\frac{V_{th3} - V_{th4}}{mV_T}\right). \tag{17}$$

As clear from (16) and (17), in order to achieve small power consumption, we have to choose small values for k_2 and k_3 ($k_{2,3} = \mu C_{ox}(W/L)_{2,3}$). In order to ensure the operation of M_{10} in the saturation region when $I_0 = I_{0\,\min}$, k_{10} must be smaller than k_4.

C. Sensitivity to Process Variations

From (15) we can see that the reference voltage generated by the proposed voltage reference is not process independent, as is usually the case in bandgap references. By neglecting matching errors on W/L ratios in (15), the sensitivity of the reference voltage is mainly due to the accuracy of the threshold voltage of the diode-connected nMOS transistor M_{10}. In order to achieve a low sensitivity to process variations, as typically required in several applications, we have to minimize the variations of the threshold voltage of M_{10}. The statistical distribution of the threshold voltage depends on both process variations and mismatch. Here, process variations are those that affect similarly adjacent transistors, and are due to intra-wafer, inter-wafer, or inter-batch non-uniformity of the process, while mismatch variations are those that cause different properties even in adjacent transistors, such as those due to random dopant fluctuations in the active area, line edge roughness, etc. The effect of process variations on the threshold voltage are not compensated in the present circuit, while those due to mismatch are dominated by random dopant fluctuations and lead to a standard deviation of the threshold voltage inversely proportional to $\sqrt{WL}$ [12]. As a consequence, such variations can be reduced by setting the channel length and width of M_{10} large enough, until mismatch is negligible compared to the effect of process variations.

From Monte Carlo simulations, we obtain that three times the standard deviation of the threshold voltage due to only process variations is 11%. From experiments, instead, we measure a smaller standard deviation either because the model overestimates process variations or because all the measured samples are in the same batch and then inter-batch variations are not considered. In such a way, an acceptable sensitivity to process variations is achieved, as will be shown later. In any case, we have to expect that the standard deviation of the reference voltage generated by the proposed circuit is larger than that of a bandgap reference. On the other hand, bandgap references use one or more operational amplifiers [1], [2], which have a non-negligible power consumption because they have to guarantee a large loop gain, and usually require some resistors, which occupy a large area on silicon. The proposed voltage reference, instead, is a very simple circuit of just 10 transistors, with no operational amplifiers nor resistors, and is therefore very promising in terms of power consumption and area occupation.

VI. Dynamic Range

The minimum supply voltage is imposed by the current generator circuit. In particular, we have to ensure that M_5 operates in the saturation region with $V_{GS5} < V_{th5}$ ($V_{th5} = -0.75$ V) and that M_1 has a drain-source voltage of at least 100 mV so that the V_{DS} dependence of the current in M_1 can be neglected. Consequently, the following expression has to be satisfied:

$$V_{DD} > |V_{GS5}| + V_{DS1MIN}. \tag{18}$$

Then the minimum supply voltage is 0.9 V in the AMS 0.35-μm CMOS process. Such voltage is also sufficient to ensure the operation of M_4 and M_8 in the saturation region. The maximum supply voltage is imposed by the maximum drain-source voltage allowed for MOS transistors, as shown below:

$$V_{DD} < |V_{DS9MAX}| + V_{REF}. \tag{19}$$

Since in the AMS 0.35-μm CMOS process the maximum value for the drain-source voltage of a MOS transistor is 3.3 V, the maximum value of the supply voltage is about 4 V.

VII. Temperature Compensation

The first-order temperature coefficient of the threshold voltage of nMOS transistors in our technology is 0.33 mV/°C. By differentiating (15) with respect to the temperature and taking into account (11), one obtains

$$\frac{\partial V_{REF}}{\partial T} = -K_{tn} + \frac{m}{N-1}\frac{k_B}{q}\sqrt{\frac{W_4/L_4}{W_{10}/L_{10}}}\ln\left(\frac{W_3/L_3}{W_1/L_1}\right) \tag{20}$$

where k_B is the Boltzmann constant and q is the electron charge. As clear from (20), the temperature coefficient is independent of the temperature dependence of the carrier mobility. Indeed, in virtue of the topology used, a perfect suppression of the temperature dependence of the mobility is achieved; this leads to a smaller temperature coefficient over a large temperature range compared to cases in which the temperature dependence of the mobility is compensated only at the reference temperature [8]. By setting (20) to zero, we obtain the condition

$$\sqrt{\frac{W_4/L_4}{W_{10}/L_{10}}} = \frac{K_{tn}(N-1)}{m\frac{k_B}{q}\ln\left(\frac{W_3/L_3}{W_1/L_1}\right)}. \tag{21}$$

Therefore, if (21) is satisfied, we obtain that the temperature coefficient (20) is zero for any temperature. It is clear that this is true within the approximation done in (11) and the simplified transistor characteristics (1) and (10). Such first-order condition for a zero temperature coefficient has been calculated by neglecting any non-ideal effect.

If (21) is satisfied, (15) can be rewritten as $V_{REF} = V_{th10} + T_0 K_{tn}$. At the reference temperature T_0, the long channel threshold voltage of an nMOS transistor in AMS 0.35-μm technology is 0.498 V (the BSIM3v3 parameter Vth0). Since in our design the transistor M_{10} has a medium channel length (L = 1 μm), its threshold voltage V_{th10} increases, due to the effect of lateral pocket implants, to 562 mV. As a consequence, by neglecting other effects on the threshold voltage, the value we expect for the reference voltage is 662 mV, which is very close to the value later obtained from experiments.

A. Non-Ideal Effects on the Temperature Coefficient

1) Channel Length Modulation Effect: In the calculation of the current I_0 in (14) the channel length modulation effect was neglected. In order to take it into account, the *I–V* characteristics of a MOS in the saturation region (such as M_3 and M_4) can be written as in (1) for $\lambda \neq 0$. Since transistors M_1 and M_2 work in the subthreshold region, the channel length modulation effect can be neglected if the drain source voltage is 4 times the thermal voltage. In such condition, using the same procedure used to calculate (14), the current I_0 is

$$I_0 = \frac{m^2 V_T^2 k_4}{2}\left(\frac{1}{N - 1/\sqrt{1+\lambda V_{DS4}}}\right)^2 \ln^2\left(\frac{W_3/L_3}{W_1/L_1}\right). \tag{22}$$

By dimensioning the channel length of M_4 large enough, we can assume that $\lambda V_{DS4} \ll 1$ and use first-order Taylor series expansion to rewrite (22) as

$$I_0 \cong I_{0NOM}\left(1 - \lambda\frac{V_{DS4}}{N-1}\right) \tag{23}$$

where I_{0NOM} is the current I_0 when the channel length modulation effect is neglected ($\lambda = 0$). By using (9) and (23) and by using again first-order Taylor series expansion, the reference voltage can be rewritten as

$$V_{REF} = V_{REF0} - (V_{REF0} - V_{th10})\frac{\lambda}{2}\frac{V_{DS4}}{N-1} \tag{24}$$

where V_{REF0} is the reference voltage calculated for $\lambda = 0$ and given by (15). The drain-source voltage $V_{DS4} = V_{DD} - |V_{GS8}|$ of M_4 can be expressed by

$$V_{DS4} = \left[V_{DD} - |V_{thp}| - (V_{REF0} - V_{th})\sqrt{\frac{W_{10}/L_{10}}{W_8/L_8}}\right] \times \left[1 + \frac{\lambda}{2}\frac{(V_{REF0} - V_{th})}{N-1}\sqrt{\frac{W_{10}/L_{10}}{W_8/L_8}}\right] \tag{25}$$

where V_{thp} is the threshold voltage of a pMOS transistor. By substituting (25) in (24), by assuming that (21) is satisfied, the temperature coefficient of the reference voltage has the following expression:

$$\frac{\partial V_{REF}}{\partial T} = -\frac{\lambda K_{tn}}{N-1}\left[V_{DD} - |V_{th8}| - (V_{REF0} - V_{th10}) \times \left(2\sqrt{\frac{W_{10}/L_{10}}{W_8/L_8}} - \frac{K_{tp}}{K_{tn}}\right)\right] \tag{26}$$

where K_{tp} is the threshold voltage temperature coefficient of a pMOS transistor and second-order terms have been neglected. By equating (26) to zero, we can derive the value of $(W_{10}/L_{10})/(W_8/L_8)$ that allows us to achieve a zero temperature coefficient as

$$\sqrt{\frac{W_{10}/L_{10}}{W_8/L_8}} = \frac{K_{tp}}{2K_{tn}} + \frac{V_{DD} - |V_{th8}|}{2(V_{REF0} - V_{th10})}. \tag{27}$$

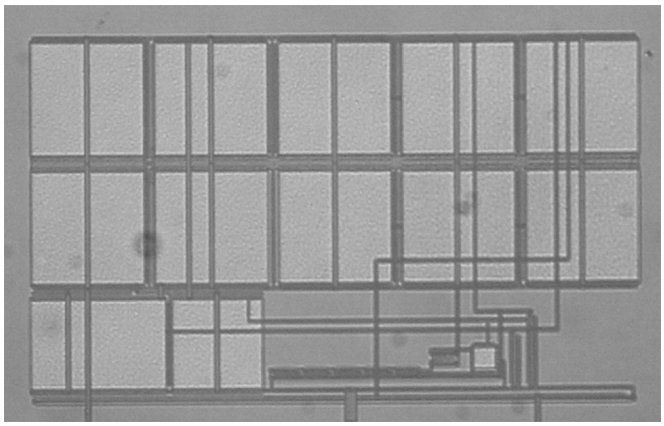

Fig. 4. Die photograph of the voltage reference generator (core).

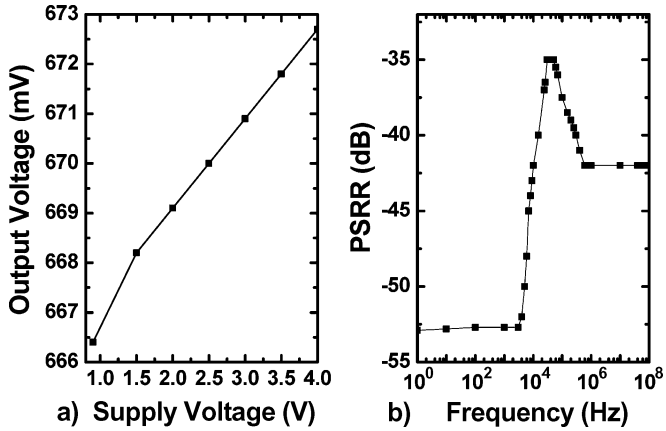

Fig. 5. Experiments: (a) Output voltage versus supply voltage at room temperature; (b) PSRR at room temperature and for a supply voltage of 2 V.

Equation (27) has been calculated for a value of V_{DD} in the middle of the supply voltage range ($V_{DD} = 2.45$ V). From (27), it is evident that if $V_{DD} > 2.45$ V, the temperature coefficient is negative, otherwise is positive.

2) Body Effect: In the proposed voltage reference there is no body effect because the bulk terminals of all nMOS transistors are grounded and the bulk terminals of all pMOS transistors are connected to the supply voltage V_{DD}.

Thanks to the topology used and to proper dimensioning, channel-length modulation and body effect are compensated, leading to a very good temperature coefficient. As in the design proposed in [11], we expect a low temperature coefficient with the advantage that the proposed voltage reference allows sub-1-V operation.

VIII. Experimental Results

The proposed voltage reference has been implemented with AMS 0.35-μm CMOS process. The die photograph is shown in Fig. 4. Measurements show that the proposed voltage reference generates a mean reference voltage of about 670 mV with a variation of 5.67 mV at room temperature, when the supply voltage varies from 0.9 V to 4 V, as shown in Fig. 5(a). The power supply rejection ratio, without any filtering capacitor, is -47 dB at 100 Hz and -40 dB at 10 MHz, for the smallest supply voltage. At larger supply voltage, the power supply rejection ratio decreases to -53 dB at 100 Hz and to -42 dB at 10 MHz, as shown in Fig. 5(b). Fig. 6 shows the output voltage dependence on temperature for different values of the supply voltage. The measured temperature coefficient at $V_{DD} = 2$ V and $V_{DD} = 3$ V is 10 ppm/°C and 13 ppm/°C, respectively, and increases to 18 and 20 ppm/°C at $V_{DD} = 4$ V and $V_{DD} = 0.9$ V, respectively, corresponding to the maximum and minimum supply voltage. At 80 °C, the current drawn at the maximum supply voltage is 70 nA and at the minimum supply voltage is 50 nA. At room temperature, instead, the current drawn at the maximum supply voltage is 55 nA and at the minimum supply voltage is 40 nA. The current drawn from the supply voltage as a function of the supply voltage for different values of the temperature is shown in Fig. 7. In order to evaluate the sensitivity of the reference voltage to process variations, 20 different samples of the same batch have been tested: the mean

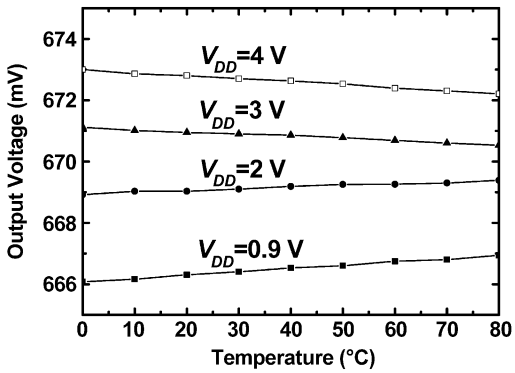

Fig. 6. Measured output voltage versus temperature for four values of the supply voltage.

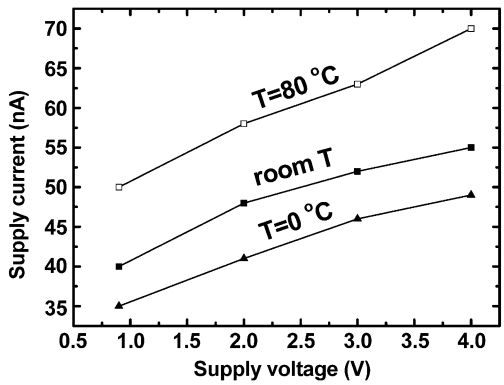

Fig. 7. Current drawn from the supply voltage versus supply voltage for different values of the temperature.

value of the reference voltage is 670 mV and the standard deviation is 3.1%. As expected, the standard deviation is worse than that of a bandgap reference, which usually is in the order of 1% [1], [2]. The occupied chip area is 0.045 mm^2. A comparison with best performing published voltage reference circuits fabricated with a standard CMOS process is shown in Table I. It can be noted that the proposed voltage reference has the smallest temperature coefficient, the minimum supply voltage, and by large the smallest power consumption, in the tens of nW range. The power supply rejection ratio (PSRR) and the line sensitivity

TABLE I
COMPARISON WITH VOLTAGE REFERENCE GENERATORS AVAILABLE IN THE LITERATURE

	This work	Leung et al. [8]	Leung et al. [2]	De Vita et al. [10]	De Vita et al. [11]
Technology	0.35 µm CMOS	0.6 µm CMOS	0.6 µm CMOS	0.35 µm CMOS	0.35 µm CMOS
Supply Voltage (V)	0.9 to 4	1.4 to 3	0.98 to 1.5	1.5 to 4.3	1.5 to 4.3
Supply Current (µA)	0.04@0.9V 0.055@4V	<9.7	<18	1.5@1.5 V 2.4@4.3V	0.08@1.5 V 0.11@4.3V
V_{ref}	670 mV	309.3mV	603 mV	168 mV	891.1 mV
TC (ppm/°C)	10	36.9	15	25	12
Line Sensitivity	0.27 %/V	0.08 %/V	0.73 %/V	0.95 %/V	0.46 %/V
PSRR @100 Hz @10 MHz	V_{DD}=0.9 V -47 dB -40 dB	V_{DD}=1.4 V -47 dB -20 dB	V_{DD}=0.98 V -44 dB -17 dB	V_{DD}=1.5 -65 dB -57 dB	V_{DD}=1.5 -59 dB -52 dB
Die area (mm^2)	0.045	0.055	0.24	0.08	0.015

are comparable to other solutions already presented in the literature. Moreover, from Table I we can see that the power consumption and the area occupation on the chip of the proposed voltage reference are much smaller, by several orders of magnitude in the case of the power consumption and by more than one order of magnitude in the case of the area occupation on the chip, than those of the bandgap reference proposed in [2].

IX. CONCLUSION

A low-voltage, extreme low-power voltage reference generator implemented in AMS 0.35-μm CMOS has been presented. The design conditions to minimize the power consumption and the temperature coefficient have been described in detail. The complete suppression of the temperature dependence of mobility in a wide temperature range, the compensation of the channel length modulation effect on the temperature coefficient, and the elimination of the body effect have allowed us to obtain a very small temperature coefficient of 10 ppm/°C. The minimum supply voltage of only 0.9 V and the maximum quiescent current of only 70 nA leads to a total absorbed power in the decananowatt range, which makes the circuit very attractive for nanopower applications.

ACKNOWLEDGMENT

The authors wish to thank Prof. P. Bruschi for help in the characterization.

REFERENCES

[1] B. S. Song and P. R. Gray, "A precision curvature-compensated CMOS bandgap reference," *IEEE J. Solid-State Circuits*, vol. SC-18, no. 6, pp. 634–643, Dec. 1983.
[2] K. N. Leung and P. K. T. Mok, "A sub-1-V 15 ppm/°C CMOS bandgap voltage reference without requiring low threshold voltage device," *IEEE J. Solid-State Circuits*, vol. 37, pp. 526–530, Apr. 2002.
[3] R. A. Blauschild, P. A. Tucci, R. S. Muller, and R. G. Meyer, "A new nMOS temperature stable voltage reference," *IEEE J. Solid-State Circuits*, vol. SC-13, no. 6, pp. 767–774, Dec. 1978.
[4] H. Tanaka, Y. Nakagome, J. Etoh, E. Yamasaki, M. Aoki, and K. Miyazawa, "Sub-1 μA dynamic reference voltage generator for battery-operated DRAMs," *IEEE J. Solid-State Circuits*, vol. 29, no. 4, pp. 448–453, Apr. 1994.
[5] M. C. Tobey, D. J. Gialiani, and P. B. Askin, "Flat-band voltage reference," U.S. Patent 3,975,648, Aug. 17, 1976.
[6] H. J. Oguey and B. Gerber, "MOS voltage reference based on polysilicon gate work function difference," *IEEE J. Solid-State Circuits*, vol. SC-15, no. 3, pp. 264–269, Jun. 1980.
[7] K. N. Leung, P. K. T. Mok, and K. C. Kwok, "CMOS voltage reference," U.S. Patent 6,441,680, Aug. 27, 2002.
[8] K. N. Leung and P. K. T. Mok, "A CMOS voltage reference based on weighted ΔV_{GS} for CMOS low-dropout linear regulators," *IEEE J. Solid-State Circuits*, vol. 38, no. 1, pp. 146–150, Jan. 2003.
[9] B.-S. Song and P. R. Gray, "Threshold-voltage temperature drift in ion-implanted MOS transistors," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 2, pp. 291–298, Apr. 1982.
[10] G. De Vita and G. Iannaccone, "An ultra-low-power, temperature compensated voltage reference generator," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, San Jose, CA, 2005, pp. 751–754.
[11] G. De Vita, G. Iannaccone, and P. Andreani, "A 300 nW, 12 ppm/°C voltage reference in a digital 0.35-μm CMOS process," in *Symp. VLSI Circuits Dig. Tech. Papers*, Honolulu, HI, 2006, pp. 81–82.
[12] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York: McGraw Hill, 2001, pp. 463–465.

Giuseppe De Vita received the Laurea *cum laude* in electrical engineering from the University of Pisa, Italy, in 2003. In 2003, he was with TU Delft, The Netherlands, working on the design of a UWB transceiver. From 2004 to 2006, he was with the University of Pisa as Ph.D. student, working on the design of low-voltage and low-power integrated circuits for passive RFID transponders, with particular focus on voltage reference and regulator.

In 2005, he was with Technical University of Denmark, Lyngby, working on the design of a low-power and low-voltage EEPROM. He is currently with Marvell Semiconductor, Pavia, Italy, working on analog ICs for power management.

Giuseppe Iannaccone (M'98) received the M.S.E.E. and Ph.D. degrees in electrical engineering from the University of Pisa, Italy, in 1992 and 1996, respectively.

In 1996, he took a permanent position as a Researcher with the Italian National Research Council, and in the same year he obtained a faculty position with the Electrical Engineering Deparment of the University of Pisa, first as an Assistant Professor, then, since January 2001, as an Associate Professor of electronics. His research interests include transport and noise in nanoelectronic and mesoscopic devices, development of device modeling and TCAD tools, and the design of extremely low-power circuits and systems for RFID and ambient intelligence scenarios.

Dr. Iannaccone has coordinated European and national projects involving multiple partners, and has acted as Principal Investigator in several research projects funded by public agencies at the European and national level, and by private organizations. He has authored or co-authored more than 110 papers published in peer-reviewed journals and more than 70 papers in proceedings of international conferences. He is on the technical committee of some international conferences and serves as a referee for leading journals in the fields of condensed matter physics, device electronics, and circuit design.