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PAPER

An Ultra Low-Voltage Ultra Low-Power CMOS Threshold Voltage Reference

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SUMMARY This paper describes a CMOS voltage reference that makes use of weak inversion CMOS transistors and linear resistors, without the need for bipolar transistors. Its operation is analogous to the bandgap reference voltage, but the reference voltage is based on the threshold voltage of an *n*MOS transistor. The circuit implemented using 0.35 μm n-well CMOS TSMC process generates a reference of 741 mV under just 390 nW for a power supply of only 950 mV. The circuit presented a variation of 39 ppm/°C for the −20°C to +80°C temperature range, and produced a line regulation of 25 mV/V for a power supply of up to 3 V.

key words: *threshold voltage, voltage reference, ultra low-power, ultra low-voltage*

1. Introduction

Voltage references are widely used in analog and mixed-mode circuits, such as A/D and D/A converters, voltage regulators, PLLs and others. These voltage references are required to be stable despite variations in temperature, power supply and fabrication process [1]. In CMOS technology, the most common voltage references are based on the bandgap voltage, which is obtained through parasitic bipolar transistors [1]–[3]. The bandgap voltage is dependent on the semiconductor material and it suffers almost no changes with doping. Unfortunately, the major limitation faced by the ultra low voltage circuits is the power supply voltage. For silicon, the bandgap voltage is approximately 1.12 eV at room temperature [1], [2] that limits the minimum power supply voltage of the entire circuit to a higher value. In the last few years researchers have been working to develop circuits capable of working under 1 V. In some new 0.13 μm CMOS processes the power supply is not higher than 1.2 V [4]. Efforts have also been made to develop bandgap reference voltages capable of working at such low voltage [3], [5]–[12], and circuits based on MOS transistors [13]–[19] which are generally very complex and may present undesirable behavior (such as startup oscillations, second order temperature compensation) and high power consumption.

In this paper, we describe a new and simple topology that provides an accurate voltage reference operating on a supply voltage lower than the bandgap value, but having similar stability for temperature and process variations.

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2. Gate-Source Voltage V_{GS} versus Temperature in Weak Inversion

The drain current I_{DS} of an MOS transistor in weak inversion is based on the channel diffusion current and can be given by Eq. (1), when referred to source voltage [20]–[22]. I_S is the characteristic current, T the absolute temperature, n the slope factor in weak inversion, k the Boltzmann constant and q is the charge of the electron (or the hole). This expression is consensus among the BSIM3v3 [20], ACM [21] and EKV [22] models.

$$I_{DS}(T) = I_S(T)\left(\frac{W}{L}\right)\exp\left(q\frac{V_{GS}-V_{TH}(T)}{nkT}\right)\cdot\left[1-\exp\left(-q\frac{V_{DS}}{kT}\right)\right] \quad (1)$$

The characteristic current I_S is, among other factors, proportional to the square of thermal voltage kT/q and the carrier electrical mobility μ [20]–[22], which in turn is dependent on the temperature. Therefore, the characteristic current I_S, as a function of the temperature, can be given by (2), where α is a process dependent parameter that relates the characteristic current to the temperature [1], [2], including the effects of temperature given by the thermal voltage and electric mobility.

$$I_S(T) \propto \mu(T)\left(\frac{kT}{q}\right)^2 \quad I_S(T) = I_S(T_o)\left(\frac{T}{T_o}\right)^{\alpha} \quad (2)$$

An MOS transistor in weak inversion is considered saturated when the drain-source voltage V_{DS} is larger than $3kT/q$ [22]. Based on Eq. (2) and considering that the transistor saturated, the drain current can be referenced to a given temperature T_o as given by Eq. (3) where the room temperature T_o is considered 27°C.

$$I_{DS}(T) = I_{DS}(T_o)\left(\frac{T}{T_o}\right)^{\alpha}\cdot\exp\left(q\frac{V_{GS}(T)-V_{TH}(T)}{nkT} - q\frac{V_{GS}(T_o)-V_{TH}(T_o)}{nkT_o}\right) \quad (3)$$

The threshold voltage can be referenced to a room temperature T_o through a first order relationship given by Eq. (4), where the coefficient θ depends mainly on the substrate doping and it is valid for the −80°C to +130°C temperature range [1], [2], [23].

$$V_{TH}(T) = V_{TH}(T_o) - \theta(T - T_o) \tag{4}$$

Equation (3) can be rewritten with the aid of Eq. (4) in order to derive an expression for gate-source voltage V_{GS} as a function of the temperature, as given by Eq. (5).

$$V_{GS}(T) = (V_{TH}(T_o) + \theta T_o)\left(1 - \frac{T}{T_o}\right) + V_{GS}(T_o)\left(\frac{T}{T_o}\right) + n\frac{kT}{q}\ln\left[\left(\frac{T_o}{T}\right)^{\alpha}\frac{I_{DS}(T)}{I_{DS}(T_o)}\right] \tag{5}$$

Observe that Eq. (5) is similar to the expression of base-emitter voltage V_{BE} as a function of the temperature for a bipolar transistor [1], [3], [18], where the threshold voltage is analogous to the bandgap voltage [1].

Therefore, the V_{GS} voltage of an MOS transistor in weak inversion has an almost linear behavior that decreases with the temperature, since the logarithmic part suffers little variation and the V_{GS} voltage is always smaller than the threshold voltage for weak inversion. The term dependent on the temperature can be minimized by the implementation of a PTAT (proportional to absolute temperature) biasing circuit, and therefore the voltage reference can be given by a well defined value: the MOS threshold voltage.

The threshold voltage is a fixed value for a CMOS process, but strongly dependent on doping [2], [23]; and thus is not known in advance. Nevertheless, depending on the process variation, this value can be considered known under the dispersion provided by the fabrication corners [4].

3. Composite Transistor in Weak Inversion

Before the implementation of a PTAT biasing circuit, it is necessary to define the concept of a composite transistor; which provides some of the desired PTAT biasing circuit features. The structure of a composite transistor is shown in Fig. 1(a) for an *n*MOS transistor. Consider that the transistors are implemented in individual wells, thus eliminating the body effect through the source-substrate of each transistor [24].

The analysis is also valid for the *p*MOS transistor. Figure 1(b) shows the symbol of the composite *n*MOS transistor. The expressions of current and voltage of the composite transistor can be derived directly from Fig. 1(a), and are given by Eq. (6).

$$I_{DSa} = I_{DSb} \quad V_{DSa} = V_{GSa} \tag{6}$$

Based on Eq. (1), that relates transistor voltage and current, and considering that the drain-source voltage applied is enough to saturate transistor Q_b, then V_{DSa} as proposed by Eq. (6) is given approximately by Eq. (7). Since the transistors are implemented in individual wells [24], an analytic solution is not possible. This expression is a function of the transistor sizes and the CMOS process parameters, valid for weak inversion only and independent of the transistor's gate-source voltage. Therefore, a variation in V_{DSb} does not affect V_{DSa}, so it is kept constant by a cascode effect [24].

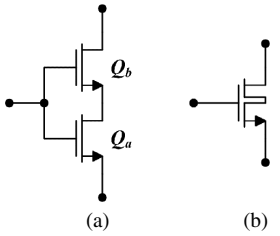

Fig. 1 Composite transistor: (a) schematic and (b) symbol.

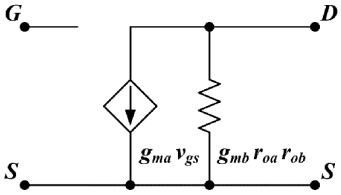

Fig. 2 Simplified small-signal model.

Another important conclusion is that voltage V_{DSa} is PTAT by the composite configuration, and therefore it is used in the implementation of the biasing circuit.

$$V_{DSa} \approx \frac{kT}{q}\ln\left(1 + \left(\frac{(W/L)_b}{(W/L)_a}\right)^n\right) \tag{7}$$

In order to maintain weak inversion saturation of Q_a, it is sufficient that $V_{DSa} \geq 3kT/q$ [22]. Once the voltageV_{DSa} is PTAT, the dimensions of the transistors required for saturation are given by Eq. (8). Observe that the drain-source voltage for saturation does not depend on the gate-source voltage and temperature. This is the basis of the composite transistor, which is valid only for weak inversion operation and not for strong inversion.

$$\left(\frac{W}{L}\right)_b \geq \left(\frac{W}{L}\right)_a \sqrt[n]{e^3 - 1} \tag{8}$$

The simplified small-signal model of transistor Q_b in saturation is given in Fig. 2. It is possible to observe an increase in the output impedance, even though the current in the composite transistor is still the same as in transistor Q_a. Thus the output resistance is multiplied by the gain of a common-gate amplifier, thus becoming larger than that of a single transistor.

Therefore, the composite transistor proposed presents a better approximation to the ideal transistor, and of an ideal current source.

4. The Proposed Voltage Reference Circuit

The proposed topology for the voltage reference is presented in Fig. 3. This topology is based on the bandgap voltage reference presented by Tzanateas [3], [18]. Transistors Q_1 and Q_3 are in fact composite transistors operating in weak inversion, whose properties are given in Sect. 3. Instead of a parasitic transistor at the output, this topology makes use of transistor Q_4 of the lower current mirror, also in weak inversion. Resistors R_1 and R_2 are placed in such a way

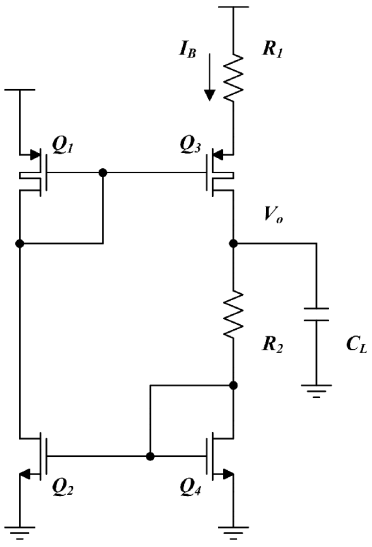

Fig. 3 Voltage reference circuit.

to make a connection to source-bulk of all transistors, and therefore eliminating the body effect of all transistors of the voltage reference circuit.

A biasing current I_B (PTAT) is generated through transistors Q_1, Q_2, Q_3 and Q_4, and resistor R_1. According to Fig. 3, the drain-source current of Q_1 is equal to Q_2, and drain-source current of Q_3 is equal to Q_4. Since the transistors are working in saturated weak inversion and voltages V_{DS1a} and V_{DS3a} are PTAT voltages, the bias current I_B is given by Eq. (9), which is a function of the size of the devices and the process parameters, where n_p is the slope factor of the pMOS transistor.

$$I_B(T) = n_p \frac{kT}{q} \frac{1}{R_1(T)} \cdot \ln\left(\frac{(W/L)_2}{(W/L)_4} \frac{(W/L)_{3a}}{(W/L)_{1a}} \frac{1 + \left(\frac{(W/L)_{1a}}{(W/L)_{1b}}\right)^{n_p}}{1 + \left(\frac{(W/L)_{3a}}{(W/L)_{3b}}\right)^{n_p}} \right) \quad (9)$$

Observe that the bias current I_B is PTAT but suffers distortion due to the resistor temperature coefficient. A poly or a diffusion resistor presents a linear dependence on the temperature [1], [25], as given by Eq. (10), where φ is the temperature coefficient, that depends on the CMOS process.

$$R(T) = R(T_o)[1 + \varphi(T - T_o)] \quad (10)$$

The biasing current I_B can be referenced to a temperature, as given by Eq. (11). Considering that the resistor has a small variation with the temperature (even in the considered temperature range), the biasing current has an almost linear variation with the temperature, which is highly desirable for implementation of a voltage reference circuit.

$$I_B(T) = I_B(T_o)\left(\frac{T}{T_o}\frac{1}{1 + \varphi(T - T_o)}\right)$$
$$I_B(T) \approx I_B(T_o)\left(\frac{T}{T_o}\right) \quad (11)$$

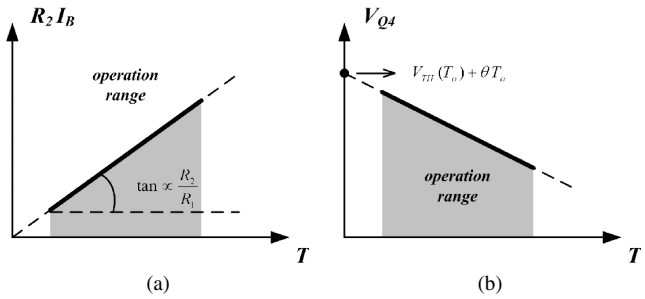

Fig. 4 Thermal voltage behavior of (a) $R_2 I_B$ and (b) V_{Q4}.

The voltage drop at resistor R_2 and transistor Q_4 generates the output voltage V_o, given by Eq. (12), where V_{Q4} is the gate-source voltage of the diode connected transistor Q_4.

$$V_o(T) = R_2(T) I_B(T) + V_{Q4}(T) \quad (12)$$

By taking Eq. (11) into Eq. (5), the voltage V_{Q4} can be expressed as given by Eq. (13), which is a function of the temperature and independent of the amount of PTAT biasing current, where n_n is the slope factor of the nMOS transistor.

$$V_{Q4}(T) = (V_{TH}(T_o) + \theta T_o)\left(1 - \frac{T}{T_o}\right) + V_{Q4}(T_o)\left(\frac{T}{T_o}\right) + (1 - \alpha) n_n \frac{kT}{q} \ln\left(\frac{T}{T_o}\right) \quad (13)$$

From Eqs. (9) and (12), the voltage V_o can be given by Eq. (14), which is a function of the devices dimensions and the CMOS process parameters. Observe that voltage V_o is independent of the exact value of resistors R_1 and R_2, but on their ratio, thus providing robustness to the structure despite of process variations.

$$V_o(T) = n_p \frac{kT}{q} \frac{R_2(T_o)}{R_1(T_o)} \ln\left(\frac{(W/L)_2}{(W/L)_4} \frac{(W/L)_{3a}}{(W/L)_{1a}} \frac{1 + \left(\frac{(W/L)_{1a}}{(W/L)_{1b}}\right)^{n_p}}{1 + \left(\frac{(W/L)_{3a}}{(W/L)_{3b}}\right)^{n_p}} \right) + V_{Q4}(T) \quad (14)$$

According to Eq. (14), the first term increases linearly with the temperature, as depicted in Fig. 4(a). The second term of $V_o(T)$, given by Eq. (13) tends to decrease linearly with the temperature (although there is a small distortion due to logarithmic terms inherent to V_{Q4}), as indicated in Fig. 4(b). Those conclusions of linearity are valid for a limited operation range, whereas outside there is just an extrapolation of the mathematical model.

Depending on the dimensions adopted for resistors and transistors, there will be a condition where the temperature dependence over V_o will be minimized. The minimum dependence on the temperature is achieved when the temperature coefficient of the first term of Eq. (14) is the sane as the temperature coefficient of the second term, given by Eq. (15).

$$\frac{R_2(T_o)}{R_1(T_o)} \ln\left(\frac{(W/L)_2}{(W/L)_4} \frac{(W/L)_{3a}}{(W/L)_{1a}} \frac{1+\left(\frac{(W/L)_{1a}}{(W/L)_{1b}}\right)^{n_p}}{1+\left(\frac{(W/L)_{3a}}{(W/L)_{3b}}\right)^{n_p}} \right) = q\frac{V_{TH}(T_o)+\theta T_o - V_{Q4}(T_o)}{n_p k T_o} - (1-\alpha) \quad (15)$$

Once the optimization is achieved, then the voltage V_o is given by the threshold voltage and a few process dependent parameters as shown in Eq. (16).

$$V_o(T) = V_{TH}(T_o) + \theta T_o - (1-\alpha) n_n \frac{kT}{q}\left[1 - \ln\left(\frac{T}{T_o}\right)\right] \quad (16)$$

It should be observed that the coefficient α is larger than 1 for bipolar transistor and smaller than 1 for MOS transistors in weak inversion. Therefore the reference voltage has a convex shape for the first case and a concave shape for the second case. At room temperature, the reference voltage V_o is given by Eq. (17).

$$V_o(T_o) = V_{TH}(T_o) + \theta T_o - (1-\alpha) n_n \frac{kT_o}{q} \quad (17)$$

Finally, capacitor C_{db} of transistor Q_2, and the other parasitic capacitances at that node provide the circuit start up [26]. A sharp variation at the power supply turns on transistor Q_1, thus reestablishing the bias point after any transient. Therefore this topology does not require any additional start up circuitry. Transitions are an inherent condition at power up.

4.1 Line Regulation Model

Line regulation is a figure of merit that shows the output voltage variation due to a variation in the power supply voltage. This dependence is related to the channel length modulation effect that occurs in saturation [27], [28]. Based on that, Eq. (1) can be rewritten as Eq. (18), in which coefficient λ models the channel length modulation.

$$I_{DS} = \frac{I_S}{1-\lambda V_{DS}} \left(\frac{W}{L}\right) \exp\left(q\frac{V_{GS}-V_{TH}}{nkT}\right) \quad (18)$$

Consequently, the PTAT biasing current given by Eq. (9) can be rewritten as Eq. (19), considering the channel length modulation effects.

$$I_B(T) = n_p \frac{kT}{q}\frac{1}{R_1(T)} \ln \left(\frac{(W/L)_2}{(W/L)_4} \frac{(W/L)_{3a}}{(W/L)_{1a}} \frac{1+\left(\frac{(W/L)_{1a}}{(W/L)_{1b}}(1-\lambda_p V_{DS1b})\right)^{n_p}}{1+\left(\frac{(W/L)_{3a}}{(W/L)_{3b}}(1-\lambda_p V_{DS3b})\right)^{n_p}} \frac{1-\lambda_n V_{DS4}}{1-\lambda_n V_{DS2}} \right) \quad (19)$$

The drain-source voltages of transistors Q_{1a} and Q_{3a} are stable and they depend only on the dimensions of the composite transistor, but do not change despite of power supply variations, due to the cascode composite transistor effect [24]. This reduces the bias current sensitivity to power supply variations, when compared to a single transistor implementation. Consequently, this effect is transferred to the output voltage, as given by Eq. (12), thus improving significantly the line regulation of the proposed voltage reference circuit. The line regulation can be given by Eq. (20), in its dominant linear behavior.

$$\frac{\partial}{\partial V_{DD}} V_o(T) \approx n_p \frac{kT}{q}\frac{R_2(T_o)}{R_1(T_o)} \left(\lambda_n + \frac{n_p}{1+\left(\frac{(W/L)_{3b}}{(W/L)_{3a}}\right)^{n_p}} \lambda_p \right) \quad (20)$$

It can be observed from Eq. (20) that the *n*MOS transistors should be larger than the *p*MOS transistors. The larger the size ratio of transistors that comprise the composite transistor Q_3, the shorter they will have to be. It is worth stressing that the composite transistors Q_1 and Q_3 increase the output impedance seen by the power supply, thus increasing the circuit PSSR as compared to a single transistor configuration.

5. Simulations and Measurements

A bias current of 240 nA was adopted for the design of a voltage reference source and Table 1 lists the transistors dimensions. In every case V_{GS} is smaller than V_{TH} to assure weak inversion operation [4], [27] for the 0.35 μm n-well CMOS TSMC process. Basically, only the resistor values must be calculated. Resistor R_1 is obtained from Eq. (9) and resistor R_2 from Eq. (15). By using linear regression, it is possible to find the value of the threshold voltage as a function of the temperature for the BSIM3v3 model [27].

According to Eq. (20), for a line regulation of 25 mV/V (a specification adopted for this design), the channel length modulation coefficients are $\lambda_n = 0.021\,V^{-1}$ and $\lambda_p = 0.143\,V^{-1}$ [4], [27], and consequently the channel lengths are 16 μm and 2 μm for *n*MOS and *p*MOS respectively. According to Eq. (8) transistor Q_{1b} should be eight times larger than transistor Q_{1a}. The values of the circuit elements are listed in Table 1.

Weak inversion operation implies large transistor dimensions, which in turn minimizes the influence of noise, mainly the flicker noise that is dominant in an MOS transistor at low frequency [1], [2]. Diffusion resistors are used in this work because they have better matching and provide larger resistivity than poly resistors [25]. The resistor used presents the temperature coefficient $\varphi = 1.4\,m°C^{-1}$, thus assuring the approximation given by Eq. (11). The

Table 1 Values of the circuit elements.

$(W/L)_{1a}$	160µm/2µm	$(W/L)_4$	120µm/16µm (6x)
$(W/L)_{1b}$	160µm/2µm (8x)	$R_1(T_o)$	130KΩ
$(W/L)_2$	120µm/16µm (3x)	$R_2(T_o)$	1570KΩ
$(W/L)_{3a}$	160µm/2µm (5x)	I_B	240nA
$(W/L)_{3b}$	160µm/2µm (16x)	V_{DD}	950mV

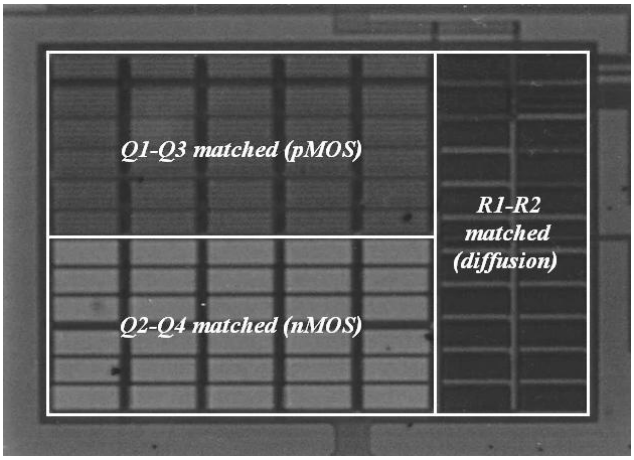

Fig. 5 Micrograph of the voltage reference circuit.

Table 2 Corner simulations (after trimming).

	Typical	Best Case	Worst Case
Minimum Power Supply	950mV	850mV	1050mV
Biasing Current	245nA	240nA	249nA
Temperature Range	− 20°C to + 80°C	− 20°C to + 80°C	− 20°C to + 80°C
nMOS Threshold Voltage	524.7mV	424.7mV	624.7mV
Power Dissipation @ 80°C	380nW	335nW	430nW
Voltage Reference	735.7mV	633.3mV	835.9mV
Temperature Coefficient	39.3ppm/°C	55.0ppm/°C	33.5ppm/°C
Line Regulation @ 1.5V	22.6mV/V	21.8mV/V	21.7mV/V
PSRR @ 1kHz	25.1dB	28.5dB	24.6dB

micrograph is shown in Fig. 5 and it occupies an area of $330\,\mu\text{m} \times 230\,\mu\text{m}$.

The results of the corner simulations are shown in Table 2. The values were obtained after individually trimming the resistors by using a set of four bits, for a room temperature of 27°C and minimum power supply voltage.

Figure 6 shows the results the DC simulation (full line) and the measurements of three samples (dots) for the reference voltage variation against temperature. The values were measured after the individual trimming of each resistor, where the same trimming is applied to the three samples. Nevertheless, it is different from the trimming used during the simulation phase.

The circuit promotes a reference voltage of 736 mV for the typical case, which is very close to the *n*MOS threshold voltage at absolute zero for the $0.35\,\mu$m n-well CMOS TSMC process. As predicted, the curve presents a concave shape for temperature variation.

In order to evaluate the circuit robustness due to parameter variation a series of simulations was conducted by considering a channel width variation of $\pm 1\,\mu$m for each transistor individually to evaluate the mismatch effects over the trimmers' adjustment. The trimmers were capable of compensating for the mismatch effects on the reference voltage for all corners listed in Table 2.

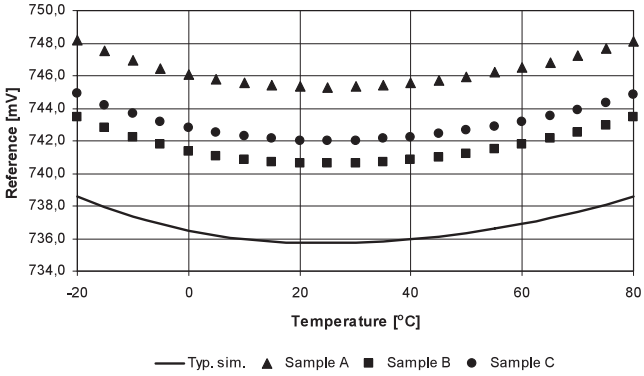

Fig. 6 Reference voltage against temperature.

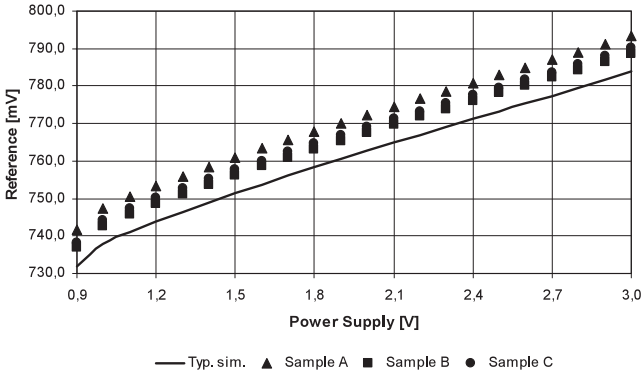

Fig. 7 Reference voltage against power supply voltage.

Figure 7 shows the DC simulation (full line) and the sample measurements (dots) for a reference voltage variation against power supply voltage. The transistors channel lengths are in accordance with the line regulation model. The results of the measurements conducted in the three samples are summarized in Table 3, for a room temperature of 27°C and minimum power supply voltage.

The circuit presents a variation of less than 4 mV in the reference voltage for the range of −20°C to +80°C. The circuit consumes only 390 nW which is less than those found in the literature. The power supply rejection ratio is 22.8 dB, which is comparable to the bandgap voltage references [3], [5]–[7]. Table 4 shows a list of measured voltage reference benchmarks. Properties of the circuit presented in Fig. 3 are shown in the first column along with other works for comparison.

The proposed threshold voltage reference circuit can operate at a minimum power supply voltage of 800 mV in a standard $0.25\,\mu$m CMOS process, generating a reference voltage in 580 mV. The circuit is capable of operating at 700 mV minimum voltage in a standard $0.18\,\mu$m CMOS pro-

Table 3 Results of the measurements in three samples.

	Sample A	Sample B	Sample C
Minimum Power Supply	950mV	950mV	950mV
Biasing Current	~ 250nA	~ 250nA	~ 250nA
Temperature Range	− 20°C to + 80°C	− 20°C to + 80°C	− 20°C to + 80°C
Power Dissipation @ 80°C	~ 390nW	~ 390nW	~ 390nW
Voltage Reference	745.3mV	740.6mV	742.0mV
Temperature Coefficient	39.0ppm/°C	38.8ppm/°C	40.1ppm/°C
Line Regulation @ 1.5V	24.1mV/V	24.4mV/V	24.7mV/V
PSRR @ 1kHz	23.4dB	23.7dB	22.8dB

Table 4 Voltage reference performance benchmark indicators.

	This work	[14]	[15]	[16]	[17]
CMOS Technology	0.35µm	0.60µm	1.20µm	0.35µm	0.18µm
Minimum Power Supply	0.95V	1.40V	1.20V	1.40V	0.85V
Temperature Range	–20°C to 80°C	0°C to 100°C	–25°C to 125°C	0°C to 70°C	–20°C to 120°C
Voltage Reference	741mV	309mV	295mV	580mV	221mV
Temperature Coefficient	39 ppm/°C	37 ppm/°C	119 ppm/°C	62 ppm/°C	194 ppm/°C
Power Dissipation	0.39µW	13.58µW	4.32µW	3.22µW	3.30µW

cess, providing a reference voltage of 510 mV. It also can run with just 600 mV in a standard 0.13 μm CMOS process, providing a reference voltage of 405 mV. Lower values are due to the process lower threshold voltages. These values were obtained using BSIM3v3 model and the typical values listed for the process [4].

Under process variations, the voltage reference can change within the limits presented by the corner simulations [4], as presented in Table 2. In order to eliminate the influence of the threshold voltage V_{TH} variations on the reference voltage V_o, a trimming circuit can be used to adjust the reference voltage V_o to any reference voltage V_{ref} within the power supply range. It can be accomplished by using an operational amplifier in a negative feedback loop as shown in Fig. 8, where R_a is a trimmable resistor.

The ratio of the resistors defines the output voltage value. By including the circuit presented in Fig. 8, the new voltage reference V_{ref} can be given by Eq. (21).

$$V_{ref} = \left(1 + \frac{R_a}{R_b}\right) V_o \tag{21}$$

Observe that the voltage reference V_{ref} now depends on

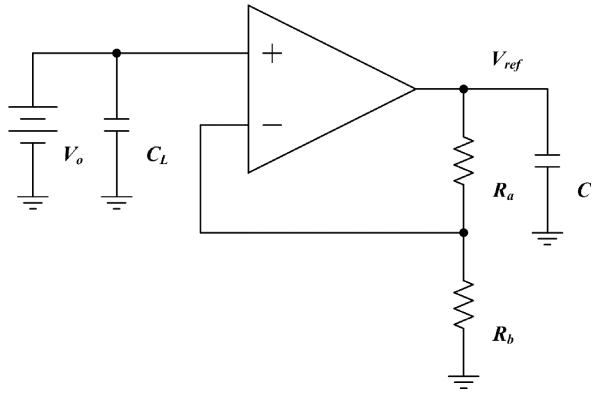

Fig. 8 Operational amplifier with a negative feedback.

a resistor ratio which is stable against temperature and process, and thus maintain the original threshold voltage reference properties. Nevertheless, it can be adjusted, thus eliminating the influence of the absolute value of V_{TH} over V_{ref}. The swing of the operational amplifier is not critical since the input and output voltage swings are well defined and the frequency response is given by a voltage reference circuit. It is desirable an ultra low voltage and low temperature coefficient topology for the operational amplifier, in order to maintain these features in the whole voltage reference circuit; one of such circuit topology is presented in [28]. This configuration allows the correction of threshold voltage due to process variations, so that the properties of the threshold voltage reference becomes very close to the bandgap reference. In fact, the circuit of Fig. 8 is also used in bandgap based circuits, in order to raise or reduce (tap in resistor R_b) the voltage reference value, or even to correct DC errors in the elements of the circuit.

6. Conclusions

This work described a weak inversion CMOS voltage reference for ultra low-voltage and ultra low-power applications without the need for bipolar transistors. Its operation is similar to the bandgap voltage reference, but is capable or working at less than 1 V supply voltage, which is well below the limit of silicon bandgap voltage. The circuit implemented in 0.35 μm n-well CMOS TSMC process can work at 950 mV supply voltage and provides a reference voltage of 741 mV, which corresponds to the threshold voltage extrapolated to the absolute zero. The reference voltage varied only 39 ppm/°C for the temperature range of −20°C to +80°C and a line regulation of 25 mV/V for a power supply voltage of up to 3 V. In newer process technologies, such as in 0.13 μm CMOS process, the power supply voltage is below the bandgap value, thus making the use of bandgap references difficult [4]. This is not a problem for the threshold voltage reference proposed in this work. The proposed reference circuit can possibly be further improved by compensating for the logarithmic dependence on temperature.

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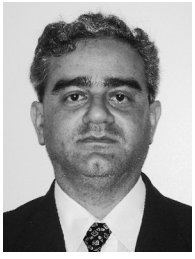

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