Middle East Technical University

Electrical-Electronics Engineering

EE 414 – Introduction to Analog Integrated Circuits

Tutorials

UMC 180 nm Layout

TABLE OF CONTENTS

1. BASICS OF LAYOUT DRAWING

Till now, you designed your circuit and simulated it in the virtual environment. In order to convert your design to real world, you need to draw the layout of it. Layout drawing is not as easy as drawing wires in the schematics because you need considering the real (physical) structure of the circuit. Do not forget that, layout drawing is quite important and it is a job title in the VLSI design centers.

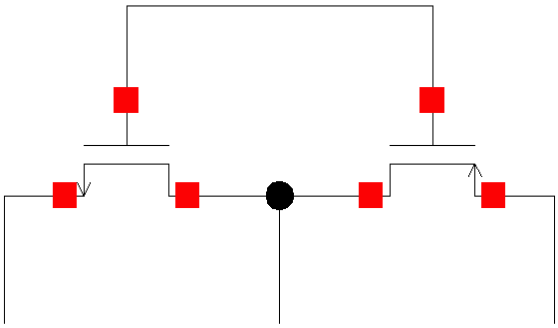
This tutorial is quite important. Although all the steps here will be lectured by your assistant, try to understand by yourself first in order to gain time.

1.1. What is LAYOUT?

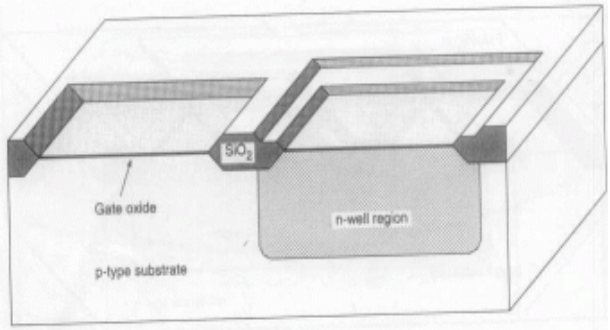
Layout is the drawings of masks used during the fabrication of the CMOS chips. Masks are kinds of filters used to shape various layers. Each layer in CMOS fabrication, like Polysilicon layer or metal layer, are shaped with a different mask. Considering our purpose as the designer, we have the ability to change very restricted number of variables during design. For instance we cannot change the thickness of the oxide layer in the gate, but we can change the width of the gate. During layout drawing, we will consider only the width and length of a metal layer, not the thickness.

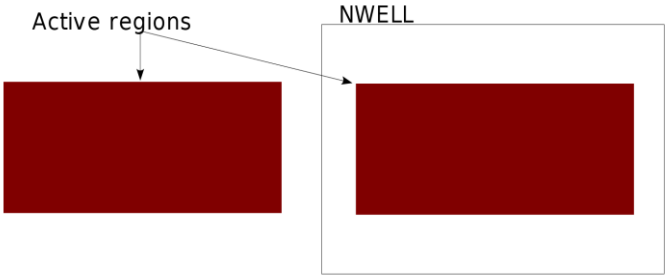
1.2. CMOS Process and Layout Drawing Step by Step

In this part, we will consider the steps of layout drawing of a CMOS inverter seen in the figure on the right. Do not forget that, the CMOS process steps are much more complex than the ones we will consider in this part. We are skipping many steps since we do not care much about them as the designer. At each step, the physical structure and the layout corresponding to this physical structure are given, and then the process is explained.



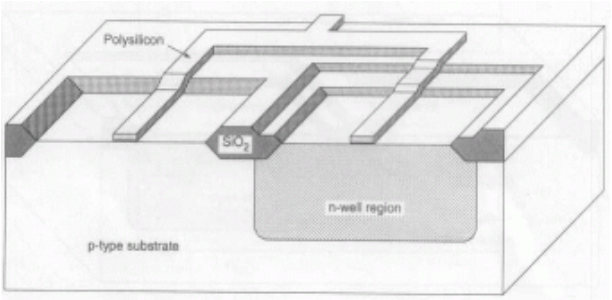
1.2.1. Step 1 –Active Regions and Wells

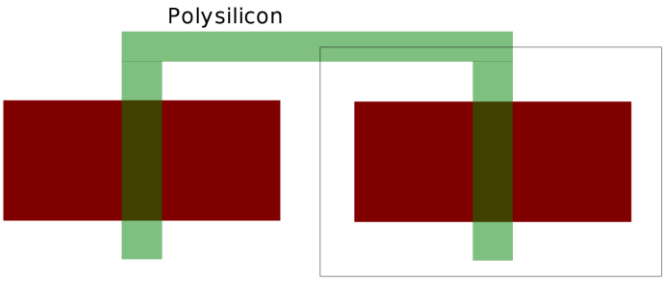




Let's start the CMOS process flow. We have a p-type substrate with single well technology, which means that NMOS transistors are implemented on p-type substrate, and PMOS transistors are implemented on NWELLs. Nwells are the n-type doped regions as seen in the figure above. Normally, front sides of the wafers are initially covered with very thick SiO_2 layer (or Si_3N_4 layer) except the regions where some active elements, like the transistors, will be implemented. A mask is used to shape these openings, which are called as **Active Regions**. And one mask is used to shape the Nwell region. So, two layers are drawn in the layout.

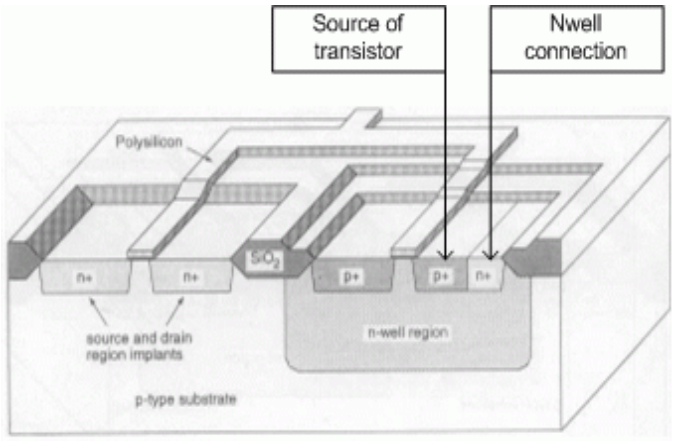
1.2.2. Step 2 - Polysilicon

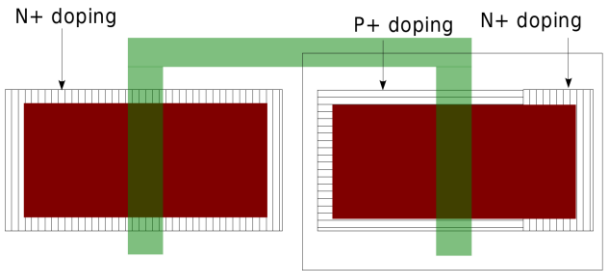




Next step is to grow and shape polysilicon layers, which will form the gate of the transistor. For this purpose, we need to draw one mask only, which is colored as red.

1.2.3. Step 3 – N+ and P+ Diffusion

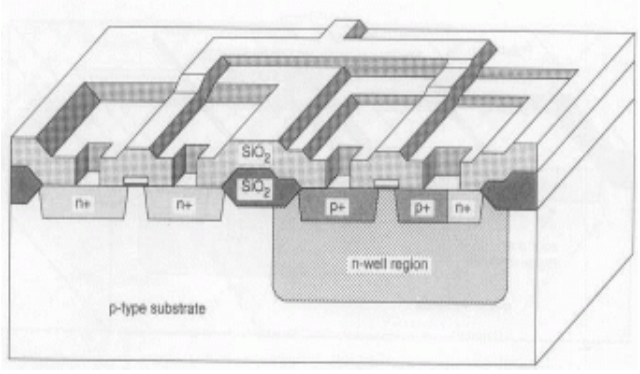


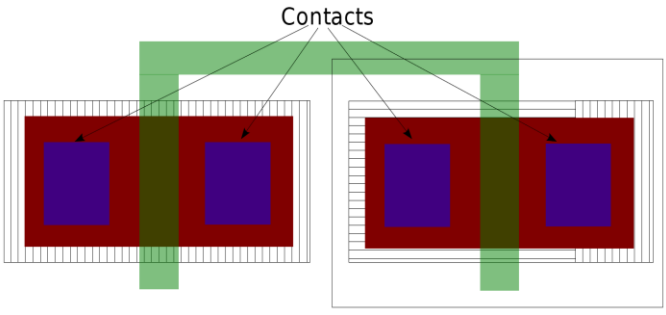


In this step, n+ and p+ regions will be doped. Doping is done on entire wafer surface. Since SiO2 and PolySilicon do not pass dopands (or impurities) to the substrate, these regions are not doped. First, a mask is used to determine the regions to be doped with p+ impurities. After p+ doping, the rest of the surface is doped by n+ dopands. So, only one mask is used.

One important point should be stated here. Nwell regions should be biased to high potential and p-substrate should be biased to lowest potential in order to minimize the leakage current on the diode formed by Nwell and p-substrate. For this purpose, a structure like the figure above is used, where the Nwell is biased with the same potential to the p+ region on the left. Note that, contact to the Nwell should be n+ in order to decrease schottky effect. See the p+ doping region mask on the right.

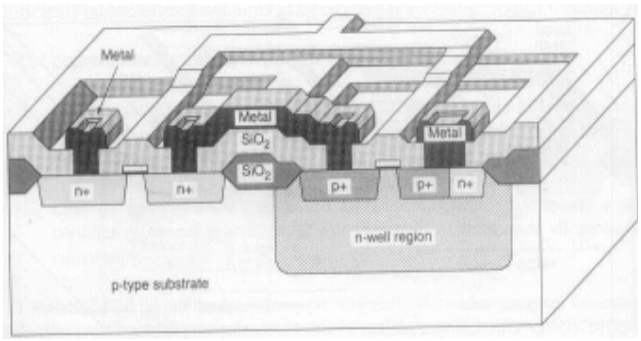
1.2.4. Step 4 - Contacts

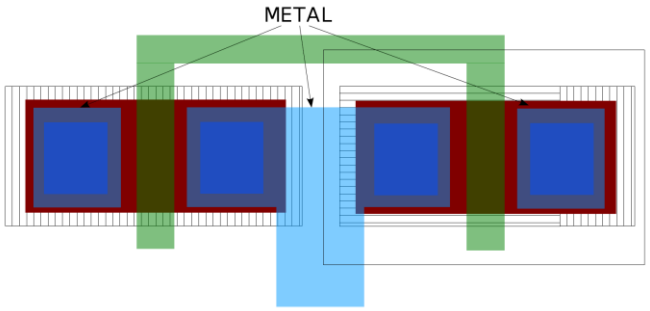




As the next step, the entire wafer surface is again covered by a thick oxide layer in order to prevent the shorts between the substrate and metal layer deposited in the next steps. In order to take connection to the substrate, one should use contacts, which are openings in the oxide layer. There are 3 different contacts and we will learn those later on. This contact is the first one and it connects the substrate to the metal layer (metal layer is not shown here, it will be grown in the next step).
Oxide layer is grown to the whole wafer surface and then the contacts are etched away. So, only contact openings should be masked as seen on the right.

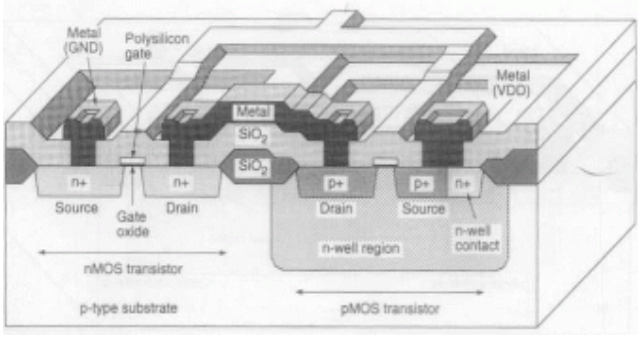
1.2.5. Step 5 – Metal Deposition

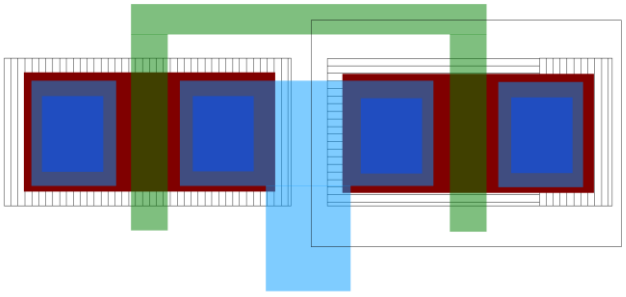




We are almost done with the process. The metal layer is grown and shaped in this step. Note that, the metals where a contact exists touches to the substrate.

1.2.6. Final View





This is it. The process is completed and our layout is ready. As you see, layout is somehow similar to the top view of a chip. Make sure that you understood every step here. Do not hesitate to ask questions, this tutorial is quite important.
Remember the definition of the layout stated at the beginning of the tutorial. It is combination of masks used during the process of the chip. So as the designer, you give the shapes of the layers that you want, and the process engineer produces the corresponding chip for you. As the designer point of view, you do not really care about the thickness of the layers, but you care only the shape of the layers. So you are in a 2-D world.

2. LAYOUT DRAWING USING CADENCE

In the previous part, layout drawing basics are given. In this tutorial, the layout will be drawn using Cadence. At the end of the tutorial the design will be checked in order to verify the physical structure of the drawn layout.

2.1. Design Rules

In this laboratory, UMC 180nm Low Power, 6 Metal 1 Poly NWELL process will be used (UMC_18_CMOS). Each technology has its own layout drawing design rules, and they should be satisfied for successful production. Design Rule Check (DRC) tools are used to determine whether the design rules are satisfied or not.

The following parts summarize the short descriptions of the layers firstly, and then give the most important design rules.

2.1.1. Layers

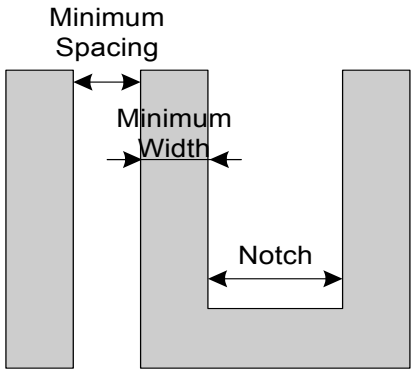
There are a number of layers to be used in the layout view. Most of these layers and abbreviated names are summarized below:

- **NWEL** represents nwell
- **DIFF** represents "active" layer, active layers are regions on which transistors can be grown
- **P01** represents the gate poly layer, which is used for constructing gates of transistors, it is also used as a conductor
- **PPLUS** represents p+ doping region
- **NPLUS** represents n+ doping region
- **CONT** represents openings in oxide, which are used to get contacts between different layers like activemetal, polymetal
- **ME1-6** represents the metal layers which are the main conducting path for routing. Since there are six metal layers, and they are isolated with oxide, six different conduction paths routed with different metals can cross over each other.
- **VI1** represents an opening in oxide between Metal 1 and Metal 2, hence connecting Metal 1 and Metal 2. Similar for VI2 to VI5.
- **VTPL** defines the 1.8V low Vt PMOS devices.
- **VTPHL** defines the 3.3V low Vt PMOS devices.
- **VTP** defines the 1.8V PMOS devices.
- **VTN** defines the 3.3V NMOS devices.
- **VTNL** defines the 1.8V low Vt NMOS devices.
- **VTNHL** defines the 3.3V low Vt NMOS devices

2.1.2. Design Rules Overview

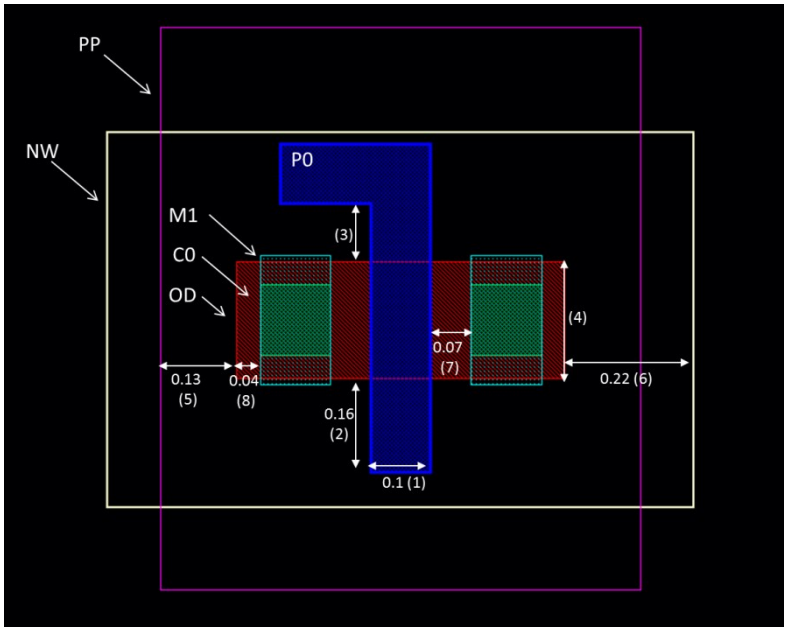
The table below shows the design rules for various layers. Minimum width shows the minimum producible width of the layers. Spacing and notch similarly show the minimum spacing and notch spaces of the layers.

LAYER	MIN. WIDTH (µM)	SPACING (µM)	NOTCH (µM)
NWEL	0.9	0or 0.9	0.9
DIFF	0.24	0.28	0.28
P01	0.18	0.28	0.28
CONT	0.24	0.26	0.26
ME1	0.24	0.24	0.24
ME2-5	0.28	0.28	0.28
ME6	0.44	0.44	0.44
VI1-5	0.28	0.28	0.2



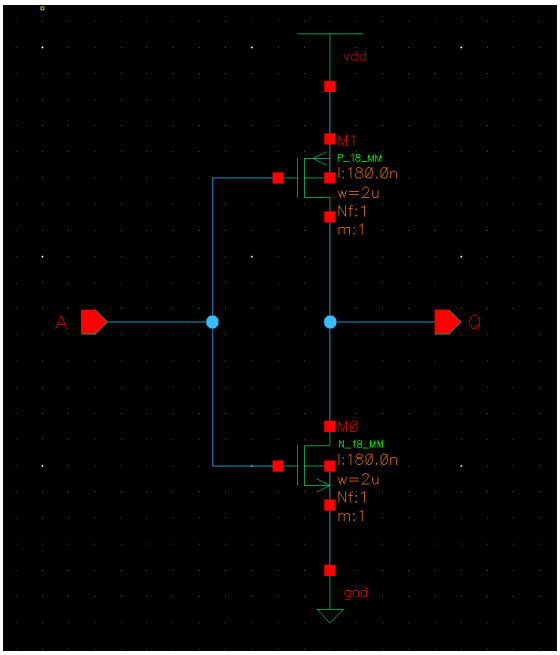
Further design rules are stated below which are required for drawing a transistor. At the moment, you may not understand all of the rules here. You will get all of these rules while drawing the layout of the inverter. The figure below illustrates the design rules.

1. Minimum GATE length 0.18 µ
2. Minimum P01 extension of GATE 0.22 µ
3. Minimum ACTIVE – P01 spacing 0.2 µ
4. Minimum GATE width 0.24 µ
5. Minimum PPLUS extension of ACTIVE 0.22 µ
6. Minimum NWEL extension of ACTIVE 0.24 µ
7. Minimum DIFFUSION CONTACT to GATE spacing 0.15 µ
8. Minimum ACTIVE extension of DIFFUSION CONTACT 0.1 µ



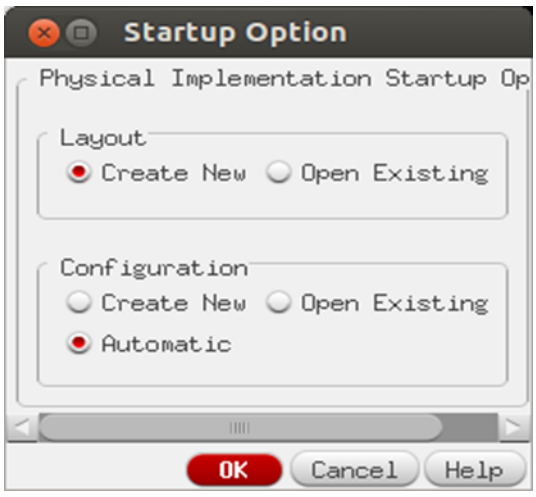
2.2. Layout of the Inverter

After you finalized the schematic design of the inverter you can continue with the layout of your design. Figure below shows the schematic of a CMOS inverter which was created in “EE414” library with cellview name “inv”.



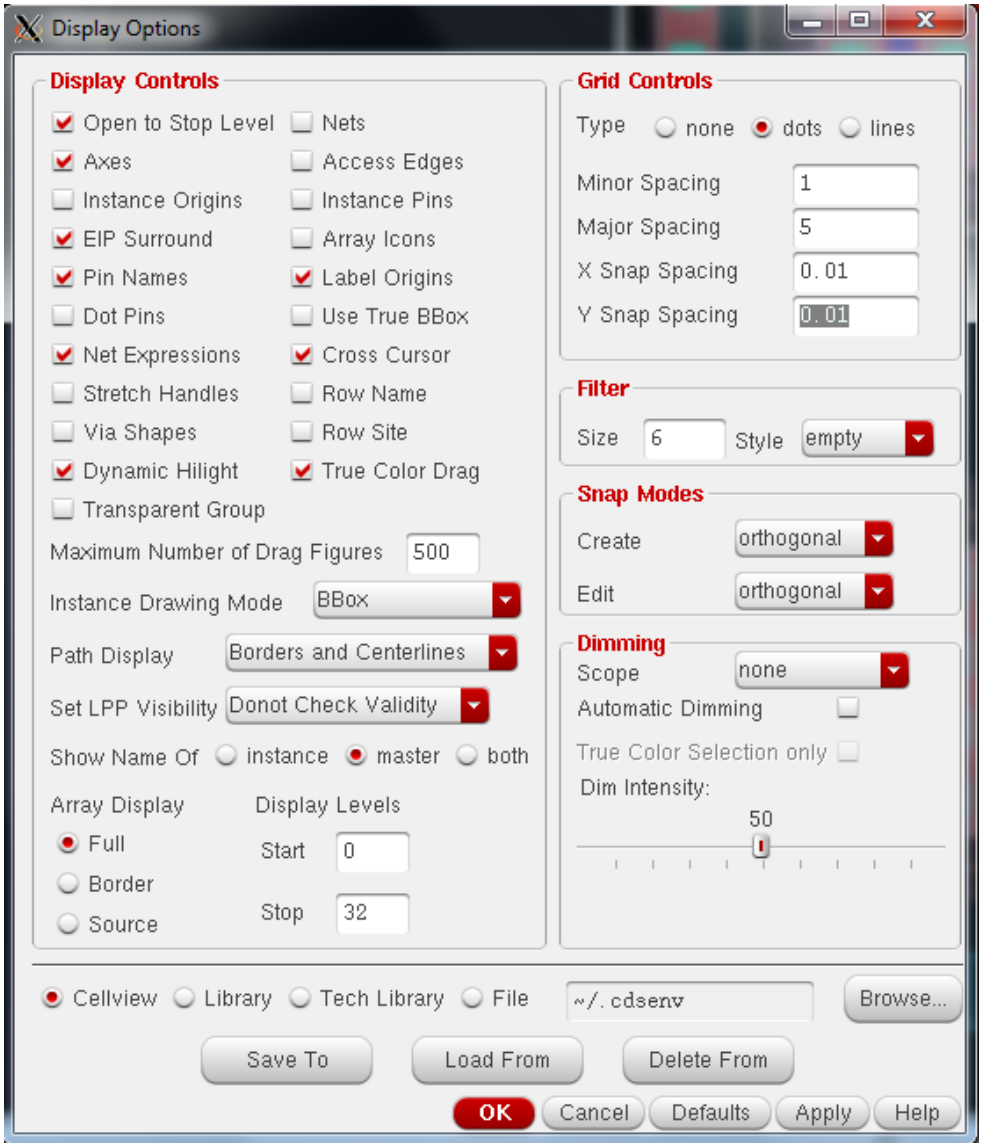
1 . Open the file manager window (It may be minimized, but should still be open). Click on the library, then on the inv. This should show schematic and symbol. If you just double click on schematic, it will open a lower level schematic editor. For most work, you should use the XL version of the editor. To get this editor, right click on the schematic, and then use <open with>. In the Application area, click on the red down arrow, and select schematics XL. You can click “always use this application for this type of file”, but it doesn't seem to remember it all the time. Click OK. The schematic editor will appear.

2 . Click <launch>, and <layout XL>. The following will pop up:



Make sure “Create New” is selected, and click OK. Make sure the cell is inv in the next pop-up window, and click OK. If any “Upgrade License” window pops up, select 'Yes' and continue. After a moment, you should have a screen that contains the schematic on one side, and the layout on the other side. On the very top of the layout window the title bar should say “Virtuoso Layout Suite XL Editing: EE414 inv layout”.

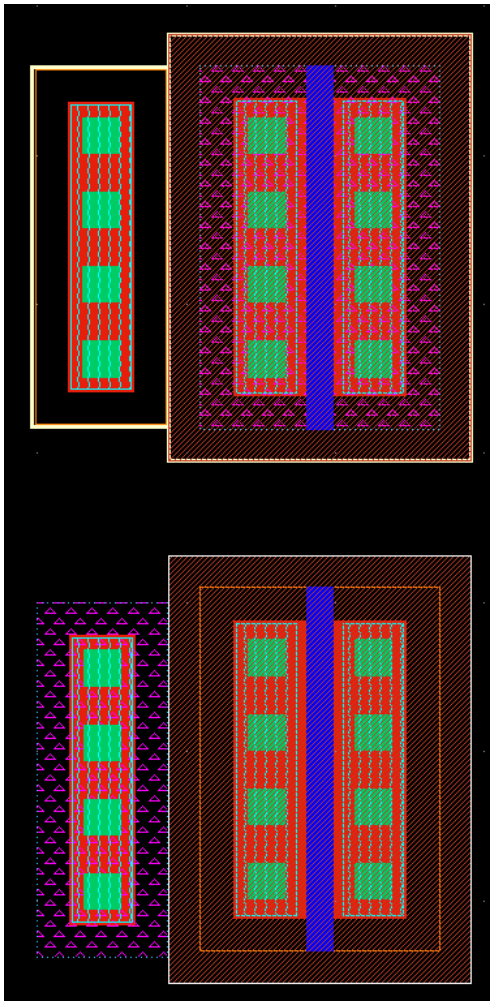
3 . In the layout, you will only see frames of the layout cells, but not the details. Let's fix this: From the Virtuoso <Options> menu, choose <Display> to open up the window shown below. Set “Display Levels Stop” to 10. Virtuoso works with the placement grid, which is specified in the “Grid Controls” menu. In our case, the objects are placed on a 10nm grid. Generally, the grid is about 5-10% of the minimum feature size (180nm for our technology). In the “Display Controls”, you can selectively choose which objects will be visible in the layout. Now click OK.



Now we can start drawing the layout of the inverter.

3. For transistor placement you can use add instance like the one in the schematic case but you should choose layout as the view of the component. Width, length and other properties of the transistor can be changed in this window, or you can leave default (minimum) sizes for the time being and change them later. You may also add a specific name (m1, m2, etc.) for your transistor. If not, a name will be assigned for you. You can now hide the “Add Instance” window by clicking on Hide below. Move to the schematic editor, and insert one NMOS transistor (N_18_MM). Do the same thing for "P_18_MM" cell, and insert one PMOS transistor. Since you are building an inverter, put PMOS transistor to the top for better readability. The device properties can be changed in the property editor. (Device sizes, names, etc). For our case we use 2 µm and 0.18 µm as width and length of both NMOS and PMOS transistors.

4. Another point is the bulk connections. As you know, transistors are 4 terminal devices. The 4th terminal of an NMOS transistor is the p-substrate, while that of PMOS transistor is the N-well. Since all the wafer is (hence all the transistors are) built on the same substrate, all NMOS transistors must have the same bulk terminal, which is the most negative voltage level in the circuit: ground, so you should consider threshold variation effects for transistors whose most negative terminals are connected to voltages other than ground. Similarly all the transistors in the same N-well have one common bulk terminal (usually VDD). However, one can place isolated N-wells and can have different bulk voltages for isolated PMOS transistors. Although this is possible, it is usually impractical to place isolated wells, since they should be placed apart from each other.
5. We will also place one other contact for the bulk. In order to bypass Schottky diode effects (metal to silicon direct connection), one should dope the silicon to guarantee a resistive contact (also consider latch-up). For an nMOS transistor, bulk connection is made to the p-substrate, so we should dope the active layer with P+ for a resistive contact; similarly for a PMOS transistor, bulk connection is made to the N-well, so we should dope the active layer below the contact with N+. Remember the discussion above (PPLUS layer is implemented with a positive mask, while NPLUS layer is implemented with a negative mask), you can conclude that we have to draw a PPLUS layer around the bulk contact for an NMOS transistor and NPLUS layer around the bulk contact for a PMOS transistor.
6. To add the bulk connections you can use vias by clicking “Create”>>“Via” (or simply use “o” as short-cut). A new window will be opened, here choose “Via Definition” as “M1_NWEL” and “M1_PDIFF” for bulk connections of PMOS and NMOS, respectively. You can increase number of contacts at the bulk by increasing the row and column numbers at the same window (See Step 8). The figure below displays 1.8V regular threshold voltage PMOS and NMOS transistors with bulk connections on the left.

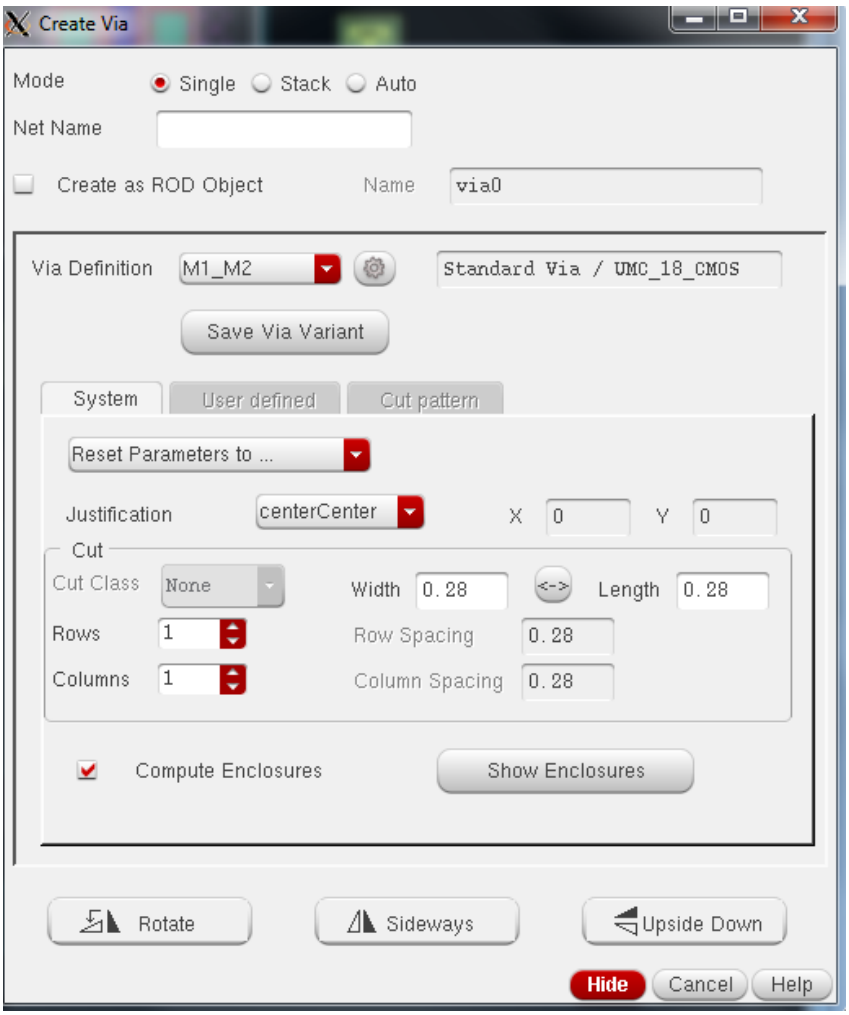


7. Now we have two transistors, what is left is connecting them together. We need to route power lines "VDD" and "ground", then connect the input "A" and output "Q". This process is specified as six metal, one poly, hence there are six different metal layers that can be used as conducting paths; however we are going to use only four metal layers at this course. Since the resistance of polysilicon (P0) is high it is not preferred to use it as a conducting path. In order to connect gates of PMOS and NMOS transistors "M1" layer is used. The convention for two metal processes are routing power lines (VDD, gnd) with the first metal, and routing signal paths (like input "A", and output "Q") with second metal. Hence, we will make metal 2 contacts for "A" and "Q". In order to connect P01 to M1 and M1 to M2 "M1_POLY" and "M2_M1" vias are used.
8. To create these vias select Create->Via. A window similar to the figure on the right will pop up.

   There are a number of via types:

   M1_POLY: Connection between P0 and M1.

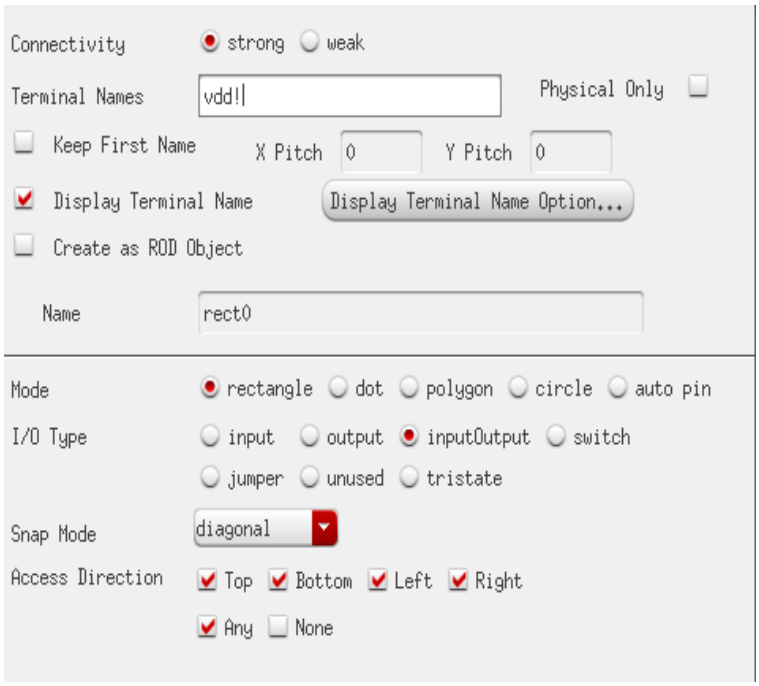
   M2_M1 : Connection between M1 and M2.



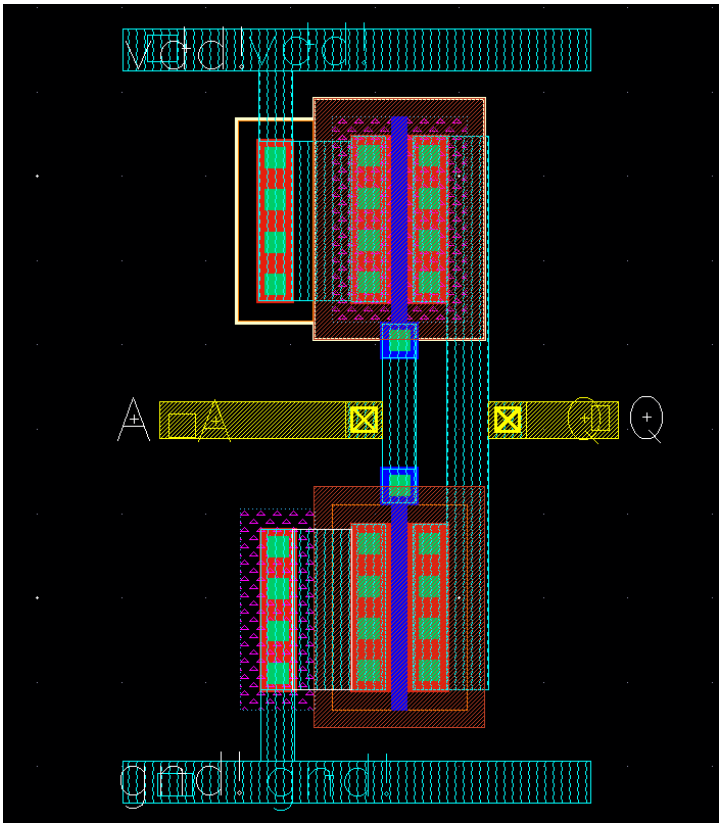
So you may choose M2_M1 via from "Via Definition" section for input and output terminals. You can also change width and length of the via and number of contacts used at the via.

As you may consider, we have not assigned names for the power or signal lines (remember ports in the schematic) yet. In this step we will create pins for "vdd!, gnd!, A, Q" (the "!" signs are necessary). Click Create->Pin. The following window pops up:

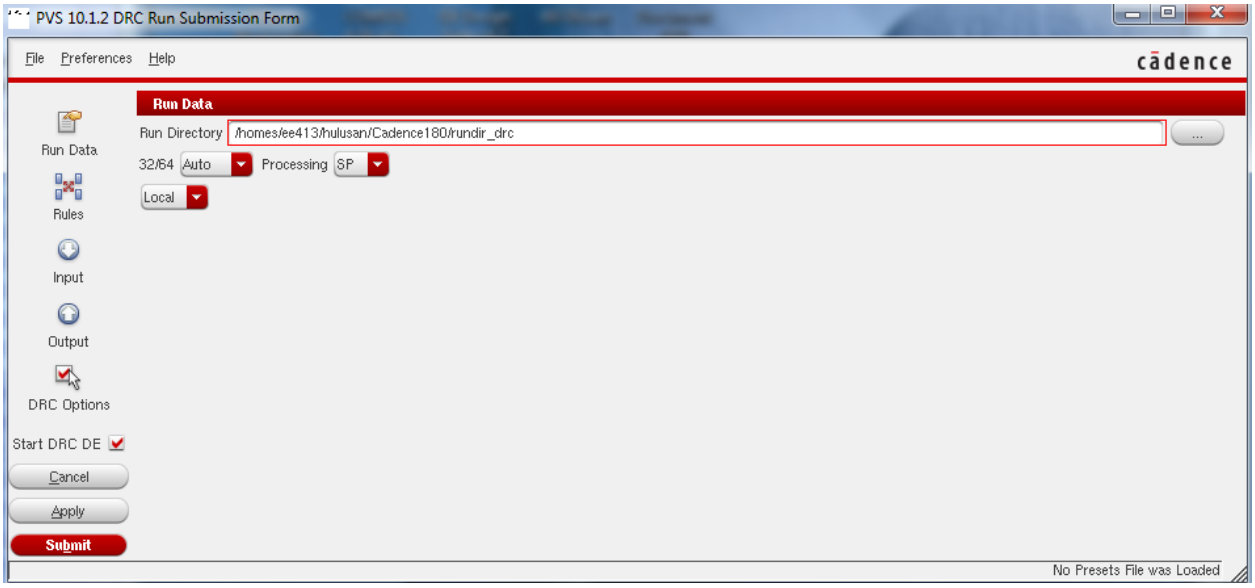
9. Write “vdd!” in "Terminal Name" field, check “Display Terminal Name” and check “inputoutput” in “I/O Type” list. Click on “Display Terminal Name Option” and write 0.5 as the height of the terminal name. Then click hide. Select “ME1” as the layer from the “Layers” window. Draw a rectangle right onto the metal line at the top of the layout (zoom in with the right mouse button, in order to place that exactly). Similarly place a “gnd!” pin on the metal line at the bottom.

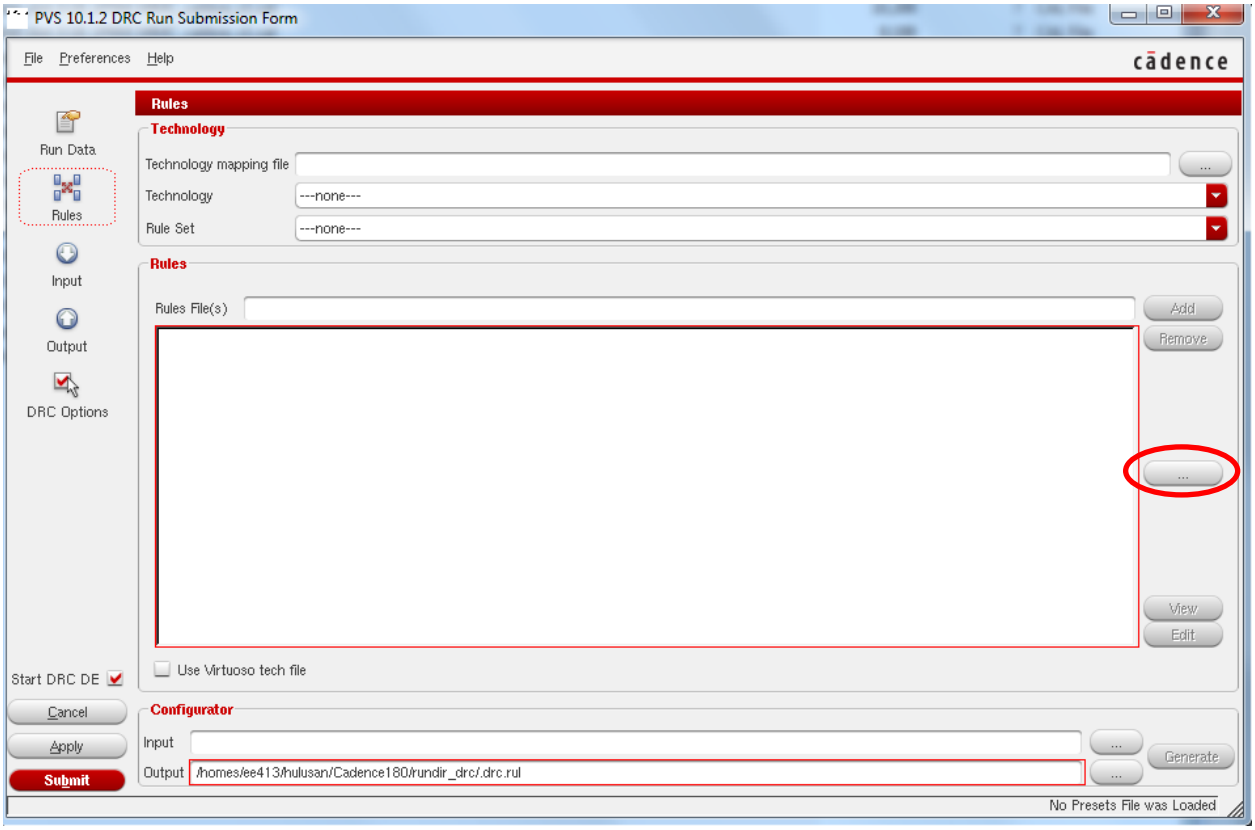


10. To create input and output pins select “ME2” as the layer and check “input” and “output” as the “I/O Type” respectively. When you are done "Hide" the pop up window and draw ME2 rectangles to input and output. To check the LVS of the layout properly we should label the lines also. Click Create->Label and label all input, output and inputoutput lines with associated label (ME1 for vdd! and gnd!, ME2 for A and Q). The final version of the layout is as follow:

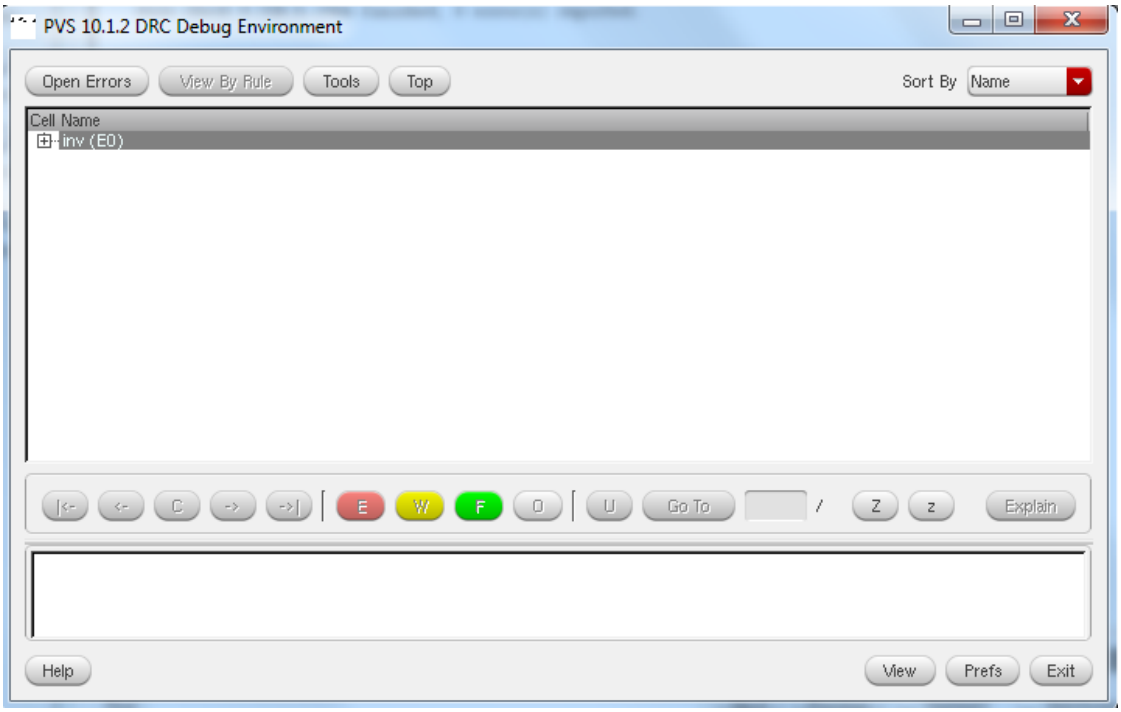


11. Now we have to check whether we have violated any design rules or not. This step is called as the DRC and is very important; any DRC error must be corrected before the layout is completed. In order to make DRC we are using the PVS tool. After you click <Lanuch> <PVS> a PVS tool is going to be appear on the toolbar. Click <PVS> <Run DRC>. A new window similar to shown below is going to be opened. Write "/homes/ee413/**<your username>**/Cadence180/rundir_drc" to Run Directory so that a directory for DRC run is going to be generated. Before submitting the DRC click on Rules which switches the window to Rules. Then click on Browse which is marked on the next figure and choose the rule files as "/homes/ee413/**<your username>**/Cadence180/RuleDecks/Calibre/DRC/G-DF-Mixed_Mode_RFCMOS18-1.8v_3.3v-1P6M-MMC-Calibre-DRC-2.11_P2".





12. Now clik on “DRC Options” to set which DRC options to be applied. Don’t change anything under the Rules pane. For the rules under the Groups pane make sure that only the “DRAWN_NPLUS” and “METOP_20KA” rules are chosen and deselect the others. Then click Submit to run DRC.
13. As a result of the DRC run you will get two new windows one of them is the **PVS Report** and the other is **PVS DRC Debug Environment**. As a result of this run you should not get any errors and the PVS DRC Debug environment window that you get must be similar with the figure below.

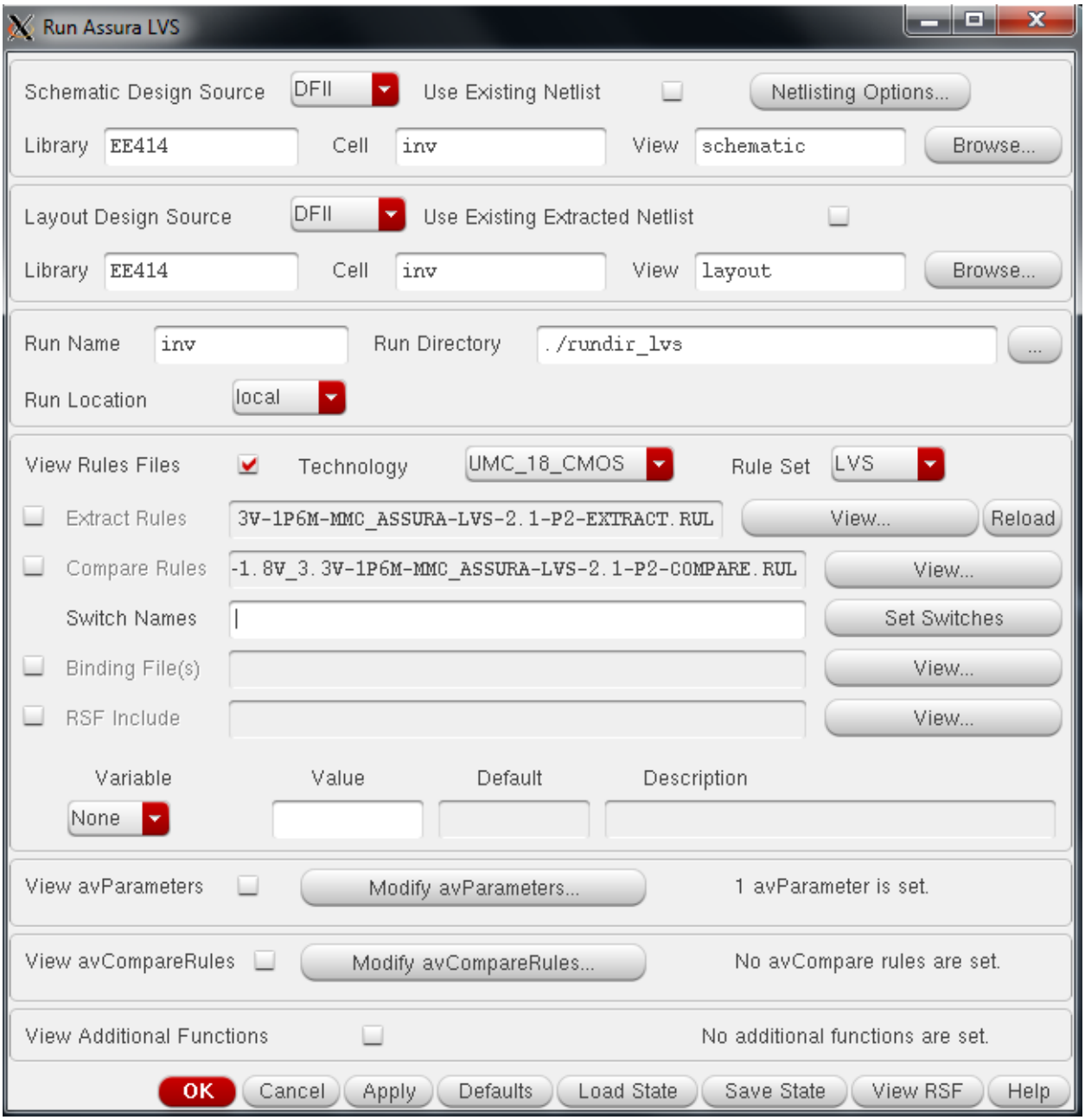


14. Make sure that there are no errors in the layout and If there are no errors, click <Design> <Save>, and **you have completed your first Layout**.

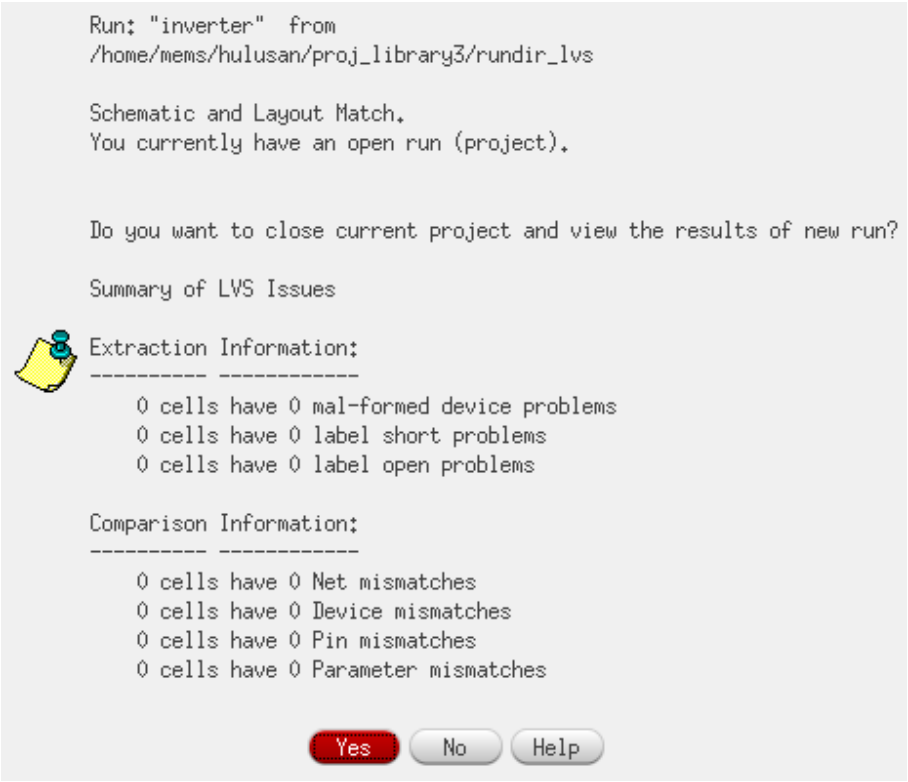
3. LAYOUT VERSUS SCHEMATİC CHECK (LVS)

Till now, you designed the schematics and layout of a CMOS inverter. However, you did not check yet whether the drawn layout is same as the schematics. In order to check whether the schematics and the layout are same, a special check mechanism is used called as LVS. What it does is to compare the netlists of the schematic view and the extracted view.

1. Click <Assura> <Run LVS>. The window below will pop up:

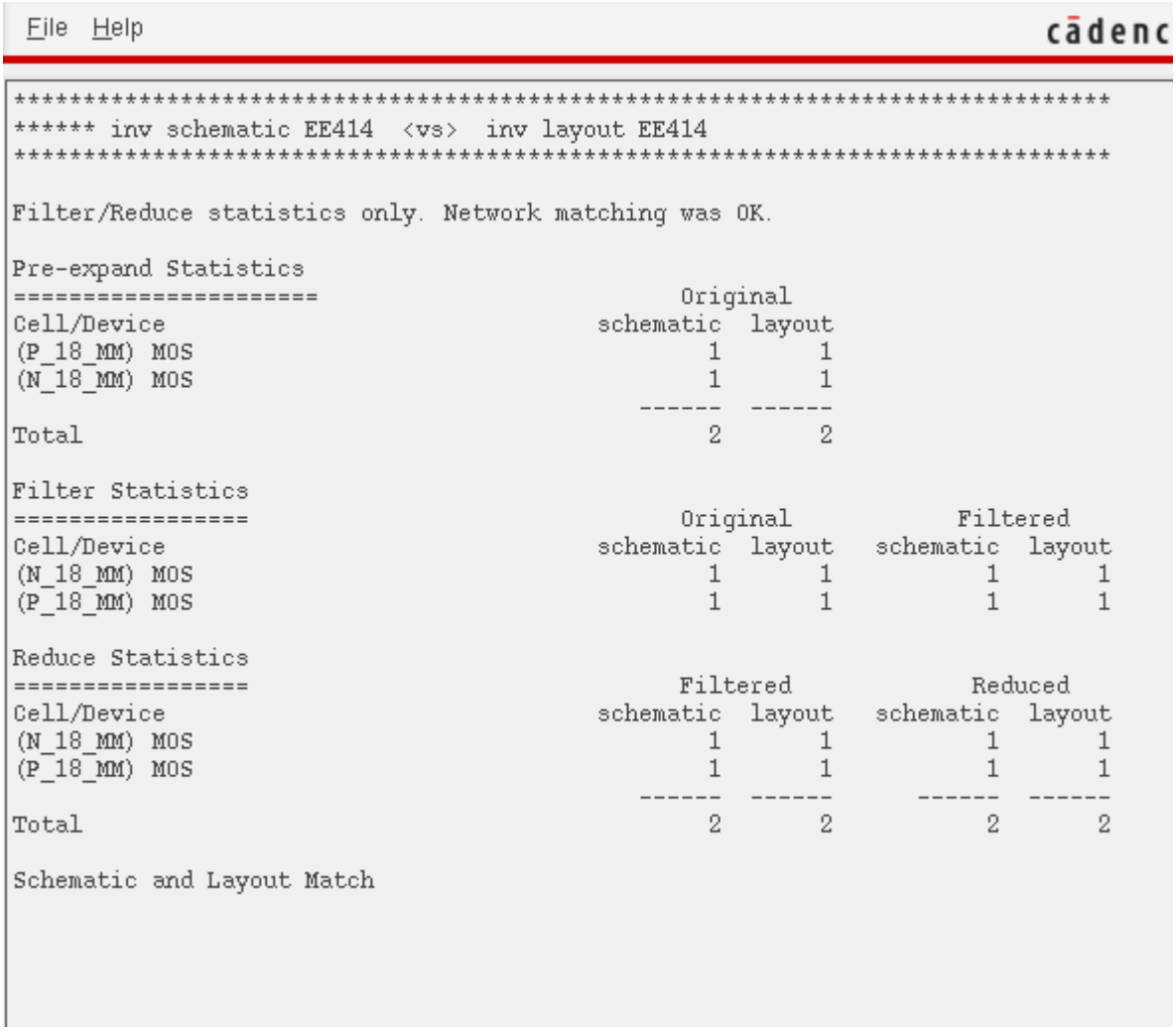


2. Give a random run name like “inverter” and write “rundir_lvs” as the Run Directory. Then choose Technology as “UMC_18_CMOS” and the Rule Set as “LVS” the remaining parts are going to be filled automatically. Then click “OK”.
3. After a short while, you will have a message box stating that the LVS check is completed. Figure below shows the window that is showing that schematic and Layout matched.



4. After you click on "YES" LVS Debug window which is shown below will pop up:

5. In order to see LVS report click on <View> <LVS Error Report (Current Cell)>.



Now, your design is ready for post-layout simulations, for post-layout simulations we are using another tool. For this purpose we need QRC extraction tool which is not included at this tutorial. For post layout simulations please get in touch with the course assistant for help.