EE 414 Supplementary Problems

Problem 1: This problem concerns the CMOS op-amp shown in Fig. 1.

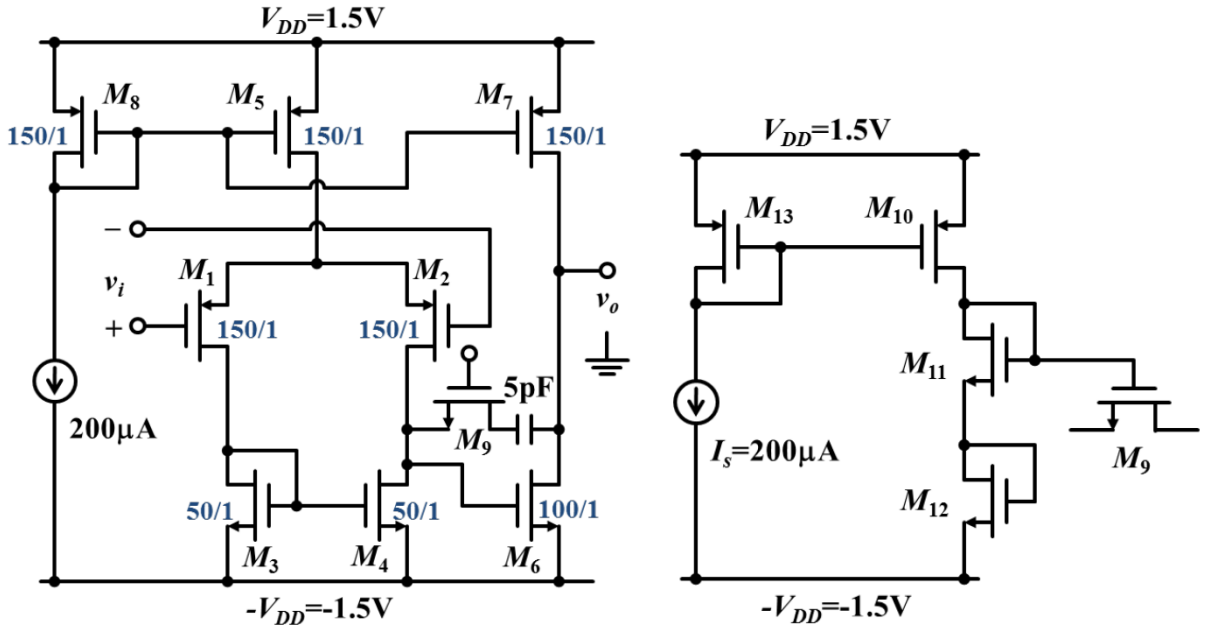

Fig. 1.

Variable	NMOS	PMOS	Unit
X_d	0.1	0.1	μm
dX_d/dV_{ds}	0.02	0.04	μm/V
t_{ox}	80	80	A
μ	450	150	cm^2/Vs
V_t	0.7	0.7	V
γ	0	0	$V^{-1/2}$

Table 1

a. Calculate the open-loop voltage gain, unity-gain bandwidth, and slew rate, for the circuit in Fig. 1 (a). Use the parameters of Table 1. Assume that the gate of M_9 is connected to the positive power supply V_{DD} and that the W/L ratio of M_9 has been chosen to cancel the right half-plane zero.

b. If the circuit of Fig. 1 (b) is used to generate the voltage to be applied to the gate of M_9 in Fig. 1 (a), calculate the required W/L ratio of M_9 to move the right-half plane zero to infinity. Let V_{DD} = 1.5V and I_s = 200μA. Use L = 1μm for all transistors, $W_{13} = W_{10}$ = 150μm, and $W_{11} = W_{12}$ = 100μm. Use Table 1 for other parameters.

c. Assuming that the zero has been moved to infinity, determine the maximum load capacitance that can be attached directly to the output node of the circuit in Fig 1 (a) and still maintain a phase margin of 45°. Neglect all higher order poles except the one due to the load capacitance. Use the value of W/L ratio obtained in part (b) for M_9 with the bias circuit of Fig. 1 (b). Ignore junction capacitance for all transistors. Use Table 1 for other parameters.

Problem 2:

What is the gain and -3 dB bandwidth (in Hz) of Fig. 2 if C_L=1 pF? Ignore reverse bias voltage effects on the pn junctions and assume the bulk-source and bulk-drain areas are given by Wx5µm. The W/L ratios for M1 and M2 are 10µm/1µm and for the remaining PMOS transistors the W/L ratios are all 2µm/1µm.

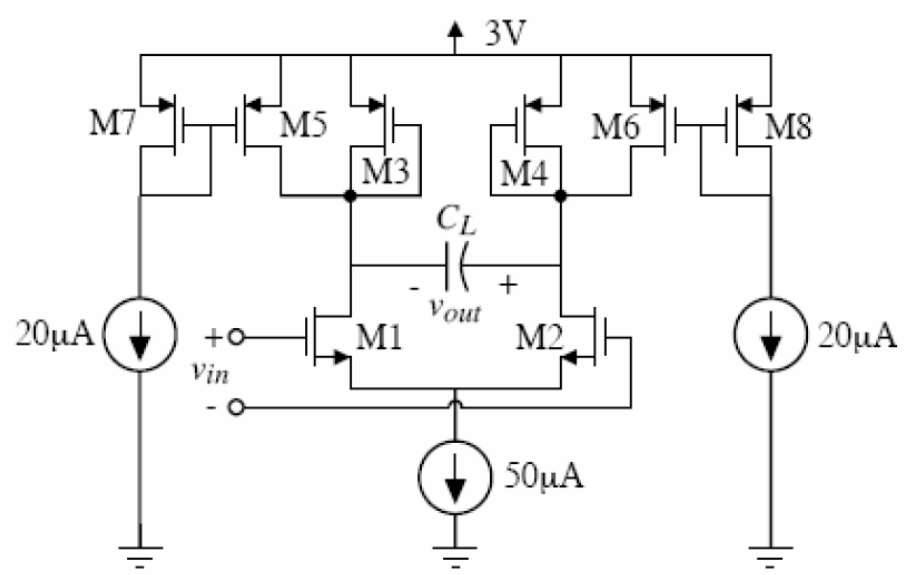

Fig. 2.