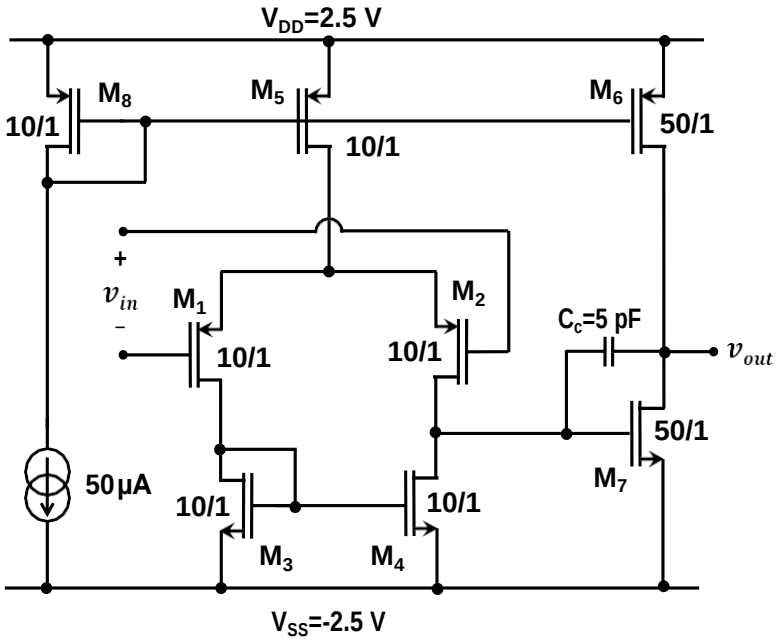
EE 414 Introduction to Analog Integrated Circuits
Supplementary Problems

Problem 1: Figure 1 shows a two stage CMOS opamp, calculate:

a. Slew rate (V/sec.)
b. Positive and negative output voltage limits (all transistors remain in saturation)
c. Positive and negative input common voltage limits (all transistors remain in saturation and use nominal parameter values).
d. Small signal voltage gain (V/V).
e. Gain-Bandwidth (MHz).
f. Power dissipation (mW). (Include the 50μA current sink)



M_N	
λ	= 0.04V^{-1}
V_{TN}	= 0.7V
K_N'	= 110μA/V^2

M_P	
λ	= 0.05V^{-1}
V_{TP}	= -0.7V
K_P'	=50μA/V^2

Figure 1

Problem 2: A push-pull output stage is presented in Figure 2.

a. Find the dc value of the collector currents when $V_{out} = 0$.
b. What is the maximum and minimum peak output voltage of this amplifier for R_L=1 kΩ? What is the maximum output current that can be delivered to the 1 kΩ resistive load?
c. What is the maximum average load power? What is the average power drawn from the sources? What is the efficiency of the circuit?

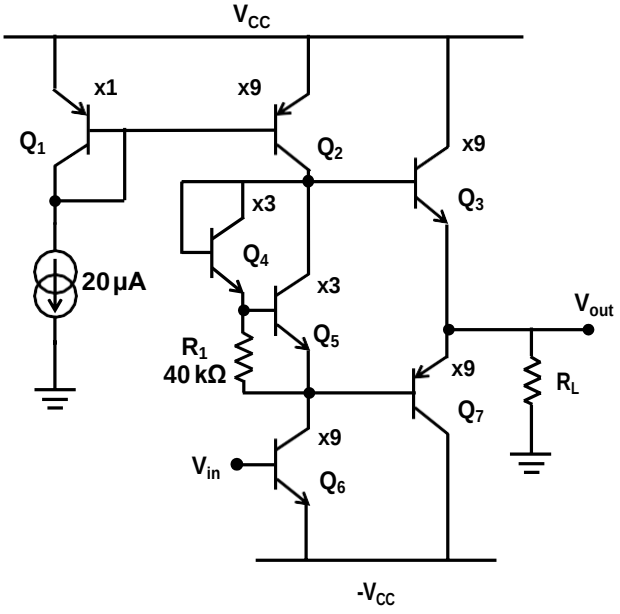


Figure 2

BJT parameters:
I_{S1} = 1.11 fA, $\beta_{npn}=\beta_{pnp}$= 100, $V_{BE\ (ON)}$ = 0.6 V, $V_{CE\ (sat)}$ = 0.2 V, V_{CC} = 10 V, V_T = 26 mV.