EE 414 Introduction to Analog Integrated Circuits
Term Project

Due Dates
Phase-1: May 08, 2015
Phase-2: June 08, 2015

In the term project, you are required to design an adjustable voltage regulator in a 180 nm CMOS technology (see Figure 1). The project groups will contain at most 2 students. Although it is not recommended, you may do your project alone. It is strongly recommended that you start your design procedure as soon as possible, it is not a weekend project and you have to spend enough time on it. Please don't hesitate to ask your questions to the course assistant, you can reach to him anytime via e-mail but don't leave it to the last minute.

A voltage regulator is a voltage reference with a strong load driving capability. An ideal voltage regulator output is independent from load, temperature, and supply. For this reason, the design specifications of a voltage regulator are related to the imperfections in the supply rejection, load driving capability, and temperature insensitivity. Table 1 shows the specifications of the required design.

Table 1: Specifications of the required design.

Design Specifications	
Input voltage (V_{IN}) range	1.3 V-3.3 V
Maximum power dissipation (no load condition)	<1 µW
Minimum resistive load	200 kΩ
Output voltage change with temperature between -40°C and 85°C	<10mV
Output voltage change with input between 1.3 V-3.3 V (Line Regulation)	<5mV
Output voltage change between full load (200 kΩ) and no load conditions (Load Regulation)	<1mV
V_{OUT} is required to be programmed with R_1 and R_2 between 1.2 V and 0.9xV_{IN}.	
Note: Do not consider the sinking capability of the voltage regulator for this design. This will simplify your design in a considerable amount.	

Each specification shown in Table 1 should be met in the worst case conditions. To illustrate, if the load regulation specification is met at room temperature, but it is not met at 40°C, your design will be considered to be unsuccessful in terms of load regulation specification. You need to perform "parametric analysis" in CADENCE in order to understand whether your design meets a specification in all conditions. You can find how to perform "parametric analysis" in CADENCE in the tutorial.

Figure 1 shows a simplified block diagram of a typical adjustable voltage regulator which is mainly composed of two parts: a voltage reference and an Opamp. The voltage output (V_{REF}) is increased by a non-inverting amplifier to a desired output value (V_{OUT}). This non-inverting amplifier also provides a strong load driving capability. Please notice that Figure 1 illustrates the operation; you are not restricted to the configuration which Figure 1 shows. Furthermore, as Figure 1 demonstrates, you need 4 terminals in your designs. First one is V_{IN} which is simply V_{DD} of the sub-blocks. Second one is GND (ground), third one is V_{OUT}, and fourth terminal is ADJ which provides the user to adjust the regulator output.

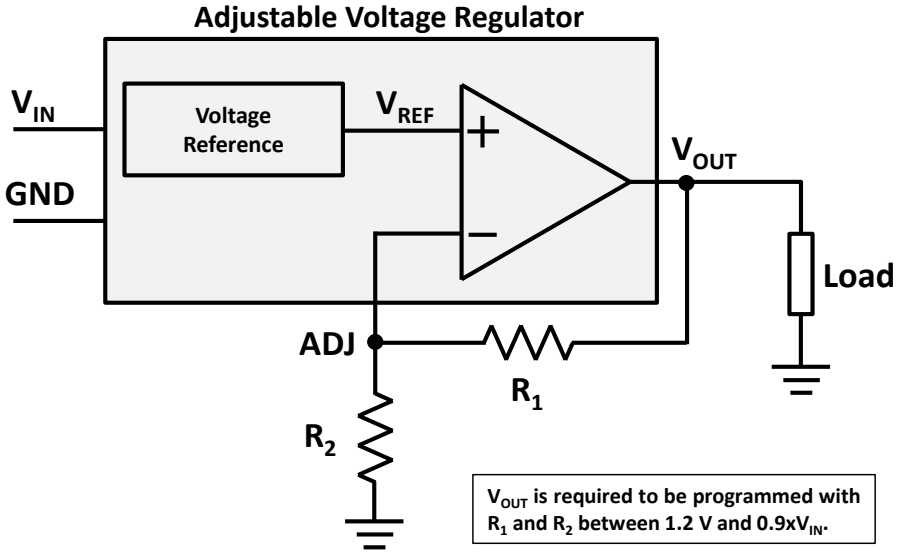

Figure 1: Simplified block diagram of a typical voltage regulator.

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By means of this project, you will have an important opportunity to consolidate your theoretical knowledge, which you gain in EE414, with a valuable design practice. Throughout this project, you will design a voltage reference and a complete Opamp.

It is strongly recommended that you start your design procedure as soon as possible. You have already learned the voltage reference and most of the fundamentals of operational amplifiers. For this reason, the project is composed of two phases. In the first phase, you will submit a 4-5 pages preliminary design report. You are not required to make a detailed design in this phase. On the other hand, you should include the detailed qualitative description of the prospective designs. In the second phase, you will implement **both schematic and layout your design in UMC 180 nm CMOS process** which is available in Student VLSI Lab. The deadlines, report contents, and percentages of the grading are shown in Table 2. In addition, there will also be a small contest according to the performances of your regulators. According to this contest, the top 3 designs whose performances are better than all of the design specifications indicated in Table 1 will be awarded with bonus grades. The bonus grades vs. the rank are shown in Table 3.

Table 2: Deadlines, report contents, and grading policy.

Phases	Deadlines	Content	Grading
Phase 1	May 08	Detailed qualitative description of top level system design and design of the sub-blocks (voltage reference, Opamp…)	10%
		Rough quantitative works related to the design specifications	5%
Phase 2	June 08	Detailed quantitative works related to the design specifications and detailed top level design procedure (both quantitative and qualitative)	20%
		Detailed design procedure of sub-blocks (both quantitative and qualitative)	25%
		Detailed simulation results verifying the operation clearly	25%
		Layout of the Design	10%
		Report Format	5%

Table 3: Bonus policy.

Design Criteria	Grading
Input voltage (V_{IN}) range	+(4-rank)%
Maximum power dissipation (no load condition)	+(4-rank)%
Minimum resistive load	+(4-rank)%
Output voltage change with temperature between -40^{o}C and 80^{o}C	+(4-rank)%
Output voltage change with input between 1.3V-3.3V (Line Regulation)	+(4-rank)%
Output voltage change between full load (200 kΩ) and no load conditions (Load Regulation)	+(4-rank)%

Enjoy the project!