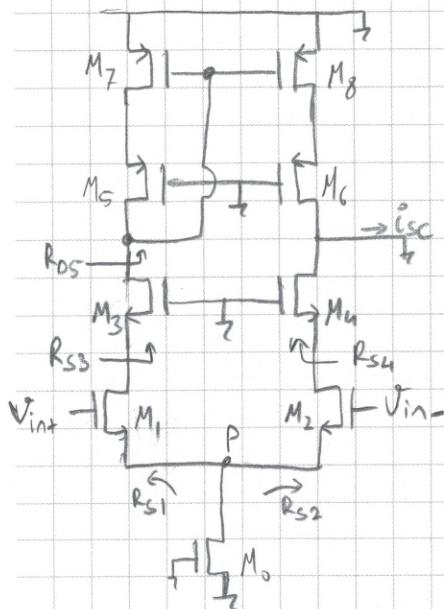


EE 414 - Introduction to Analog Integrated Circuits

Take Home Exam 3

Problem 1



a.) Without using half circuit: Do not take node "P" as a virtual ground. At the first glance, there is no symmetry. So, use superposition. Apply V_{int+}

$$R_{S2} \approx \frac{1}{g_m_{1,2}}$$

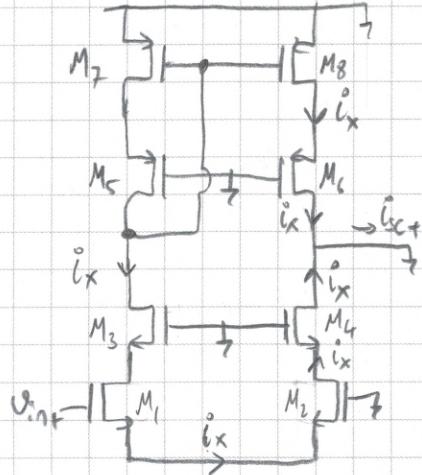
notice that $R_{S1} \approx g_m_{1,2}$.

Similarly, $R_{S3} \approx \frac{1}{g_m_{3,4}}$ so this cct can be simplified as;

$$i_x = V_{int+} \cdot \frac{g_m_{1,2}}{2} \quad (\text{since } \frac{1}{g_m_{3,4}} \ll R_{S1})$$

⇒ So, overall circuit can be simplified as; ($V_{in-} = 0$)

* Notice that the current through M_7 is mirrored to M_8 .



$$\text{So, } i_{M_8} = i_x \Rightarrow i_{SC+} = 2i_x = V_{int+} g_m_{1,2}$$

Similarly you can find $i_{SC-} = -V_{int-} g_m_{1,2}$ → ground V_{int-}

$$i_{SC} = i_{SC+} + i_{SC-} = (V_{int+} - V_{int-}) g_m_{1,2} \Rightarrow G_m = g_m_{1,2}$$

• Note that by taking "P" as a virtual ground when applying $\frac{(V_{int+} - V_{int-})}{2}$

to the positive terminal & $-(V_{int+} - V_{int-})/2$ to the negative terminal, you'll get the same result easily. Even if there is an asymmetry, $R_{S1} \approx R_{S2} \Rightarrow$ the cct is almost symmetric on a reference point "P". For this reason, that cct can be taken as a symmetric cct in "short-circuit current" analysis.

b.) R_{out} can easily be found by assuming "P" as a virtual ground.

$$R_{out} \approx [g_{m6} r_{o6} r_{o8} \parallel g_{m4} r_{o4} r_{o2}]$$

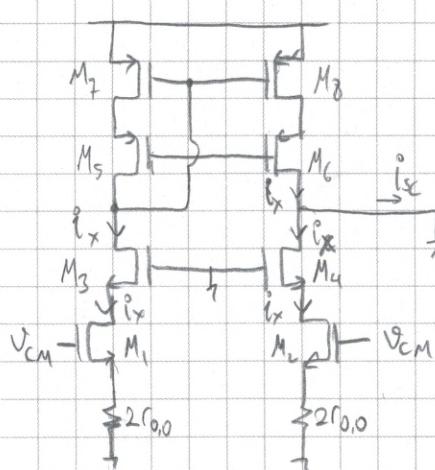
c.) $A_v = G_m R_{out} = g_{m1,2} [g_{m3,4} r_{o1,2} r_{o3,4} \parallel g_{m5,6} r_{o5,6} r_{o7,8}]$

d.) Neglect parasitic capacitances. In fact, it is a reasonable assumption because the resistance seen from the load capacitance is very high comparing with other resistances. For this reason even if C_L is not much higher than the parasitic capacitances, the pole at the output is the dominant pole.

Furthermore, it is also reasonable to neglect C_{gd} capacitances for the output pole since they are much lower than C_L . So,

$$\left. \begin{aligned} BW = W_{out} &= \frac{1}{R_{out} C_L} \\ A_v &= R_{out} \cdot G_m \end{aligned} \right\} G_BW = A_v \cdot BW = \frac{G_m}{C_L} = \frac{g_{m1,2}}{C_L}$$

e.) Let's draw the simplified common mode small signal model of the cct.



$$i_x = g_{m1,2} \left(\frac{V_{CM}}{2r_{o,0}} \right) V_{CM}$$

Since i_x generated from left side is mirrored to the right side the short-circuit current at the output is $i_{sc} = i_x - i_x = 0$

hence $A_{CM} = 0$

$$CMRR = \frac{A_v}{A_{CM}} \Rightarrow \infty$$

f.) Restrictions due to M_7 & M_8

$$\left. \begin{array}{l} V_{BP} + |V_{TPl}| + V_{ovS} \leq V_{DD} - V_{ovZ} \\ V_{DD} - V_{ovS} - |V_{TPl}| \leq V_{BP} + V_{TP} \end{array} \right\} \left. \begin{array}{l} V_{DD} - V_{ovS} - 2|V_{TPl}| \leq V_{BP} \leq V_{DD} - V_{ovZ} - |V_{TPl}| - V_{ovS} \\ V_{ovZ} \leq |V_{TPl}| \end{array} \right.$$

Restrictions due to right half branch:

In a typical design procedure, you will be free to set gate voltages.

So, in PMOS:

$$V_{SD} \geq V_{SG} - |V_{TPl}| \Rightarrow \boxed{V_{SDmin} = V_{ov}} \Rightarrow \text{you can set } V_G = V_S - V_{ov} \text{ after determining } V_{ov}.$$

$$\Rightarrow \text{Similarly in NMOS: } \boxed{V_{DSmin} = V_{ov}}$$

* So, if you are free to set gate voltages you can perform a design such that each transistor dissipates V_{ov} . But, since there will be some small signal variations in each node & some variations in the threshold voltages and/or bias voltages, some margins should be inserted to the design.

* For our case assume that no margin is needed.

$$\text{So, } \boxed{V_{out, max} = V_{DD} - V_{ovS} - V_{ovB}}$$

$$\boxed{V_{out, min} = V_{ovL} + V_{ovZ} + V_{ovD}} \Rightarrow \text{if we are free to set the gate voltages of } M_{1,2}. \text{ For this reason,}$$

$$\boxed{V_{out, min} = V_{D2, min} + V_{ovL} = V_{CM} - V_{TN} + V_{ovL}} \text{ if the gate voltages of the input transistors are fixed to } V_{CM}.$$

* Extra Information: What about input CM range?

$$V_{BN} \leq V_{out} + V_{TN}$$

$$V_{INCM} \leq V_{BN} - V_{ovL} - V_{TN} + V_{TN}$$

} For the worst case

$$V_{BN} \leq V_{out, min} + V_{TN}$$

$$V_{INCM} + V_{ovL} \leq V_{BN}$$

$$\boxed{V_{INCM} \leq V_{out, min} + V_{TN} - V_{ovL}}$$

$$\boxed{V_{INCM, max} = V_{out, min} + V_{TN} - V_{ovL}}$$

Similarly in order to avoid the lin. op. of M₀,

$$V_{INCM} - V_{OV2} - V_{TN} \geq V_{OVO}$$

$$V_{INCMmin} = V_{OVO} + V_{OV2} + V_{TN}$$

* Assume that overdrive voltages are very small:

then, $V_{INCMmax} = V_{OVMmin} + V_{TN} \Rightarrow$ This limitation does not allow to have a high input voltage swing

Assume that $V_{TN} = 500mV$ & 1Vpp symmetric swing is desired.

Neglect V_{OV4}

$$\Rightarrow V_{INCMmax} = V_{mid} - 500mV + 500mV = V_{mid} \Rightarrow \text{no input CM variation is allowed!!}$$

This is problematic especially for buffer connections! \Rightarrow Since output & input CM ranges are same. So assuming symmetric swing around V_{mid} ,

$$V_{mid} + \Delta V = V_{mid} - \Delta V + V_{TN} \quad (\text{neglect } V_{OV4})$$

$$\Delta V = \frac{V_{TN}}{2}$$

very small CM range!!

For this reason, for a typical buffer connection telescopic cascode are not used!

Problem 2:

Writing the restrictions due to the specifications will ease our design:

(i) $I_{sup} < 20mA$

(ii) $\frac{g_{min}}{C_L} > 2\pi S_0 M$, $g_m = \sqrt{2 K_n \left(\frac{W}{L}\right)} I_D$ $\Rightarrow I_D = I_{sup}/2$
 $\Rightarrow S_p$ per transistor

(iii) Gate potential of the input transistors are fixed:

$$\underbrace{V_{out1,max}}_{2.15} \leq V_{DD} - V_{OV8} - V_{OV6}$$

$$\underbrace{V_{out1,min}}_{1.15} \geq V_{cm} - V_{TN} + V_{OV4}$$

(iv) $(W/L)_{in} C_{ox} \leq 1 \mu F$, take $L = 0.34 \mu m$ for min. size transistor

Note that (i), (ii), and (iv) are related to the input transistors:

We are not expected to perform an "Optimum Design", So, fix some parameters

Take $I_{sup} = 20 \text{ mA}$

$$W \leq \frac{1 \mu F}{5 \text{ pF}/\mu m^2} \cdot \frac{1}{L} = \frac{200}{0.34 \mu m} = 588.3 \mu m$$

take $\boxed{W = 580 \mu m}$
 $L = 0.34 \mu m$

Since we are taking the limiting case, g_m must satisfy (ii.).

Otherwise, there will be no solution.

$$g_m = \sqrt{K_n' \left(\frac{W}{L} \right) I_{sup}} = \sqrt{150 \mu \times (1705.9) \times 20 \mu} = 2.26 \text{ mS}$$

$$\frac{g_m}{C_L} = \frac{2.26 \text{ mS}}{5 \text{ pF}} = 452.64 \frac{\text{mrad}}{\text{s}} = 72 \text{ MHz} \geq 50 \text{ MHz}$$

\checkmark GRW spec. is satisfied.

* Now using (iii) determine $(\frac{W}{L})$ of other transistors:

$$V_{ov8} + V_{ov6} \leq 1.15 \text{ V}$$

$$V_{ov4} \leq 0.1 \text{ V}$$

by the way also remember from Problem-1: $V_{ov7,8} \leq |V_{TP}|$,

take $V_{ov8} = V_{ov6} = 0.5 \text{ V}$ (you can take larger values, but it is)

$V_{ov4} = 0.05 \text{ V}$ better to put some margin

For PMOS

$$I_D = \frac{K_p'}{2} \left(\frac{W}{L} \right)_p V_{ov6,8}^2 \Rightarrow \boxed{\left(\frac{W}{L} \right)_{5,6,7,8} = \frac{10}{35} = 1.14}$$

For NMOS

$$I_D = \frac{K_n'}{2} \left(\frac{W}{L} \right)_{3,4} V_{ov3,4}^2 \Rightarrow \boxed{\left(\frac{W}{L} \right)_{3,4} = \frac{10/75}{25 \times 10^{-4}} = 53.33}$$

For Mo there is no rough specification, but to ensure its operation in lin. region:

$$V_{DD} \geq V_{OV,0} \Rightarrow V_{OV,0} \leq V_{INCM} - V_{TN} - \underbrace{V_{OVIN}}_{\text{around } 70mV}$$

$$\text{select } V_{OV,0} = 200mV \Rightarrow I_D = \frac{k'_N}{2} \left(\frac{W}{L} \right)_0 V_{OV,0}^2 \Rightarrow \left(\frac{W}{L} \right)_0 = \frac{10/75}{0,04} = 3,33$$

Now set bias voltages:

$$V_{BP} \leq V_{DD} - \underbrace{(V_{OV8} + V_{OV6})}_{1V} - |V_{TP}| \quad \text{put some margin into this inequality}$$

(we can put 75 mV margin)

Putting margin directly narrows the swing in the same amount. Since we have 0.15 V extra headroom, this margin will not yield problem. But for this question, you are not needed to put this margin.

$$V_{BP} = V_{DD} - \underbrace{(V_{OV8} + V_{OV6})}_{1V} - \underbrace{|V_{TP}|}_{0.7} - \underbrace{V_{margin}}_{75mV}, V_{BP} = 1.525V$$

(Notice that $V_{OUTmax} = 2.225V$ ($V_{BP} + |V_{TP}|$))

$(V_{OUTmax} \text{ can be also found as: } V_{OUTmax} = V_{DD} - V_{OV8} - V_{OV6} - V_{margin}, V_{BP} = 2.225V)$

$$V_{BN} \geq V_{INCM} - V_{TN} + V_{OV4} + V_{TN} = V_{INCM} + V_{OV4} \quad (\text{Let's put } 25mV \text{ margin})$$

$$V_{BN} = 1.65 + 0.05V + 0.025V = 1.725V \Rightarrow V_{OUTmin} = \underline{V_{BN} - V_{TN}} = 1.125V \checkmark$$

For simplicity after determining V_{OV} you can directly set

$$V_{BP} = V_{DD} - (V_{OV8} + V_{OV6}) - |V_{TP}| = 1.6V \Rightarrow V_{OUTmax} = 2.3V$$

$$V_{BN} = V_{INCM} + V_{OV4} = 1.7V$$

\Rightarrow All the margins are now in output swing.

Design Summary:

$$\left(\frac{w}{L}\right)_{1,2} = \frac{580\mu}{0,34\mu}, \quad \left(\frac{w}{L}\right)_{3,4} = \frac{18,13\mu}{0,34\mu}, \quad \left(\frac{w}{L}\right)_{5,6,7,8} \approx \frac{0,4\mu}{0,34\mu}$$

$$V_{BIAS} = V_{OV_0} + V_{TN} = 800mV \quad V_{BP} = 1.6V \text{ (with some margin 1.525V)}$$

$$\left(\frac{w}{L}\right)_0 = \frac{1,13\mu}{0,34\mu}$$

$$V_{CN} = 1.7V \quad (" " " " 1.725V)$$

Problem 3:

Single ended voltage & short circuit gains of "single-ended topology" is two times of the single-ended gains of "fully differential topologies".

But, in the single ended topology due to the mirroring operation, a pole appears (called mirror pole) @ $\omega = \frac{g_m}{2(C_{GS7,8})}$ is a large parasitic

⇒ This second pole directly degrades the GBW product for a reasonable phase margins. Note that GBW does not depend on this pole but in order to have a resonable phase margin, GBW product should be adjusted that it does not exceed the second pole for at least 45° PM.

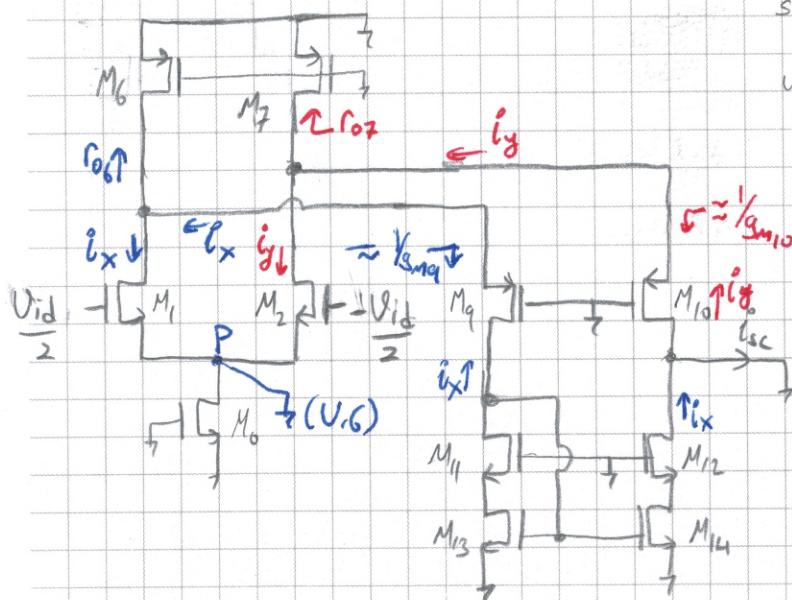
(g_m/C_L is set to W_{P2} for 45° PM margin)

For now, it is enough that you know introducing mirror pole degrades the speed and/or stability.
(bandwidth)

Problem 4:

a) Let's first draw the simplified small signal model of the circuit

$$V_{id} = V_{in+} - V_{in-}$$



$$i_x = g_{m1} \frac{V_{id}}{2}$$

$$i_y = -g_{m2} \frac{V_{id}}{2}$$

$$i_{sc} = i_x - i_y$$

$$g_{m1} = g_{m2}$$

$$i_{sc} = g_{m1,2} V_{id} = g_{m1,2} (V_{in+} - V_{in-})$$

$$G_m = \frac{i_{sc}}{V_{in+} - V_{in-}} = g_{m1,2}$$

b) Like in Problem 1 assuming "P" is the virtual ground (V.G.)

R_{out} can be calculated as:

$$R_{out} = [g_{m1,2} (r_{o11,12} \parallel r_{o13,14})] \parallel [g_{m9,10} r_{o9,10} (r_{o6,7} \parallel r_{o1,2})]$$

$$C_i) A_v = G_m R_{out} = g_{m1,2} [g_{m11,12} (r_{o11,12} \parallel r_{o13,14})] \parallel [g_{m9,10} r_{o9,10} (r_{o6,7} \parallel r_{o1,2})]$$

d-) Similar with Telescopic cascode amplifier C_L can be considered as the dominant capacitance Hence.

$$BW = W_{R_{out}} = \frac{1}{R_{out} C_L}$$

$$A_v = R_{out} G_m$$

$$GBW = A_v BW = \frac{G_m}{C_L} = \frac{g_{m1,2}}{C_L}$$

e.) Since the circuit can be considered as symmetric circuit (like Telescopic Cascade amplifier) the common mode gain (A_{cm}) of the circuit is $A_{cm} = \underline{0}$.

The result can be easily seen by considering the short circuit current. The generated short circuit current from two inputs are cancel each other ($I_{sc} = 0$).

Therefore

$$\boxed{CMRR = \frac{A_v}{A_{cm}} \rightarrow \infty}$$

f.) By considering bias voltages of the circuit is determined properly to operate all the transistors in SAT region.

$$\boxed{V_{out\max} = V_{DD} - V_{ov7} - V_{ov10}}$$

$$\boxed{V_{out\min} = V_{ov12} + V_{ov14}}$$