A Voltage Reference Circuit with Ultra-low Power Using Subthreshold and Body Effect Techniques

Huimin Zhang
State Key Laboratory of Electronic Thin Films and Integrated Devices
UESTC
Chengdu, China
zhang_hm0315@163.com

Yun Zhou
State Key Laboratory of Electronic Thin Films and Integrated Devices
UESTC
Chengdu, China
zhouy@uestc.edu.cn

Kai Yuan
State Key Laboratory of Electronic Thin Films and Integrated Devices
UESTC
Chengdu, China
yuankai@uestc.edu.cn

Yadong Jiang
State Key Laboratory of Electronic Thin Films and Integrated Devices
UESTC
Chengdu, China

***Abstract*—We have demonstrated a voltage reference circuit with ultra-low power by a standard 0.5 µm complementary metal oxide semiconductor (CMOS) N-well process. Two voltages with opposite temperature coefficient are added to produce a reference voltage which is approximately equal to the threshold voltage of a metallic oxide semiconductor field effect transistor (MOFET) at absolute temperature of zero degree. In addition, a current that is proportional to the square of absolute temperature, which can accurately compensate the pre-exponential factor of subthreshold current is introduced. Experimental results show that the proposed circuit can provide a reference voltage with a temperature coefficient of 5.54 ppm/°C over a range from -20 to 85 °C, a total supply current of 123 nA, as well as an ultra-low power of only 0.209 µW under a supply voltage of 1.7 V at room temperature.**

Keywords-voltage reference circuit; ultra-low power consumption; subthreshold; body effect techniques

I. INTRODUCTION

The growing trend of the analog and digital large scale integrated circuit (LSI) functions on a chip has given rise to the development of precision and small analog components in metal oxide semiconductor (MOS) technology, Those LSIs would be suitable for power aware applications, such as portable mobile devices, smart intelligent sensors and Life-log/Life-assist medical devices [1]. As a promising step toward such LSIs can be realized by utilizing the properties of devices operated in the subthreshold region.

Reference circuits are the foremost building blocks in the mixed-signal ultra-low power domain. To resolve this problem, many reference circuits that consist of the subthreshold operation of MOSFETs have been proposed [2]-[3]. However, these needed a number of large resistances to reach a low current and a variety of capacitances to compensate unnecessary null points and poles. As we known, such high resistances and capacitances could not only occupy a large area, but also consume relatively high power. Recently, many improved reference circuits have been reported [4]-[7]. For example, these circuits that consist of subthreshold MOSFETs without resistor achieved ultra-low power, while the simple current mirror with differential amplifier may cause some errors to the following circuits. In consideration of those factors, a voltage reference circuit with ultra-low power using subthreshold and body effect techniques is proposed. It has small temperature coefficient and micro area occupation on the chip owing to no capacitor and resistor to use.

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II. TEMPERATURE CHARACTERISTICS

The current-to-voltage (I-V) characteristics of an N-channel metal oxide semiconductor (NMOS) transistor that operates in the saturation and in the subthreshold region can be expressed as (1) and (2), respectively,

$$I_{DS} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 = \frac{\mu_n C_{ox}}{2} K (V_{GS} - V_{TH})^2 \quad (1)$$

$$I_{DS} = \mu_n C_{ox} V_T^{\,2}(\eta - 1)\frac{W}{L}\exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) = I_0 K \exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \quad (2)$$

Where $I_0 = \mu_n C_{ox} V_T^{\,2}(\eta - 1)$ is the pre-exponential factor of the subthreshold current, μ_n is the carrier mobility in the channel, C_{ox} is the gate-oxide capacitance, V_{TH} is the threshold voltage, W and L are the channel width and length, $V_T = \frac{kT}{q}$ is the thermal voltage, η is the subthreshold slope factor[4]. The temperature dependence of the carrier mobility μ_n is given by $\mu_n = \mu_0\left(\frac{T_o}{T}\right)^m$, where μ_0 is the mobility at T_0, m is the temperature exponent.

We will utilize this relation between temperature and current that has been investigated to discuss and analyze the principle of following circuit.

III. PROPOSED VOLTAGE REFERENCE

Our proposed voltage reference circuit that consists of three main subcircuits is shown in figure1. The first is a PTAT^2 current subcircuit composed of transistors working in subthreshold (M_4, M_6) and others in saturation. It will generate a current I_2, which is proportional to the square of absolute

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temperature. The second is a voltage reference subcircuit composed of two source-coupled pairs (M_{11}-M_{15}), among which all transistors are operated in the subthreshold except for M_{16}-M_{18}. It accepts the current I_2 through current mirrors and generates two voltages with a negative temperature coefficient V_{TH} and a positive temperature coefficient V_T. Then the two voltages are combined to produce a reference voltage V_{REF} with a zero TC. The third is a start-up circuit composed of MS1, MS2 and MS3 that are used to making sure the entire circuit work in stable state. The following trifles will describe the operation in details.

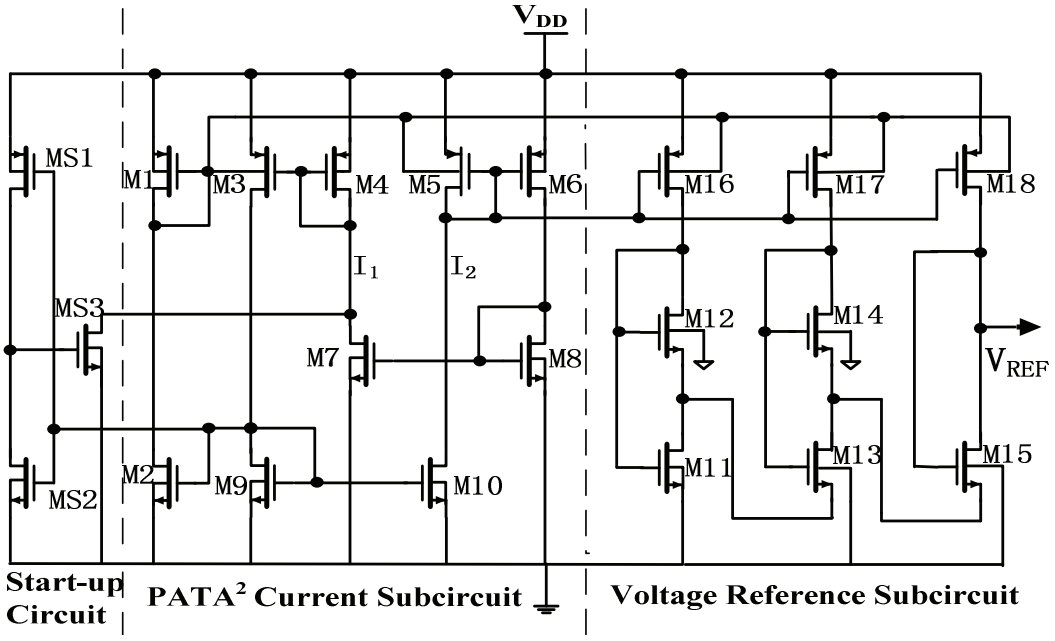

Figure1 . Proposed voltage reference circuit

A. The PTAT² current subcircuit

The PTAT² current generator circuit is composed of M_3-M_{10} and M_1-M_2 that provide forward bias for the source-bulk junction to reduce the threshold voltage of the NMOS transistors [9]. The current mirror consisted by transistors M_9 and M_{10} imposes equal current I_2 in M_3 and M_5, meanwhile, the current mirror consisted by transistors M_7 and M_8 imposes equal current I_1 in M_4 and M_6. To bias M_4, M_6 in the subthreshold region and M_3, M_5 in the saturation region, two different threshold voltages must be achieved, meanwhile considered producing in standard digital MOS transistors, forward bias for the source-bulk junction is introduced[9]. Therefore, in order to avoid turning on the p-n junction of the source-bulk junction at the highest temperature, the forward bias voltageV_{GS1} and the threshold voltages of M_4, M_6 transistors must set appropriate value at room temperature, thereby, temperature- dependent bulk current of these transistors are small enough to neglect[9]. Except M_4 and M_6, all the transistors operate in the saturation region. The I-V characteristics of a NMOS transistor in the saturation and the subthreshold regions can be approximated by (1) and (2), respectively. Assuming M_4 and M_6 in subthreshold with a drain current I_1 and M_3 and M_5 in saturation with a drain current I_2, the gate-source voltages of M_3 and M_4 (M_5 and M_6) are identical, so we can obtain

$$V_{TH3}+\sqrt{\frac{2I_2}{\mu_n C_{ox}\,W_3/L_3}}=V_{TH4}+\eta V_T\ln\left(\frac{I_1}{\mu_n C_{ox}V_T^{\,2}\,W_4/L_4}\right) \tag{3}$$

$$V_{TH5}+\sqrt{\frac{2I_2}{\mu_n C_{ox}\,W_5/L_5}}=V_{TH6}+\eta V_T\ln\left(\frac{I_1}{\mu_n C_{ox}V_T^{\,2}\,W_6/L_6}\right) \tag{4}$$

Here we have neglected channel length modulation ($\lambda=0$) and taken advantage of the source-bulk junction to provide forward bias voltages of M_4 and M_6, so $V_{TH4}=V_{TH6}$ and $V_{TH3}=V_{TH5}$. By subtracting (3) from (4), we can obtain the expression of the current I_2:

$$I_2=\frac{\mu_n C_{ox}\,W_5/L_5}{2\left(\sqrt{(W_5/L_5)/(W_3/L_3)}-1\right)^2}\eta^2 V_T^{\,2}\ln^2\left(\frac{W_6/L_6}{W_4/L_4}\right) \tag{5}$$

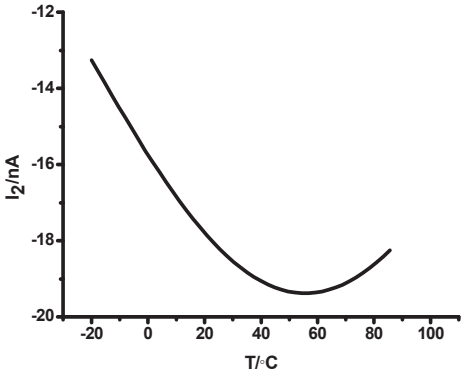

Figure2 . Measured current I_2 as a function of temperature.

Figure 2 shows the simulated relationship between temperature and current with a typical working temperature of 27°C, we can find the simulated result coincides with theoretical result well. Compared with I_P in [7], the obtained PATA[2] current that is independent on the voltage reference will be better for offsetting the pre-exponential factor of the subthreshold current I_0 in V_{REF} and compensating the output voltage reference. Therefore, a voltage that is insensitive to the temperature can be obtained.

B. The voltage reference subcircuit

The right of figure1 shows the voltage reference subcircuit we used [7]. It consists of transistors M_{11}- M_{15} that all MOSFETs are operated in the subthreshold region except current mirrors. We can discover that the gate-source voltages (M_{11}-M_{15}) of transistors form a closed loop, and the current in M_{11} and M_{13} are $3I_2$ and $2I_2$.Since the output voltage V_{REF} of the circuit is given by

$$V_{REF} = V_{GS11} - V_{GS12} + V_{GS13} - V_{GS14} + V_{GS15} \tag{6}$$

From equation (2), we find

$$V_{GS} = V_{TH} + \eta T_T \ln\left(\frac{I_{DS}}{KI_0}\right) \tag{7}$$

We can assume that the temperature dependence of the threshold voltage can be written by

$$V_{TH}(T) = V_{TH}(T_0) - \kappa(T - T_0) \tag{8}$$

Where T is the absolute temperature, T_0 is the initial absolute temperature and κ is the TC of V_{TH}. Since a gate-source to another gate-source voltage ΔV_{GS} from M_i to M_j that two transistor operated in subthreshold region can be expressed as

$$\Delta V_{GS} = \eta V_T \ln\left(\frac{K_j}{K_i}\right) \tag{9}$$

The reference voltage V_{REF} can be obtained by (6), from (8), this can be expressed as

$$\begin{aligned} V_{REF} &= V_{GS11} + \eta V_T \ln\left(\frac{2K_{12}K_{14}}{K_{13}K_{15}}\right) \\ &= V_{TH} + \eta V_T \ln\left(\frac{3I_2}{K_{11}I_0}\right) + \eta V_T \left(\frac{2K_{12}K_{14}}{K_{13}K_{15}}\right) \end{aligned} \tag{10}$$

Because of equation (10) expressed as a negative and positive temperature dependence V_{TH} ,V_T respectively, the output voltage reference V_{REF} with a zero TC can be obtained by adjusting the size of the transistors. From [6], we also assumed $V_{REF} - V_{TH0} \ll \kappa T$, $\eta V_T \ll \kappa T$ and the temperature dependence of the reference voltage V_{REF} in Eq. (9) is rewritten as

$$\begin{aligned} V_{REF} &= V_{TH0} - \kappa T \\ &+ \eta V_T \ln\left[\frac{3\eta^2 K_5 K_{12} K_{14}}{(\eta-1)(\sqrt{K_5/K_3}-1)^2 K_{11} K_{13} K_{15}} \ln^2\left(\frac{K_6}{K_4}\right)\right] \end{aligned} \tag{11}$$

The TC of V_{REF} is expressed by

$$\begin{aligned} \frac{dV_{REF}}{dT} &= -\kappa + \eta \frac{k_B}{q} \\ &\times \ln\left[\frac{3\eta^2 K_5 K_{12} K_{14}}{(\eta-1)(\sqrt{K_5/K_3}-1)^2 K_{11} K_{13} K_{15}} \ln^2\left(\frac{K_6}{K_4}\right)\right] \end{aligned} \tag{12}$$

Therefore, a zero TC can be gotten on condition that

$$-\kappa + \eta \frac{k_B}{q} \ln\left[\frac{3\eta^2 K_5 K_{12} K_{14}}{(\eta-1)(\sqrt{K_5/K_3}-1)^2 K_{11} K_{13} K_{15}} \ln^2\left(\frac{K_6}{K_4}\right)\right] = 0 \tag{13}$$

An independence temperature voltage reference can be received, at the same time, by substituting (13) in (11) we get

$$V_{REF} = V_{TH0} \tag{14}$$

Based on the above discuss, the value of reference voltage is equal to the threshold voltage of MOSEFTs at 0 K.

From [7], [9], we find both V_{TH0} and its temperature coefficient κ depend on process variations, mismatch on current mirror, channel doping concentration N_A and as a function of temperature T. In order to obtain a low sensitivity TC to process variation, some measures such as a large WL values, thus the mismatch can be negligible in compared to the effect of process variations, a common centroid technique were adopted in this proposed circuit. We also find from [7], κ is a logarithmic function of N_A, Therefore we can neglect the dependence of temperature coefficient κ on process variation.

IV. EXPERIMENTAL RESULTS

The proposed voltage reference shown in figure 1 was successfully implemented 0.5μm standard N-well CMOS technology, where the threshold voltage of a MOSEFT at 0 K was about 1.27 V. Figure 3 showed the results of the output reference voltage V_{REF} as a function of temperature, which was to 1.271 V, approximately equal to the threshold voltage of a MOSEFT at 0K. The temperature average coefficient were 5.54ppm/ °C in a temperature range from -20 °C to 85°C with the supply voltage as a parameter. So we can get a reference voltage that was insensitive to the temperature. Figure 4 showed the supply voltage dependences of the output reference voltage V_{REF}. The circuit operated with supply voltage ranging from 1.4 to 3.3V and so the line sensitivity was 18ppm/V in the region. We can find the proposed reference voltage circuit was insensitive to temperature and process variations, which could be used as a fundamental references voltage circuit for ultra-low power CMOS LSIs in this process or other smaller process conditions. The performance of the proposed voltage reference circuit comparing with those of other designs already reported in the literature and implemented in various processes was shown in Table I. We can find that the proposed voltage reference circuit was able to work with the lower power consumption and insensitivity temperature, and these characters will be fitting the requirements of modern ultra-low power LSIs. Moreover, the proposed circuit showed very good performance in terms of process variations in sensitivity and the more wide voltage range.

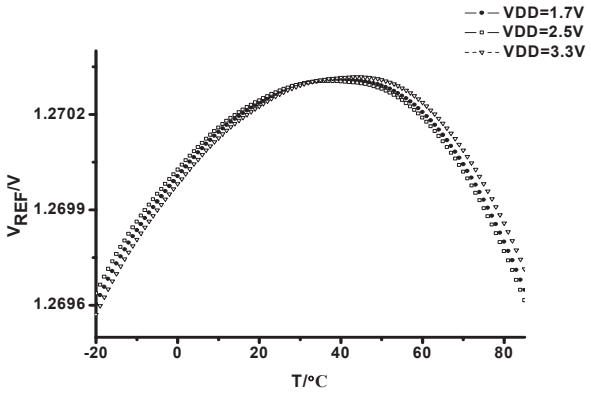

Figure3 . The results of the output reference voltage V_{REF} as a function of temperature

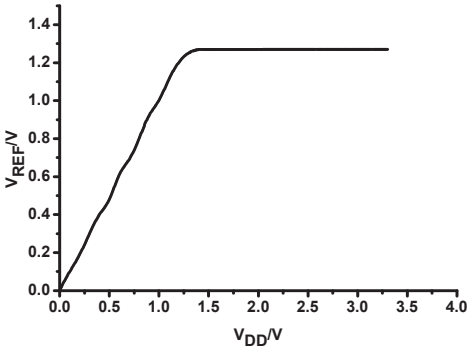

Figure4 . The supply voltage dependence of the output reference voltage V_{REF}

TABLE I. COMPARED WITH OTHER DESIGNS ALREADY REPORTED IN THE LITERATURE AND IMPLEMENTED IN VARIOUS PROCESS.

The stimulation results	**The already reported stimulation results**				
	This work	***[7]***	***[9]***	***[5]***	***[6]***
Technology	0.5μm standard CMOS	0.35μm CMOS	0.18μm CMOS	0.35μm CMOS	0.6μm CMOS
Temperature range	-20 to 85°C	-20 to 80°C	-40 to 85°C	0 to 80°C	0 to 100°C
Minimum supply voltage	1.7V	1.4V	0.58V	0.9V	1.4V
V_{REF}	1.271V	754mV	342mV	670mV	309mV
Power consumption	0.209μW	0.3μW	0.06μW	0.036μW	13.6μW
TC	5.54ppm/ °C	7ppm/ °C	4.6ppm/ °C	10ppm/ °C	36.9ppm/ °C
Line sensitivity	18ppm/V	20ppm/V	2800ppm/V	2700ppm/V	830ppm/V

V. CONCLUSION

The proposed voltage reference circuit that generates two voltages having opposite temperature coefficient, which are added to produce an voltage reference that is approximately equal to the threshold voltage of a MOSEFT at absolute temperature of zero degree. A current that is proportional to the square of absolute temperature is obtained to compensate the pre-exponential factor of the subthreshold current. It is superior to that reported in [7], [9], of which the voltage of V_{REF} has influence on the gate-source voltage and resistance of M_{R1}. We can find the proposed reference voltage circuit is insensitive to the temperature and process variations, using as a fundamental references for nanowatt power CMOS LSIs in other smaller process conditions.

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