A Nanopower CMOS Bandgap Reference with 30ppm/degree C from -30 degree C to 150 degree C

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***Abstract*—A nanopower subthreshold bandgap reference with 30ppm/℃ from -30℃ to 150℃ has been implemented in 0.18μm CMOS. This design is based on weighted ΔV_{GS} and is free of resistors. The major advantage of this design is that with nanopower consumption, the temperature range is extremely wide. To achieve high performance of subthreshold bandgap operating in high temperature (above 80℃), a leakage current elimination technique which enables subthreshold bandgap operate properly until 150℃ was proposed. Such modification does not require additional die area and power consumption. This topology can also generate multiple reference voltages whose values are integer times of the minimum reference voltage. The line regulation of the reference voltage is 0.677mV/V when the supply voltage is increased from 1 V to 2.5 V. The core circuit consumes 46nW at 1V at room temperature. The active area occupies 0.0036mm^2.**

I. INTRODUCTION

Voltage references are indispensable building blocks in many analog and digital integrated circuits such as ADCs, DRAMs, voltage regulators, etc [1]. As the demand for portable devices, low power circuits are required widely. Low power voltage reference can be achieved in conventional triode based bandgap [2]. However, this kind of design needs resistors with a high resistance of several hundred megaohms to achieve low-current, subthreshold operation [2]. Such a high resistance needs large area to implement. Subthreshold bandgap reference without resistor, in contrast, does not have this disadvantage. However, the temperature range of conventional triode based bandgap is much wider than that of subthreshold bandgap reference in most of presented literature [2], [3], [5]. The typical temperature range is -25℃ to 125℃ for conventional bandgap, and -20℃ to 80℃ for subthreshold bandgap, respectively. Temperature range of subthreshold bandgap limits its application in special field. Besides, the output voltage of subthreshold is usually process dependent only, which cannot be adjusted to the specified applications [2]. This paper presents a new technique to enlarge the temperature range of subthreshold bandgap, and also presents a new topology to generate more flexible output voltage. As a result, the proposed circuit can operate properly in the whole designed temperature range, i.e., -30℃ to 150℃, and can generate three output voltage for special applications.

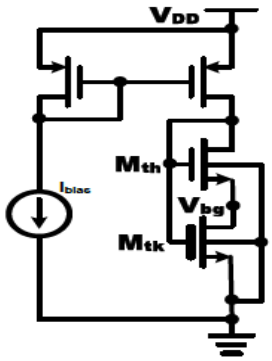

Figure 1. Topology of a typical subthreshold bandgap

This paper is organized as follows. Section II discusses the circuit proposed in previous literature and expresses the principle of this paper. Section III explains the new technique and new topology of output circuit. Section IV shows the measurement results of a prototype device fabricated in a 0.18μm standard CMOS process technology. Conclusion is drawn in Section V.

II. EXISTING CMOS SUBTHRESHOLD BANDGAP

Most of CMOS subthreshold bandgap circuits are based on the weighted difference between gate-source voltages of two transistors [4]. Figure 1 shows a typical topology [3]. M_{th} has thin gate oxide and M_{tk} has thick gate oxide. Current mirror is used to copy I_{bias} to bias M_{th} and M_{tk} in subthreshold region.

For an n-MOSFET operating in the weak-inversion region, with the condition of $V_{DS} \geq 3V_T$, which is always coordinated in this design, its drain current can be given by:

$$I_D = \frac{W}{L} I_0 \exp\left(\frac{Vgs - Vth}{\eta V_T}\right) \qquad (1)$$

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Where $I_0=\mu Cox*(\eta-1)V_T^2$, V_{th} is the threshold voltage of a MOSFET, μ is the carrier mobility, Cox is the gate-oxide capacitance, η is the subthreshold slope factor, $V_T = kT/q$ is the thermal voltage[2].

The temperature dependence of threshold voltage is given by

$$Vth(T) = Vth_0 - \kappa T \tag{2}$$

where T is the concerned temperature, V_{TH0} is the threshold voltage at 0 K, and κ is the TC of V_{TH}.

According to equation (1) and V_{bg}(ideal) can be given by:

$$V_{bg(ideal)} = V_{gs,tk} - V_{gs,th} = V_{th,tk} - V_{th,th} + \frac{\eta kT}{q}\ln\left[\frac{t_{ox,tk}(W/L)_{th}}{t_{ox,tm}(W/L)_{tk}}\right] \tag{3}$$

Temperature compensation can be achieved by selecting W/L ratios for M_{th} and M_{tk} which satisfy the following equation:

$$\frac{(W/L)_{th}}{(W/L)_{tk}} = \frac{t_{ox,th}}{t_{ox,tk}}\exp\left[(\kappa_{tk} - \kappa_{th})\times\eta\frac{q}{k}\right] \tag{4}$$

Where κ_{tk} is the TC of $V_{th,tk}$, κ_{th} is the TC of $V_{th,th}$, and other physical parameters have the same meanings as defined above.

From figure 1, it is easy to find that the source-bulk pn junction and drain-bulk pn junction are backward biased. The leakage current from drain/source to bulk increase exponentially when temperature goes up. Thus, If the current in each branch of the circuit was designed to be 10 nA, the leakage current would cause a 10% error from the desired current in each branch. Experiments at various temperature shows that the leakage current is a hundred picoampere in 100℃, 1 nanoampere in 125℃ and 8 nanoampere in 150℃. Therefore, the drain current both in M_{tk} and M_{th} cannot be considered equal to each other. As a result, an error is introduced in equation (2). Equation (2) should be replaced by:

$$\begin{aligned} V_{bg} &= V_{gs,tk} - V_{gs,th} = V_{th,tk} - V_{th,th} + \frac{\eta kT}{q}\ln\left[\frac{t_{ox,tk}(W/L)_{th}}{t_{ox,th}(W/L)_{tk}}\times\frac{I_{D,tk}}{I_{D,th}}\right] \\ &= Vbg(ideal) + \frac{\eta kT}{q}\ln\left(\frac{I_{D,tk}}{I_{D,th}}\right) = Vbg(ideal) + Vbg(error) \end{aligned} \tag{5}$$

In equation (5), the error cannot be eliminated by compensation theory above. Besides, the error varies with temperature. It is about 15mV variation in the temperature range of 100℃ to 120℃, which is not acceptable in most applications. Therefore, This error is the main reason for that the performance above 80℃ of subthreshold bandgap is not as well as that in temperature range of -20℃ to 80℃.

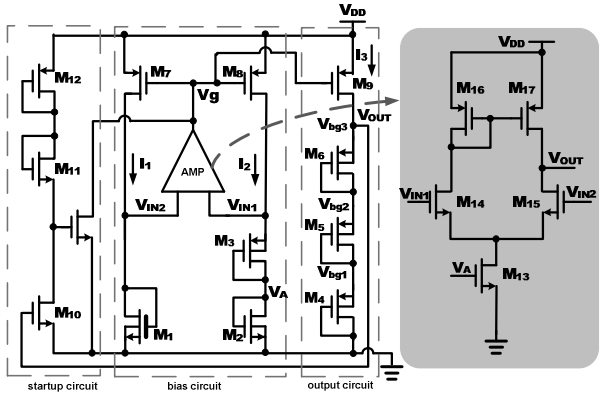

Figure 2. Proposed wide temperature range subthreshold bandgap.

III. PROPOSED CIRCUIT

The topology of the proposed circuit is shown in Figure 2. M_1 and M_2 are NMOS, M_1 has thick gate oxide and M_2 has thin gate oxide. The MOSFETs of M_3 to M_6 are PMOS, and they are identical to each other. A 1-stage differential-to-single-ended opamp is used to ensure V_{IN1} equal to V_{IN2}. The DC gain of the subthreshold opamp is 70 dB. All MOSFETs in the opamp operate in subthreshold region to achieve low power design.

A. Leakage current elimination technique

From the analysis in Section II, in order to enable the subthreshold bandgap to operate properly in high temperature (above 100℃), it is necessary to eliminate the error caused by leakage current. In figure 2, the sources and the bulks of all effective MOSFETs, M_1 to M_6, are connected together. As a result, for all effective MOSFETs, the bias voltage across source-bulk pn junction turns to be zero and the leakage current from source to bulk is eliminated. Although the bias voltage across drain-bulk pn junction still exits, there is only one path to flow for the current from source. That is, the current from source can only flow to the drain. Therefore, I_D equals to I_S in full designed temperature range. Both in bias circuit and output circuit, leakage current is eliminated in whole temperature range. Equation (1) is available in full designed temperature range. Therefore, the error caused by leakage current can be eliminated.

M_3 to M_6 use PMOS instead of NMOS, because the source and the bulk of PMOS can always be connected together in standard CMOS process.

B. Voltage reference generation

The idea of proposed circuit is using current mode instead of voltage mode.

In the bias circuit, The loop gain formed by the error amplifier and the common-source amplifiers , then

$$V_{IN1} = V_{IN2} \tag{6}$$

Therefore, V_{DS} of M_3 equals to V_{IN2} minus V_A.

$$V_{DS3} = V_{IN2} - V_A \quad (7)$$

Because V_{IN2} equals to $V_{GS,1}$, V_A equals to $V_{GS,2}$, then (7) can be given by:

$$V_{DS3} = V_{gs,1} - V_{gs,2} \quad (8)$$

The current of I_1, I_2, and I_3 equals to each other due to the current mirror. I_D equals to I_S for all MOSFETs both in bias circuit and output circuit:

$$I_{D,3} = I_{D,4} = I_{D,5} = I_{D,6} = I_{S,3} = I_{S,4} = I_{S,5} = I_{S,6} \quad (9)$$

Then equation (3) is available, and choosing values in equation (4) for M_1 and M_2, $V_{DS,3}$ is independent of temperature.

Because M_3 to M_6 are identical, and their source to drain current is the same, from I-V characteristic in subthreshold region, it can be found that the $V_{DS,4}$ to $V_{DS,6}$ are also temperature independent, that is $V_{GS,4}$ to $V_{GS,6}$ are temperature independent.

From the output circuit topology, the output voltage can be given by:

$$\begin{aligned} Vbg_1 &= Vgs4 = Vgs3 \\ Vbg2 &= Vgs4 + Vgs5 = 2 \times Vgs3 \\ Vbg3 &= Vgs4 + Vgs5 + Vgs6 = 3 \times Vgs3 \end{aligned} \quad (10)$$

By stacking MOSFETs identical to M_3 in series, more voltage references can be given.

C. Design consideration

Mismatch between M_3, M_4, M_5 and M_6 partly decides the TC (temperature coefficient) accuracy of output reference voltage. In order to reduce the mismatch, the width and length of these four MOSFETs should be large enough. In this design, we choose the channel length ten times of the characteristic length. From Monte Carlo simulation, the maximum variation in temperature-output voltage curve is 5mV in 50 sets simulation.

Considering the offset voltage of the amplifier,

$$V_{IN1} = V_{IN2} + Vos \quad (11)$$

The $V_{ds,3}$ in equation (8), including the effect of Vos, is given by

$$Vds3 \cong Vgs1 - Vgs2 - Vos \quad (12)$$

And the TC of $V_{ds,3}$ is given by

$$\frac{dVds3}{dT} \cong \frac{d(Vgs1 - Vgs2)}{dT} - \frac{dVos}{dT} = \frac{dVbg(ideal)}{dT} - \frac{dVos}{dT} \quad (13)$$

If Vbg(ideal) is temperature independent, the TC of $V_{ds,3}$ is dominated by the TC of Vos.

Enlarging the value of input transistors of amplifier is an effective way to decrease the value of Vos. From Monte Carlo simulation, 5μm/5μm is chosen for input transistors, i.e., about thirty times of the characteristic length.

A start-up circuit is used to avoid the stable state in the zero bias condition.

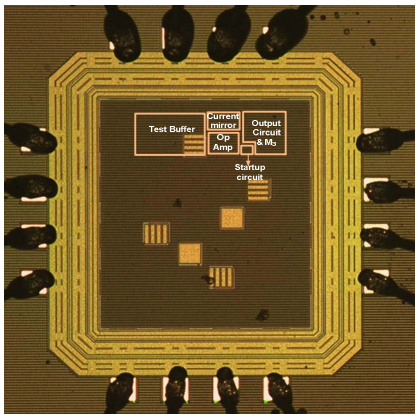

Figure 3. Chip micrograph

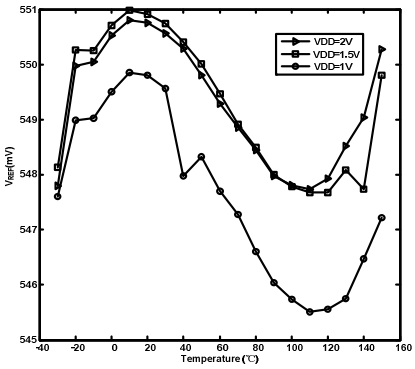

Figure 4. Measured temperature dependences with different VDDs

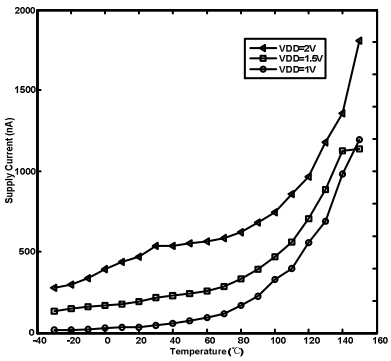

Figure 5. Measured total current versus temperature with different VDDs

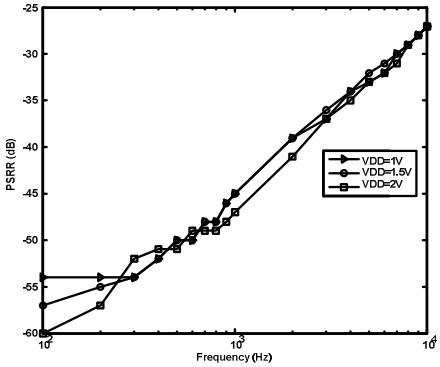

Figure 6. Measured PSRR with different VDDs

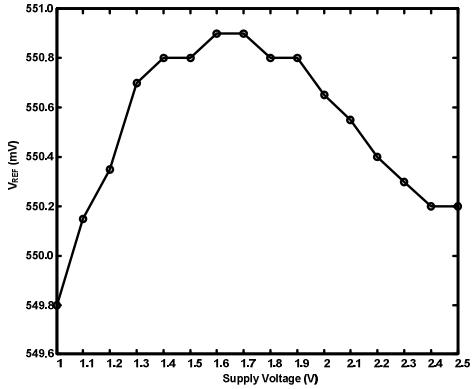

Figure 7. Measured output voltage versus supply voltage at room temperature

IV. MEASUREMENT RESULTS

The proposed circuit was fabricated in a standard 0.18μm 1P6M CMOS process. The sample was packaged in COB (chip on board) package. The active core area is 0.0036 mm^2 (90μm×40μm). Micrograph of the bandgap reference die is shown in Figure 3. Here Vbg3 is used to test the performance. Figure 4 shows the measured results of temperature dependences in the temperature range from -30℃ to 150℃ with different supply voltages: 1.0V, 1.5V and 2.0V. The average output voltage reference is 548mV. From figure 4, it can be attained that the variation in the range of 100℃ to 150 ℃ is comparable with the variation in the range of -30℃ to 80 ℃. Therefore, it is reasonable to believe that output voltage circuit can operate properly from 100℃ to 150℃ and the measured temperature coefficient is around 30ppm/℃. The measured current consumption dependences of temperature in different supply voltages (1V, 1.5V and 2.0V) is shown in figure 5 and as shown in figure 5, the current is 46nA at 1V at room temperature. Figure 6 shows the PSRR (power supply rejection ratio) at room temperature without any filtering capacitor with different supply voltages (1V, 1.5V and 2.0V). The PSRR is less than -54dB at 100Hz. And figure 7 shows the measured output voltage dependences in supply voltage at room temperature. There is 1mV variation when supply voltage varies from 1V to 2.5V, that is, the line linearity is 0.677mV/V. Performance conclusion and comparison with previously published circuits has been summarized in Table I.

V. CONCLUSION AND COMPARISON

A nanopower subthreshold bandgap reference with 30ppm/℃ from -30℃ to 150℃ has been proposed in this paper. This design is based on weighted ΔV_{GS} and is free of resistors. With nanopower consumption, the temperature range is extremely wide. Leakage current elimination technique was proposed and this technique enables subthreshold bandgap operate properly until 150℃. Such modification does not require additional die area and power consumption. This topology can also generate multiple reference voltages whose values are integer times of the minimum reference voltage. The proposed circuit has been fabricated in 0.18μm standard CMOS. And the measurement results show that TC is 30ppm/℃ in the temperature range of -30℃ to 150℃, the power consumption is 46nW at 1V at room temperature. This circuit is suitable for low power, high temperature range or multiple references required applications.

TABLE I. PERFORMANCE COMPARISON

Parameter	This work	[2]	[3]	[5]
Technology	0.18μm CMOS	0.35μm CMOS	0.35μm CMOS	0.35μm CMOS
Temperature range	-30℃-150℃	-20℃-80℃	-20℃-80℃	0℃-80℃
Supply Voltage	1 V-2.5 V	1.4 V-3 V	1.1 V-4 V	0.9 V-4 V
Vbg	548 mV	745 mV	96.6 mV	670 mV
Power	46nW @1V@ room temp	300nW @1.4V@ room temp	20nA @1.1V@ room temp	40nA @0.9V
TC	30 ppm/℃	7ppm/℃	11.4ppm/℃	10ppm/℃
PSRR@ room temp	-54dB @100Hz @1V	-45dB @100Hz	<-60dB @100Hz @3V	-47dB @100Hz @0.9V
Active area	0.0036mm^2	0.055mm^2	0.0189mm^2	0.045mm^2

REFERENCES

[1] A. Wang, B. H. Clhoun, and A. P. Chandracasan, Sub-Threshold Design for Ultra Low-Power Systems. New York: Springer, 2006.

[2] Ueno K, Hirose T, Asai T and Amemiya Y, "A 300 nW, 15 ppm/degrees C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs," IEEE J. Solid-State Circuits, vol. 44, no.7, pp. 2047–2054, Jul. 2009.

[3] Yan W, Li W, Liu R, "Nanopower CMOS sub-bandgap reference with 11 ppm/degrees C temperature coefficient," ELECTRONICS LETTERS, vol. 45, no.12, pp. 627–628, JUN 4 2009.

[4] K.N. Leung and P.K.T. Mok, "A CMOS Voltage ReferenceBased on Weighted VGS for CMOS Low-Dropout LinearRegulators," IEEE Journal of Solid-State Circuits, vol. 38,pp.146-150, Jan. 2003.

[5] G. De Vita and G. Iannaccone, "A sub-1-V, 10 ppm/ C, nanopower voltage reference generator," IEEE J. Solid-State Circuits, vol. 42, no.7, pp. 1536–1542, Jul. 2007.