# A 210 nW 29.3 ppm/˚C 0.7 V Voltage Reference with a Temperature Range of -50 to 130 ˚C in 0.13 µm CMOS

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## Abstract

A low-voltage, low-power CMOS voltage reference with high temperature stability in a wide temperature range is presented. The temperature dependence of mobility and oxide capacitance is removed by employing transistors in saturation and triode regions and the temperature dependence of threshold voltage is removed by exploiting the transistors in weak inversion region. Implemented in 0.13um CMOS, the proposed voltage reference achieves temperature coefficient of 29.3ppm/˚C against temperature variation of -50 – 130˚C and line sensitivity of 337ppm/V against supply variation of 0.7–1.8V, while consuming 210nW from 0.7V supply and occupying 0.023mm$^2$.

Keywords: Voltage reference, low power, low voltage, temperature compensation

## Introduction

Over the past decade, low-voltage circuits have received much attention due to the growing interest in extremely low-power applications such as self-powered sensors. While various low-voltage, low-power circuits have been proposed for analog, RF and digital circuits [1-4], low-voltage voltage reference, an essential building block for low-voltage electronics, has not received as much attention. Although several low-voltage voltage references have recently been presented [6-9], none of them covers all the key properties of a voltage reference, which are output voltage stability against temperature and supply variations over a wide temperature range and low power consumption. In this paper, a 0.7V voltage reference is presented which achieves temperature sensitivity of 29.3 ppm/˚C over a temperature range of -50 ~ 130˚C, which is nearly twice the operating range of previously reported state-of-the-art voltage references.

## Proposed Low-Voltage Low-Power Voltage Reference

The schematic of the proposed voltage reference is shown in Fig. 1, where $M_1$ and $M_2$ operate in saturation and triode regions, respectively and $M_3 \sim M_6$ and $M_7$ act as current sources. By using first order I-V equations of a MOSFET in strong inversion region, the output reference voltage, $V_{OUT}$, can be expressed as,

$$V_{OUT} = V_{TH} + V_{DS2}\left[\frac{K_2}{K_1} + \sqrt{\left(\frac{K_2}{K_1}\right)^2 - \frac{K_2}{K_1}}\right] \quad (1)$$

where $K_1$ and $K_2$ are the ratios of the width and length of $M_1$ and $M_2$, respectively. As can be seen, $V_{OUT}$ is unaffected by the temperature dependence of mobility and gate oxide capacitance and is affected only by the temperature dependence of the threshold voltage and $V_{DS2}$. The threshold voltage of a MOSFET can be modeled as the following equation [5],

$$V_{TH}(T) = V_{TH0} - K_{VTH}T \quad (2)$$

where $T$ is the absolute temperature, $V_{TH0}$ is the threshold voltage at $0K$ and $K_{VTH}$ is the temperature coefficient of the threshold voltage. Since $V_{TH}$ is proportional to temperature with a negative temperature coefficient, current source formed by $M_3 \sim M_6$ should be designed such that $V_{DS2}$ is proportional to temperature with a positive temperature coefficient, in order to achieve temperature independent $V_{OUT}$. This is achieved by having $M_3 \sim M_4$ in weak inversion region where current depends on thermal voltage that has positive temperature coefficient. With $M_2$ in triode region and thus acting as a resistor, $M_3$ and $M_4$ can be operated in the weak inversion region and hence the following equation can be obtained,

$$V_{DS2} = V_{GS4} - V_{GS3} = mV_T \ln\left(\frac{K_3}{K_4}\right) = m\frac{kT}{q}\ln\left(\frac{K_3}{K_4}\right) \quad (3)$$

where $V_T$ is the thermal voltage and $m$ is the subthreshold slope parameter. Substituting (3) and (2) into (1), the output voltage of the voltage reference can be described as

$$V_{OUT} = V_{TH0} - \left[K_{VTH} - \frac{mk}{q}\ln\left(\frac{K_3}{K_4}\right)\cdot\left(\frac{K_2}{K_1} + \sqrt{\left(\frac{K_2}{K_1}\right)^2 - \frac{K_2}{K_1}}\right)\right]T. \quad (5)$$

Note that the output voltage is independent of the supply voltage to the first-order. To minimize the supply sensitivity to second-order effects such as channel length modulation, an opamp based on two-stage topology is added. The temperature coefficient of $V_{OUT}$ can be set to zero if the following condition is met.

$$\frac{qK_{VTH}}{mk} = \ln\left(\frac{K_3}{K_4}\right)\left[\frac{K_2}{K_1} + \sqrt{\left(\frac{K_2}{K_1}\right)^2 - \frac{K_2}{K_1}}\right]. \quad (7)$$

The minimum supply voltage is determined by the condition that $M_5$ has to operate in the saturation region and hence,

$$V_{DD} > V_{OUT} + V_{OV5} \quad (8)$$

where $V_{OV5}$ is the overdrive voltage of $M_5$ which is approximately 0.2V. With $V_{OUT}$ of about 0.5V, the proposed circuit operates down to a supply voltage of about 0.7 V.

## Experimental Results

The proposed voltage reference is fabricated in a 0.13µm standard CMOS process. The die micrograph is shown in Fig. 2 where the core area is about 165 × 140 µm$^2$. The voltage reference consumes 210nW from 0.7V supply. To verify the stability of the generated output voltage, temperature and supply voltage are varied from -50 ˚C to 130˚C and from 0.7 V to 1.8 V, respectively. Measured results are shown in Fig. 3, where it can be seen that the proposed voltage reference has a temperature drift of ±1.07$m$V which corresponds to a temperature coefficient of 23.8 ppm/˚C. The line sensitivity of the voltage reference is 337ppm/V as shown in Fig. 3 (b). In order to investigate the effect of process variation, the distribution of temperature coefficient of twelve samples from the same lot is shown in Fig. 4. The average and the standard deviation of temperature coefficient are 29.3ppm/˚C and 5.2ppm/˚C, respectively. The performance of the voltage reference is summarized and compared with that of the recently reported CMOS voltage references in Table I. It can be seen that the proposed voltage reference achieves the widest temperature range by approximately a factor of two and the lowest supply voltage. Moreover, under this wide temperature range, the temperature stability of the reference voltage is comparable to the state-of-the-art works. Another notable fact is that all previous works are based on old process technologies which allow the use of very long length devices (up to 150µm) for improved line sensitivity. The proposed circuit is based on shorter length technology which prohibits the use of a long devices (< 50µm). Lastly, a key merit of the proposed voltage reference is its simplicity compared to others and hence can be easily adapted in various applications.

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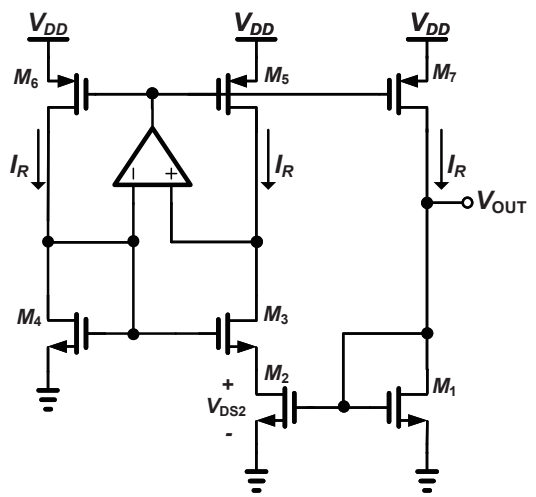


Fig. 1. Schematics of proposed voltage reference circuit. (Start-up circuit not shown)

Table I. Performance summary and comparison

| | [9] | [8] | [7] | [6] | **This work** |
|---|---|---|---|---|---|
| Process [CMOS] | 0.35µm | 0.35µm | 0.35µm | 0.6µm | **0.13µm** |
| Temp. Range [°C] | -20 to 80 | 0 to 80 | 0 to 80 | 0 to 100 | **-50 to 130** |
| VDD [V] | 1.4 to 3 | 0.9 to 4 | 1.5 to 4.3 | 1.4 to 3 | **0.7 to 1.8** |
| $V_{REF}$ [mV] | 745 ±14 | 670 | 890 | 310 ± 20 | **501 ± 24** |
| Power [µW] | 0.3 @ 1.4 V | 0.036 @ 0.9 V | 0.3 @ 2 V | 29.1 @ 3 V | **0.21 @ 0.7 V** |
| Temp. Coefficient [ ppm/°C ] | Min. = 7 Max. = 45 Avg. = 15 | 10 to 20 | 12 to 22 | Min. = 2.7 Max. = 62 Avg. = 37 | **Min. = 23.8 Max. = 41.1 Avg. = 29.3** |
| Line Sensitivity [ppm/V] | 20 | 2700 | 4600 | 1600 | **337** |
| Chip Area [ $mm^2$] | 0.055 | 0.045 | 0.015 | 0.055 | **0.023** |
| Samples | 17 | 1 | 1 | 15 | **12** |

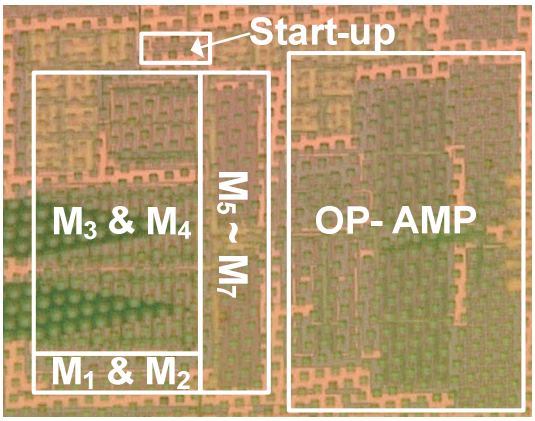


Fig. 2. Micrograph of chip.

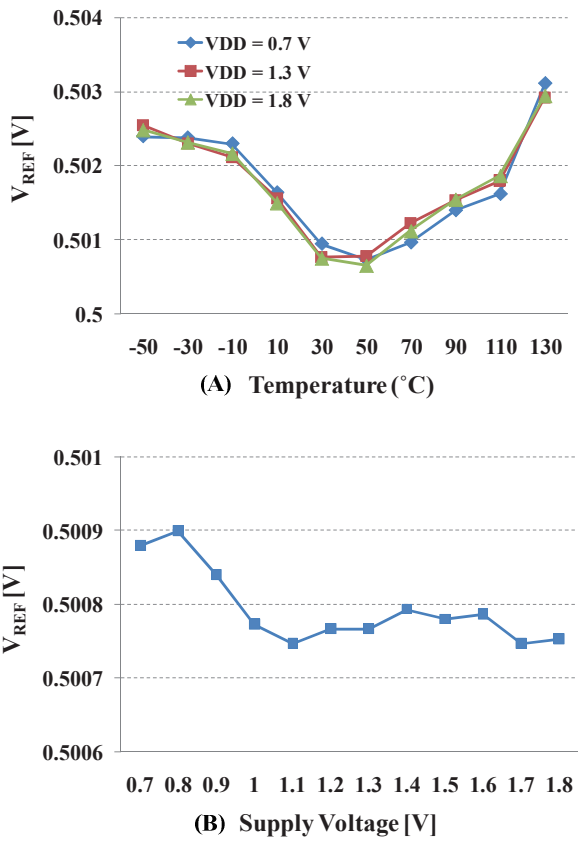


Fig. 3. Measured output voltage against (a) temperature and (b) supply voltage.

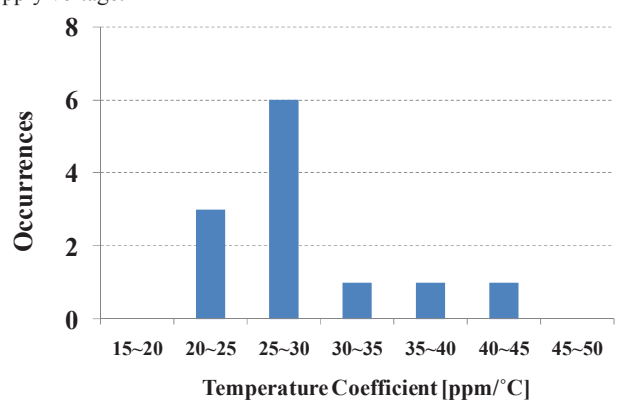


Fig. 4. Distribution of temperature coefficient for 12 samples.