A Sub-0.6V,34.8nW,4.6ppm/°C CMOS Voltage Reference using Subthreshold and Body Effect Techniques

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***Abstract*—An ultra low-voltage and low-power CMOS voltage reference was proposed in this paper. Subthreshold and body effect techniques are used to achieve temperature compensation. No resistor and BJT are used in this structure. The proposed circuit has been simulated with Charted 0.18-μm standard CMOS process. The simulated results show that the voltage reference can operate with sub-0.6V supply and total supply current is 60nA at 0.58V supply at room temperature. The temperature coefficient of the output voltage is 4.6ppm/℃, in a range from -40℃ to 85℃.**

I. INTRODUCTION

With the expansion of the portable battery operated products market, the demand for small area, low voltage and low power electronic system drives a strong demand for the smaller area, lower supply voltage and lower power consumption voltage reference which can be implemented with a standard CMOS process nowadays [1]. In CMOS technology, parasitic vertical bipolar junction transistor (BJT) formed in a p- or n-well is widely used to implement a bandgap voltage reference [1], [2]. Unfortunately, for silicon, the reference voltage is around 1.25 V and common-collector structure of the parasitic vertical BJT and the input common-mode voltage of the amplifier are the major limitations to design an ultra low voltage circuit [3]. Such constraints can be overcome by using current mode [4], [5] and resistive subdivision methods [6] that allow us to get sub-1V operation. But these structures still require large-area parasitic BJTs with large turn-on voltage and resistors. A nanopower voltage reference generator without any BJT and resistor [7] has been presented to solve these problems. But this structure has two high threshold voltage devices, which will increase the cost of fabrication.

To address the above-mentioned design problems, an ultra low-voltage and low-power voltage reference circuit without BJT and resistor in a standard CMOS process, is presented in this paper. Its key feature is that no high threshold voltage device or any other special device is needed.

The introduction of the voltage reference has mentioned above in Section Ⅰ. The design techniques and analysis of the minimum supply voltage are presented in detail in Section Ⅱ. In Section Ⅲ, the simulation results are presented. The summary is given in Section Ⅳ.

II. PRINCIPLE OF THE PROPOSED VOLTAGE REFERENCE

The complete circuit of the proposed voltage reference is shown in Fig.1. The structure is composed of forward bias circuit, current generator circuit and start-up circuit.

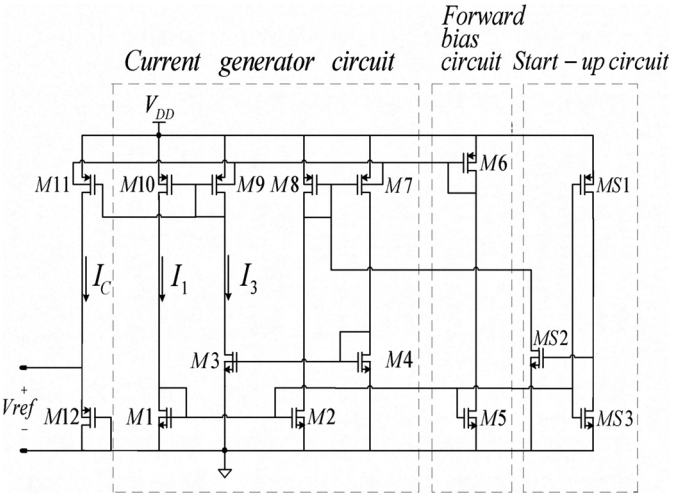

Fig. 1. Complete circuit of the proposed voltage reference.

A. Forward bias circuit

The forward bias circuit consists of M5 and M6, which is used to forward bias the source-bulk junction to reduce the threshold voltages of the PMOS transistors [6]. Since the threshold voltage of a PMOS transistor is given by [6]

$$|V_{thp}| = |V_{thpo}| + \gamma(\sqrt{2|\phi_f| - V_{SB}} - \sqrt{2|\phi_f|}) \quad (1)$$

where $|V_{thpo}|$ is the threshold voltage with zero biased source-bulk voltage, γ is the body bias coefficient, and Φ_f is the bulk Fermi potential. The V_{SB} dependence of V_{thp} at 27℃ and

bulk current I_{sub} at 85℃ are shown in Fig.2 (a) and Fig.2 (b), respectively. Fig.2 (a) shows that the threshold voltage can be reduced significantly with this body effect technique. Fig.2 (b) shows that the turn-on voltage of the p-n junction of the source-bulk junction at 85 ℃ is about 450mV, and for industrial application, the operation temperature range is from -40℃ to 85℃. Therefore, in order to avoid turning on the p-n junction of the source-bulk junction at the highest temperature, the forward bias voltage $|V_{GS6}|$ is set to about 300mV at room temperature. At this time, the threshold voltages of M7, M9 and M11 transistors are about 220mV at room temperature and the temperature-dependent bulk current of these transistors are small enough to neglect.

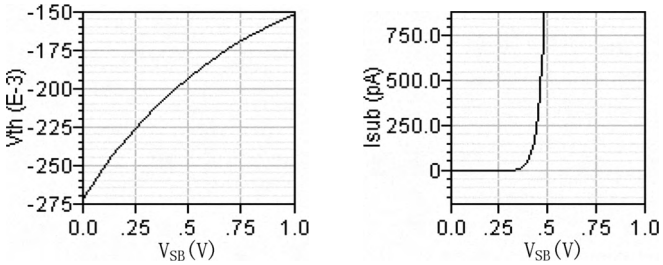

Fig. 2 (a) The V_{SB} dependence of V_{thp}. (b)The V_{SB} dependence of substrate current I_{sub}

B. Current generator circuit

The current generator circuit is made up of M1~M4, M7~M10, which generates the I_3 that is mirrored to Ic, such current is then injected into the diode-connected PMOS transistor M12 for temperature compensation. Since $W_1/L_1=W_2/L_2$ and $W_3/L_3=W_4/L_4$, the current mirror composed by transistors M1 and M2 imposes equal current I_1 in M8 and M10, also, the current mirror composed by transistors M3 and M4 imposes equal current I_3 in M7 and M9. All the transistors are standard digital MOS transistors. To bias M8 and M10 in the subthreshold region, and, at the same time, to bias M7 and M9 in the saturation region. This situation can be achieved by two different threshold voltages using body effect technique. Except M8 and M10, all the transistors operate in the saturation region. Assuming the channel length is long enough and $V_{DS}>4V_T$, the I-V characteristics of a PMOS transistor in the saturation and the subthreshold regions can be approximated by (2) and (3) respectively [7], [8], [9].

$$I_D = \frac{\mu_p C_{ox}}{2}\frac{W}{L}(V_{SG}-|V_{thp}|)^2 \tag{2}$$

$$I_D = \mu_p C_{ox} V_T^{\,2}\frac{W}{L}\sqrt{\frac{q\varepsilon_{si}N_{CH}}{2\phi_B}}\exp(\frac{V_{SG}-|V_{thp}|}{nV_T}) \tag{3}$$

Where V_T is the thermal voltage, n is the subthreshold slope parameter, Φ_B is the Bulk Fermi potential, ε_{si} is the permittivity of Si and N_{CH} is the channel doping concentration. The gate-source voltages of M7 and M8 (M9 and M10) are identical, and M10 and M8 in subthreshold with drain current I_1 and M9 and M7 in saturation with a drain current I_3. Then, we have

$$|V_{thp8}|+nV_T\ln(\frac{I_1}{\mu_p C_{ox}V_T^2(W_8/L_8)\sqrt{\frac{q\varepsilon_{si}N_{CH}}{2\phi_B}}})=|V_{thp7}|+\sqrt{\frac{2I_3}{\mu_p C_{ox}(W_7/L_7)}} \tag{4}$$

$$|V_{thp10}|+nV_T\ln(\frac{I_1}{\mu_p C_{ox}V_T^2(W_{10}/L_{10})\sqrt{\frac{q\varepsilon_{si}N_{CH}}{2\phi_B}}})=|V_{thp9}|+\sqrt{\frac{2I_3}{\mu_p C_{ox}(W_9/L_9)}} \tag{5}$$

where W_X and L_X are the width and length of MOSFET X. For the source-bulk junction forward bias voltages of M7 and M9 are same, the $V_{th7}=V_{th9}$. Assuming $W_{11}/L_{11}=W_9/L_9$, so Ic= I_3. Since Ic=I_3, $V_{th8}=V_{th10}$ and $V_{th7}=V_{th9}$, by subtracting (4) from (5), we can get the expression of the current

$$I_C = \frac{\mu_p C_{ox}W_9/L_9}{2(\sqrt{(W_9/L_9)/(W_7/L_7)}-1)^2}n^2V_T^2\ln^2(\frac{W_{10}/L_{10}}{W_8/L_8}) \tag{6}$$

The previous generated current Ic, given by (6), is then injected into the diode-connected transistor M12, that can generate an output voltage for temperature compensation. M12 operates in the saturation region and then by using (2) and (6), we can derive the output reference voltage

$$V_{ref}=|V_{thp12}|+\frac{nV_T}{\sqrt{(W_9/L_9)/(W_7/L_7)}-1}\sqrt{\frac{W_9/L_9}{W_{12}/L_{12}}}\ln(\frac{W_{10}/L_{10}}{W_8/L_8}) \tag{7}$$

According to the temperature variation characteristic of threshold voltage [7], [10], we can assume that the threshold voltage of an NMOS transistor linearly decreases with the increment of the temperature, as shown below:

$$|V_{thp}(T)|=|V_{thpo}|+\alpha(T-T_o) \tag{8}$$

where T is the absolute temperature, T_o is the room temperature, and α is the temperature coefficient of V_{thp}. The temperature dependence of V_{thp} from −40℃ to 85℃ is shown in Fig.3.

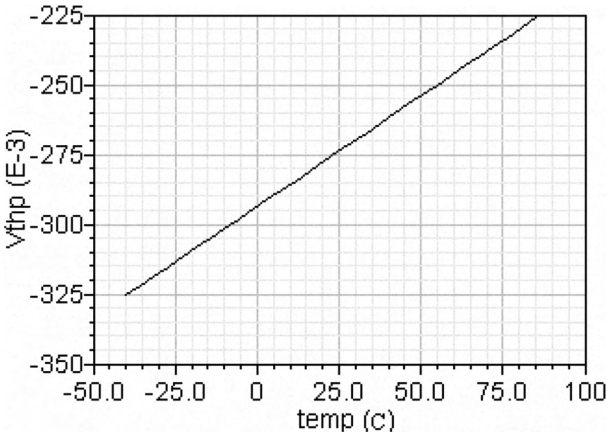

Fig. 3 The temperature dependence of V_{thp}.

Fig.3 shows that the temperature coefficient of V_{thp} is about -0.813mV/℃, so α can be approximate to -0.813mV/℃.The temperature dependence of output reference voltage can be obtained by differentiating (7) with respect to temperature, as shown below:

$$\frac{\partial V_{ref}}{\partial T} = -\alpha + \frac{nk}{(\sqrt{(W_9/L_9)/(W_7/L_7)}-1)q}\sqrt{\frac{W_9/L_9}{W_{12}/L_{12}}}\ln(\frac{W_{10}/L_{10}}{W_8/L_8}) \quad (9)$$

where k is the Boltzmann constant and q is the electron charge. For setting (9) to zero, we then obtain

$$\sqrt{W_{12}/L_{12}} = \frac{nk}{(\sqrt{(W_9/L_9)/(W_7/L_7)}-1)q\alpha}\sqrt{W_9/L_9}\ln(\frac{W_{10}/L_{10}}{W_8/L_8}) \quad (10)$$

Hence, V_{ref} can be a zero-temperature coefficient output reference voltage by design the W_{12}/L_{12}. Equation (7) can be achieved with temperature ranging from -40℃ to 85℃ by setting the source-gate voltages of M7, M8 and M9, M10 to 300mV and 260mV at room temperature, respectively.

C. *Start-up circuit*

Since this circuit has two stable states, one state is normal state that the current Ic is given by (6); the other is called zero-state. A start-up circuit composed of MS1, MS2 and MS3 is used to ensure that the first stable state is achieved. When this circuit is in the zero-state, the current in branch is zero. At this time, the gate voltage of M1 is very low and the gate voltage of MS2 is high, so MS2 generator a current, such current injected into the diode-connected PMOS transistor M8, then the circuit will operate in the normal state.

D. *Analysis of the minimum supply voltage*

The supply voltage must ensure every transistor which should operate in the saturation region do not operate in the triode region. Such supply voltage also has to ensure the V_{DS} of transistors which should operate in the subthreshold region higher than $4V_T$. Hence, we have

$$V_{DDmin} = \max\{|V_{GS8}|+V_{DSsat2}, |V_{GS9}|+V_{DSsat3}, 4V_T+V_{GS1}, V_{DSsat7}+V_{GS4}, |V_{GS6}|+V_{DSsat5}, |V_{GS12}|+V_{DSsat11}\} \quad (11)$$

The six items in the bracket represent the six branches of the proposed circuit. $|V_{GS9}|$ and $|V_{GS8}|$ ($|V_{GS6}|$) have set to 260mV and 300mV at room temperature, respectively. For a good matching of current mirror, the V_{DSsatx} is chosen about 100mV. Therefore, $|V_{GS12}|$, $V_{GS1,4}$ can be lower than 400mV because the threshold voltage of NMOS and PMOS is 245mV and -275mV at room temperature, respectively. According to above-mentioned, the minimum supply voltage can be lower than 0.5V in theory.

III. SIMULATION RESULTS AND COMPARISON

To evaluate the performance of the design, the simulations based on Charted 0.18-μm CMOS process have been carried out. In Fig.4 the Vref shifts as a function of temperature for different supply voltage, it shows that temperature coefficient of the Vref is 4.6ppm/℃ over the range from -40℃ to 85℃ under the supply voltage of 0.58V. Fig.5 (a) is the curve of Vref versus power supply voltage, it shows Vref variation is 5.68mV when the power supply varies from 0.58V to 2V at room temperature, so the line regulation of this circuit is 4mV/V. Fig.5 (b) shows the PSRR of this circuit from 1Hz to 1GHz without any filter capacitor. The PSRR is -40.45dB at 100Hz.

Fig. 6 displays the supply current versus supply voltage at multiple temperatures, it shows that total supply current is 60nA at room temperature when the power supply is 0.58V. Therefore, the power consumption is only 34.8nW in this work. Moreover, the comparisons among different voltage references are listed in Table Ⅰ. It can be noted that the proposed circuit has much lower supply voltage. As compared with [7], the proposed circuit does not need extra high threshold voltage device. And, it also has a quite low temperature coefficient.

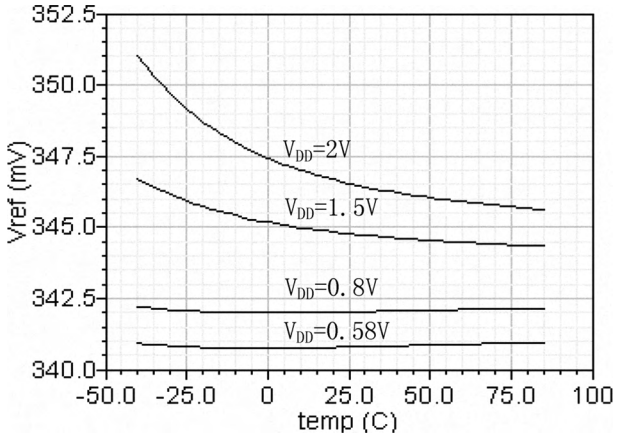

Fig. 4 Vref versus temperature over the range from -40℃ to 85℃ at multiple supply voltage.

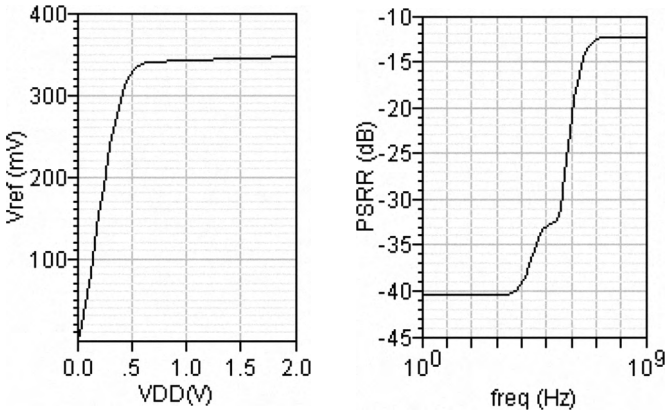

Fig. 5 (a) Vref versus supply voltage over the range from 0V to 2V, (b)PSRR of the proposed circuit over the range from 1Hz to 1GHz.

IV. CONCLUSION

In this paper, an ultra low-voltage and ultra low-power CMOS voltage reference is proposed and simulated, which is based on Charted 0.18-μm CMOS process. The method of temperature compensation has been described in detail. Comparing to the structure proposed previously [7], this circuit does not need the high threshold voltage device because of body effect technique. The temperature coefficient of output reference voltage is only 4.6ppm/℃ ranging from -40℃ to 85℃, the line regulation is 4mV/V for a power supply voltage varies from 0.58V to 2V and PSRR is -40.45dB at 100Hz. This structure does not need any resistor and BJT,

TABLE I. COMPARISON OF THE VOLTAGE REFERENCE

	This work	[4]	[6]	[7]
Process	0.18-μm CMOS	0.4-μm CMOS	0.6-μm CMOS	0.35-μm CMOS
Temperature coefficient	4.6ppm/℃	59ppm/℃	15ppm/℃	10ppm/℃
Temperature range	-40℃ to 85℃	27℃ to 125℃	0℃ to 100℃	0℃ to 80℃
High threshold voltage device	None	None	None	Exist
Passive resistors	None	Exist	Exist	None
Parasitic BJTs	None	Exist	Exist	None
Supply voltage	0.58V~2V	2.2V~4V	0.98V~1.5V	0.9V~4V
Total supply current	0.06μA@0.58V	2.2μA	18μA	0.04μA@0.9V
Line regulation	4mV/V	3.88mV/V	4.4mV/V	1.8mV/V
PSRR@100Hz	-40.45dB	Not show	-44dB	-47dB

which can save chip area. The power supply voltage can be sub-0.6V and the quiescent current is only 60nA at 0.58V supply voltage, which leads to a very low power consumption, in tens of nW range. This structure is very suitable for low-voltage and low-power applications.

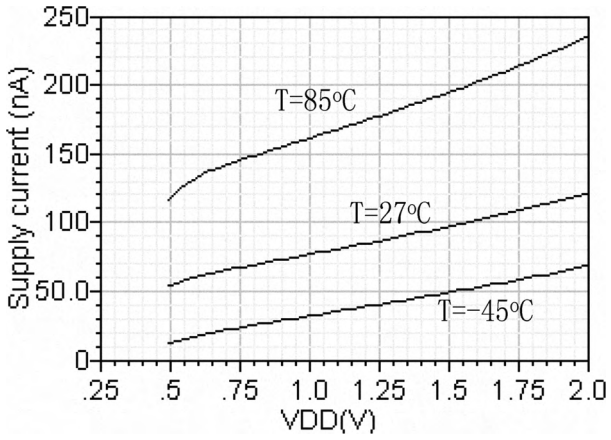

Fig. 6 The supply current versus supply voltage at multiple temperature.

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